

Motion Control Application Manual

January, 1987

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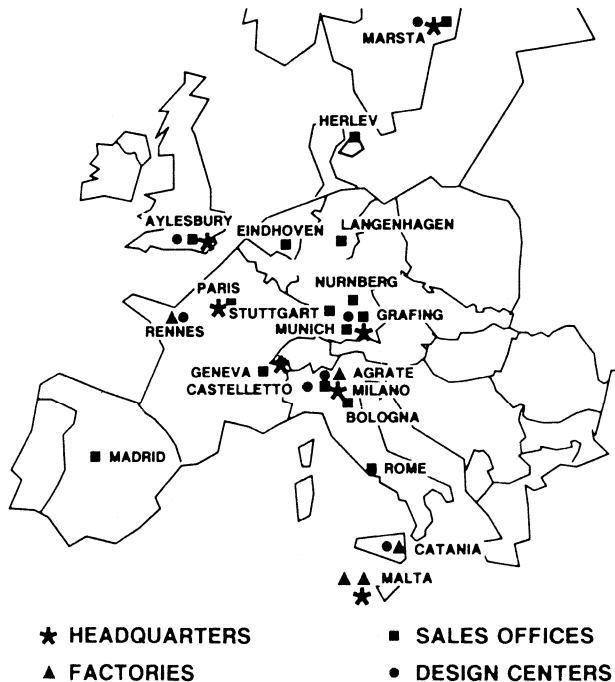
IDENTITY

Late in 1957, SGS was founded around a team of researchers who were already carrying out pioneer work in the field of semiconductors. From that small nucleus, the company has evolved into a Group of Companies, operating on a worldwide basis as a broad range semiconductor producer, with bilings over 300 million dollars and employing over 9500 people.

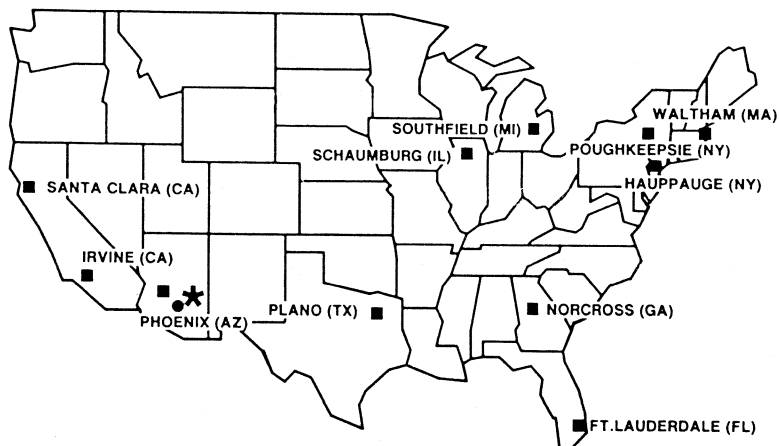
The SGS Group of Companies has now reached a total of 11 subsidiaries, located in Brazil, France, Germany, Italy, Malta, Malaysia, Singapore, Sweden, Switzerland, United Kingdom and the USA.

To go with its logo, the company takes the motto "Technology and Service", underlining the accent given to the development of state-of-the-art technologies and the corporate commitment to offer customers the best quality and service in the industry.

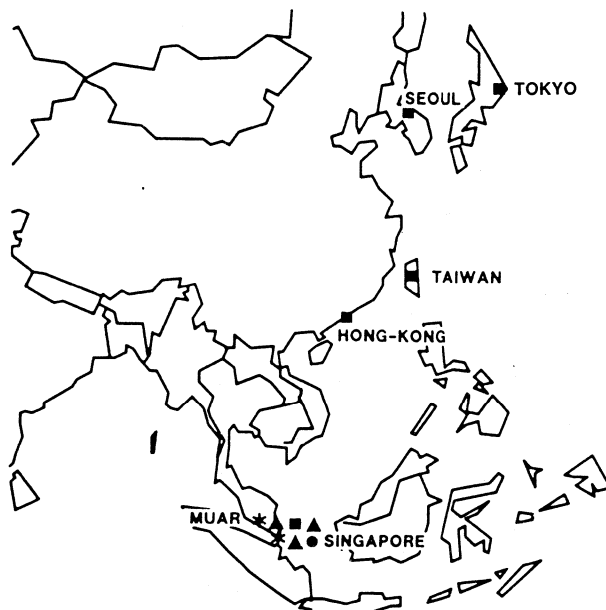
SGS IN EUROPE



SGS IN NORTH AMERICA



SGS IN ASIA/PACIFIC



* HEADQUARTERS

■ SALES OFFICES

▲ FACTORIES

● DESIGN CENTERS

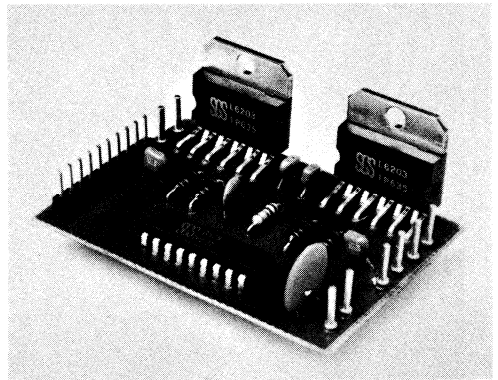
TECHNOLOGY AND INNOVATION SOLVE YOUR MOTION CONTROL PROBLEMS

Since the first high power ICs emerged at the end of the 1960s SGS has set the pace in power IC process technology, plastic power packages and innovative circuit design. Originally this technology know-how was applied to consumer circuits such as high power audio amplifiers and TV vertical deflection stages, so when real motor driving ICs emerged at the end of the seventies SGS already possessed a unique understanding of the problems involved and, more important, how they could be solved.

Already in 1979, while other companies were still content to produce darlington arrays, SGS launched a switchmode DC motor driver, the L292, capable of delivering 70W useful power to the load. The L292 was assembled in the SGS-developed Multiwatt™ package, now a much-copied industry standard power package.

Since then the company has introduced many other world-beating power ICs for motor and solenoid driving applications: the L295 Dual Switchmode Solenoid Driver, the L298 Dual Bridge Motor Driver, the L272 Dual Power Op Amp, the L6230 Brushless Motor Driver and many more.

Continuing this tradition of innovation, today SGS has introduced new high power bridge driver ICs, the L6202 and L6203, which exploit DMOS output transistors to achieve very high efficiency and fast switching capability.



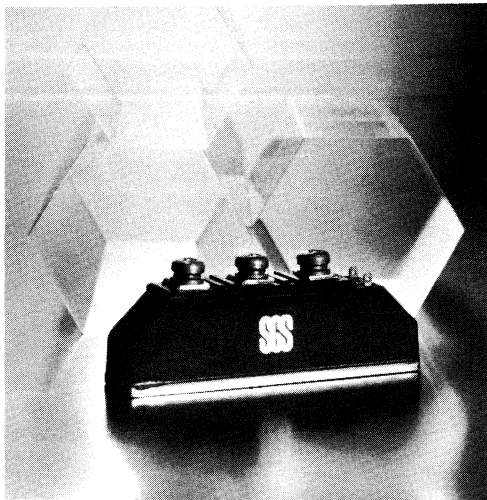
Two L6203 DMOS bridge driver ICs and an L6506 current controller make a complete stepper motor drive system delivering 3A/phase with very high efficiency.

Based on a unique technology called Multi-power-BCD, which combines bipolar linear, CMOS logic and power DMOS, these ICs are probably the most significant development in semiconductor technology since the dynamic RAM. Because of its high efficiency the L6202 can deliver 70W to the load, yet the device is assembled in a DIP package; and the L6203 delivers an unheard-of 250W.

Another SGS pacesetter product is the VB100 intelligent duty cycle controller. This VIPower™ device combines a high voltage, high current Darlington with on-chip intelligence for duty cycle control and thermal protection. The same VIPower™ technology

is used for the VB010 self protected switch which features a 400V Power Darlington capable of 10A output current with built-in protection circuits.

SGS has also kept ahead in POWER MOS transistors by exploiting high density cell structures. The SGSP322HD has a reduced chip area but equal overall performance to the original SGSP322 so offers a cost reduction for the user.



TO-240 — The unique SGS combination of advanced chip technology in a truly "user friendly" package, gives the solution to meet all high power system requirements.

Moving up in power, the SGS150MA010D1 isolated TRANSPACK module containing SGS POWER MOS transistors is designed for high switching speed DC motor control applications. On resistance is as low as 0.009Ω and the easy drive and rugged DMOS technology make this module ideal for high power applications.

These advances do not stop with silicon technology, SGS's established expertise in packaging has led to the recent introduction of a fully isolated package for power transistors. Used in place of the SOT-93 (TO-218), the ISOWATT218™ provides guaranteed isolation of 4kV DC and compliance with VDE specifications for creepage distance and clearance in electrical equipment.

All of these products are included in this book, along with the application informa-

tion you'll need to use them. The Motion Control Application Manual also contains a selection of SGS' innovative power supply products which will be useful in your system.

Dependable Delivery

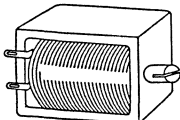
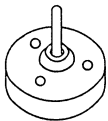
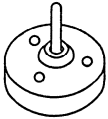
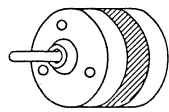
Advanced technology and innovation are just two of the reasons for SGS' remarkable growth performance. The third is manufacturing science — the ability to produce advanced products in high volumes, dependably, and with competitive quality & reliability. Just for bipolar linear and mixed bipolar/MOS ICs SGS has four 5" wafer fabs — in France, Italy and Singapore. Another two state-of-the-art 5" wafer fabs are dedicated to power transistor production. In addition, the company has highly-automated assembly facilities in Italy, France, Malta, Malaysia and Singapore.

SGS also has local design centers in all major semiconductor markets — USA, England, France, West Germany, Singapore and Italy — to speed the development of new products to satisfy the special needs of your application. And a worldwide network of sales offices and distributors means that SGS technology is never far away.

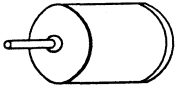
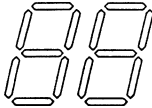
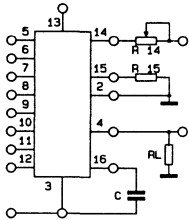
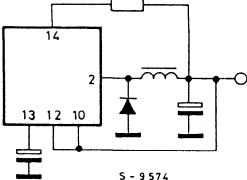


New diffusion facilities give SGS the advantage in Service, Quality and cost. State-of-the-art 5" wafer fabs are used for both linear ICs and power transistors.

PRODUCT SELECTOR (Integrated Circuits)

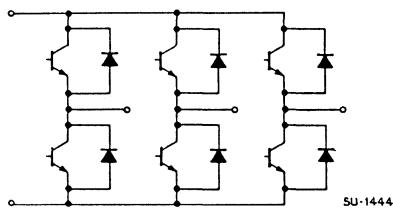
Applications	Type and Functions
SOLENOID/HAMMER/NEEDLE/RELAY 	L294 – Switch-Mode Solenoid Driver L295 – Dual Switch-Mode Solenoid Driver L601/2/3/4 – Darlington Arrays L702 – 2A Quad Darlington Array L3654S – Printer Solenoid Driver L5832 – Solenoid Controller L6212 – High Current Solenoid Driver L6221A/N – Quad Darlington Switches L6222 – Quad Transistor Switch L6503 – Hammer Solenoid Controller L6504 – Solenoid Controller L7150/52/80/82 – Quad Darlington Switches L9222 – Quad Inverting Transistor Switch L9305A/C – Dual High Current Relay Drivers L9306/C – Dual Relay Drivers L9335/6 – Solenoid Drivers L9342 – Six-Solenoid Driver ULN2001A/2A/3A/4A – Seven Darlington Arrays ULN2064B to ULN2071B – Quad Darlington Switches ULN2074B to ULN2077B – Quad Darlington Switches ULN2801A/2A/3A/4A/5A – Eight Darlington Arrays ULQ2001R/2R/3R/4R – Seven Darlington Arrays
UNIPOLAR STEPPER MOTORS 	L297/A – Stepper Motor Controllers L702 – 2A Quad Darlington Switch L6100/1/2 – 100V-1A Quad DMOS Power Switch L6506 – Current Controller for Stepping Motors L7150/52/80/82 – Quad Darlington Switches ULN2064B to ULN2071B – Quad Darlington Switches ULN2074B to ULN2077B – Quad Darlington Switches
BIPOLAR STEPPER MOTORS 	L297/A – Stepper Motor Controllers L298N – Dual Full Bridge Driver L6202 – 1.5A DMOS Full Bridge Driver L6203 – 3A DMOS Full Bridge Driver L6207 – Dual Full Bridge Driver L6209 – 3A Full Bridge Driver With Diodes L6210 – Dual Schottky Diode Bridge L6217/A – Stepper Motor Driver L6506 – Current Controller for Stepping Motors MC3479C – Stepper Motor Driver PBL3717A – Stepper Motor Driver GS-D200 – Switch-Mode Stepper Motor Driver (Complete Module)
BRUSHLESS MOTORS 	L6230 -- Bidirectional Three-Phase Brushless DC Motor Driver L6231 – Three-Phase Brushless DC Motor Driver L6233 – Phase Locked Frequency Controller TDA8116 – Four Phase Brushless Motor Driver

PRODUCT SELECTOR (Integrated Circuits)

Applications	Type and Functions
DC MOTORS 	L290 – Tachometer Converter L291 – 5 Bit D/A Converter and Position Amplifier L292 – Switch-Mode Driver for DC Motors L149 – 4A Linear Driver L165 – 3A Power Operational Amplifier L272/M – Dual Power Operational Amplifiers L2720/2 – Low Drop Dual Power Operational Amplifiers L293/E – Push-Pull Four Channel Drivers L293C – Push-Pull Four Channel/Dual H-Bridge Driver L293D – Push-Pull Four Channel Driver With Diodes L298N – Dual Full-Bridge Driver L9350 – Low Saturation Driver TDA7272 – Full Bridge DC Motor Regulator TDA8115 – Dual Motor Driver
DISPLAYS 	M5450/1 – Led Display Drivers M5480/81/82 – Led Display Drivers L3654S – Printer Solenoid Driver L601/2/3/4 – Darlington Arrays ULN2001A/2A/3A/4A – Seven Darlington Arrays ULQ2001R/2R/3R/4R – Seven Darlington Arrays
SPECIAL FUNCTIONS 	AM26LS31 – Quad High Speed Differential Line Driver AM26LS32/3 – RS422 and RS423 Quad Differential Line Receivers MC1488 – RS232C Quad Line Driver MC1489/A – Quad Line Receiver DAC0806/7/8 – 8 Bit D/A Converters AM6012/A – 12 Bit High Speed Multiplying D/A Converters L6570A/B – 2-Channel Floppy Disk Read/Write Circuits
POWER SUPPLIES  S - 9 574	L200 – Adjustable Voltage and Current Regulator L296/P – High Current Switching Regulators L387A – Very Low Drop 5V Regulator L4901/2/3/4 – Dual 5V Regulators with Reset L4920/1 – Very Low Drop Adjustable Regulators L4941 – Very Low Drop 1A Regulator L4960/2 – Power Switching Regulators SG1524/1525/1527/2524/2525/2527/3524/3525/3527 – Regulating Pulse width modulator TDA4601 – Switch-Mode Power Supply Controller TDA8130/2 – Current Mode PWM Controllers TL7700 series – Supply Voltage Supervisors UC1840/2840/3840 – Programmable, Off-Line, PWM Controllers UC1842/3/4/5 - UC2842/3/4/5 - UC3842/3/4/5 – Current Mode PWM Controllers

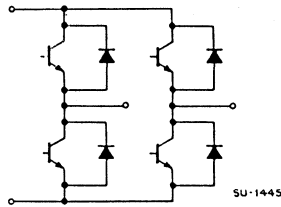
PRODUCT SELECTOR (Transistors, Diodes and TO-240 Modules)

3 PHASE BRIDGE INVERTER



380V ~		220V ~		96V		48V	
Type	Nom. KVA	Type	Nom. KVA	Type	Nom. KVA	Type	Nom. KVA
SGS30DA070D	36	SGS50DA045D	45	SGS100DA025D	20	SGS150MA010D1	12
SGS25DB080D	30	SGS40TA045D	36	BUR51	5.0	BUR50	3.5
SGS15DB080D	22	SGS30DB045D	22	2N7056	2.5	SGSP571/471	1.5
BUX98C	13	SGS30MA050D1	18	SGSP577/477	2.5	SGSP561/461	1.0
BUX48C	6	SGSD310	8	SGSP567/467	1.0		
		SGSD00030	7				
		BUX98A	8				
		BUX48A	4.5				
		SGSP574/474	5				
		SGSP579/479	3				
		2N7059	4				
		BUW42	6				
		BUW32	3.6				
		BUW22	2.2				
SGS35R120	30	SGS60R40	26	SGS20R20	6.0	SGS20R10	3.0

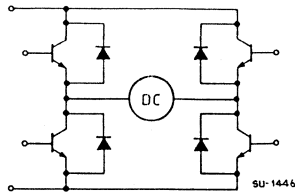
SINGLE PHASE BRIDGE INVERTER



380V ~		220V ~		96V		48V	
Type	Nom. KVA	Type	Nom. KVA	Type	Nom. KVA	Type	Nom. KVA
SGS30DA070D	30	SGS50DA045D	37	SGS100DA025D	20	SGS150MA010D1	12
SGS25DB080D	24	SGS40TA045D	30	BUR51	5	BUR50	3.5
SGS15DB080D	15	SGS30DB045D	15	2N7056	2.5	SGSP571/471	1.5
BUX98C	10	SGS30MA050D1	15	SGSP577/477	2.5	SGSP561/461	1.0
BUX48C	5	SGSD310	7	SGSP567/467	1.0		
		SGSD00030	6				
		BUX98A	6				
		BUX48A	3				
		SGSP574/474	5				
		SGSP579/479	2.5				
		2N7059	4				
		BUW42	5				
		BUW32	3				
		BUW22	1.8				
SGS35R120	30	SGS60R40	26	SGS20R20	6.0	SGS20R10	3.0

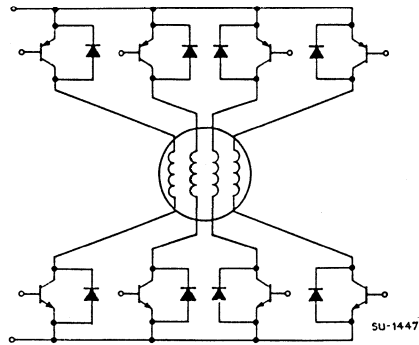
PRODUCT SELECTOR (Transistors, Diodes and TO-240 Modules)

DC MOTORS



220V ~		96V		48V		28V	
Type	Nom. KVA	Type	Nom. KVA	Type	Nom. KVA	Type	Rating, A
SGS50DA045D	15	SGS100DA025D	10	SGS150MA010D1	3.5	SGSP592/492	25.0
SGS40TA045D	12	BUR51	3.0	BUR50	2.0	SGSP482/382	15.0
SGS30MA050D1	4.0	SGSP577/477	1.0	SGSP571/471	0.7	SGSP422/322	6.5
SGSP574/474	1.8	SGSP567/467	0.5	SGSP561/461	0.4	SGSP358	4.0
SGSP579/479	1.5	2N7056	1.0				
2N7059	1.5						
SGSD310	4.0						
BUX98A	5.0						
BUX48A	2.5						
BUW42	2.5						
BUW32	1.5						
BUW22	1.0						

STEPPER MOTORS



200V		96V		48V		28V	
Type	Config. Rating, A	Type	Config. Rating, A	Type	Config. Rating, A	Type	Config. Rating, A
BUR20	25.0	BUR50	35.0	SGSD100	10.0	BDW93	5.0
BUV21	12.0	BUV20	25.0	SGSD200	-10.0	BDW94	-5.0
BUV22	10.0	BUX10P	10.0	BDW93C	5.0	SGSP386	25.0
BUX11	6.0	BDX53F	2.0	BDW94C	-5.0	SGSP592/492	25.0
SGSP573/473	13.0	BDX54F	-2.0	BDX53C	3.0	SGSP482/382	15.0
SGSP463/363	6.5	SGSP577/477	13.0	BDX54C	-3.0	SGSP422/322	6.5
SGSP516/316	3.5	SGSP467/367	6.5	SGS132	4.0	SGSP358	3.0
		SGSP517/317	3.5	SGS137	-4.0		
				SGSP572/472	19.0		
				SGSP562/362	10.0		
				SGSP512/312	4.5		
				SGSP352	3.0		

PRODUCT SELECTOR (Transistors, Diodes and TO-240 Modules)

PART NUMBER IDENTIFICATION

SGS__DB__	types are	TO-240 Darlington Transistor Half-bridge modules with fast freewheel diode.
SGS__DA__	types are	TO-240 Darlington Transistor Quarter-bridge modules with fast freewheel diode.
SGS__TA__D	types are	TO-240 Transistor Quarter-bridge modules with fast freewheel diode.
SGS__MA__D1	types are	TO-240 Power Mos Transistor Quarter-bridge modules with normal freewheel diode.
SGSD__	types are	TO-3 and SOT-93 Darlington Transistors with inactive collector-emitter diode.
SGSP5__	types are	TO-3 Power Mos Transistors.
SGSP4__	types are	SOT-93 Power Mos Transistors.

SEMI-CUSTOM TRANSPACK

The existing standard Transpack range of power modules consists of 15 bipolar versions and 4 types containing POWER MOS devices. These types cover a large quantity of customer needs but the increase in sophistication of high power designs has led to numerous requests for minor variations to SGS standard types.

With the introduction of the SGS Semi-Custom Series, customers can include unique design variations and end up with a high power module which is customised to their own needs. To support this new phase of high power modules SGS has identified 40 basic designs utilising advanced silicon manufactured on our high volume lines. The maximum ratings for each design are based on using the maximum number of chips within the chosen internal layout.

For maximum flexibility SGS Semi-Custom Transpack modules can be configured to the customers own unique circuit design using SGS power devices, this option is limited only by some straightforward design rules, and the package pinning.

Customer supplied silicon can also be included in this customised option.

This Product Selector Guide illustrates only a small selection of products and package types available from SGS. Consult your local SGS sales office for further information.

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ALPHANUMERICAL INDEX

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BUR50	HIGH CURRENT, HIGH SPEED, HIGH POWER NPN TRANSISTOR	889
BUR50S	HIGH CURRENT, HIGH SPEED, HIGH POWER NPN TRANSISTOR	889
BUR51	HIGH CURRENT, HIGH SPEED, HIGH POWER NPN TRANSISTOR	895
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BUV48	HIGH VOLTAGE POWER SWITCHING NPN TRANSISTOR	925
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BUW22A	HIGH VOLTAGE POWER SWITCHING PNP TRANSISTOR	907
BUW22AP	HIGH VOLTAGE POWER SWITCHING PNP TRANSISTOR	907
BUW22P	HIGH VOLTAGE POWER SWITCHING PNP TRANSISTOR	907
BUW32	HIGH VOLTAGE POWER SWITCHING PNP TRANSISTOR	915
BUW32A	HIGH VOLTAGE POWER SWITCHING PNP TRANSISTOR	915
BUW32AP	HIGH VOLTAGE POWER SWITCHING PNP TRANSISTOR	915
BUW32P	HIGH VOLTAGE POWER SWITCHING PNP TRANSISTOR	915
BUW42	HIGH VOLTAGE POWER SWITCHING PNP TRANSISTOR	921
BUW42A	HIGH VOLTAGE POWER SWITCHING PNP TRANSISTOR	921
BUW42AP	HIGH VOLTAGE POWER SWITCHING PNP TRANSISTOR	921
BUW42P	HIGH VOLTAGE POWER SWITCHING PNP TRANSISTOR	921
BUX48	HIGH VOLTAGE POWER SWITCHING NPN TRANSISTOR	925
BUX48A	HIGH VOLTAGE POWER SWITCHING NPN TRANSISTOR	925
BUX48B	HIGH VOLTAGE POWER SWITCHING NPN TRANSISTOR	933
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NEW DEVELOPMENTS IN INTELLIGENT POWER TECHNOLOGY

Recent developments in power IC technology greatly expand the capabilities of integrated circuits combining control circuits and high power drive stages. This note describes the new power processes, new packages and the latest generation of power ICs.

While chips integrating both signal and power elements have been with us for several years, recent developments have greatly expanded the capabilities of these technologies. With the latest processes designers can integrate many circuits that were previously uneconomic or simply impossible. Moreover, the enlarged horizons of intelligent power technology—and packaging—are prompting new trends in the partitioning of systems.

Not only are intelligent power ICs becoming more common, they are also becoming more intelligent, to the point where designers can aim to integrate a complete power subsystem. Moreover, the current and voltage capabilities of these technologies have increased dramatically, enlarging the field of applications.

Since system designers are often responsible for partitioning electronic systems and specifying new devices it is important for them to understand the capabilities of the latest technologies. This is now more true than ever, both because IC technology has advanced so rapidly and because the latest generation of power ICs have a much greater 'system' content.

THE NEW TECHNOLOGIES

Intelligent power technologies have evolved from two earlier species: linear IC technology and discrete transistor technology.

Processes of the first type are enhancements of the basic planar IC structure where all of the connections are on the top surface of the chip. In contrast,

those intelligent power technologies that have been developed from discrete transistor processes have a collector, or drain, contact on the lower surface of the die. A fundamental consequence of this structural difference is that with processes of the first type it is possible to integrate any number of isolated power transistors and interconnect them in any configuration. SGS calls these Multipower processes.

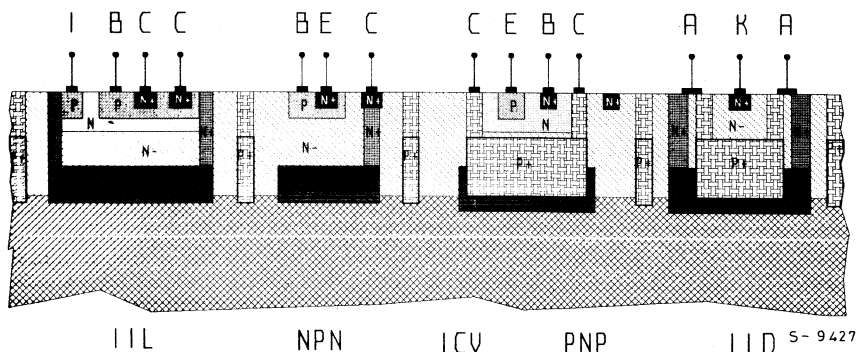
Where a bottom contact is used it is only possible to integrate a single power transistor, or several with common collectors (or drains), therefore configurations such as the H-bridge cannot be integrated but higher current and voltage capability of several hundred volts is possible. SGS has named this type of process VIPower™ (Vertical Intelligent Power). Both technologies can be further subdivided into those which are pure bipolar and mixed technologies containing a mixture of bipolar and MOS structures. In both fields significant progress has been made recently.

PURE BIPOLAR MULTIPOWER PROCESSES

Just how far bipolar technology has advanced is illustrated by SGS' new Multipower-S²P² and Multipower-HDS²P² processes.

Multipower-S²P² (figure 1) is a 60V process that integrates bipolar linear, IIL logic, NPN and PNP power transistors and a new low leakage diode structure.

Fig. 1 - Multipower-S²P², a 60V bipolar process, combines linear, IIL logic, ICV PNP power transistors and low leakage diodes.



One of the most important characteristics of this process is that it offers a new Isolated-Collector Vertical PNP (ICV PNP) structure which is much closer to discrete PNP transistors in performance terms than the usual lateral PNP type. These ICV PNP transistors provide, in fact, a current density of 0.8A/mm^2 at $V_{\text{sat}} = 1\text{V}$ — compared to 2A/mm^2 for NPN types — and a cutoff frequency of 20 to 30MHz.

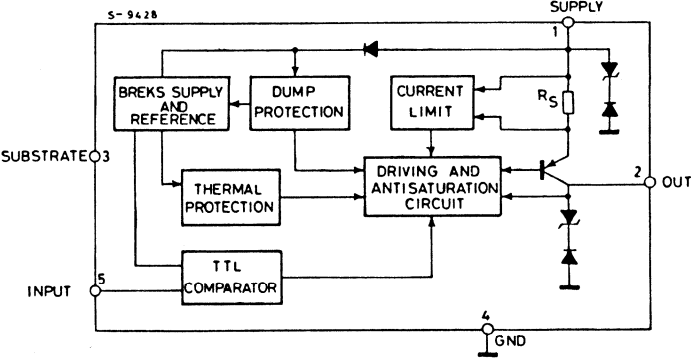
The possibility of integrating high performance power PNP transistors on an intelligent power IC allows designers to choose any output configuration. Moreover, the ICV PNPs low voltage drop can be exploited for applications where drop-out is a critical parameter. Another advantage, specifically for automotive applications, is that an ICV PNP output stage can withstand battery reversal

indefinitely.

Another important feature of Multipower-S²P² is the inclusion of a new low leakage diode structure that has a parasitic PNP gain about four orders of magnitude lower than conventional structures. This new structure is ideal for the recirculation diodes in high power ICs driving inductive loads such as motors and solenoids.

The first device to be produced with this process is a relatively simple high side driver, the L9350, originally designed to the specification of a customer in the automotive electronics market (figure 2). An ICV PNP output transistor is used in this device to obtain very low saturation, high gain (about 30 with 1A output current) and the ability to withstand load dump transients.

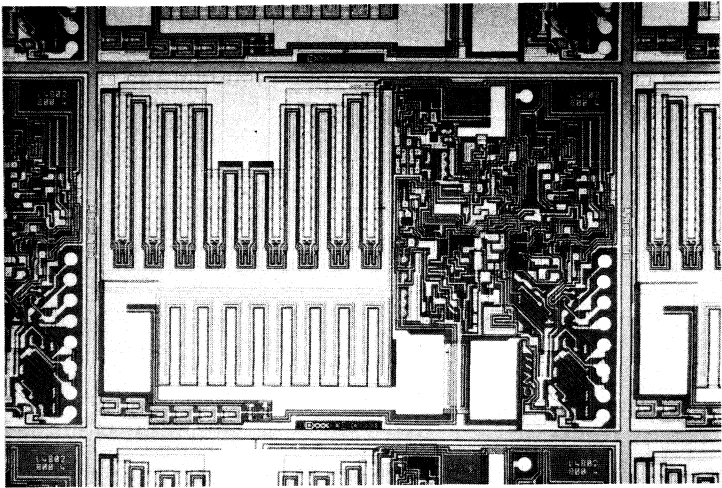
Fig. 2 - Designed primarily for automotive applications, the L9350 high side solenoid driver exploits Multipower-S²P²'s ICV PNP structure to obtain very low saturation voltage.



Another device realized with this technology is a single-chip alternator regulator (figure 3) which integrates for the first time all of the power and signal devices needed to regulate the output voltage

of a car alternator. Perhaps the most interesting aspect of this IC is that it needs no external components.

Fig. 3 - Another Multipower-S²P² design, the L9480 alternator regulator is a circuit which needs no external components.

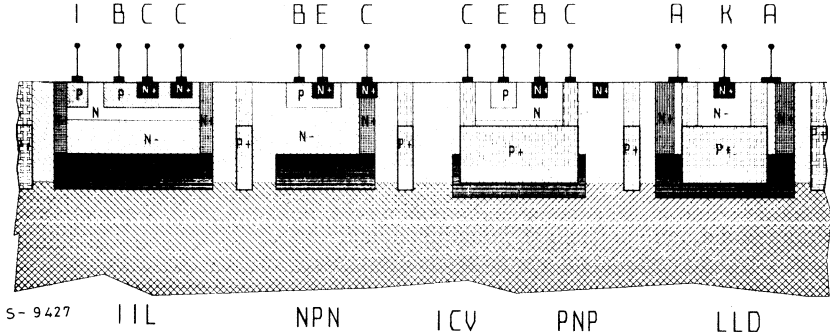


Multipower-HDS²P³ (figure 4) is a similar pure bipolar process. Like Multipower-S²P² it integrates linear, IIL, LLD and ICV PNP structures. In addition it also offers ECL logic.

But the most important characteristic of this process is high density. Dimensioned for 20V capability, it is aimed at low voltage applications where more complex signal processing circuits are needed — up to 270 IIL gates can be shoehorned into one square millimeter of silicon.

Multipower-HDS²P² is also characterized by an

Fig. 4 - Multipower HDS² P² is a 20V process characterized by very high density in the signal part (270 IIL gates/mm²) and exceptionally high current density.



MIXED MULTIPOWER TECHNOLOGY

Another area where remarkable progress has been made is in mixed bipolar/MOS technology. Though several mixed technologies of the 'vertical' type are available, a much more significant development is SGS' Multipower-BCD process (figure 5), which combines linear, CMOS logic and DMOS power transistors without placing any limit on the number and connection of the power devices.

Thanks to the DMOS power transistors this process allows efficiencies above 95% and switching frequencies up to 500kHz. In addition, there are no

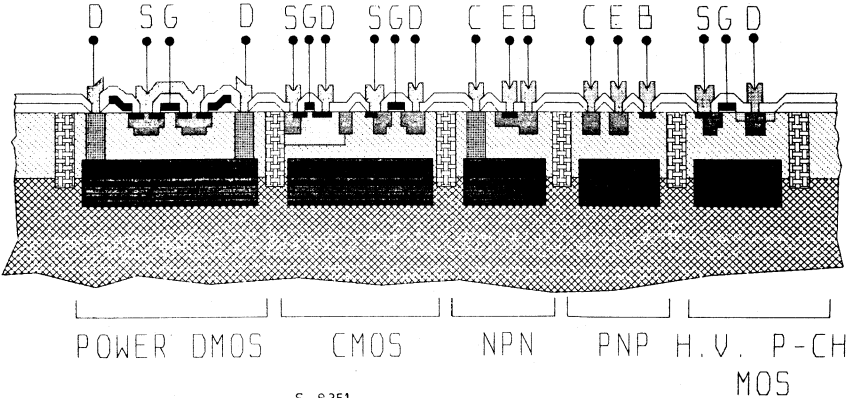
exceptionally high current density: 6A/mm² for NPN transistors; 2A/mm² for PNP (at V_{sat}= 1V and H_{fe}= 10).

This process has been applied to produce a custom stepper motor control/drive chip, where the high density of the process allows translator and chopper circuits to be integrated economically on the power drive chip. It is also used for a new 1.5A voltage regulator, the L4940, where the ICV PNP provides very low voltage drop and low quiescent current.

secondary breakdown limitations, paralleling of devices is simpler and there is an intrinsic 'fast' recirculation diode in the power DMOS structure which is adequate for most applications.

For intelligent power devices the very high efficiency of power DMOS is an important advantage. The power output of a chip is limited by the maximum dissipation allowed in the package. By reducing dissipation in the chip it is possible to put power ICs in low cost packages with modest power handling capability. Alternatively, packaged in existing high power packages, DMOS chips can deliver hitherto unreachable power levels.

Fig. 5 - A mixed technology, Multipower-BCD integrates linear, CMOS logic and power DMOS devices on the same chip. Unlike other mixed technologies it places no limit on the number or connection of the power transistors.



Moreover, the saturation loss of a power DMOS transistor can be reduced by increasing the area. Designers therefore have the possibility of trading costly copper and aluminum, materials used in packages and heatsinks, for silicon, which tends to decrease in cost as wafer fabrication techniques are improved and automated.

Another important way in which Multipower-BCD differs from pure bipolar technologies is that it allows the mixing of low voltage and medium voltage elements on the same chip: lateral DMOS transistors with a breakdown voltage of 60V can be

produced in an epitaxial layer dimensioned for 20V linear and CMOS circuits.

The first product to be developed using this process is the L6202 motor driver (figure 6), which uses four DMOS power transistors in a H-bridge output stage.

Assembled in a powerdip package this device can deliver 1.5A at 54V with no external heatsink. In the photograph, figure 7, the four DMOS power transistors can be clearly seen in the lower part of the die.

Fig. 6 - A motor driver chip, the L6202, is the first product to be realized with the Multipower-BCD process. The DMOS H-bridge output of this chip delivers 1.5A at 54V but thanks to the high efficiency no heatsink is needed.

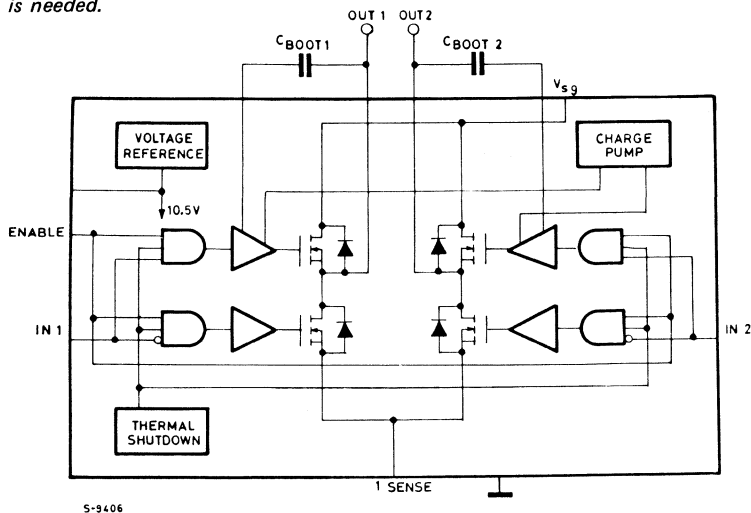
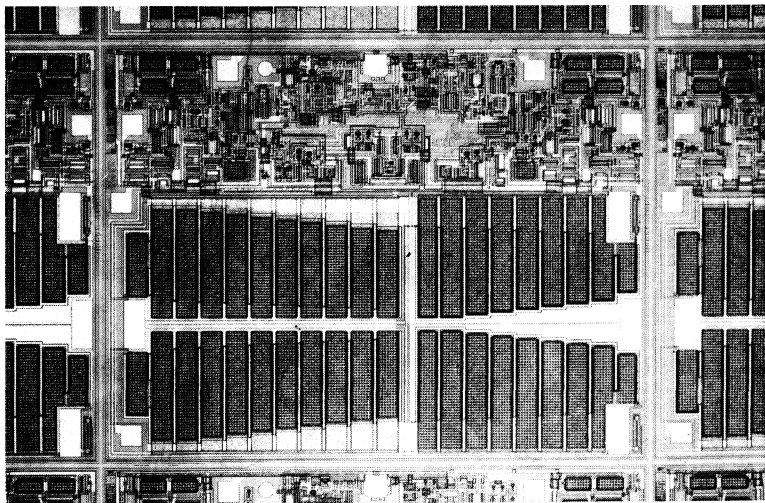


Fig. 7 - The four DMOS power transistors occupy about 2/3 of the L6202 die.



VERTICAL PROCESSES

While the "Multipower" processes are more versatile SGS is also developing bipolar and mixed vertical technologies, called VIPower-M1 and VIPower-M2.

VIPower-M1 (figure 8) combines 400V NPN power transistors and bipolar low voltage (up to 30V V_{ce0}) drive circuits, while VIPower-M2 (figure 9) will offer 80V DMOS power transistors and mixed CMOS/bipolar drive circuits.

Though these processes cannot be used for devices with bridge and half-bridge output stages, they offer higher voltage capability and VIPower-M2 features a lower ON resistance than Multipower-BCD.

VIPower-M2 is suitable for applications such as high current high side drivers and DC-DC converters while VIPower-M1 is suitable for applications like high voltage solenoid drivers, motor drives and off-line power supplies.

Fig. 8 - VIPower-M1 technology integrates 400V NPN power transistors and 30V drive circuitry.

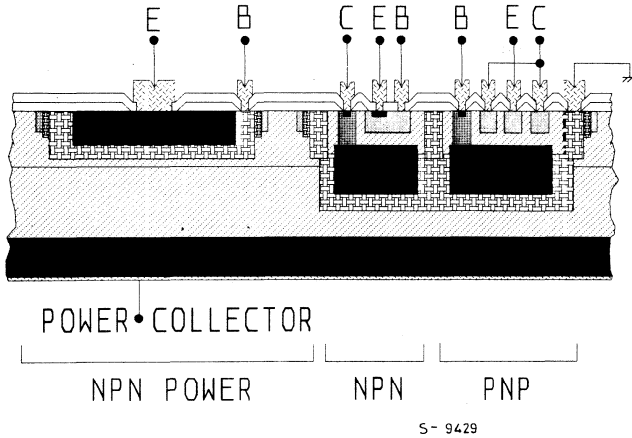
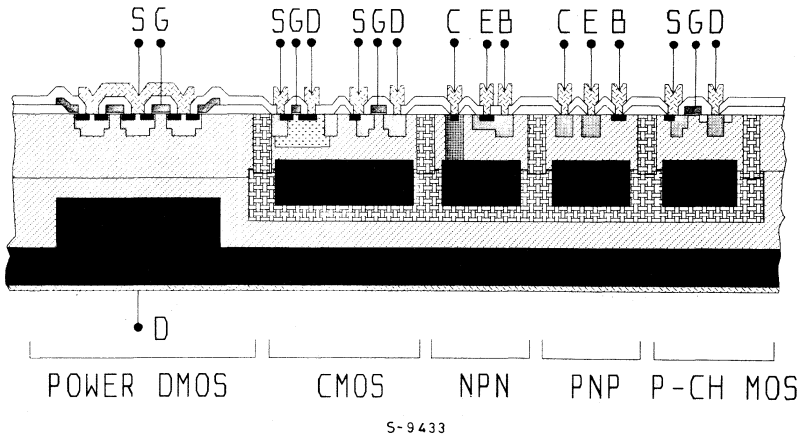


Fig. 9 - Another 'vertical' power process, VIPower-M2 combines 80V DMOS power transistors and mixed CMOS/bipolar drive circuits.



The first products proposed in VIPower-M1 are 400V 5A to 10A NPN darlington switches (figure 10) with direct logic compatible drive. In addition on chip thermal, overcurrent and overvoltage

sensing can shutdown the power switch and provide a diagnostic output to inform the system microprocessor of the overload condition.

CHOOSING THE RIGHT PROCESS

The choice of process depends on the output stage configuration, current, voltage and the complexity of the signal processing section.

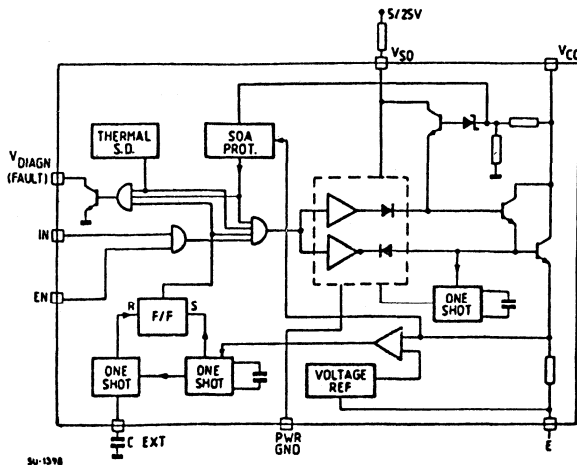
Mixed bipolar/DMOS is the best for lower current devices where the signal processing circuitry is very complex. Pure bipolar processes, in contrast, are better for low voltage, high current applications because the current density is much greater. However future developments of Multipower-BCD are likely to erode this advantage in a few years.

One area where mixed technology will not replace pure bipolar processes completely is automotive electronics. This is because of the high energy load dump transients which occur on the battery rail.

To withstand these transients a DMOS technology must have a BV_{DSS} breakdown voltage greater than the peak dump voltage, while a bipolar NPN transistor can be turned off to take advantage of the BV_{CBO} breakdown voltage, which is much greater than the BV_{CE0} breakdown voltage.

Mixed bipolar/DMOS technology will become increasingly important in very complex power devices. In the near future the Multipower-BCD process will be applied to produce specialized peripheral drivers, optimized for one load type. Multipower-BCD is ideal for these applications because it offers high precision bipolar linear circuits (for signal conditioning etc), high density CMOS (for complex logic) and high efficiency DMOS (for the power stage).

Fig. 10 - VIPower-M1 will be used to produce a 400V/10A NPN darlington switch which connects directly to standard logic.



POWER PACKAGE DEVELOPMENTS

For a power IC the package is extremely important, since it determines both the power capability and the cost.

At present SGS assembles most high power ICs of the Multipower type in power-tab packages like the Pentawatt, Heptawatt and Multiwatt® (which are attached to a heatsink), or in special DIP packages with a leadframe designed to reduce thermal resistance. All of these packages are 'insertion' types. However, several trends have now emerged which call for the design of completely new power packages.

Firstly, the increasingly widespread use of surface mounting techniques and automatic assembly has brought the need for surface mounting power packages. For medium power (up to 2W) one solution, which SGS already has in production, is a plastic chip carrier with a special leadframe.

Derived from the 44-lead PCC, this package uses 33 leads for connections and the other 11 leads to transfer heat to the substrate (figure 11). This package has a junction-case thermal resistance of less than 7°C/W, allowing dissipation up to 2W.

For higher power devices development is concentrated on a new generation of packages. One package family being studied (figure 12) has a junction-case thermal resistance of less than 5°C/W, 3-17 pins and a lead spacing of 50mils. These packages will have an SO-width body and gull-wing leads, allowing the use of SO package handling equipment. The low thermal resistance of these packages is obtained by a copper heat spreader on the lower surface of the package. When the package is soldered in place the spreader is in contact with the substrate. Clearly the amount of power that can be dissipated in the device depends on the conductivity of the substrate.

Fig. 11 - The leadframe of a plastic chip carrier can be modified to reduce thermal resistance. This '33+11' lead configuration allows power dissipation up to 2W

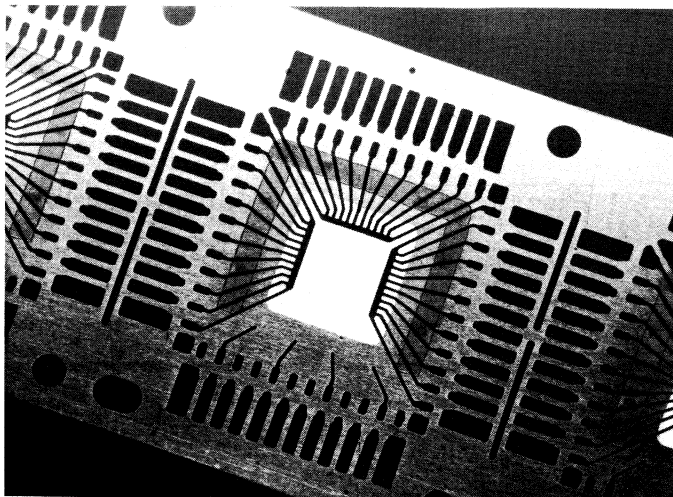
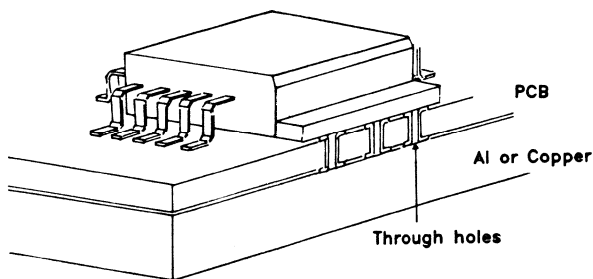


Fig. 12 - For power dissipation above 2W new surface mounting packages are being developed. This type, compatible with SO-package handling equipment, has a thermal resistance of about 5°C/W.



S-9434

In view of this trend there is now considerable interest in high conductivity substrates and the various alternatives, such as a plastic board bonded to an aluminum or copper sheet. Plated-through holes in the PCB reduce the thermal resistance between the package and the metal sheet.

Another development area is the inclusion of a copper heat spreader on the under-side of plastic chip carriers. These power chip carriers will, like many new packages, be pre-molded types, which eliminates stress on the die caused by polymerization shrinkage of the molding resin.

New packaging concepts are being studied for chips like the L9480 which need no external components. Since there is no need to mount such devices on a substrate they will probably be assembled in packages designed to be bolted to the load (figure 13) and equipped with 'Faston'-type connectors.

Fig. 13 - New packaging concepts are being studied for 'silicon-only' circuits where there is no point in mounting the device on a conventional substrate because there are no other components needed.

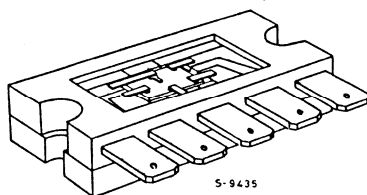
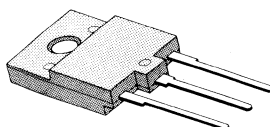


Fig. 14 - In the ISOWATT-218 package the copper frame is completely surrounded by molding resin to isolate the device from the heatsink.



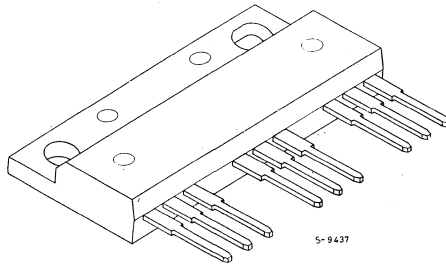
ISOLATED PACKAGES

ICs produced using VIPower™ technology pose a different problem because the lower surface of the die is the collector (or drain) contact and because greater heat dissipation capability is needed. For these ICs SGS is developing multi-lead versions of the ISOWATT-218™ plastic package (figure 14) where a copper frame is

completely surrounded by molding resin — even on the lower surface — to provide electrical isolation. Low thermal resistance is assured by the thickness and high thermal conductivity of the resin.

One of the new packages in development is shown in figure 15. This packages will achieve better than 2.5°C/W thermal resistance and 2500V AC isolation.

Fig. 15 – Isolated packages with higher pin counts are in development



A HIGH EFFICIENCY, MIXED-TECHNOLOGY MOTOR DRIVER

A new mixed technology called Multipower-BCD allows the integration of bipolar linear circuits, CMOS logic and DMOS power transistors on the same chip. This note describes a H-bridge motor driver IC realized with this technology.

The miniaturization and integration of complex systems and subsystems has led in recent years to the implementation of monolithic circuits integrating logic functions and power sections.

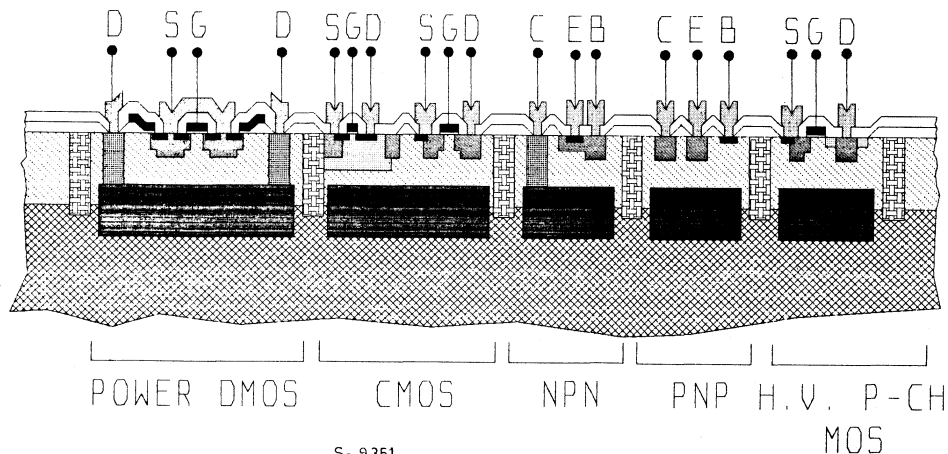
For these applications SGS has developed a new technology called Multipower BCD which allows the integration on the same chip of isolated Power DMOS elements, bipolar transistors and C-MOS logic.

Thanks to high efficiency, fast switching speed and the absence of secondary breakdown, this technology is particularly suitable for fast, high current

solenoid drivers and high frequency switching motor control. The free-wheeling diode intrinsic to the DMOS structure (necessary if the device drives an inductive load) and the great flexibility available in the choice of the logic and driving section components allow the complete integration of power actuators without further expense in silicon area—and a compact implementation of complex signal functions.

This technology has been applied to produce a switching power driver — the L6202/3 — capable of delivering 4A per phase, which is suitable for speed and position control in D.C. motor applications.

Fig. 1 – A schematic cross section of Bipolar, C-MOS, DMOS structures (BCD)



MULTIPOWER BCD TECHNOLOGY

Multipower BCD technology combines the well known vertical DMOS silicon gate process, used for discrete POWER MOS devices, and the standard junction isolation, sinker and buried layer process. The architecture of the process is centred around the vertical DMOS silicon gate, a self aligned structure, which guarantees short channel length (1.5µm) with consequent low $R_{DS(ON)}$ for the device.

In standard IC technologies the voltage capability is determined essentially by the thickness of the epitaxial layer and it is the same for signal and power components. But if the epi thickness is increased to allow the inclusion of high voltage transistors even the linear dimension of small signal transistors must be increased proportionally. In contrast MULTIPOWER BCD permits the realization of high voltage lateral DMOS structures in an epi-layer dimensioned for low voltage bipolar linear elements. Thus it is possible to mix on the same die very dense CMOS logic, high precision bipolar linear circuits, very efficient DMOS power devices and high voltage lateral DMOS structures.

In this way the constraints which limit the complexity of signal processing circuits that can be integrated economically on a high chip are greatly reduced.

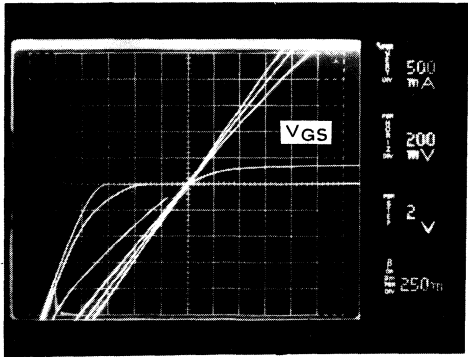
The active structures available in Multipower BCD technology are represented in fig. 1.

Within the vertical DMOS is indicated an intrinsic diode that can operate as a fast free-wheeling diode in switch mode applications. In fact DMOS, as a result of the way by which it is realized, is almost a symmetrical bidirectional device. That is, it can operate with the electrical I-V characteristic shown in the 3rd quadrant of fig. 2; that is, as a controlled resistor of value decreasing inversely with the gate source voltage applied to the power to which it is associated, up to a minimum equal to the $R_{DS(ON)}$ of the device itself, shunted by the body-drain diode intrinsic to the structure that limits the negative excursion of V_{DS} . Of the devices represented in fig. 1 the table 1 lists the electrical characteristics.

Table 1 : DEVICES IN MULTIPOWER BCD TECHNOLOGY

• Vertical DMOS • Lateral DMOS • P-channel with Drain Extension • Bipolar NPN • Bipolar PNP • C-MOS N and P-channel	$BV_{DSS} > 60V$ $BV_{DSS} > 100V$ $BV_{DSS} > 85V$ $LV_{CEO} > 20V$ $LV_{CEO} > 20V$ $BV_{DSS} > 20V$	$V_{TH} \cong 3V$ $V_{TH} \cong 3V$ $V_{TH} \cong 3V$ $\beta = 35$ $\beta = 20$ $V_{TH} \cong 3V$	$f_T > 1GHz$ $f_T > 800MHz$ $f_T > 200MHz$ $f_T > 300MHz$ $f_T > 7MHz$
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Fig. 2 - I-V characteristic of DMOS N-channel power device



THE L6202 & L6203 H-BRIDGE DRIVERS

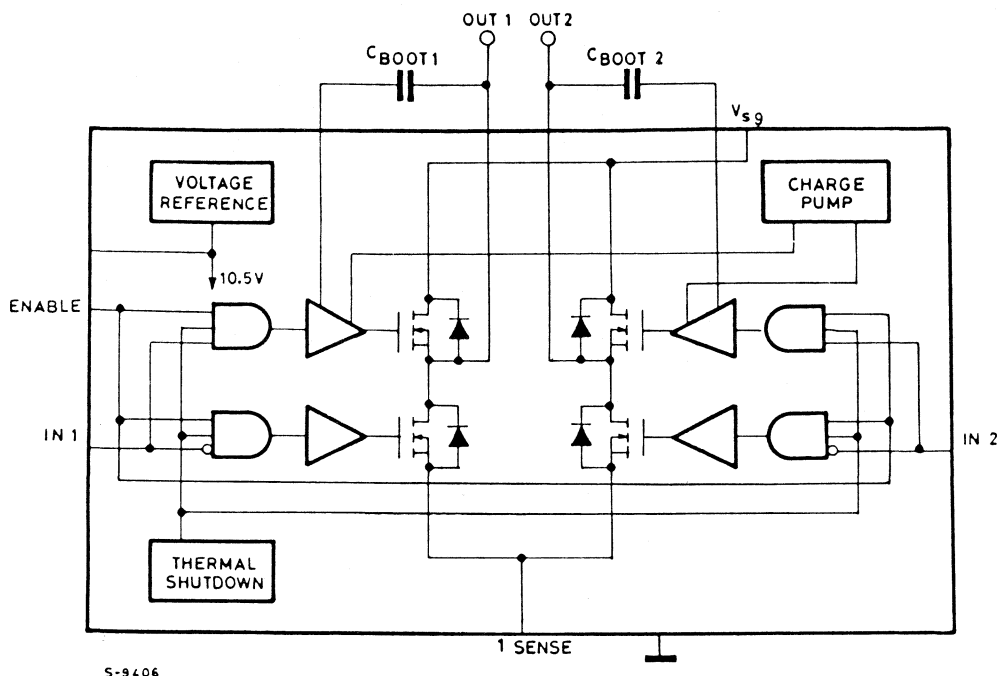
Using this technology a H-bridge IC has been realized which accepts TTL or C-MOS compatible signals and is suitable for high efficiency, high frequency switching control of DC and stepping motor. The power stage consists of four DMOS N-channel transistors with $R_{DS(ON)} \cong 0.3\Omega$.

When this device is supplied with the maximum voltage of 60V it can deliver a DC current of 1.5A in a standard DIP.16 (L6202) and up to 5A in a MULTIWATT package (L6203).

The device can also operate with a peak current of 8A for a time interval essentially determined by the time constant of heat propagation (< 200 ms).

The system diagram representing the internal function blocks and external components (outside the dashed line) is shown in fig. 3.

Fig. 3 - L6202-6203 BLOCK DIAGRAM



The integrated circuit has 3 Inputs: Enable, Input 1, Input 2. When Enable is "low" all power devices are off; when it is "high" their conduction state is controlled by the logic signals Input 1 and Input 2 that drive independently a single branch of the full bridge. When Input 1 (Input 2) is "high" DMOS 1 (DMOS 2') is "on" and DMOS 2 (DMOS 2') is "off", when is "low" DMOS 1 (DMOS 1') is "off" and DMOS 2 (DMOS 2') is "on".

A thermal protection circuit has been included that will disable the device if the junction temperature reaches 150°C. When the thermal protection is removed the device restarts under the control of the Input and Enable signals.

ON-OFF SYNCHRONIZATION CIRCUIT

ON-OFF synchronization of the power devices located on the same leg of the bridge must prevent simultaneous conduction, with obvious advantages in terms of power dissipation and of spurious signals on the ground and on sensing resistors.

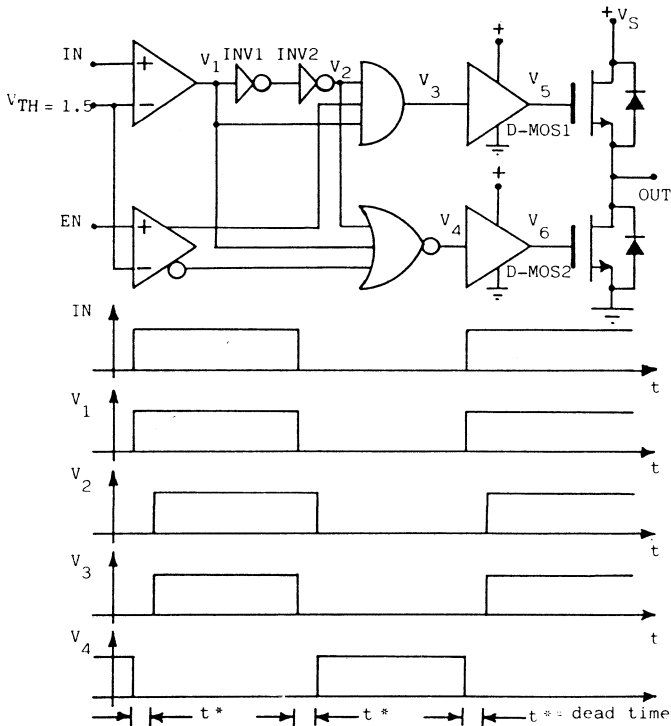
Because of the very short turn-on, turn-off times characteristic of POWER MOS devices a dead time (time in which all power transistors are "off") of 40 ns is sufficient to prevent rail-to rail shorts. The circuit that provides this time interval is shown in

fig. 4 with the voltage waveforms that explain how it works. Let us suppose Enable = "high". Because of the delay times introduced by INV1 and INV2, V2 and V3 are two waveforms contained one in the other and of polarity suitable to assure that the turn-on of a power transistor happens only after the turn-off of the other. The gate voltages V5 and V6 of DM1 and DM2 are represented in fig. 5. In fig. 3 we can see also the modality of operation of the Enable signal, charge pump and bootstrap circuits.

Concerning POWER MOS driving, it must be noted that it is necessary to assure to all DMOS N-channel a gate-source voltage of about 10V to guarantee full conduction of the POWER MOS itself. While there are no particular problems for driving the lower POWER MOS device (its terminals is referred to ground) for the upper one it is necessary to provide a gate voltage higher than the positive supply because it has the drain connected to the positive supply itself.

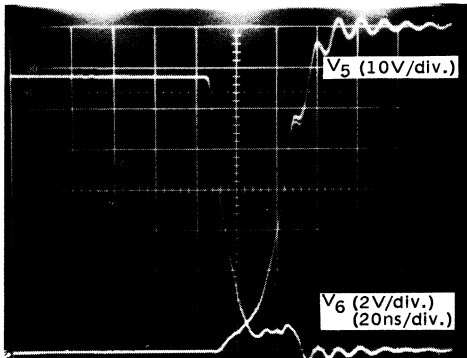
This is obtained using a system that combines a charge pump circuit, that assures DC operation, with a bootstrapping technique suitable to provide high switching frequencies. The circuit that satisfies to all these requirements is represented in the schematic diagram of fig. 6.

Fig. 4 - A schematic representation of ON-OFF synchronism circuit



S-9353/1

Fig. 5 - POWER MOS gate voltage waveforms



In the description of this circuit we can assume that C_{BOOT} is absent and IN commutes from the "low" to the "high" level.

In this condition, by means of D1, the circuit charges immediately the DMOS1 gate capacitance to V_S while the charge pump, activated by the signals IN = "low", as it can be seen in fig. 7, must supply only a voltage of about 10V.

In the switching operation it will be C_{BOOT} that

guarantees a faster turn-on of the upper POWER MOS and consequently high commutation frequencies.

In fact during the period in which DMOS2 is "on" C_{BOOT} is charged to a voltage of about 12V.

When V_{out} raises because DMOS2 is deactivated D2 and D1 became "off" while D3, that remains "on" connects the gate circuit to C_{BOOT} that raises higher than V_S and makes DMOS1 full "on" in a very short time interval (20 ns).

It must be noted that the switch M4 in the fig. 6 circuit, driven by a complementary phase respect to M3 disconnects D4, D5 and D6 from 12V when M5 goes "on" to assure the "turn-off" of DMOS1.

PERFORMANCE

One of the most important features is the very high efficiency achieved.

To appreciate the benefits of low power dissipation, and consequently of high efficiency, of a circuit realized in DMOS technology we must refer to the equivalent bipolar solution and also consider separate DC and AC operation.

Consider the typical Darlington power stage frequently used in integrated circuit and a DMOS power stages both represented in fig. 8.

where: V_S = Supply voltage, I_L = Peak load current,
 $T_{COM.} = T_{TURN-ON} = T_{TURN-OFF}$,
 f_{SWITCH} = Chopper frequency.

Because $T_{COM.}$ in DMOS case is $\ll$ than in bipolar case at a fixed frequency we have a lower dissipation or at fixed dissipation we can tolerate higher switching frequency.

Considering all these aspects, with a power device consisting of about 2200 cells we have realized DMOS power devices characterized by $R_{DS(ON)}$ 0.3Ω and by switching times t_r , t_f of 50 ns. Other characteristics of the device when is configured as shown in fig. 9 are listed in table 2.

Fig. 10 shows the supply current with no load, vs. switching frequency.

Fig. 9

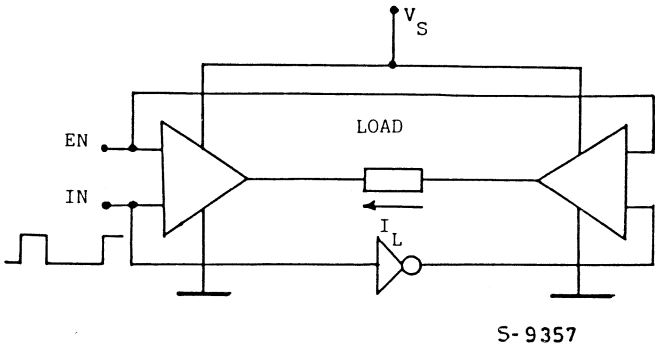
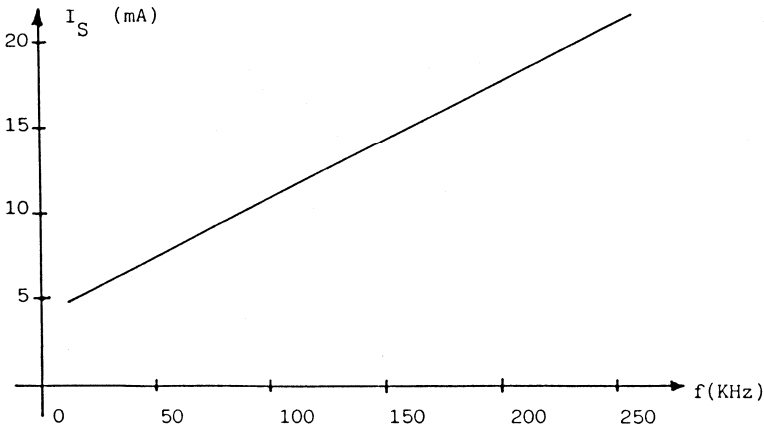


Table 2 : MAIN FEATURES OF L6202/L6203

• V_S (maximum supply voltage)	=	60V
• I_L (maximum output current)	=	1.5A DIP.16
• Efficiency	η	= 90%
• Power dissipation	P_d	= 1.5W
• t_d (turn-on, turn-off propagation delay)		= 100 ns
5A MULTIWATT package : I_L = 1.5A $f_{chopper}$ = 50KHz V_S = 54V		

Fig. 10



S-9356

STEPPER MOTOR DRIVING

Dedicated integrated circuits have dramatically simplified stepper motor driving. To apply these ICs designers need little specific knowledge of motor driving techniques, but an understanding of the basics will help in finding the best solution. This note explains the basics of stepper motor driving and describes the drive techniques used today.

From a circuit designer's point of view stepper motors can be divided into two basic types: unipolar and bipolar.

A stepper motor moves one step when the direction of current flow in the field coil(s) changes, reversing the magnetic field of the stator poles. The difference between unipolar and bipolar motors lies in the way that this reversal is achieved (Figure 1):

Fig. 1a - BIPOLAR — with one field coil and two chargeover switches that are switched in the opposite direction.

Fig. 1b - UNIPOLAR — with two separate field coils and are chargeover switch.

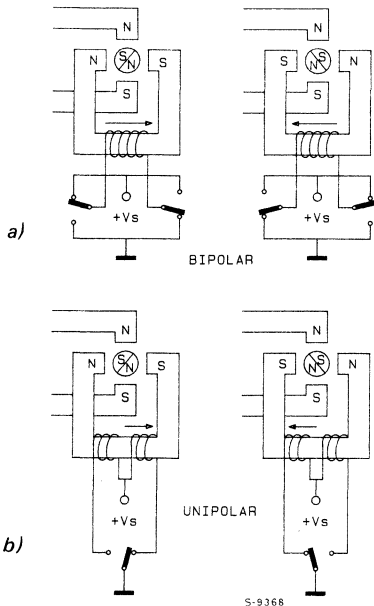
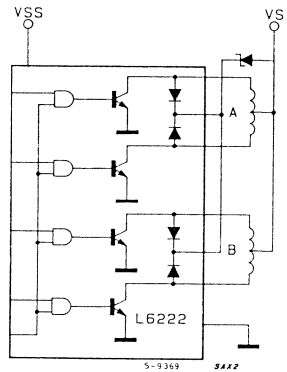
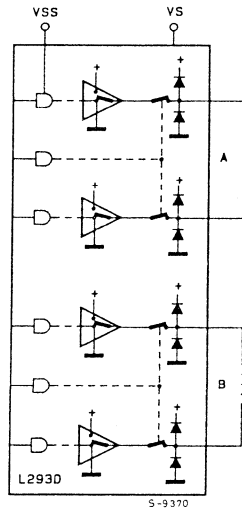


Fig. 2 - ICs for unipolar and bipolar driving

UNIPOLAR



BIPOLAR



The advantage of the bipolar circuit is that there is only one winding, with a good bulk factor (low winding resistance). The main disadvantages are the two changeover switches because in this case more semiconductors are needed.

The unipolar circuit needs only one changeover switch. Its enormous disadvantage is, however, that a double bifilar winding is required. This means that at a specific bulk factor the wire is thinner and the resistance is much higher. We will discuss later the problems involved.

Unipolar motors are still popular today because the drive circuit appears to be simpler when implemented with discrete devices. However with the integrated circuits available today bipolar motors can be driver with no more components than the unipolar motors. Figure 2 compares integrated unipolar and bipolar devices.

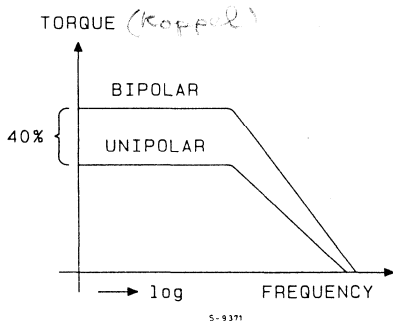
BIPOLAR PRODUCES MORE TORQUE

The torque of the stepper motor is proportional to the magnetic field intensity of the stator windings. It may be increased only by adding more windings or by increasing the current.

A natural limit against any current increase is the danger of saturating the iron core, though this is of minimal importance. Much more important is the maximum temperature rise of the motor, due to the power loss in the stator windings. This shows one advantage of the bipolar circuit, which, compared to unipolar systems, has only half of the copper resistance because of the double cross section of the wire. The winding current may be increased by the factor $\sqrt{2}$ and this produces a direct proportional affect on the torque. At their power loss limit bipolar motors thus deliver about 40% more torque (Fig. 3) than unipolar motors built on the same frame.

If a higher torque is not required, one may either reduce the motor size or the power loss.

Fig. 3 - Bipolar motors driver deliver more torque than unipolars



CONSTANT CURRENT DRIVING

In order to keep the motor's power loss within a reasonable limit, the current in the windings must be controlled.

A simple and popular solution is to give only as much voltage as needed, utilizing the resistance (R_L) of the winding to limit the current (Fig. 4a). A more complicated but also more efficient and precise solution is the inclusion of a current generator (Fig. 4b), to achieve independence from the winding resistance. The supply voltage in Fig. 4b has to be higher than the one in Fig. 4a. A comparison between both circuits in the dynamic load/working order shows visible differences.

Fig. 4 - Resistance current limiter (a) and current generator limiting

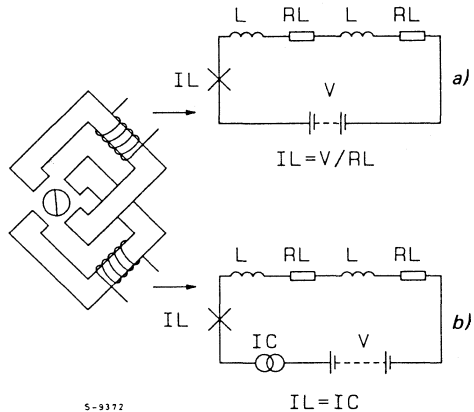
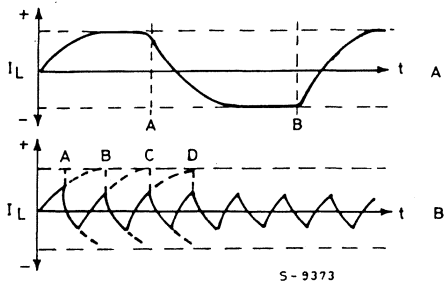


Fig. 5 - At high step frequencies the winding current cannot reach its setting value because of the continuous direction change



It has already been mentioned that this power of the motor is, among others, proportional to the winding current.

In the dynamic working order a stepper motor changes poles of the winding current in the same stator winding after two steps. The speed with which the current changes its direction in the form of an exponential function depends on the specified inductance, the coil resistance and on the voltage. Fig. 5a shows that at a low step rate the winding current I_L reaches its nominal value V_L/R_L before the direction is changed. However, if the poles of the stator windings are changed more often, which corresponds to a high step fre-

quency, the current no longer reaches its saturating value because of the limited change time; the power and also the torque diminish clearly at increasing number of revolutions (Fig. 5).

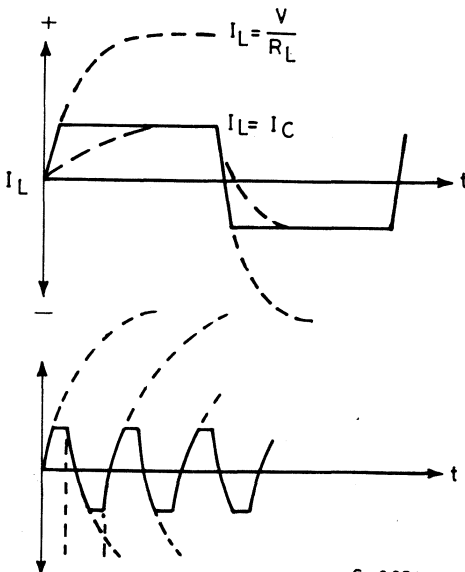
MORE TORQUE AT A HIGHER NUMBER OF REVOLUTIONS

Higher torque at faster speeds are possible if a current generator as shown in Fig. 4b is used. In this application the supply voltage is chosen as high possible to increase the current's rate of change. The current generator itself limits only the phase current and becomes active only the moment in which the coil current has reached its set nominal value. Up to this value the current generator is in saturation and the supply voltage is applied directly to the winding.

Fig. 6, shows that the rate of the current increase is now much higher than in Figure 5. Consequently at higher step rates the desired current can be maintained in the winding for a longer time. The torque decrease starts only at much higher speeds.

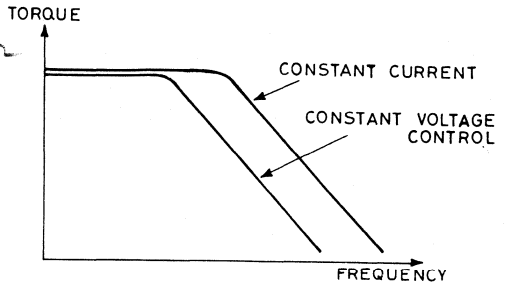
Fig. 7 shows the relation between torque and speed in the normal graphic scheme, typical for the stepper motor. It is obvious that the power increases in the upper torque range where it is normally needed, as the load to be driven draws most energy from the motor in this range.

Fig. 6 - With a step current slew it is not a problem to obtain, even at high step frequencies sufficient current in windings.



S-9374

Fig. 7 - Constant current control of the stepper motor means more torque at high frequency.



S-9375

EFFICIENCY - THE DECISIVE FACTOR

The current generator combined with the high supply voltage guarantees that the rate of change of the current in the coil is sufficiently high.

At the static condition or at low numbers of revolutions, however, this means that the power loss in the current generator dramatically increases, although the motor does not deliver any more energy in this range; the efficiency factor is extremely bad.

Help comes from a switched current regulation using the switch-transformer principle, as shown in Fig. 8. The phase winding is switched to the supply voltage until the current, detected across R_S , reaches the desired nominal value. At that moment the switch, formerly connected to $+V_S$, changes position and shorts out the winding. In this way the current is stored, but it decays slowly because of inner winding losses. The discharge time of the current is determined during this phase by a monostable or pulse oscillator. After this time one of the pole changing switches changes back to $+V_S$, starting an induction recharge and the clock-regulation-cycle starts again.

Since the only losses in this technique are the saturation loss of the switch and that of the coil resistance, the total efficiency is very high.

The average current that flows from the power supply line is less than the winding current due to the concept of circuit inversion. In this way also the power unit is discharged. This kind of phase current control that has to be done separately for each motor phase leads to the best ratio between the supplied electrical and delivered mechanical energy.

POSSIBLE IMPROVEMENTS OF THE UNIPOLAR CIRCUIT

It would make no sense to apply the same principle to a stabilized current controlled unipolar circuit, as two more switches per phase would be necessary for the shortening out of the windings during the free phase and thus the number of components would be the same as for the bipolar circuit; and moreover, there would be the well known torque disadvantage.

From the economic point of view a reasonable and justifiable improvement is the "Bi-Level-Drive" (Fig. 9). This circuit concept works with two supply voltages; with every new step of the motor both windings are connected for a short time to a high supply voltage. This considerably increases the current rate of change and its behaviour corresponds more or less to the stabilized power principle. After a pre-determined the switch opens, a no a lower supply voltage is con-

nected to the winding thru a diode.

This kind of circuit by no means reaches the performance of the clocked stabilized power control as per Fig. 8, as the factors: distribution voltage oscillation, B.e.m.f., thermal winding resistance, as well as the separate coil current regulation are not considered, but it is this circuit that makes the simple unipolar R/L-control suitable for many fields of application.

Fig. 8 - With switch mode current regulation efficiency is increased.

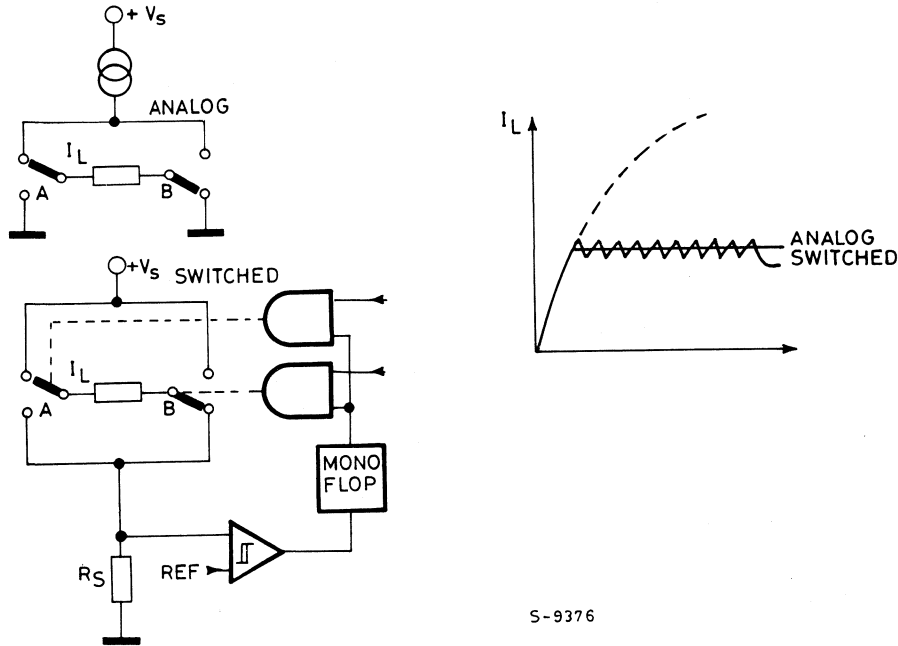
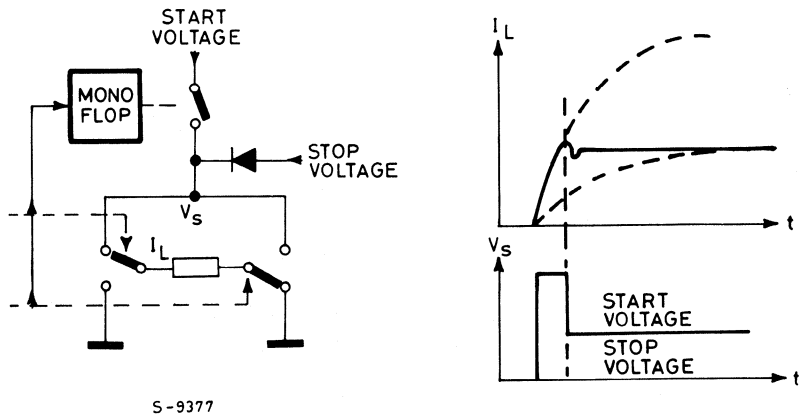


Fig. 9 - At every new step of the motor, it is possible to increase the current rate with a bilevel circuit.

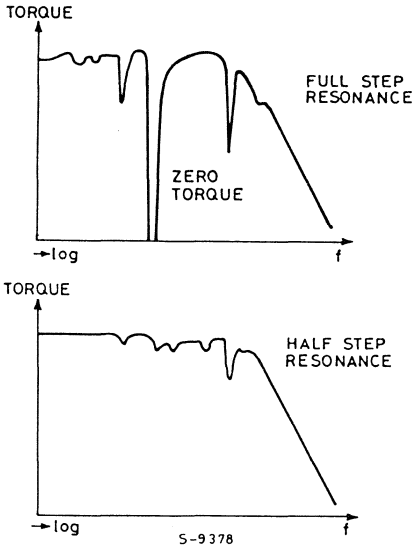


ADVANTAGES AND DISADVANTAGES OF THE HALF-STEP

An essential advantage of a stepper motor operating at half-step conditions is its position resolution increased by the factor 2. From a 3.6 degree motor you achieve 1.8 degrees, which means 200 steps per revolution.

This is not always the only reason. Often you are forced to operate at half-step conditions in order to avoid that operations are disturbed by the motor resonance. These may be so strong that the motor has no more torque in certain step frequency ranges and loses completely its position (Fig. 10). This is due to the fact that the rotor of the motor, and the changing magnetic field of the stator forms a spring-mass-system that may be stimulated to vibrate. In practice, the load might deaden this system, but only if there is sufficient frictional force.

Fig. 10 - The motor has no more torque in certain step frequency ranges with full step driving.



In most cases half-step operation helps, as the course covered by the rotor is only half as long and the system is less stimulated.

The fact that the half-step operation is not the dominating or general solution, depends on certain disadvantages:

- the half-step system needs twice as many clock-pulses as the full-step system; the clock-frequency is twice as high as with the full-step.
- In the half-step position the motor has only about half of the torque of the full-step.

For this reason many systems use the half-step operation only if the clock-frequency of the motor is within the resonance risk area.

The dynamic loss is higher the nearer the load moment comes to the limit torque of the motor. This effect decreases at higher numbers of revolutions.

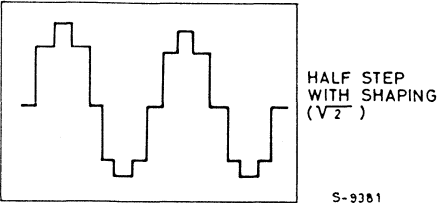
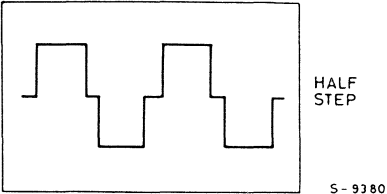
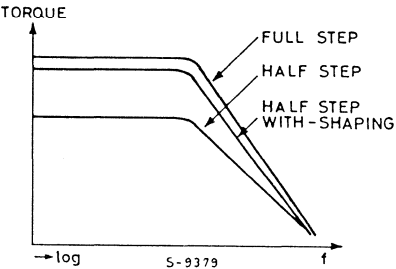
TORQUE LOSS COMPENSATION IN THE HALF-STEP OPERATION

It's clear that, especially in limit situations, the torque loss in half-step is a disadvantage. If one has to choose the next larger motor or one with a double resolution operating in full-step because of some insufficient torque percentages, it will greatly influence the costs of the whole system.

In this case, there is an alternative solution that does not increase the costs for the bipolar chopping stabilized current drive circuit.

The torque loss in the half-step position may be compensated for by increasing the winding current by the factor $\sqrt{2}$ in the phase winding that remains active. This is also permissible if, according to the motor data sheet, the current limit has been reached, because this limit refers always to the contemporary supply with current in both windings in the full-step position. The factor $\sqrt{2}$ increase in current doubles the stray power of the

Fig. 11 - Half step driving with shaping allows to increase the motor's torque to about 95% of that of the full step.



active phase. The total dissipated power is like that of the full-step because the non-active phase does not dissipate power.

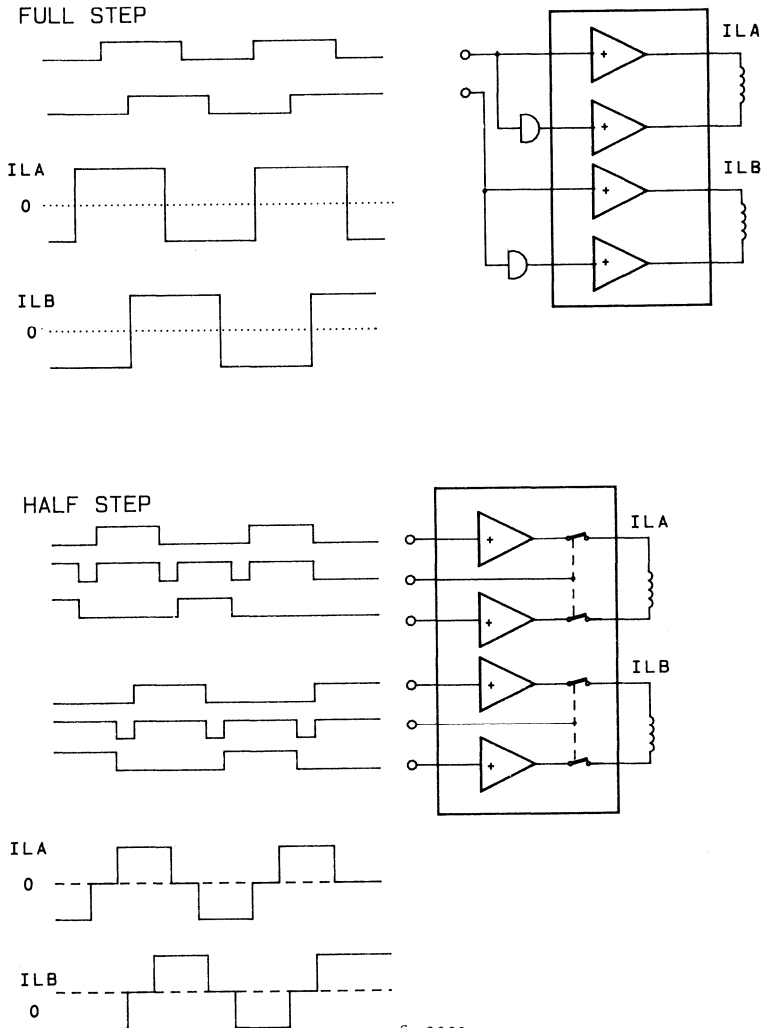
The resulting torque in the half-step position amounts to about 90% of that of the full-step, that means dynamically more than 95% torque compared to the pure full-step; a neglectable factor.

The only thing to avoid is stopping the motor at

limit current conditions in a half-step position because it would be like a winding thermal phase overload concentrated in one.

The best switch-technique for the half-step phase current increase will be explained in detail later on Fig. 11 shows the phase current of a stepping motor in half-step control with an without phase current increase and the pertinent curves of step frequency and torque.

Fig. 12 - Only two signals for full step driving are necessary while four (six if three-state is needed on the outputs stages) for half step.



DRIVE SIGNALS FOR THE MICRO ELECTRONIC

A direct current motor runs by itself if you supply it with voltage, whereas the stepping motor needs the commutation signal in for of several separated but linkable commands. In 95% of the applications today, the origin of these digital commands is a microprocessor system.

In its simplest form, a full-step control needs only two rectangular signals in quadrature. According to which phase is leading, the motor axis rotates clockwise or counter-clockwise, whereby the rotation speed is proportional to the clock frequency.

In the half-step system the situation becomes more complicated. The minimal two control signals become four control signals. In some conditions as many as six signals are needed, if the Tri-state-command for the phase ranges without current, necessary for high motor speeds, may not be obtained from the 4 control signals. Fig. 12 shows the relationship between the phase current diagram and the control signal for full and half-step.

Since all signals in each mode are in defined relations with each other, it is possible to generate

them using standard logic. However, if the possibility to choose full and half-step is desired, a good logic implementation becomes quite expensive and an application specific integrated circuit would be better. Such an application specific integrated circuit could reduce the number of outputs required from a microprocessor from the 6 required to 3 static and dynamic control line.

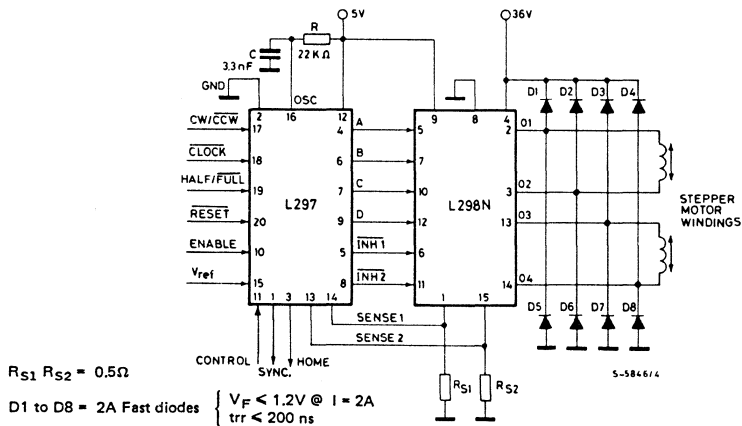
A typical control circuit that meets all these requirements is the L297 unit (Fig. 13).

Four signals control the motor in all operations:

1. **CLOCK:** The clock signal, giving the stepping command
2. **RESET:** Puts the final level signals in a defined start position
3. **DIRECTION:** Determines the sense of rotation of the motor axis
4. **HALF/FULL:** Decides whether to operate in full or in half-step.

Another inhibit input allows the device to switch the motor output into the Tri-state-mode in order to prevent undesired movements during undefined operating conditions, such as those that could occur during.

Fig. 13 - The L297 avoids the use of complicated standard logic to generate both full and half-step driving signals together with chopper current control.



SWITCH-MODE CURRENT REGULATION

The primary function of the current regulation circuit is to supply enough current to the phase windings of the motor, even at high step rates.

The functional blocks required for a switchmode current control are the same blocks required in switching power supplies; flip-flops, comparators; and an oscillator are required. These blocks can easily be included in the same IC that generates the phase control signals. Let us consider the implementation of chopper current control in the L297.

The oscillator on pin 16 of the L297 resets the two flip-flops at the start of each oscillator period. The

flip-flop outputs are then combined with the outputs of the translator circuit to form the 6 control signals supplied to the power bridge (L298).

When activated, by the oscillator, the current in the winding will raise, following the L/R time constant curve, until the voltage across the sense resistor (pin 1, 15 of L298) is equal to the reference voltage input. (pin 15, L297) the comparator then sets the flip-flop, causing the output of the L297 to change to an equiphase condition, thus effectively putting a short circuit across the phase winding. The bridge is activated into a diagonally conductive state when the oscillator resets the flip-flop at the start of the next cycle.

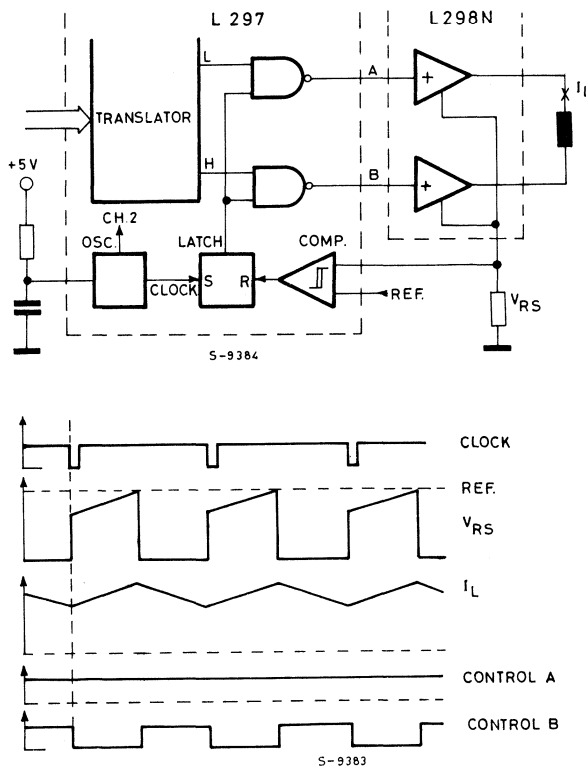
Using a common oscillator to control both current regulators maintains the same chopping frequency for both, thus avoiding interference between the two.

The functional block diagram of the L297 and the power stage (L298) are shown in Figure 14 along with the operating wave forms.

An important characteristics of this circuit implementation is that, during the reset time, the flip-flops are kept reset. The reset time can be selected by selecting the impedance of the R/C network or pin 16.

In this way, the current spike and noise across the sense resistors that may occur during switching will not cause a premature setting of the flip-flop. Thus the recovery current spike of the protection diodes can be ignored and a filter in the sense line is avoided.

Fig. 14 - Two ICs and very few external components provide complete microprocessor to bipolar stepper motor interface.



THE RIGHT PHASE CURRENT FOR EVERY OPERATING CONDITION

The Chopper principle of the controller unit reveals that the phase current in the motor windings is controlled by two data: the reference voltage at pin 15 of the controller and the value of the sense resistance at pins 1 and 15 of the L298, that is $I_L = V_{REF}/R_S$. By changing V_{REF} it is very easy to vary the current within large limits. The only question is for which purpose and at which conditions.

More phase current means more motor torque, but also higher energy consumption.

An analysis of the torque consumption for different periods and load position changes shows that there is no need for different energies.

There is a high energy need during the acceleration or break phases, whereas during continuous operation or neutral or stop position less energy has to be supplied. A motor with its phase current continuously oriented at the load moment limit, even with the load moment lacking, consumes needlessly energy, that is completely transformed into heat.

Therefore it is useful to resolve the phase current in at least two levels controllable from the processor. Fig. 18 shows a minimal configuration

with two resistance and one small signal transistor as changeover switch for the reference input. With another resistance and transistor it is possible to resolve 2 Bits and consequently 4 levels. That

is sufficient for all imaginable causes.

Fig. 16 shows a optimal phase current diagram during a positioning operation.

Fig. 15 - Because of the set-dominant latch inside the L297 it is possible to hide current spikes and noise across the sense resistors thus avoiding external filters.

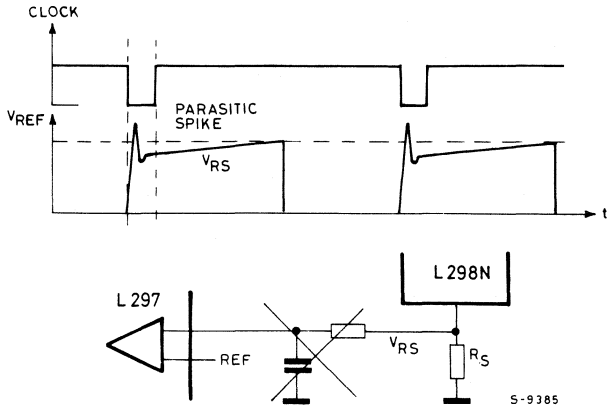
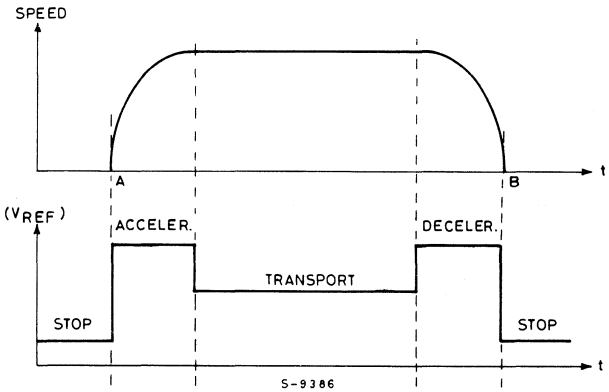


Fig. 16 - More energy is needed during the acceleration and break phases compared the continuous operation, neutral or stop position.



HIGH MOTOR CLOCK RESETS IN THE HALF-STEP SYSTEM

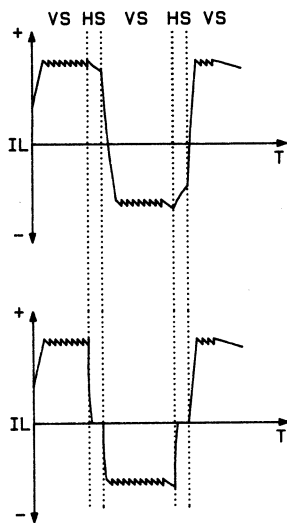
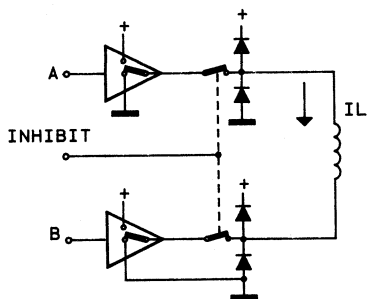
In the half-step position one of the motor phases has to be without current. If the motor moves from a full-step position into a half-step position, this means that one motor winding has to be completely discharged. From the logic diagram this means for the high level bridge an equivalent status of the input signals A/B, for example in the HIGH-status. For the coil this means short circuit (Fig. 17 up) and consequently a low reduction of the current. In case of high half-step speeds the short circuit discharge time constant of the phase winding is not sufficient to discharge the

current during the short half-step phases. The current diagram is not neat, the half step is not carried out correctly (Fig. 17 center).

For this reason the L297 controller-unit generates an inhibit-command for each phase bridge, that switches the specific bridge output in the half-step position into Tri-state. In this way the coil can start swinging freely over the external recovery diodes and discharge quickly. The current decrease rate of change corresponds more or less to the increase rate of change (Fig. 17 below).

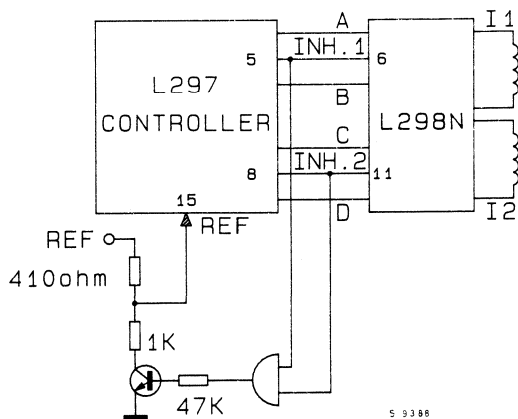
In case of full-step operation both inhibit-outputs of the controller (pin 5 and 8) remain in the HIGH-status.

Fig. 17 - The inhibit signal turns off immediately the output stages allowing thus a faster current decay (mandatory with half-step operation).



S- 9387

Fig. 18 - With this configuration it is possible to obtain half-step with shaping operation and therefore more torque.



S 9388

MORE TORQUE IN THE HALF-STEP POSITION

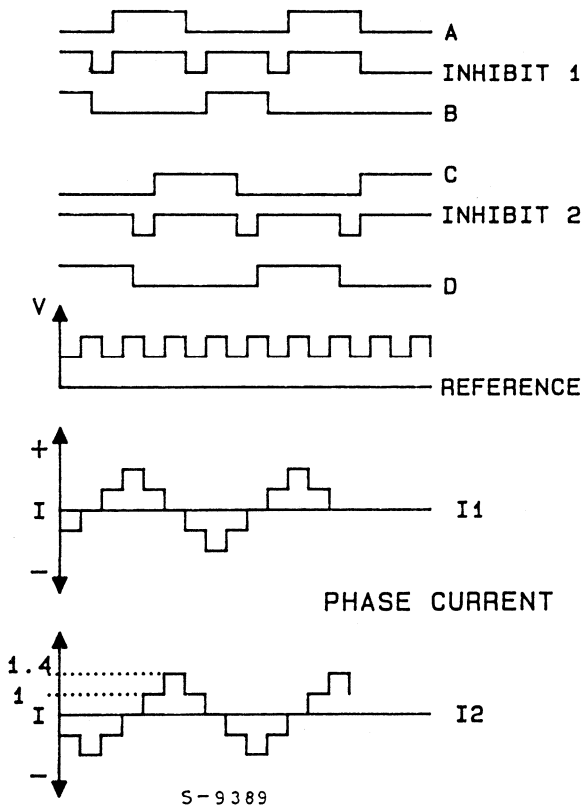
A topic that has already been discussed in detail. So we will limit our considerations on how it is carried out, in fact quite simply because of the reference voltage controlled phase current regulation.

With the help of the inhibit-signals at outputs 5 and 8 of the controller, which are alternatively active only when the half-step control is programmed, the reference voltage is increased by

the factor 1.41 with a very simple additional wiring (Fig. 18), as soon as one of the two inhibit-signals switches LOW. This increases the current in the active motorphase proportionally to the reference voltage and compensates the torque loss in this position. Fig. 19 shows clearly that the diagram of the phase current is almost sinusoidal, in principle the ideal form of the current graph.

To sum up we may say that this half-step version offers most advantages. The motor works with poor resonance and a double position resolution at a torque, that is almost the same as that of the full-step.

Fig. 19 - The half-step with shaping positioning is achieved by simply changing reference voltages.



BETTER GLIDING THAN STEPPING

If a stepper motor is supposed to work almost gliding and not step by step, the form of the phase current diagram has to be sinusoidal.

The advantages are very important:

- no more phenomena of resonance
- drastic noise reduction
- connected gearings and loads are treated with care

- the position resolution may be increased further.

However, the use of the L297 controller-unit described until now is no longer possible of the more complicated form of the phase current diagram the Controller may become simpler in its functions.

Fig. 20 shows us an example with the L6505 unit. This IC contains nothing more than the clocked phase current regulation which works according to

the same principle as L297. The four control signals emitting continuously a full-step program are now generated directly by the microprocessor. In order to obtain a sinusoidal phase current course the reference voltage inputs of the Controller are modulated with sinusoidal half-waves.

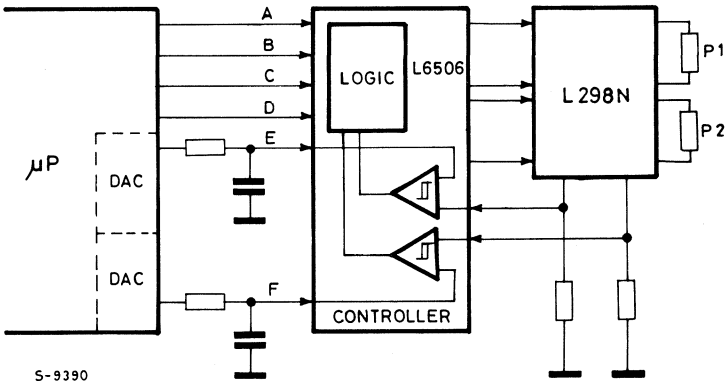
The microprocessor that controls the direction of the current phase with the control signals also generates the two analog signals.

For many applications a microprocessor with dedicated digital to analog converters can be chosen. Eliminating the need for separate D/A circuits.

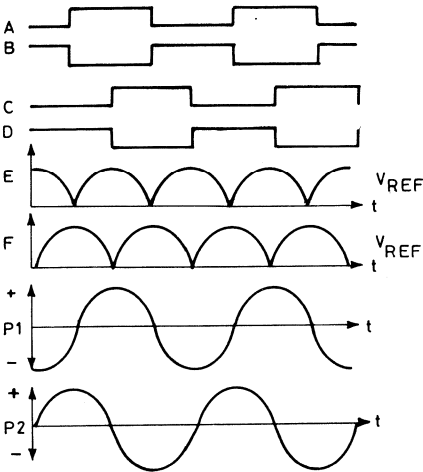
About 5 bit have proved to be the most suitable subdivision of the current within one full-step. A higher resolution brings no measurable advantages. On the contrary, the converter clock frequency is already very high in case of low motor revolutions and very difficult to process by the processor-software. It is recommended to reduce the D/A resolution at high step frequencies.

In case of higher motor revolutions it is more convenient to operate only in full-step, since harmonic control is no longer an advantage as the current has only a triangular waveform in the motor winding.

Fig. 20 - L6506 unit gives the possibility to modulate separately the two reference voltage inputs in order to obtain a sinusoidal phase current.



S-9390



S-9423

PRECISION OF THE MICRO STEP

Any desired increase of the position resolution between the full step position has its physical limits. Those who think it is possible to resolve a 7.2° - stepper motor to 1.8° with the same precision as a 1.8° - motor in full-step will be received, as there are several limits:

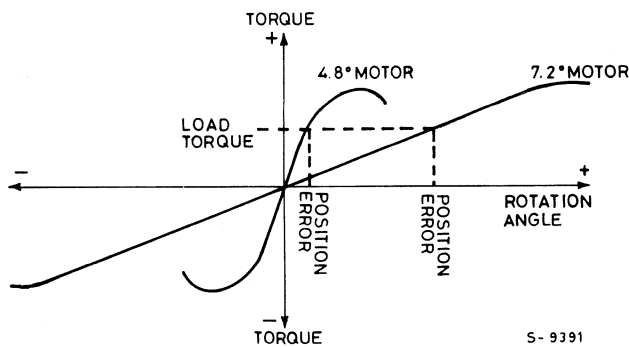
The rise rate of the torque diagram corresponding to the twisting angle of the rotor for the 7.2° - motor is flatter by a factor of 4 then for the original 1.8° - motor. Consequently with friction or load moment, the position error is larger

(Fig. 21).

For most of the commercial motors there isn't a sufficiently precise, linear relationship between a sinusoidal-current-diagram and an exact micro step angle. The reason is a dishomogeneous magnetic field between the rotor and the two stator fields.

Above all, problems have to be expected with motors with high pole feeling. However, there are special stepper motors in which an optimized micro step operation has already been considered during the construction phase.

Fig. 21 - Better resolution is achieved with low degree motor but more torque is delivered with high degree motor.



CONCLUSIONS

The above described application examples of modern integrated circuits show that output and efficiency of stepper motors may be remarkably increased without any excessive expense increase

like before.

Working in limit areas, where improved electronics with optimized drive sequences allow the use of less expensive motors, it is even possible to obtain a cost reduction.

CONSTANT-CURRENT CHOPPER DRIVE UPS STEPPER-MOTOR PERFORMANCE

**Pulse width-modulated drive improves motor torque
and speed yet adds no complexity to circuit**

Designers opting to use a fractional-horsepower stepper motor in applications such as computer printers can improve the motor's efficiency and its torque and speed characteristics by using a constant-current pulse-width-modulated (PWM) chopper-drive circuit. What's more, for high-power drives, dedicated control chips and a constant-current chopper drive can be as simple to use as direct drive.

A basic problem for a directly driven stepper is that the motor winding's time constant (L/R) causes the current to increase slowly in the winding during each pulsed input. It may, therefore, never reach full-rated value, especially at high speed, or high pulsing rates, unless the voltage (V_s) across the terminals is high. In the simplest stepper drive (see Fig. 1a), transistor or Darlington switches

sequentially activate the windings to drive the motor (see box, "Stepper motor basics").

This type of drive performs poorly because the supply voltage must be low so that the steady-state current is not excessive. As a result, the average winding current - and hence the torque - is very low at high drive motor speed.

Often, this problem is overcome by introducing a series resistance, thereby increasing the overall value by a factor of four - giving an $L/4R$ ratio - and also by increasing the supply voltage (see Fig. 1b). This arrangement reduces the motor's time constant, which improves torque at high step rates. However such an approach is inefficient, because the series resistor constitutes a substantial waste of power.

Fig. 1 - Common unipolar stepping drives (a) produce insufficient torque output because their supply voltage must be kept low to limit current. Adding series resistance to an $L/4R$ ratio (b) and raising the supply voltage proportionately improves torque output, especially at high step rates.

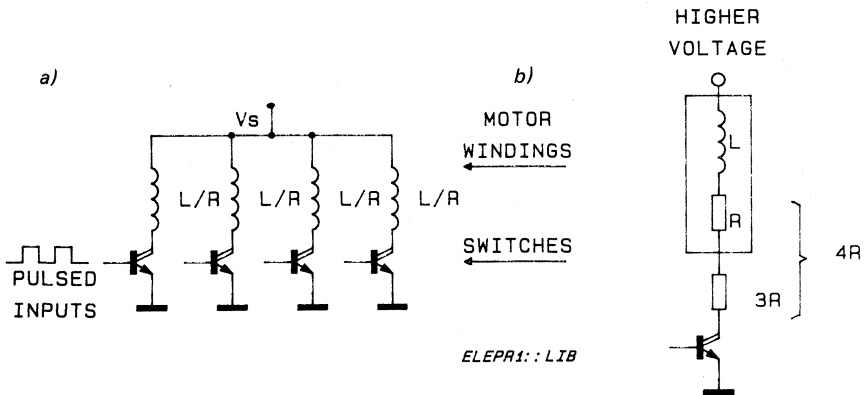
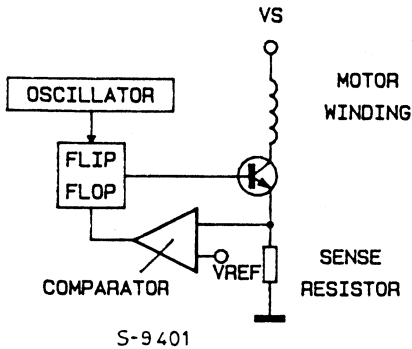


Fig. 2 - A pulse-width-modulated, or chopper, drive overcomes most of the problems of the simpler direct drive or even linear constant-current drives.



CONSTANT CURRENT IS BEST

Introducing a feedback loop to control the winding current is a better solution. Linear constant-current control is possible but is rarely used because of high power losses in the power stage. However, a pulse-width-modulation scheme - a chopper

circuit - not only solves the L/R time-constant problem but cuts power dissipation too (see Fig. 2).

A four-phase bifilar/hybrid unipolar stepper motor could use a quad Darlington like the SGS L7180 as a chopper driver and a chip like the SGS L6506 as a current controller (see Fig. 3). The quad Darlington can drive motors at up to 1.4A/phase - which is suitable for a carriage motor in a medium-size printer.

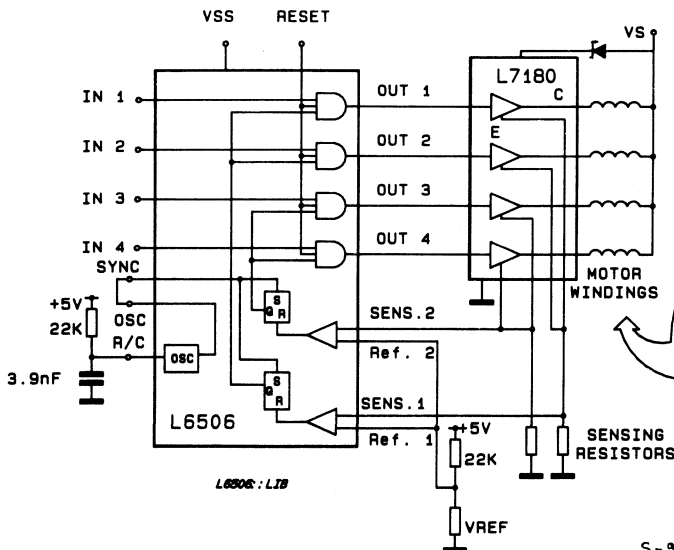
The L6506, which contains all the chopper circuitry, is simple to use. An external RC network sets the oscillator frequency, and a voltage divider (or trimmer) sets the reference voltages, and hence the phase currents. Normally an oscillator frequency of over 20KHz is chosen to avoid motor noise. The maximum usable frequency depends on the L/R time constant of the motor.

Control signals for the four-phase inputs can be provided by a micro-computer chip or a simple repetitive sequence from a logic circuit. Note that the L6506 contains just two independent chopper-control loops - sufficient for a four-phase unipolar stepping motor because opposing windings never energize together.

DRIVING BIPOLAR MOTORS

Bipolar stepper motors, preferred for their better torque/weight ratio, however, are normally driven by H-bridge output stages. They enable a single-polarity supply to drive each motor winding and sequentially to achieve a polarity-reversal effect on the windings.

Fig. 3 - A simple chopper drive for a unipolar stepping motor, can be assembled with just two chips: a quad Darlington output driver IC and a constant-current feedback controller IC.



STEPPER-MOTOR BASICS

In computer-peripheral office-equipment applications, the most popular stepper motors are permanent-magnet types with two-phase bipolar windings or bifilar-wound unipolar windings. Stripped to the essentials, both types consist of a permanent-magnet rotor surrounded by stator poles carrying the windings.

A two-pole motor would have a step angle of 90° . However, most motors have multiple poles to reduce the step angle to a few degrees.

A bipolar permanent-magnet stepper motor has a single winding for each phase – and the current must be reversed to reverse the stator field. Bifilar/ hybrid unipolar motors, however, have two windings wound in opposite directions for each phase, so that the field can be reversed with a single-polarity drive. Unipolar motors were once popular because the drive was simpler. But with today's dual bridge

(H-bridge) ICs, it is just as easy to drive a bipolar motor.

In the most popular drive technique – two-phase-on – both phases are always energized, and the rotor poles are aligned is stator pole between steps. In another method – called the wave drive – one phase is energized at a time.

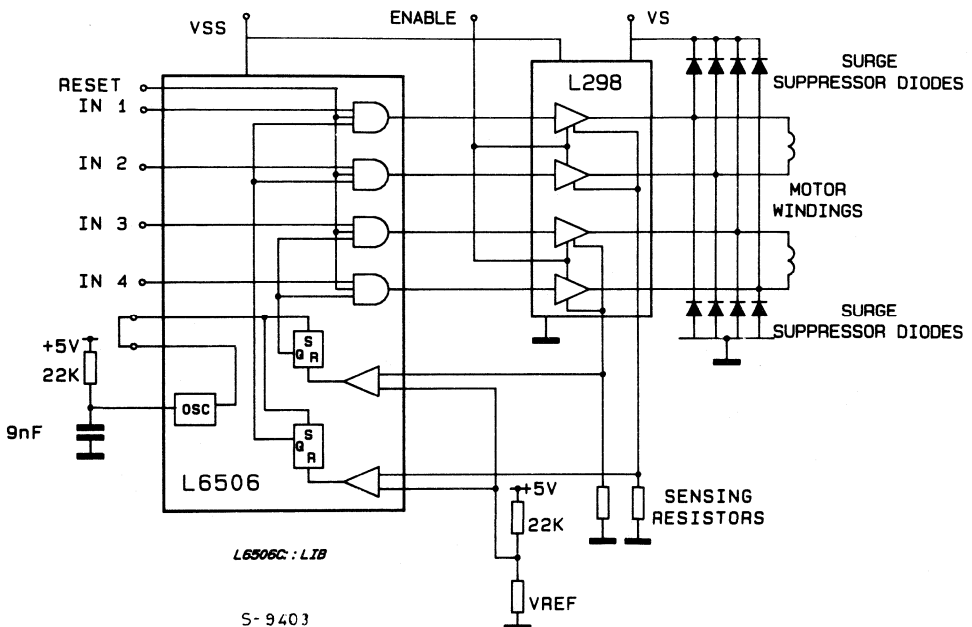
A third technique combines the two sequences and drives the motor one half-step at a time. Half-stepping is very useful because motor mechanically designed for very small step angles are much more complex – and costly – to build. It is more economical to use a 100-step motor in half steps rather than a 200-step motor in full step.

Recently designers have started microstepping, or driving the motor at one-quarter stepping rather or less. This type of operation can obtain fine step control without using mechanically complex motors with small step angles.

A two-phase bipolar motor needing up to 1A/phase can be driven by a single IC – the SGS L298 dual bridge (see Fig. 4). It contains two H-bridges with all the necessary level shifters and gates to directly interface low-level input logic signals.

As before, a complete chopper drive can be built by adding a current-controller chip and the necessary protective diodes, an RC network to define the oscillator frequency and a reference-voltage divider to set the current level. Four-phase signals to the controller are provided by a controlling micro-

Fig. 4 - A dual-bridge IC provides a simple power-stage design solution for a bipolar stepper motor.



computer or by another dedicated controller chip - the SGS L297 stepper-motor controller.

Containing an internal translator circuit controlled by step-and-direction inputs, the L297 motor controller (see Fig. 5) allows operation in three modes: two-phase-on, half-step and wave-drive.

The normal two-phase-on mode is selected by a low level on the half/full input when the device has been reset to start.

Half-step drive is selected by a high level on the half/full step input. To initialize the wave-drive mode, the user disables the output stage (brings enable low), resets the device, steps the translator one step, brings half/full low, and then reenables the outputs.

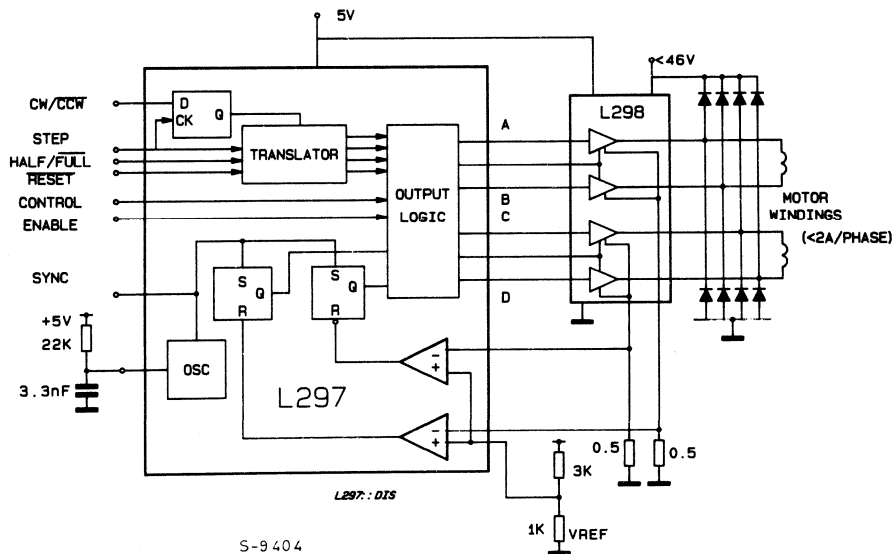
The L297 also lets the designer select either phase

or inhibit chopping. Phase chopping provides lower ripple and is suitable for unipolar motor, whereas inhibit chopping returns energy to the supply and is better for bipolar motors.

In applications such as printer-paper feed, the motor is often at rest. Since the full torque is not usually necessary to hold the motor in position, designers can save power by switching the current to a lower level between runs. With an L297 or L6506 control chip, this task can be done by simply switching the reference input between two levels.

Where several chopper drives are used in the same system, they should be synchronized to prevent intermodulation effects. This is done by connecting the sync pins to one another and omitting the oscillator RC network on all but one device.

Fig. 5 - Controlled by step, direction, and mode inputs, the SGS L297 stepper-motor controller chip performs some of the functions of a controlling microcomputer.



HANDLING HIGH CURRENT

For current drives greater than 2A/phase, the two bridges in an L298 IC can be paralleled by connecting inputs to the corresponding outputs. However, for a more equal distribution of the load and chip heating, driver 1 should be paralleled with driver 4, and driver 2 with driver 3. Additionally, total current should be derated by 0.5A to allow for the maximum possible imbalance between the current in each bridge. Thus two L298s can drive motors rated at 3.5A/phase.

A different configuration for microstepping stepper motors is employed in the SGS PBL3717A control circuit. It contains all of the control and

power circuitry for one phase of a motor. An H-bridge output stage can drive motors rated at up to 1A/phase. Two of these devices are needed to drive a two-phase bipolar motor.

The output current level from the PBL3717A is set both by an analog-reference input and two logic inputs (I_1 and I_0), which select one of three preset current levels (the fourth combination disables the outputs stage). This feature implements the microstepping, in which several current levels are used to obtain very small step angles for even more precise control (but at the expense of a less regular torque). Unlike the L297 and L6506, the PBL3717A has a constant off-time chopper driver which is ideal for microstepping.

USING THE L6506 FOR CURRENT CONTROL OF STEPPING MOTORS

The L6506 is a linear integrated circuit designed to sense and control the current in stepping motors and other similar devices. When used in conjunction with power stages like the L293, L298N, or L7180 the chip set forms a constant current drive for inductive loads and performs all the interface functions from the control logic through the power stage.

The L6506 may be used with either two phase bipolar or four phase unipolar motor configurations. The circuit in Figure 1 shows the L6506 used in conjunction with the L298N in a 2 phase bipolar stepper motor application. The circuit in Figure 2 implements a similar 4 phase unipolar application.

CURRENT CONTROL LOGIC

In these two circuits, the L6506 is used to sense and control the current in each of the load wind-

ings. The current is sensed by monitoring the voltage across a sense resistor (R_{sense}) and using a Pulse Width Modulated control to maintain the current at the desired value.

An on-chip oscillator drives the dual chopper and sets the operating frequency. An RC network on pin 1 sets the operating frequency, which is given by the equation:

$$f \approx \frac{1}{0.69 R_1 C_1} \quad (1)$$

for $R_1 > 10K\Omega$

The oscillator provides pulses to set the two flip-flops, which in turn cause the outputs to activate the power actuator. Once the outputs have been activated the current in the load starts to increase, limited by the inductive characteristic of the load.

Fig. 1 – Application circuit for Bipolar 2 phase stepper motor

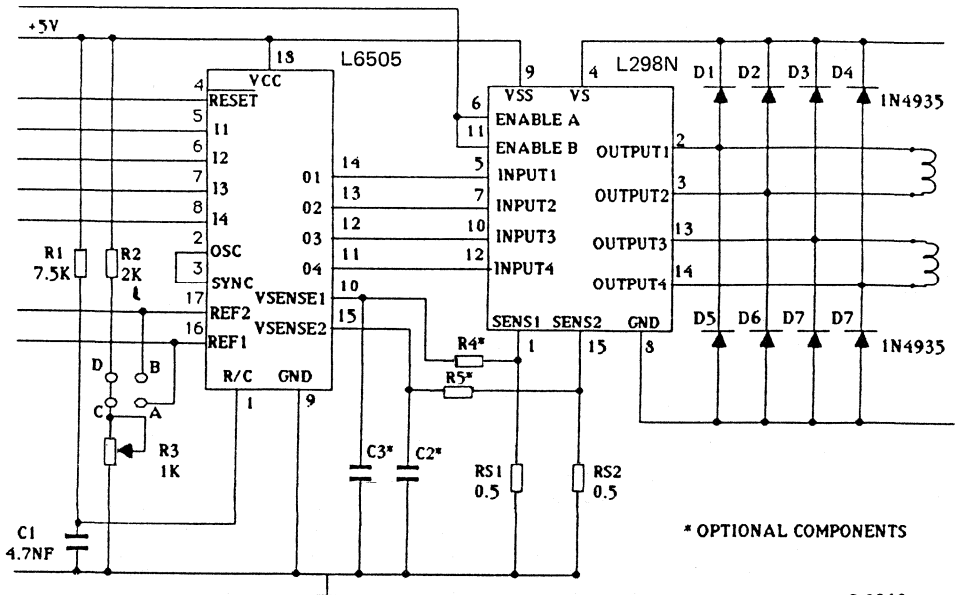
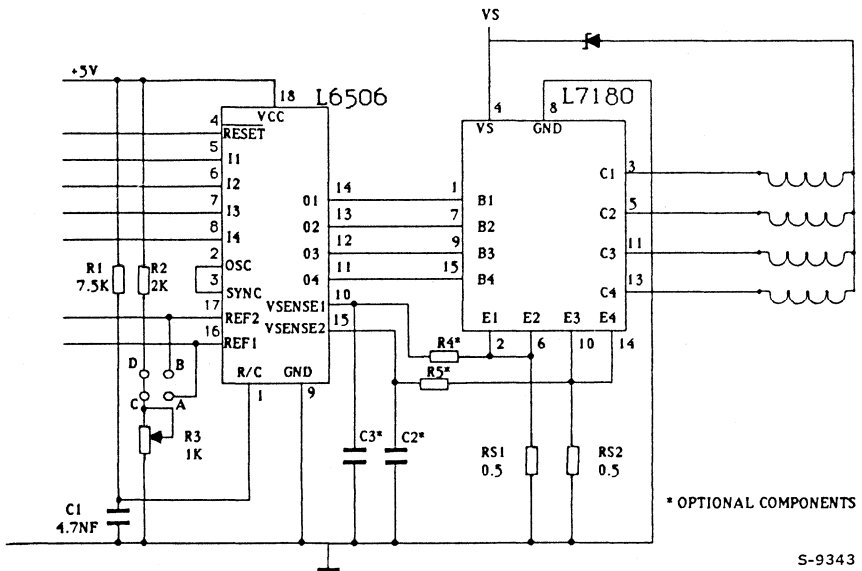


Fig. 2 - Application circuit for unipolar 4 phase stepper motor



When the current in the load winding reaches the programmed peak value, the voltage across the sense resistor (R_{sense}) is equal to reference voltage input (V_{ref}) and the corresponding comparator resets its flip-flop. This interrupts the drive and allows the current to decay through a recirculating path until the next oscillator pulse occurs. The peak current in each winding is programmed by selecting the value of the sense resistor and V_{ref} and is given by the equation:

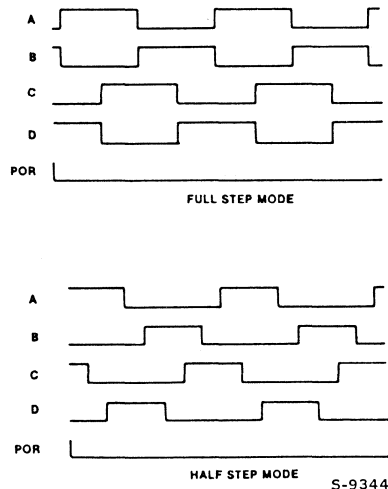
$$I_{\text{peak}} = \frac{V_{\text{ref}}}{R_{\text{sense}}} \quad (2)$$

The minimum output pulse width is determined by the pulse width of the oscillator, or other signal applied to the sync input. The internal oscillator is designed to provide narrow pulses to the sync input but the pulse width should be considered carefully. In some applications it is desirable to set the pulse width of this sync pulse to be just longer than the turn on delay time of the actuator stage. This may be useful in systems where the switching noise or recovery current of the catch diodes, which passes through the sense resistor, causes the comparator to sense a current above the peak current. By making the sync pulse wide enough to hold the flip-flop set at the time the switching transient occurs will cause the device to ignore this false data.

When the internal oscillator is used the pulse width can be modified by changing the value of the capacitor on pin 1.

Increasing the capacitance will widen the pulse width.

Fig. 3 - Input signal for stepper motor drive



The L6506 may be used with either a bridge driver, as shown in Figure 1, for bipolar motors or a quad darlington array, as shown in Figure 2, for 4 phase unipolar motors. For eigher configuration, half step may be implemented using the 4 phase inputs with the input waveforms shown in Figure 3.

The recirculation path for the motor current is through a catch diode for unipolar motors, or a catch diode and one of the lower transistors of the bridge for bipolar motors. Both of these implementations produce a low ripple current since

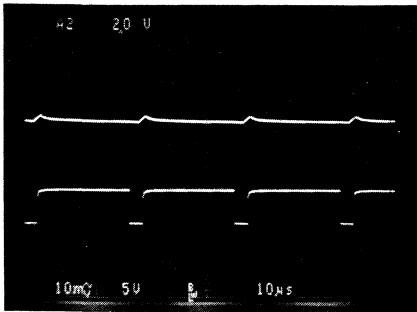
the voltage across the motor during the recirculation time is much less than the power supply voltage. Figure 4 shows the ripple current for bipolar motor applications using the L6506 and the L298.

When implementing a half step drive, both outputs of the L6506 will be low during the half step of one phase. This means a very long time is required for the current in the "off" winding to decay when driving bipolar motors.

Alternately, the power stage (L298) may be inhibited to put the output in the state and achieve a faster current decay.

Since separate V_{ref} inputs are provided for each channel, each of the loads may be programmed independently allowing the device to be used to implement microstepping or applications with different peak and hold currents. In this type of application, changing the reference voltage (V_{ref}) will change the load current, effectively implementing a transconductance amplifier.

Fig. 4 - Ripple current in Bipolar motors



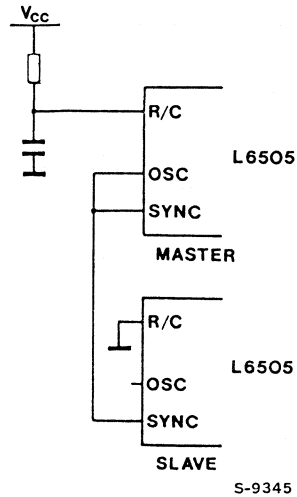
SYNCHRONIZING MULTIPLE DEVICES

Ground noise problems in multiple configurations can be avoided by synchronizing the oscillators. This may be done by connecting the sync pins of each of the devices with the oscillator output of the master device and connecting the R/C pin of the unused oscillators to ground as shown in Figure 5. The devices may be synchronized to external circuits by applying synchronizing pulses to the sync pins. It should be noted, however, that the input pulse sets the minimum on time of the outputs and will therefore set a minimum output average current.

SELECTING THE OSCILLATOR COMPONENTS

When selecting the values for the external components for the oscillator one of the primary considerations is the operating frequency. In addition there is another important consideration for these components.

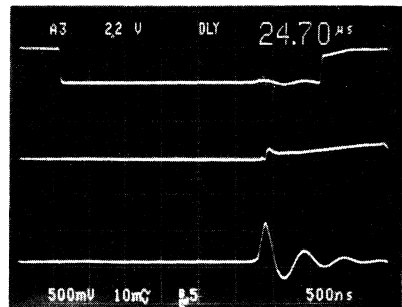
Fig. 5 - Synchronizing multiple devices



In many applications the reverse recovery current of the free wheeling diodes and of parasitic elements in the power stage will flow through the sensing resistor in addition to the load current. Also there is sometimes noise generated in the system when the power stage is switched on. These two sources of error can fool the current limiting stage and make it appear to operate at a subharmonic of the desired frequency. With the proper selection of the oscillator components this behavior can be avoided.

The design of the L6506 is such that the flip-flops used in the device are set dominant so that whenever the sync input is low the Q output of the flip-flop will be high even if the reset is applied by the comparator at the same time. This characteristic of the flip-flops can be used to make the current sensing immune to the recovery currents and noise spikes that occur when the power devices switch. If the sync pulse is longer than the turn on delay time of the power stage, as shown in Figure 6, these two sources of errors will be ignored.

Fig. 6 - Load current and sync pulse



To select the proper values for the oscillator components a more detailed equation for the operating frequency and duty cycle of the oscillator is required. The required equations can be derived from the equivalent circuit for the oscillator section shown in Figure 7.

As can be seen from figure 7, the full equation for the operating frequency includes not only the external resistance and capacitance but the internal discharge resistor as well. The full equation for the operating frequency is:

$$f = \frac{1}{0.69 C \left(R1 + \left(\frac{R1 Ri}{R1 + Ri} \right) \right)} \quad (3)$$

The equations for the active time of the sync pulse (T2), the inactive time of the sync signal (T1) and the duty cycle can also be found by looking at the figure 7 and are:

$$T2 = 0.69 C1 \frac{R1 Ri}{R1 + Ri} \quad (4)$$

$$T1 = 0.69 R1 C1 \quad (5)$$

$$DC = \frac{T2}{T1 + T2} \quad (6)$$

By substituting equations 4 and 5 into equation 6 and solving for the value of R1 the following equations for the external components can be derived:

$$R1 = \left(\frac{1}{DC} - 2 \right) Ri \quad (7)$$

$$C1 = \frac{T1}{0.69 R1} \quad (8)$$

Looking at equation 4 it can easily be seen that the minimum pulse width of T2 will occur when the value of Ri is at its minimum and the value of R1 at its maximum. Therefore, when evaluating equation 7 the minimum value for Ri of 700Ω (1KΩ - 30%) should be used to guarantee the required pulse width.

For a typical application using the L298, which has a maximum turn on delay of 2.5μs, with the L6506 consider the following operating points:

$$\begin{aligned} f &= 25\text{KHz} \\ T1 + T2 &= 40\mu\text{s} \\ T2 \text{ min} &= 3\mu\text{s} \end{aligned}$$

From equation 6:

$$DC = \frac{3\mu\text{s}}{40\mu\text{s}} = 0.075$$

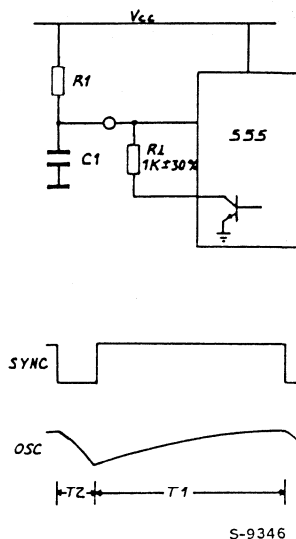
From equation 7:

$$R1 = \left(\frac{1}{0.075} - 2 \right) 700 = 7.9\text{K}\Omega$$

From equation 8:

$$C1 = \frac{37\mu\text{s}}{(0.69) (7.9\text{K})} = 6.7\text{nF}$$

Fig. 7 - Oscillator circuit and waveforms



S-9346

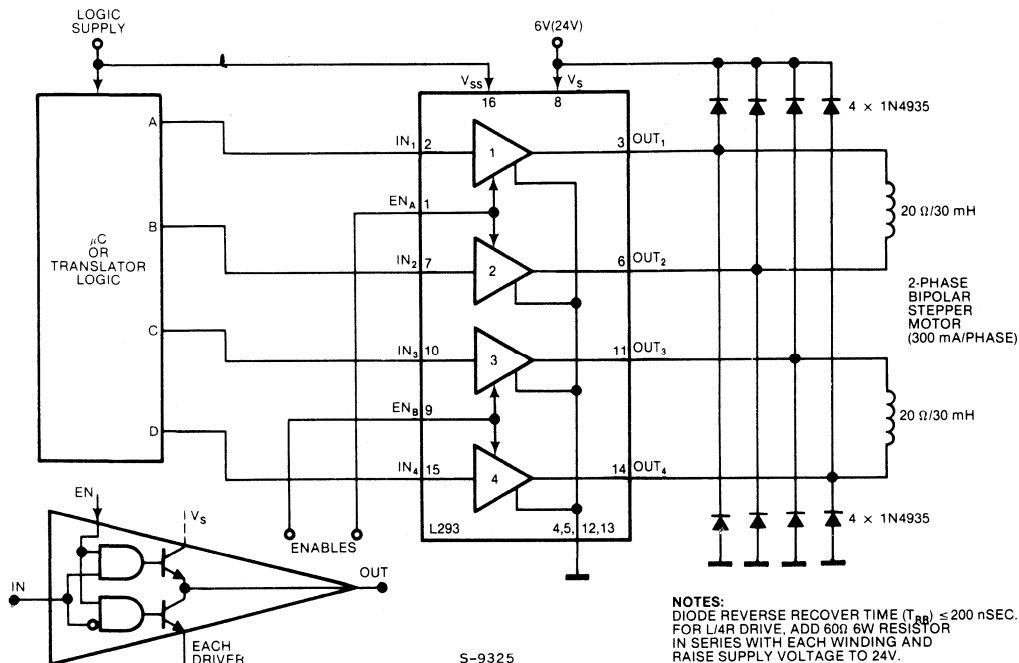
HIGH-POWER, DUAL-BRIDGE ICs EASE STEPPER-MOTOR-DRIVE DESIGN

In addition to simplifying design problems, a family of dedicated chips improves stepper-motor drive-circuit reliability by significantly reducing the component count.

The L293, L293E and L298N dual-bridge ICs (see box, "Inside the dual-bridge ICs") significantly reduce the problems encountered in the design of stepper-motor drive circuitry. They can, for example, simplify the design and increase the efficiency of constant-current choppers.

And with a single chip replacing the transistors and predriver stages, circuit performance improves. Best of all, the devices have applications in complex as well as basic driver networks.

Fig. 1 - The simplest stepper-motor drive technique is the basic L/R configuration. Adding series resistors and raising the supply to make an L/4R drive improves torque at high steps rates but reduces efficiency.



SIMPLEST DESIGN IS AN L/R DRIVE

The simplest motor-drive configuration (Fig. 1) consists of a μC that performs the translator function in software (see **box**, "Generating switching sequences") and drives the motor through a L293 dual bridge. Only eight external components are required; these are diodes that protect the device's output transistors against inductive spikes generated when a winding de-energizes.

The L293 handles 1A continuous (for higher cur-

rent use an L298N). However, if you plan to run the motor continuously with two phases on, dissipation will be the limiting factor.

You can improve the performance of this basic L/R drive by increasing the series resistance and raising the supply voltage to restore the original phase current. At high speeds, torque improves, but efficiency decreases. Normally, you increase each winding's resistance by a factor of four through the addition of a 3R series resistance, resulting in the L/4R drive.

INSIDE THE DUAL-BRIDGE ICs

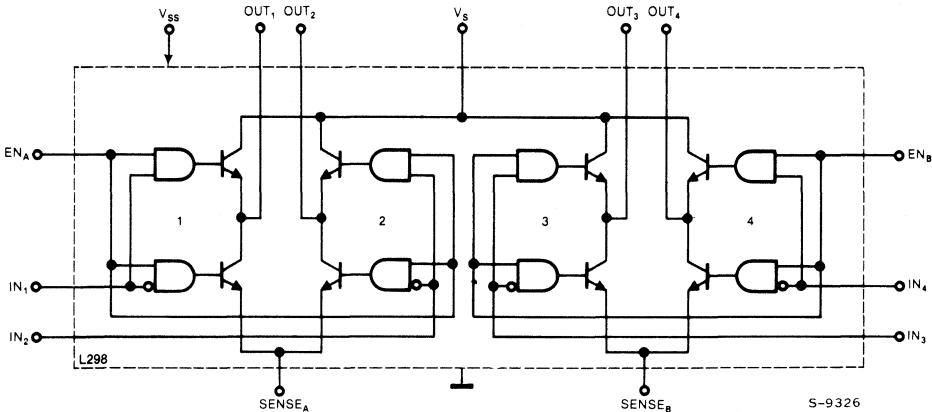
The L293, L293E and L298N (figure) contain two power-transistor bridges, predriver stages, control logic and protection circuitry. There's a control input for each bridge and an enable input for each half bridge; inputs connect directly to μCs , CMOS or TTL. The ICs integrate level shifters with a separate logic-supply pin. For current sensing, the L293E and L298N have external emitter connections.

A single package drives a 2-phase bipolar stepper motor, challenging the assumption held by many that unipolar motors are easier to drive.

You can use a bipolar motor — simpler and less expensive than a unipolar motor — without building complex power stages. Furthermore, you don't have to worry about simultaneous conduction of a half bridge's source and sink transistors — a basic problem with discrete-component bridge circuits. Chip design makes it impossible for both transistors to be on at the same time.

Designers should also discard the mistaken idea that constant-current chopper drivers are complicated and expensive. You can build one with two bridge ICs and a few passive components.

Dual-bridge driver ICs reduce the parts count of bipolar stepper motors and simplify design. The schematic of the L298N is functionally similar to those of the L293 and L293E.



Type	IO	IO(PEAK)	VS	PACKAGE	SENSING CONNECTIONS
L293	1A	1.5A	36V	16 DIP	—
L293E	1A	1.5A	36V	20 DIP	ONE PER HALF BRIDGE
L298N	2A	2.5A	46V	MULTIWATT 15	ONE PER BRIDGE

MULTIPLE SUPPLIES BOOST PERFORMANCE

A dual-level supply also improves the performance of a basic L/R circuit. A high supply voltage yields good torque characteristics when the motor is running. A lower-than-rated voltage provides some holding torque when the motor is at rest, thereby saving power when the motor is idle.

Fig. 2 shows a suitable voltage-switch circuit. R_x sets the holding current, which can be low because a permanent magnet or hybrid stepper motor provides some holding torque at zero current. However, make certain the L293's motor-supply input never goes below the logic-supply voltage. While there's no danger of damaging the device, it's impossible to drive the output transistors correctly under such conditions.

The dual bridge's enable inputs offer a means of extending the chip's flexibility. For example, you can connect them directly to the logic supply — no resistors are needed — to enable the chip permanently. As an alternative, use the enable inputs to disable the motor during the power-on reset sequence.

In wave-drive and half-step modes, use the enable inputs to increase torque at high speeds. When a winding de-energizes, flux collapse is a function of the current-decay rate. During this decay, the de-

energized winding opposes the efforts of the next winding in sequence, partially cancelling the torque. You can minimize this effect by disabling a bridge only when the winding it drives is turned off; because the $\Delta i/\Delta t$ of an inductor equals E/L , disabling the bridge accelerates the current decay. This action discharges the winding's stored energy through its supply and maintains the terminal voltage E at V_s plus two diode drops. If you were to leave the bridge enabled, the current would flow to ground through one diode and one transistor, and it would lower the terminal voltage. This scheme doesn't apply with drives with two phases on because no winding ever de-energizes.

Fig. 2 - Switching the supply to a lower voltage when the motor is idle saves current without compromising driving power

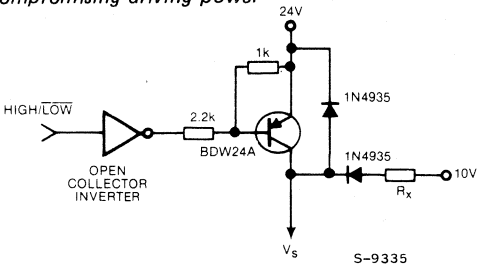
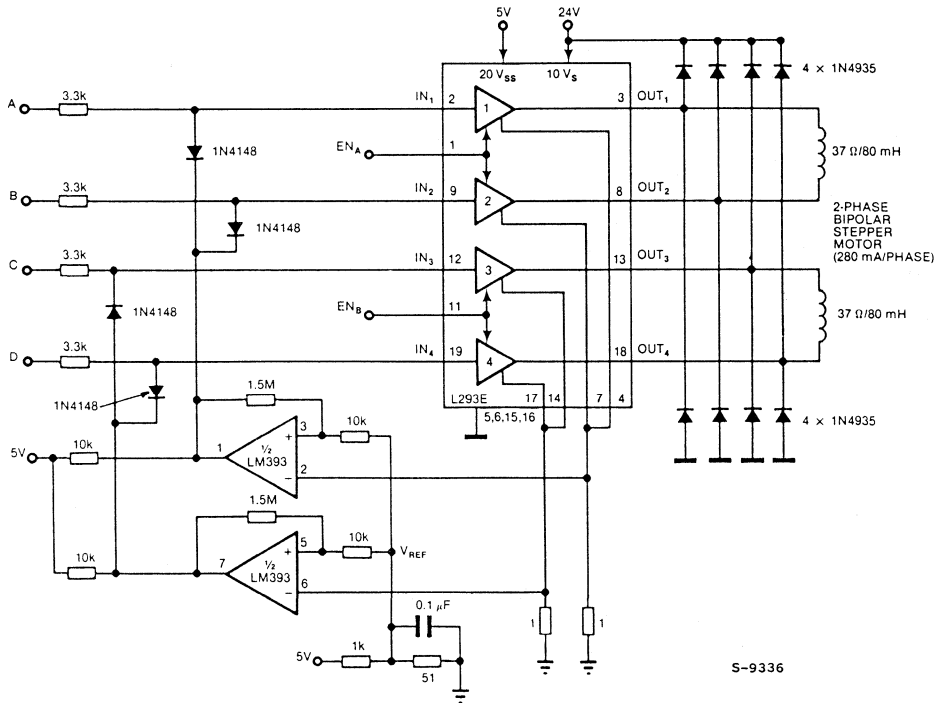


Fig. 3 - Maintaining a constant-average phase current this fixed-ripple chopper provides improved performance and efficiency V_{REF} controls the phase current

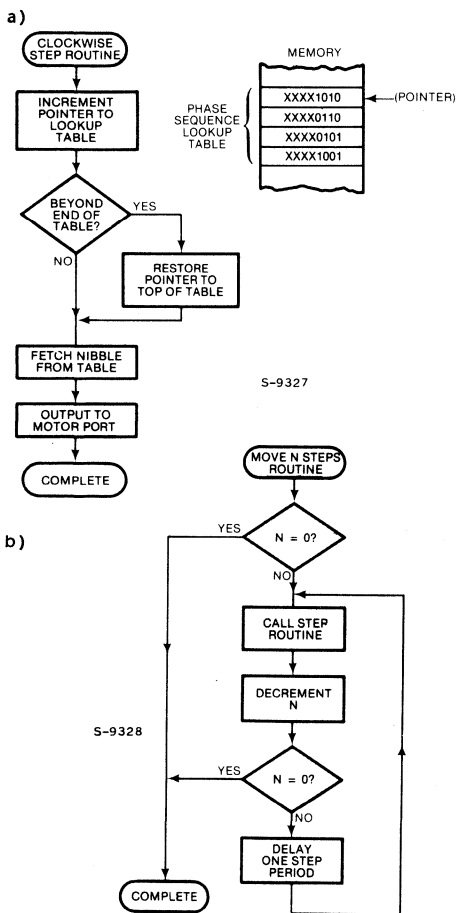


GENERATING SWITCHING SEQUENCES

In addition to selecting a motor and determining power-stage design, you must also decide how to generate the switching sequences that step the motor. Programming a μC or using a special piece of hardware called a translator accomplishes this task.

Software translation is more economical, and it is the first choice for large-volume products. Fig. A shows a basic step procedure (a) that you can integrate into a routine (b); the routine executes a clockwise rotation of N steps at a fixed rate. The step rate is defined by a software loop, but you can also use programmed timer interrupts.

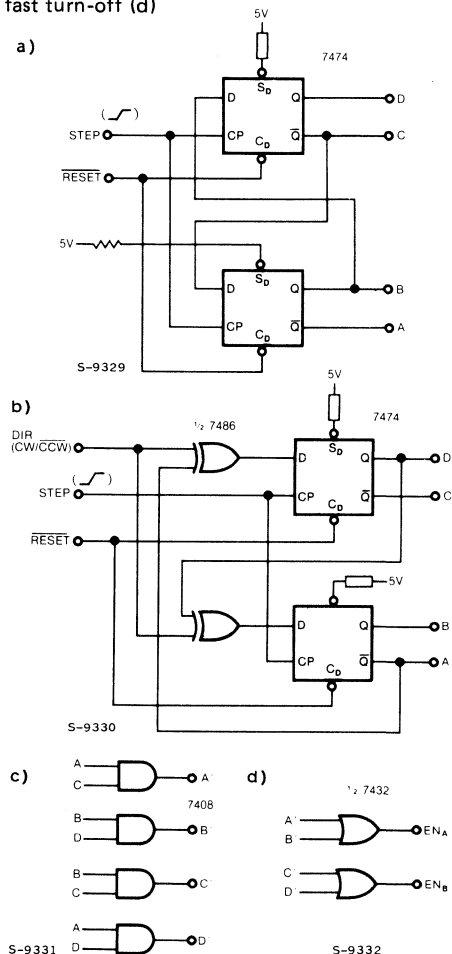
Fig. A - A μC can generate the phase sequence (a) for a stepper motor. A routine (b) expands a single-step routine into one that executes a move of N steps



A simpler approach uses the software equivalent of a shift register. For example, you can load a 99 (hex) into a register and take the phases from bits 0 to 3. A Rotate Left instruction yields a clockwise step; a Rotate Right instruction causes a counterclockwise move.

When software translation ties up your μC , lighten the load by adding a hardware translator. In applications involving unidirectional motors, this logic circuit (Fig. B) requires only one pulse for each step; you'll also need a direction signal (b) if your motor rotates in both directions. By adding a 7408 to a 2-phase translator, you can satisfy a wave-drive application (c), while the addition of two OR gates provides fast turnoff in wave-drive mode.

Fig. B - Built a simple 2-phase hardware translator using a dual flip-flop, for single (a) or bidirectional (b) rotation. Add some extra ICs for wave-drive signals (c) and to provide fast turn-off (d)



Often a μC controls the translator, setting the direction line and providing a pulse for each step. Software is thus simplified, and if you use a programmed interrupt scheme, the μC is free to handle other tasks. Fig. C describes an absolute-positioning routine for a step with a direction-control translator; Fig. D outlines how programmed timer interrupts are used to

relieve the burden on the μC . Two special cases call for hardware translation. The first is in a system for which you have already designed in control circuitry to provide step and direction signals. The second case involves single-quantity and small-run applications, in which the cost of a few ICs is a small price to pay for simplified software.

Fig. C - For use with a hardware translator this absolute-positioning routine sets the direction line and sends the appropriate number of step pulses.

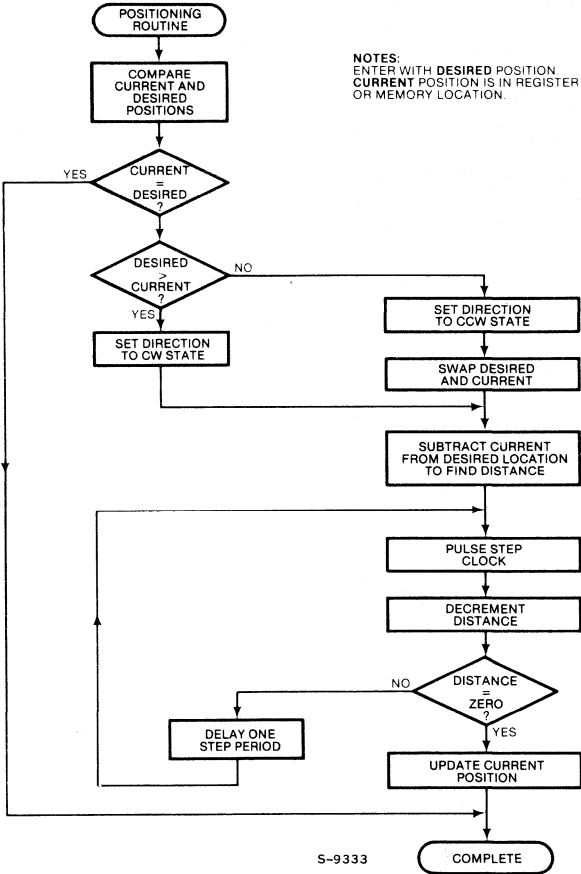
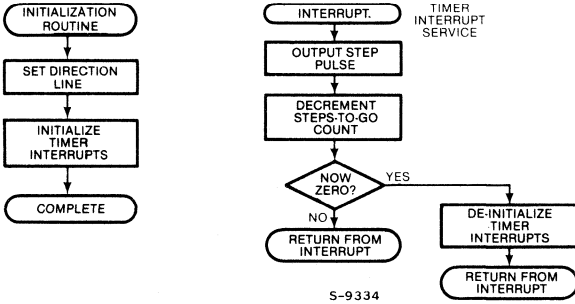


Fig. D - To set a motor step rate, used programmed timer interrupts in place of software timing loops.



CHOPPER CIRCUIT OFFERS MORE ENHANCEMENTS

Adding a chopper circuit to maintain a constant-average phase current improves performance and efficiency. Fig. 3 shows a simple constant-current drive that employs a dual bridge, dual comparator and a few passive components. This circuit requires an L293E, because this dual-bridge IC offers access to the lower emitter connections, thus letting you insert current-sensing resistors.

Operation of this fixed-ripple chopper drive is straightforward. When the μC or translator activates a bridge, the increasing load current raises the voltage across the sensing resistor until it equals the comparator's reference voltage. The comparator then switches, clamping the translator signals through the diodes to deactivate the bridge. As the current decays, the voltage across the sensing resistor decreases until it equals the comparator's lower threshold. The comparator switches again, allowing the μC or translator to activate a bridge and restart the cycle. As long as the translator drives the bridge, this sequence repeats to provide a constant-average phase current with fixed ripple.

V_{ref} adjusts the lower current limit, while the comparator's hysteresis sets the ripple, and hence the peak current. Although a divider establishes the value of V_{ref} in this case, you can employ the

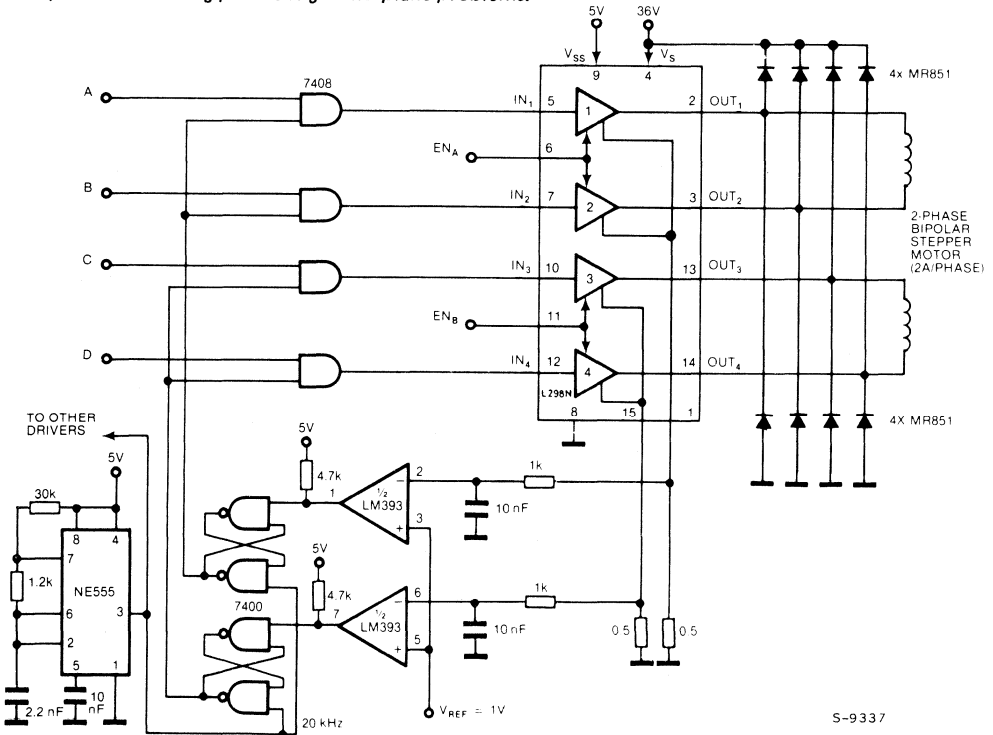
dual-supply design approach and switch V_{ref} to a lower value when the motor is idle. In addition, use of a D/A converter establishes V_{ref} for microstepping applications. This drive circuit, with its fixed-ripple current characteristics, is well suited for such service.

FIXED-FREQUENCY CHOPPER IS MOTOR INDEPENDENT

Fig. 3's drive has some disadvantages. First, the chopper frequency depends on motor characteristics, and these parameters vary from unit to unit. In addition, it's impossible to synchronize the choppers, and this shortcoming can cause trouble on the ground plane.

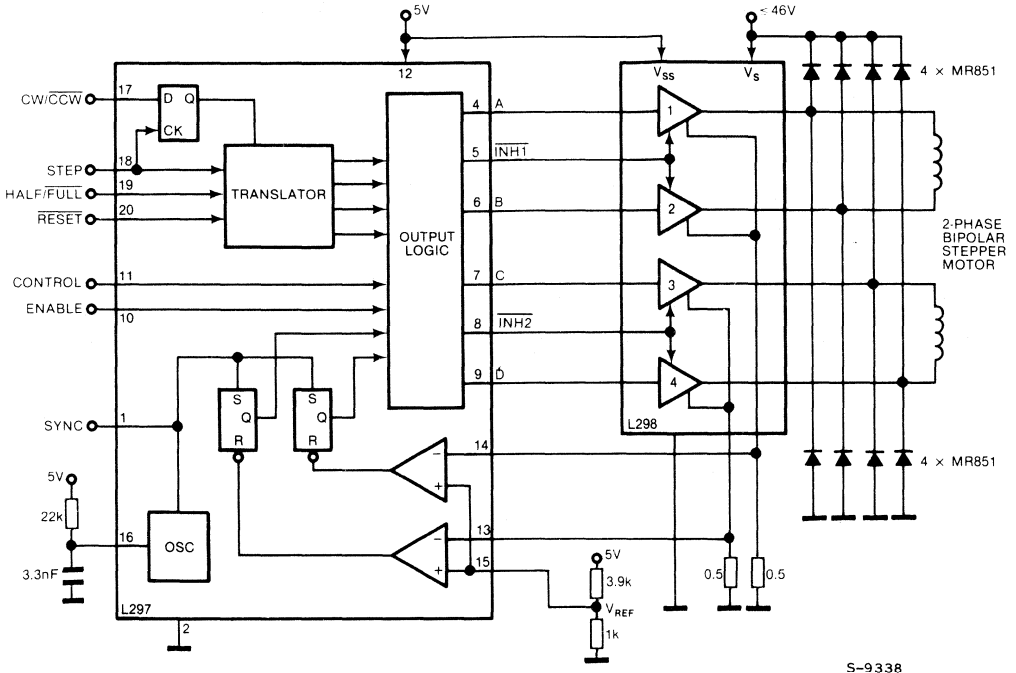
Using a flip flop/comparator arrangement (Fig. 4) to develop a fixed-frequency chopper overcomes these problems. In this circuit, the NE555 timer generates negative pulses that reset the flip flops to enable the phase-control signals from the translator. If these signals are set to energize a winding, the current in that winding rises until the voltage across the sensing resistor switches the comparator, thus setting the flip flop. This disables the phase signals and deactivates the bridge. Current in the winding falls until the next clock pulse resets the flip flop, and the sequence repeats to maintain a constant current.

Fig. 4 - This fixed-frequency constant-current chopper driver enables the synchronization of several drives, thus minimizing potential ground-plane problems.



S-9337

Fig. 5 – A special translator-chopper control circuit cuts the drivers components count to the minimum



S-9338

CONTROLLER IC REDUCES COMPONENT COUNT

If you're using a hardware translation and constant-current choppers, you can further reduce the component count by using a controller chip such as the L297 – a 20-pin DIP that houses a translator and a dual fixed-frequency chopper circuit. Under the control of step and direction inputs, the L297 generates normal, wave-drive and half-step sequences.

As shown in Fig. 5, the controller connects directly

to a dual bridge. External component requirements are minimal: and RC network to set the chopper frequency and a resistive divider to establish the comparator reference voltage (V_{ref}).

To accommodate motors with a phase current as great as 3.5A, replace the single dual-bridge IC with two devices configured in parallel (input to input, enable to enable, etc) to form a single bridge. It's extremely important that you pair the half bridges – 1 with 4 and 2 with 3 – to ensure optimum current sharing.

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INTRODUCING THE L297 STEPPER MOTOR CONTROLLER

The L297 integrates all the control circuitry required to control bipolar and unipolar stepper motors. Used with a dual bridge driver such as the L298N forms a complete microprocessor-to-bipolar stepper motor interface. Unipolar stepper motor can be driven with an L297 plus a quad darlington array. This note describes the operation of the circuit and shows how it is used.

The L297 Stepper Motor Controller is primarily intended for use with an L298N or L293E bridge driver in stepper motor driving applications.

It receives control signals from the system's controller, usually a microcomputer chip, and provides all the necessary drive signals for the power stage. Additionally, it includes two PWM chopper circuits to regulate the current in the motor windings.

With a suitable power actuator the L297 drives two phase bipolar permanent magnet motors, four phase unipolar permanent magnet motors and four phase variable reluctance motors. Moreover, it handles normal, wave drive and half step drive modes. (This is all explained in the section "Stepper Motor Basics").

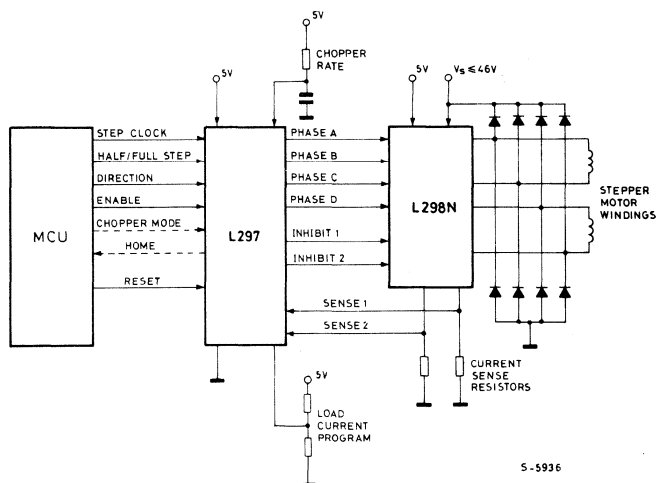
Two versions of the device are available: the regular

L297 and a special version called L297A. The L297A incorporates a step pulse doubler and is designed specifically for floppy-disk head positioning applications.

ADVANTAGES

The L297 + driver combination has many advantages: very few components are required (so assembly costs are low, reliability high and little space required), software development is simplified and the burden on the micro is reduced. Further, the choice of a two-chip approach gives a high degree of flexibility — the L298N can be used on its own for DC motors and the L297 can be used with any power stage, including discrete power devices (it provides 20mA drive for this purpose).

Fig. 1 - In this typical configuration an L297 stepper motor controller and L298 dual bridge driver combine to form a complete microprocessor to bipolar stepper motor interface.



S-5936

For bipolar motors with winding currents up to 2.5A the L297 should be used with the L298N; for winding currents up to 1A the L293E is recommended (the L293 will also be useful if the chopper isn't needed). Higher currents are obtained with power transistors or darlingtontons and for unipolar motors a darlington array such as the L7180 is suggested. The block diagram, figure 1, shows a typical system.

Applications of the L297 can be found almost everywhere. . . . printers (carriage position, daisy position, paper feed, ribbon feed), typewriters, plotters, numerically controlled machines, robots, floppy disk drives, electronic sewing machines, cash registers, photocopiers, telex machines, electronic carburetors, telecopiers, photographic equipment, paper tape readers, optical character recognisers, electric valves and so on.

The L297 is made with SGS' analog/digital compatible 1^2L technology (like Zodiac) and is assembled in a 20-pin plastic DIP. A 5V supply is used and all signal lines are TTL/CMOS compatible or open collector transistors. High density is one of the key features of the technology so the L297 die is very compact.

THE L298N AND L293E

Since the L297 is normally used with an L298 or L293E bridge driver a brief review of these devices will make the rest of this note easier to follow.

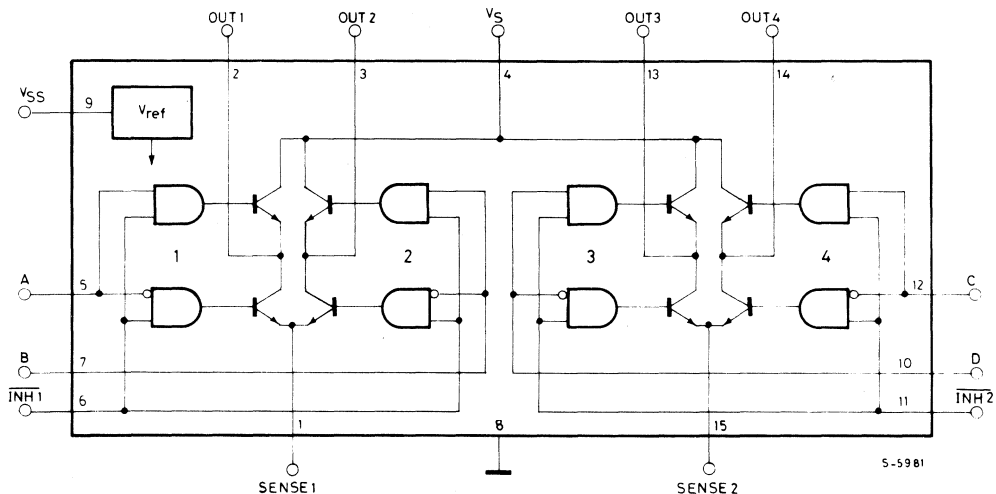
The L298N and L293E contain two bridge driver stages, each controlled by two TTL-level logic inputs and a TTL-level enable input. In addition, the emitter connections of the lower transistors are brought out to external terminals to allow the connection of current sensing resistors (figure 2).

For the L298N SGS' innovative ion-implanted high voltage/high current technology is used, allowing it to handle effective powers up to 200W (46V supply, 2.5A per bridge). A separate 5V logic supply input is provided to reduce dissipation and to allow direct connection to the L297 or other control logic.

In this note the pins of the L298N are labelled with the pin names of the corresponding L297 terminals to avoid unnecessary confusion.

The L298N is supplied in a 15-lead Multiwatt[®] plastic power package. It's smaller brother, the functionally identical L293E, is packaged in a Powerdip — a copper frame DIP that uses the four center pins to conduct heat to the circuit board copper.

Fig. 2 - The L298N contains two bridge drivers (four push pull stages) each controlled by two logic inputs and an enable input. External emitter connections are provided for current sense resistors. The L293E has external connections for all four emitters.



STEPPER MOTOR BASICS

There are two basic types of stepper motor in common use: permanent magnet and variable reluctance. Permanent magnet motors are divided into bipolar and unipolar types.

Bipolar motors

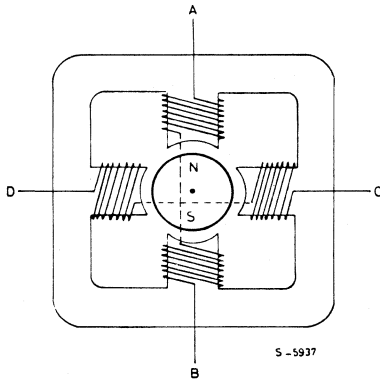
Simplified to the bare essentials, a bipolar per-

manent magnet motor consists of a rotating permanent magnet surrounded by stator poles carrying the windings (figure 3). Bidirectional drive current is used and the motor is stepped by switching the windings in sequence.

For a motor of this type there are three possible drive sequences.

The first is to energize the windings in the sequence AB/CD/BA/DC (BA means that the winding AB is

Fig. 3 – Greatly simplified, a bipolar permanent magnet stepper motor consist of a rotating magnet surrounded by stator poles as shown.



energized but in the opposite sense). This sequence is known as "one phase on" full step or wave drive mode. Only one phase is energized at any given moment (figure 4a).

The second possibility is to energize both phases together, so that the rotor always aligns itself between two pole positions. Called "two-phase-on" full step, this mode is the normal drive sequence for a bipolar motor and gives the highest torque (figure 4b).

The third option is to energize one phase, then two, then one, etc., so that the motor moves in half step increments. This sequence, known as half step mode, halves the effective step angle of the motor but gives a less regular torque (figure 4c).

For rotation in the opposite direction (counter-clockwise) the same three sequences are used, except of course that the order is reversed.

As shown in these diagrams the motor would have a step angle of 90°. Real motors have multiple poles to reduce the step angle to a few degrees but the number of windings and the drive sequences are unchanged. A typical bipolar stepper motor is shown in figure 5.

Fig. 4 – The three drive sequences for a two phase bipolar stepper motor. Clockwise rotation is shown.

Fig. 4a – Wave drive (one phase on)

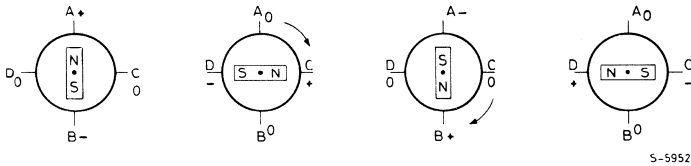


Fig. 4b – Two phase on drive

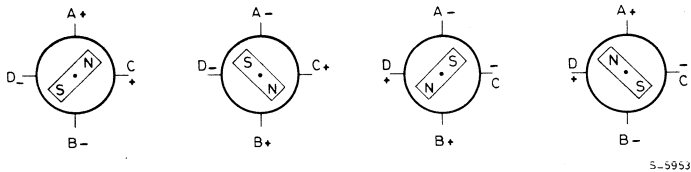


Fig. 4c – Half step drive

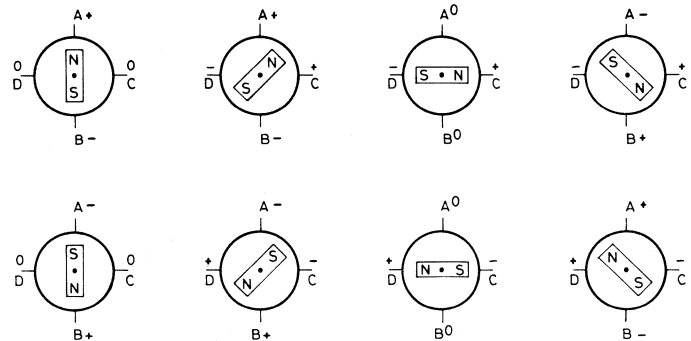
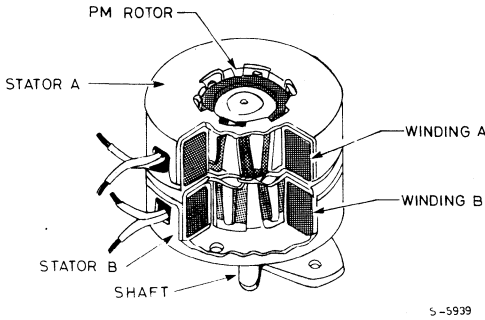


Fig. 5 – A real motor. Multiple poles are normally employed to reduce the step angle to a practical value. The principle of operation and drive sequences remain the same.



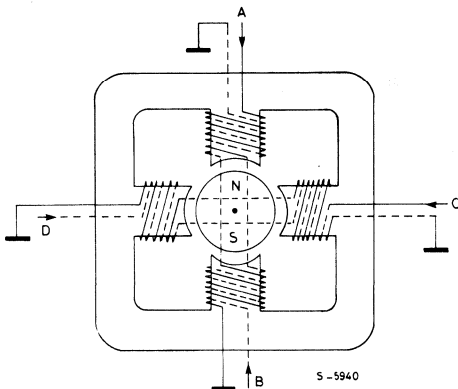
Unipolar motors

A unipolar permanent magnet motor is identical to the bipolar machine described above except that bifilar windings are used to reverse the stator flux, rather than bidirectional drive (figure 6).

This motor is driven in exactly the same way as a bipolar motor except that the bridge drivers are replaced by simple unipolar stages — four darlingtontons or a quad darlington array. Clearly, unipolar motors are more expensive because they have twice as many windings. Moreover, unipolar motors give less torque for a given motor size because the windings are made with thinner wire. In the past unipolar motors were attractive to designers because they simplify the driver stage. Now that monolithic push pull drivers like the L298 are available bipolar motors are becoming more popular.

All permanent magnet motors suffer from the counter EMF generated by the rotor, which limits the rotation speed. When very high slewing speeds are necessary a variable reluctance motor is used.

Fig. 6 – A unipolar PM motor uses bifilar windings to reverse the flux in each phase.



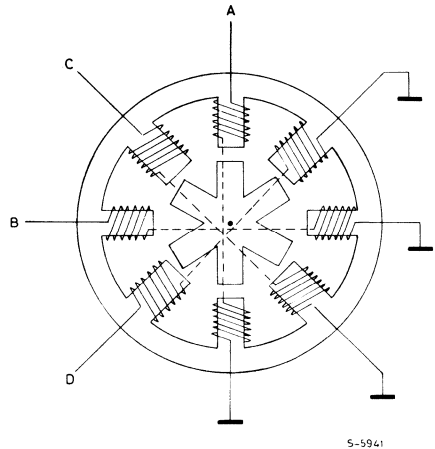
Variable reluctance motors

A variable reluctance motor has a non-magnetized soft iron rotor with fewer poles than the stator (figure 7). Unipolar drive is used and the motor is stepped by energizing stator pole pairs to align the rotor with the pole pieces of the energized winding.

Once again three different phase sequences can be used. The wave drive sequence is A/C/B/D; two-phase-on is AC/CB/BD/DA and the half step sequence is A/AC/C/CB/B/BD/D/DA. Note that the step angle for the motor shown above is 15°C, not 45°.

As before, practical motors normally employ multiple poles to give a much smaller step angle. This does not, however, affect the principle of operation or the drive sequences.

Fig. 7 – A variable reluctance motor has a soft iron rotor with fewer poles than the stator. The step angle is 15° for this motor.



GENERATING THE PHASE SEQUENCES

The heart of the L297 block diagram, figure 8, is a block called the translator which generates suitable phase sequences for half step, one-phase-on full step and two-phase-on full step operation. This block is controlled by two mode inputs — direction (CW/CCW) and HALF/FULL — and a step clock which advances the translator from one step to the next.

Four outputs are provided by the translator for subsequent processing by the output logic block which implements the inhibit and chopper functions.

Internally the translator consists of a 3-bit counter plus some combinational logic which generates a basic eight-step gray code sequence as shown in figure 9. All three drive sequences can be generated easily from this master sequence. This state sequence corresponds directly to half step mode, selected by a high level on the HALF/FULL input.

The output waveforms for this sequence are shown in figure 10.

Note that two other signals, $\overline{INH1}$ and $\overline{INH2}$ are generated in this sequence. The purpose of these signals is explained a little further on.

The full step modes are both obtained by skipping alternate states in the eight-step sequence. What happens is that the step clock bypasses the first stage of the 3-bit counter in the translator. The least significant bit of this counter is not affected

therefore the sequence generated depends on the state of the translator when full step mode is selected (the HALF/FULL input brought low).

If full step mode is selected when the translator is at any odd-numbered state we get the two-phase-on full step sequence shown in figure 11.

By contrast, one-phase-on full step mode is obtained by selecting full step mode when the translator is at an even-numbered state (figure 12).

Fig. 8 - The L297 contains translator (phase sequence generator), a dual PWM chopper and output control logic.

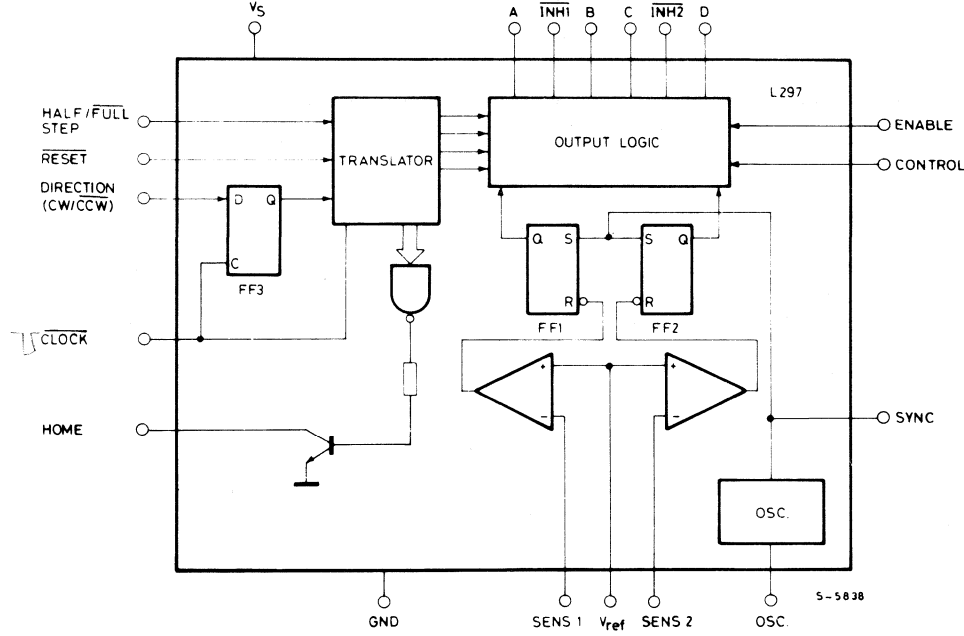


Fig. 9 - The eight step master sequence of the translator. This corresponds to half step mode. Clockwise rotation is indicated.

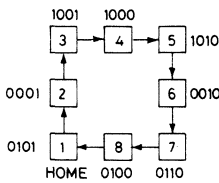


Fig. 10 - The output waveforms corresponding to the half step sequence. The chopper action is not shown.

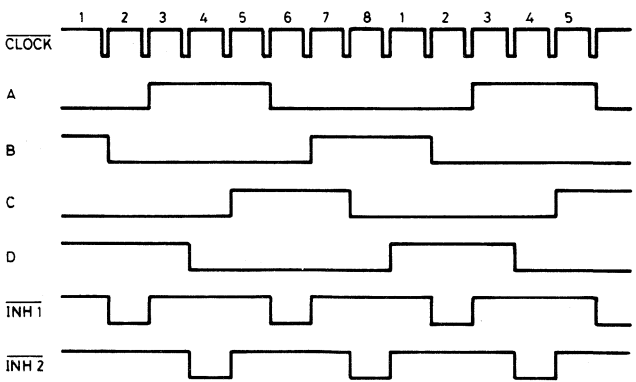


Fig. 11 – State sequence and output waveforms for the two phase on sequence. $\overline{INH1}$ and $\overline{INH2}$ remain high throughout.

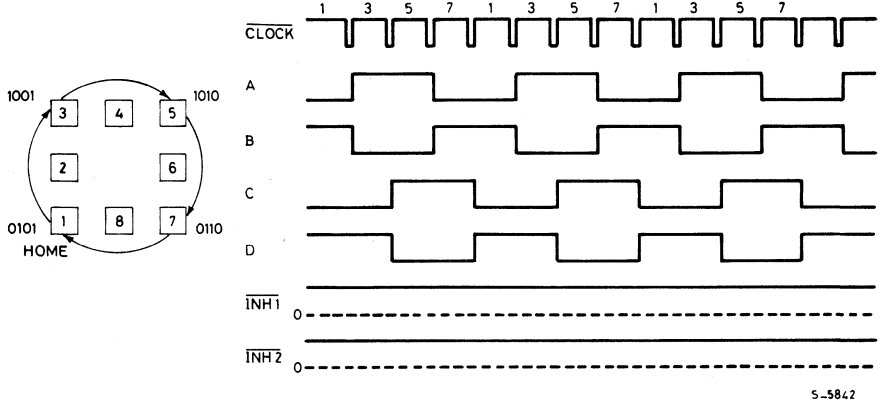
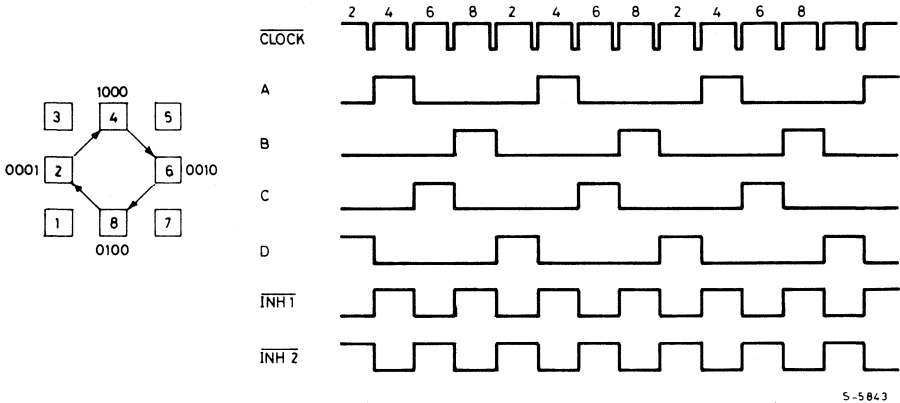


Fig. 12 – State sequence and output waveforms for wave drive (one phase on).



$\overline{INH1}$ AND $\overline{INH2}$

In half step and one-phase-on full step modes two other signals are generated: $\overline{INH1}$ and $\overline{INH2}$. These are inhibit signals which are coupled to the L298N's enable inputs and serve to speed the current decay when a winding is switched off.

Since both windings are energized continuously in two-phase-on full step mode no winding is ever switched off and these signals are not generated.

To see what these signals do let's look at one half of the L298N connected to the first phase of a two-phase bipolar motor (figure 13). Remember that the L298N's A and B inputs determine which transistor in each push pull pair will be on. $\overline{INH1}$, on the other hand, turns off all four transistors.

Assume that A is high, B low and current flowing through Q1, Q4 and the motor winding. If A is now brought low the current would recirculate through D2, Q4 and R_s , giving a slow decay and in-

creased dissipation in R_s . If, on the other hand, A is brought low and $\overline{INH1}$ is activated, all four transistors are turned off. The current recirculates in this case from ground to V_s via D2 and D3, giving a faster decay thus allowing faster operation of the motor. Also, since the recirculation current does not flow through R_s , a less expensive resistor can be used.

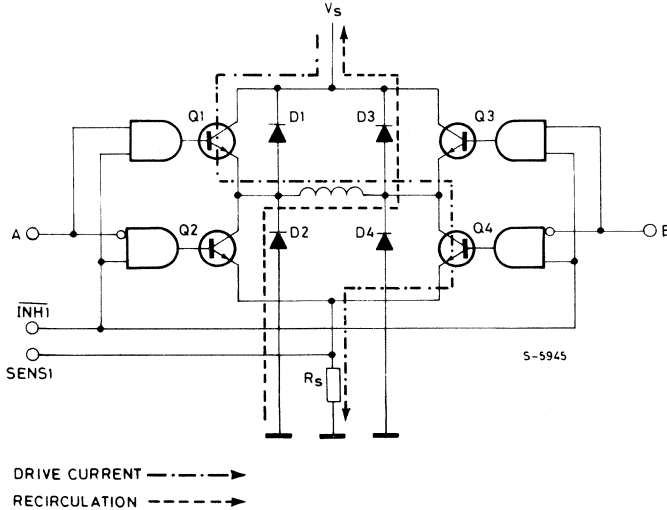
Exactly the same thing happens with the second winding, the other half of the L298 and the signals C, D and $\overline{INH2}$.

The $\overline{INH1}$ and $\overline{INH2}$ signals are generated by OR functions:

$$A + B = \overline{INH1} \qquad C + D = \overline{INH2}$$

However, the output logic is more complex because the inhibit lines are also used by the chopper, as we will see further on.

Fig. 13 - When a winding is switched off the inhibit input is activated to speed current decay. If this were not done the current would recirculate through D2 and Q4 in this example. Dissipation in R_s is also reduced.



OTHER SIGNALS

Two other signals are connected to the translator block: the RESET input and the HOME output.

RESET is an asynchronous reset input which restores the translator block to the home position (state 1, ABCD = 0101). The HOME output (open collector) signals this condition and is intended to be ANDed with the output of a mechanical home position sensor.

Finally, there is an ENABLE input connected to the output logic. A low level on this input brings $\overline{\text{INH1}}$, $\overline{\text{INH2}}$, A, B, C and D low. This input is useful to disable the motor driver when the system is initialized.

LOAD CURRENT REGULATION

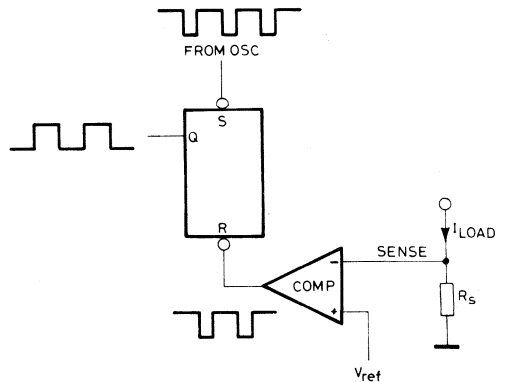
Some form of load current control is essential to obtain good speed and torque characteristics. There are several ways in which this can be done — switching the supply between two voltages, pulse rate modulation chopping or pulse width modulation chopping.

The L297 provides load current control in the form of two PWM choppers, one for each phase of a bipolar motor or one for each pair of windings for a unipolar motor. (In a unipolar motor the A and B windings are never energized together so they can share a chopper; the same applies to C and D).

Each chopper consists of a comparator, a flip flop and an external sensing resistor. A common on-chip oscillator supplies pulses at the chopper rate to both choppers.

In each chopper (figure 14) the flip flop is set by each pulse from the oscillator, enabling the output and allowing the load current to increase. As it increases the voltage across the sensing resistor increases, and when this voltage reaches V_{ref} the flip flop is reset, disabling the output until the next oscillator pulse arrives. The output of this circuit (the flip flop's Q output) is therefore a constant rate PWM signal. Note that V_{ref} determines the peak load current.

Fig. 14 - Each chopper circuit consists of a comparator, flip flop and external sense resistor. A common oscillator clocks both circuits.



S-5942

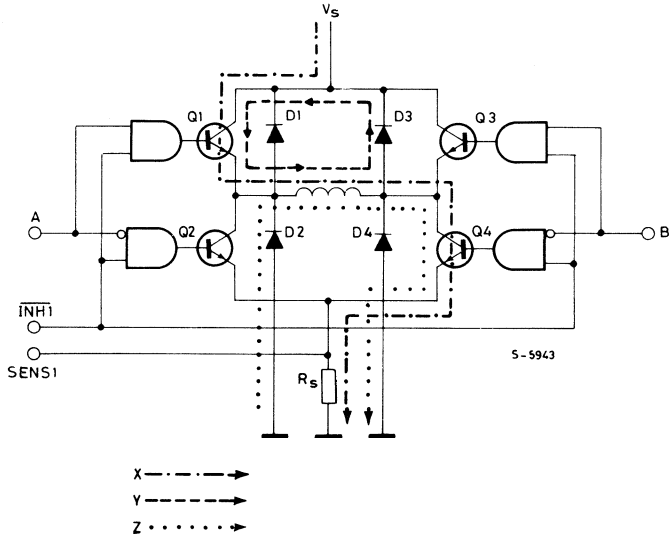
PHASE CHOPPING AND INHIBIT CHOPPING

The chopper can act on either the phase lines (ABCD) or on the inhibit lines INH1 and INH2. An input named CONTROL decides which. Inhibit chopping is used for unipolar motors but you can choose between phase chopping and inhibit chopping for bipolar motors. The reasons for this choice

are best explained with another example. First let's examine the situation when the phase lines are chopped.

As before, we are driving a two phase bipolar motor and A is high, B low (figure 15). Current therefore flows through Q1, winding, Q4 and R_s . When the voltage across R_s reaches V_{ref} the chopper brings B high to switch off the winding.

Fig. 15 - Phase chopping. In this example the current X is interrupted by activating B, giving the recirculation path Y. The alternative, de-activating A, would give the recirculation path Z, increasing dissipation in R_s .

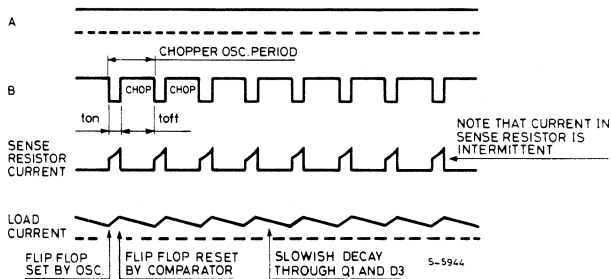


The energy stored in the winding is dissipated by current recirculating through Q1 and D3. Current decay through this path is rather slow because the voltage on the winding is low ($V_{CEsat} Q1 + V_{D3}$) (figure 16).

is to avoid the current decaying through R_s . Since the current recirculates in the upper half of the bridge, current only flows in the sensing resistor when the winding is driven. Less power is therefore dissipated in R_s and we can get away with a cheaper resistor.

Why is B pulled high, why push A low? The reason

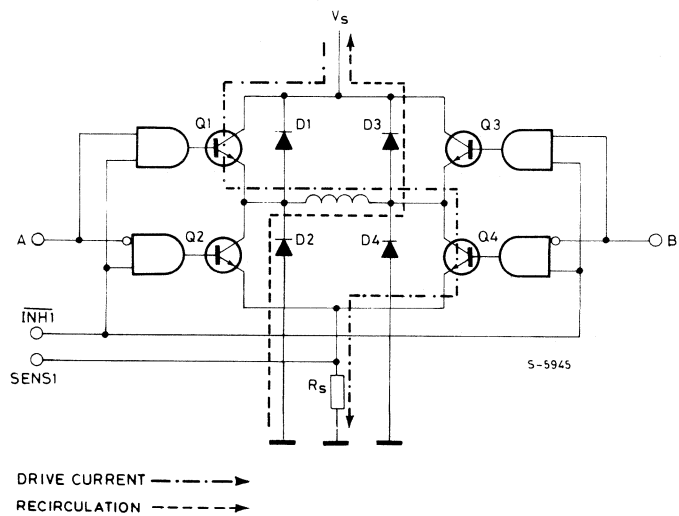
Fig. 16 - Phase chopping waveforms. The example shows AB winding energized with A positive with respect to B. Control is high.



This explains why phase chopping is not suitable for unipolar motors: when the A winding is driven the chopper acts on the B winding. Clearly, this is no use at all for a variable reluctance motor and would be slow and inefficient for a bifilar wound permanent magnet motor.

The alternative is to tie the CONTROL input to ground so that the chopper acts on INH1 and INH2. Looking at the same example, A is high and B low. Q1 and Q4 are therefore conducting and current flows through Q1, the winding, Q4 and R_s (figure 17).

Fig. 17 - Inhibit chopping. The drive current (Q1, winding, Q4) in this case is interrupted by activating INH1. The decay path through D2 and D3 is faster than the path Y of figure 15.



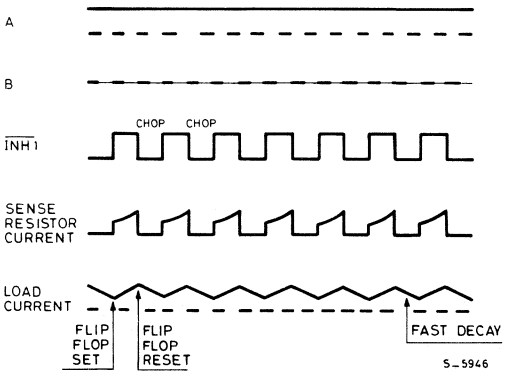
In this case when the voltage across R_s reaches V_{REF} the chopper flip flop is reset and INH1 activated (brought low). INH1, remember, turns off all four transistors therefore the current recirculates from ground, through D2, the winding and D3 to V_s . Discharged across the supply, which can be up to 46V, the current decays very rapidly (figure 18).

on this pin (figure 19). Subsequent L297s do not need the oscillator components and use SYNC as a clock input. An external clock may also be injected at this terminal if an L297 must be synchronized to other system components.

The usefulness of this second faster decay option is fairly obvious; it allows fast operation with bipolar motors and it is the only choice for unipolar motors. But why do we offer the slower alternative, phase chopping?

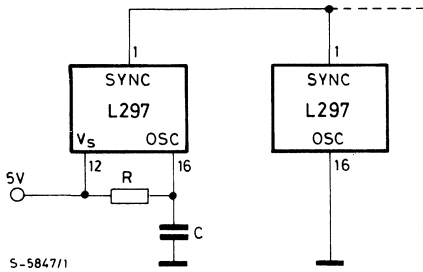
Fig. 18 - Inhibit chopper waveforms. Winding AB is energized and CONTROL is low.

The answer is that we might be obliged to use a low chopper rate with a motor that does not store much energy in the windings. If the decay is very fast the average motor current may be too low to give an useful torque. Low chopper rates may, for example, be imposed if there is a larger motor in the same system. To avoid switching noise on the ground plane all drivers should be synchronized and the chopper rate is therefore determined by the largest motor in the system.



Multiple L297s are synchronised easily using the SYNC pin. This pin is the squarewave output of the on-chip oscillator and the clock input for the choppers. The first L297 is fitted with the oscillator components and outputs a squarewave signal

Fig. 19 – The chopper oscillator of multiple L297s are synchronized by connecting the SYNC inputs together.



THE L297A

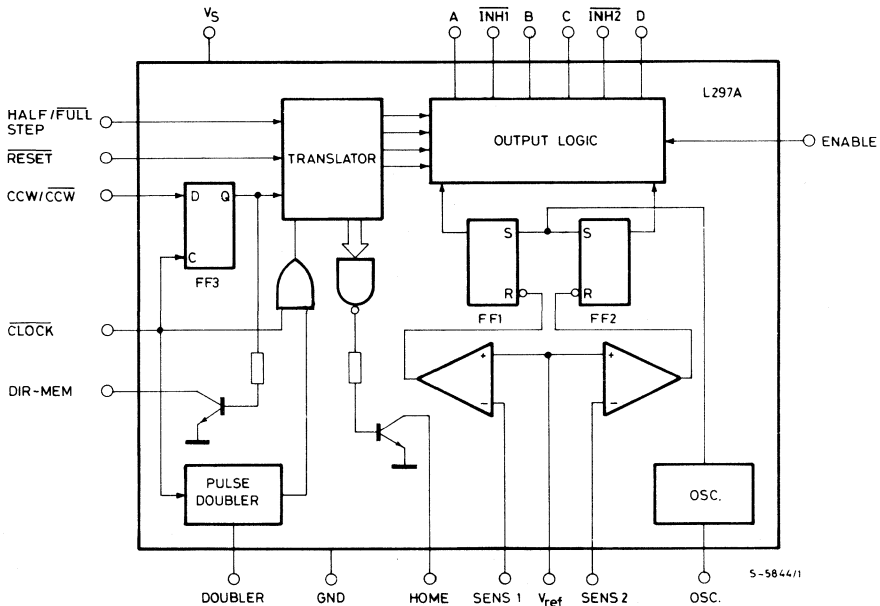
The L297A is a special version of the L297 developed originally for head positioning in floppy disk drives. It can, however, be used in other applications.

Compared to the standard L297 the differences are the addition of a pulse doubler on the step clock input and the availability of the output of the direction flip flop (block diagram, figure 20). To add these functions while keeping the low-cost 20-pin package the CONTROL and SYNC pins are not available on this version (they are not needed anyway). The chopper acts on the ABCD phase lines.

The pulse doubler generates a ghost pulse internally for each input clock pulse. Consequently the translator moves two steps for each input pulse. An external RC network sets the delay time between the input pulse and ghost pulse and should be chosen so that the ghost pulses fall roughly halfway between input pulses, allowing time for the motor to step.

This feature is used to improve positioning accuracy. Since the angular position error of a stepper motor is noncumulative (it cancels out to zero every four steps in a four step sequence motor) accuracy is improved by stepping two or four steps at a time.

Fig. 20 – The L297A, includes a clock pulse doubler and provides an output from the direction flip flop (DIR – MEM).

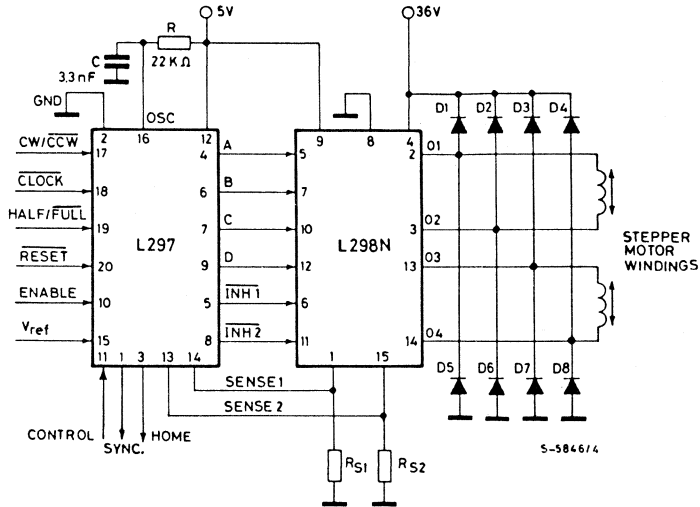


APPLICATION HINTS

Bipolar motors can be driven with an L297, an L298N or L293E bridge driver and very few external components (figure 21). Together these two chips form a complete microprocessor-to-stepper motor interface. With an L298N this configuration drives

motors with winding currents up to 2.5A; for motors up to 1A per winding an L293E is used. If the PWM choppers are not required an L293 could also be used (it doesn't have the external emitter connections for sensing resistors) but the L297 is underutilized. If very high powers are required the bridge driver is replaced by an equivalent circuit

Fig. 21 - This typical application shows an L297 and L298N driving a bipolar stepper motor with phase currents up to 2A



$$R_{S1} R_{S2} = 0.5\Omega$$

$$D1 \text{ to } D8 = 2 \text{ Fast Diodes } \left\{ \begin{array}{l} V_F \leq 1,2V @ I = 2A \\ t_{rr} \leq 200 \text{ ns} \end{array} \right.$$

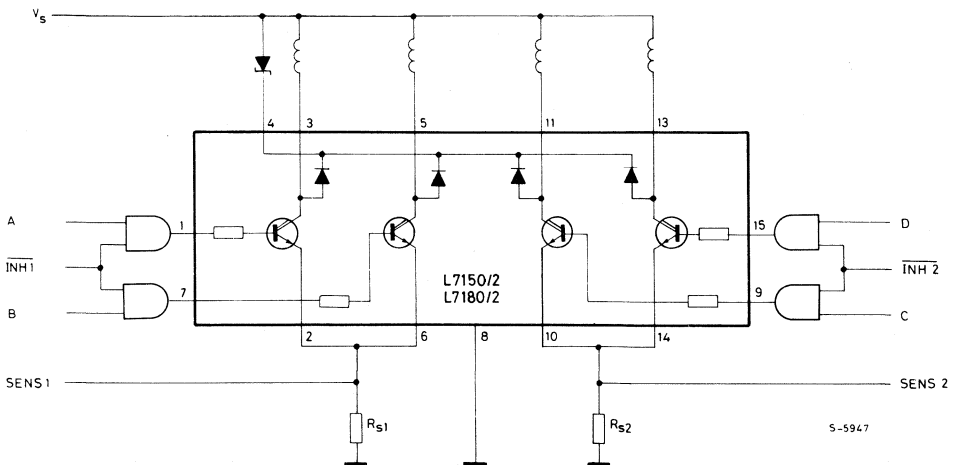
made with discrete transistors. For currents up to 3.5A two L298N's with paralleled outputs may be used.

For unipolar motors the best choice is a quad darlington array. The L702 can be used if the choppers are not required but an L7150 or L7180 is preferred. These quad darlington arrays have external

emitter connections which are connected to sensing resistors (figure 22). Since the chopper acts on the inhibit lines, four AND gates must be added in this application.

Also shown in the schematic is a zener diode in series with the suppression diodes. This serves to increase the voltage across which energy stored in

Fig. 22 - For unipolar motors a quad darlington array is coupled to the L297. Inhibit chopping is used so the four AND gates must be added.

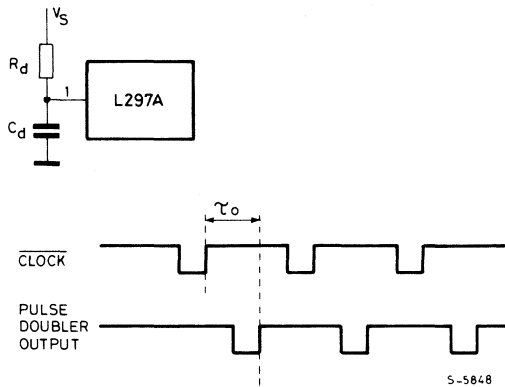


the winding is discharged and therefore speed the current decay.

In all applications where the choppers are not used it is important to remember that the sense inputs must be grounded and V_{REF} connected either to V_S or any potential between V_S and ground.

The chopper oscillator frequency is determined by the RC network on pin 16. The frequency is roughly $1/0.7 RC$ and R must be more than $10K\Omega$. When the L297A's pulse doubler is used, the delay time is determined by the network $R_D C_D$ and is approximately $0.75 R_D C_D$. R_D should be in the range $3 k\Omega - 100 k\Omega$ (figure 23).

Fig. 23 – The clock pulse doubler inserts a ghost pulse τ_o seconds after the input clock pulse. $R_D C_D$ is chosen to give a delay of approximately half the input clock period.



PIN FUNCTIONS – L297

N°	NAME	FUNCTION
1	SYNC	Output of the on-chip chopper oscillator. The SYNC connections of all L297s to be synchronized are connected together and the oscillator components are omitted on all but one. If an external clock source is used it is injected at this terminal.
2	GND	Ground connection.
3	HOME	Open collector output that indicates when the L297 is in its initial state (ABCD = 0101). The transistor is open when this signal is active.
4	A	Motor phase A drive signal for power stage.
5	$\overline{INH1}$	Active low inhibit control for driver stages of A and B phases. When a bipolar bridge is used this signal can be used to ensure fast decay of load current when a winding is de-energized. Also used by chopper to regulate load current if CONTROL input is low.
6	B	Motor phase B drive signal for power stage.

PIN FUNCTIONS – L297 (continued)

N°	NAME	FUNCTION
7	C	Motor phase C drive signal for power stage.
8	$\overline{\text{INH2}}$	Active low inhibit control for drive stages of C and D phases. Same functions as $\overline{\text{INH1}}$.
9	D	Motor phase D drive signal for power stage.
10	ENABLE	Chip enable input. When low (inactive) $\overline{\text{INH1}}$, $\overline{\text{INH2}}$, A, B, C and D are brought low.
11	CONTROL	Control input that defines action of chopper. When low chopper acts on $\overline{\text{INH1}}$ and $\overline{\text{INH2}}$; when high chopper acts on phase lines ABCD.
12	V_s	5V supply input.
13	SENS_2	Input for load current sense voltage from power stages of phases C and D.
14	SENS_1	Input for load current sense voltage from power stages of phases A and B.
15	V_{ref}	Reference voltage for chopper circuit. A voltage applied to this pin determines the peak load current.
16	OSC	An RC network (R to V_{CC} , C to ground) connected to this terminal determines the chopper rate. This terminal is connected to ground on all but one device in synchronized multi - L297 configurations. $f \cong 1/0.69 RC$, $R > 10 \text{ k}\Omega$.
17	$\text{CW}/\overline{\text{CCW}}$	Clockwise/counterclockwise direction control input. Physical direction of motor rotation also depends on connection of windings. Synchronized internally therefore direction can be changed at any time.
18	$\overline{\text{CLOCK}}$	Step clock. An active low pulse on this input advances the motor one increment. The step occurs on the rising edge of this signal.
19	$\text{HALF}/\overline{\text{FULL}}$	Half/full step select input. When high selects half step operation; when low selects full step operation. One-phase-on full step mode is obtained by selecting FULL when the L297's translator is at an even-numbered state. Two-phase-on full step mode is set by selecting FULL when the translator is at an odd numbered position. (The home position is designated state 1).

PIN FUNCTIONS – L297(continued)

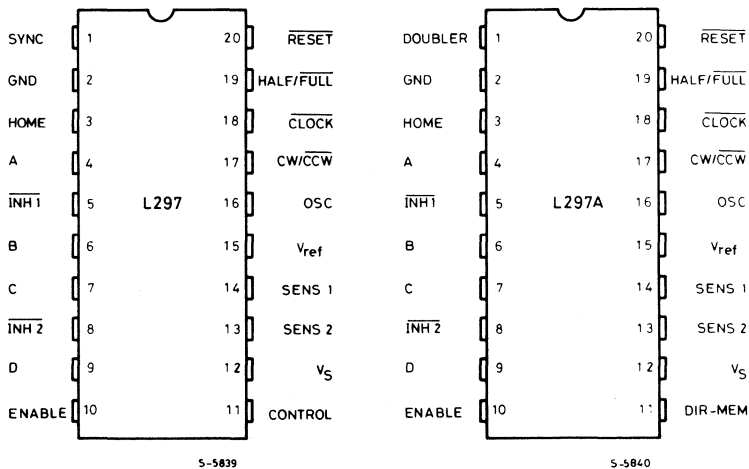
N°	NAME	FUNCTION
20	RESET	Reset input. An active low pulse on this input restores the translator to the home position (state 1, ABCD = 0101).

PIN FUNCTIONS - L297A

Pin function of the L297A are identical to those of the L297 except for pins 1 and 11.

N°	NAME	FUNCTIONS
1	DOUBLER	An RC network connected to this pin determines the delay between an input clock pulse and the corresponding ghost pulse.
11	DIR-MEM	Direction Memory. Inverted output of the direction flip flop. Open collector output.

Fig. 24 – Connection diagrams



APPLICATIONS OF MONOLITHIC BRIDGE DRIVERS

High power monolithic bridge drivers are an attractive replacement for discrete transistors and half bridges in applications such as DC motor and stepper motor driving. This application guide describes three such devices – the L293, L293E and L298 – and presents practical examples of their application.

The L293, L293E and L298 each contain four push-pull power drivers which can be used independently or, more commonly, as two full bridges. Each driver is controlled by a TTL-level logic input and each pair of drivers is equipped with an enable input which controls a whole bridge. All three devices feature a separate logic supply input so that the logic can be run on a lower supply voltage, reducing dissipation. This logic supply is internally regulated.

Additionally, the L293E and L298 are provided with external connections to the lower emitters of

each bridge to allow the connection of current sense resistors. The L293E has separate emitter connections for each channel; the L298 has two, one for each bridge.

Figure 1 shows the internal structure of the L293, L293E and L298. The L293 and L293E are represented as four push pull drivers while the internal schematic is given for the L298. Though they are drawn differently the L293E and L298 are identical in structure; the L293 differs in that it does not have external emitter connections.

Fig. 1 – The L293, L293E and L298 contain four push pull drivers. Each driver is controlled by a logic input and each pair (a bridge) is controlled by an enable input. Additionally, the L293E has external emitter connections for each driver and the L298 has emitter connections for each bridge.

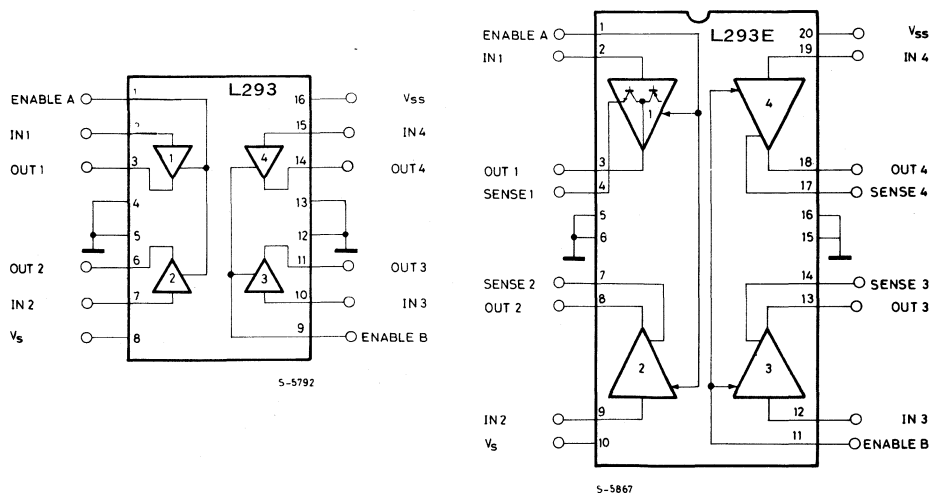
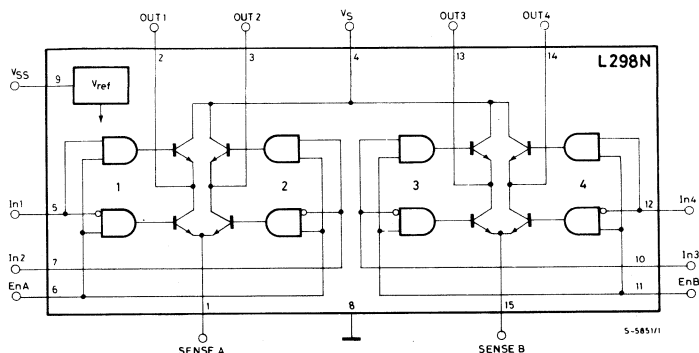


Fig. 1 (continued)



The L293 is packaged in a 12 + 4 lead POWERDIP package (a 16-pin DIP with the four center leads used to conduct heat to the PC board copper) and handles 1A per channel (1.5 peak) at voltages up to 36V.

The L293E, also rated at 1A/36V, is mounted in a 16 + 4 lead POWERDIP package. A 15-lead MULTIWATT plastic power package is used for the L298N which handles up to 2A per channel at voltages to 46V.

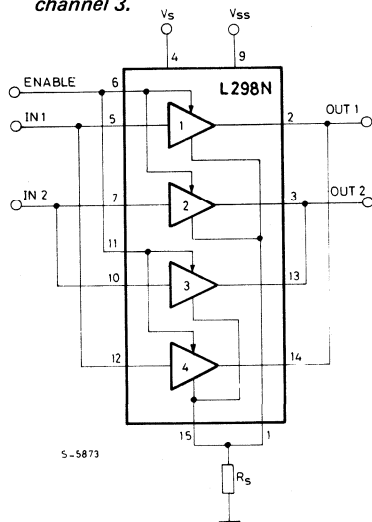
All three devices includes on-chip thermal protection and feature high noise immunity. The high switching speed makes them particularly suitable for switch mode control.

PARALLELING OUTPUTS

Higher output currents can be obtained by paralleling the outputs of both bridges. For example, the outputs of an L298N can be connected in parallel to make a single 3.5A bridge. To ensure that the current is fairly divided between the bridges they must be connected as shown in figure 2. In other words, channel one should be paralleled with channel four and channel two paralleled with channel three. Apart from this rule the connection is very straightforward — the inputs, enables, outputs and emitters are simply connected together.

The outputs of an L293 or L293E can also be paralleled — in this case too channel 1 must be paralleled with channel 4 and channel 2 with channel 3.

Fig. 2 - For higher currents outputs can be paralleled. Take care to parallel channel 1 with channel 4 and channel 2 with channel 3.



But if two bridges are needed this is not a good idea because an L298N may be used. However, if only one bridge is required an L293 connected as a single bridge may be cheaper than an underutilized L298N.

SHORT CIRCUIT PROTECTION

L293 and L298N drivers can be damaged by short circuits from the output to ground or to the supply. Short circuits to ground are by far the most common and can be protected against by the circuit shown in figure 3.

When the output is short circuited the input is pulled low after a delay of roughly 10 μ s, a period determined by the RC time constant. The upper transistor of the output stage is thus turned off, interrupting the short circuit current. When the short is removed the circuit recovers automatically. This is shown by the waveforms of figure 4.

Note that if the short circuit is removed while V1 is high the output stays low because the capacitor C is charged to V1H. The system is reset by the falling edge of V1, which discharges C.

Fig. 3 - This circuit protects a driver from output short circuits to ground.

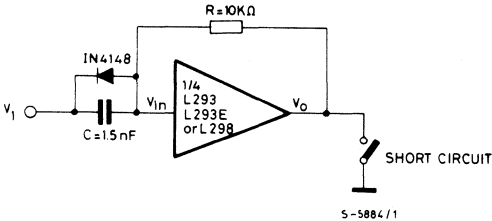
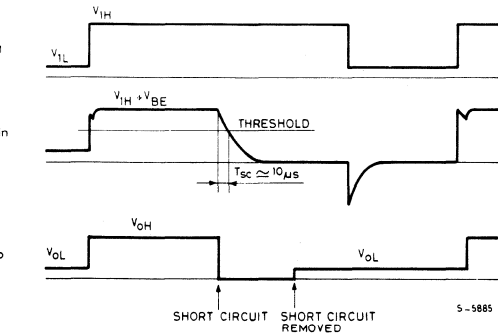


Fig. 4 - Waveforms illustrating the short circuit protection provided by the circuit of fig. 3.



DC MOTOR DRIVING

In applications where rotation is always in the same sense a single driver (half bridge) can be used to drive a small DC motor. The motor may be connected either to supply or to ground as shown in figure 5.

The only difference between these two alternatives is that the control logic is inverted – a useful fact to remember when minimising control logic.

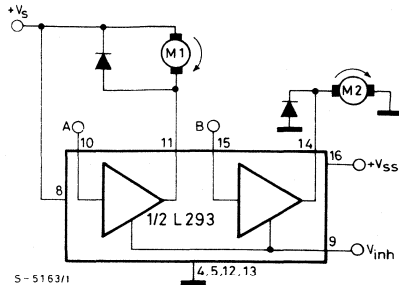
Each device can drive four motors connected in this way. The maximum motor current is 1A for the L293 and 2A for the L298N. However if several motors are driven continuously care should be taken to avoid exceeding the maximum power dissipation of the package.

Each motor in this configuration is controlled by its own logic input which gives two alternatives: run and fast stop (the motor shorted by one of the transistors).

The enable/inhibit inputs also allow a free running motor stop by turning off both transistors of the driver. Since these inputs are common to two channels (one bridge) this feature can only be used when both channels are disabled together.

A full bridge configuration is used to drive DC motors in both directions (figure 6). Using the logic inputs of the two channels the motor can be

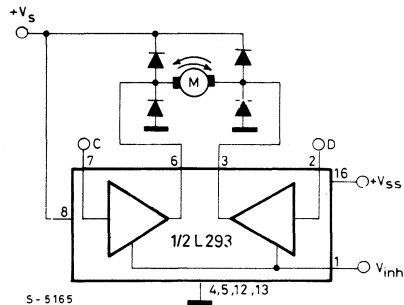
Fig. 5 - For rotation in one direction DC motors are driven by one channel and can be connected to supply or ground.



V _{inh}	A	M1	B	M2
H	H	Fast motor stop	H	Run
H	L	Run	L	Fast motor stop
L	X	Free running motor stop	X	Free running motor stop

L = Low H = High X = Don't care

Fig. 6 - A bridge is used for bidirectional drive of DC motors.



INPUTS		FUNCTION
V _{inh} = H	C = H; D = L	Turn right
	C = L; D = H	Turn left
	C = D	Fast motor stop
V _{inh} = L	C = X; D = X	Free running motor stop

L = Low H = High X = Don't care

made to run clockwise, run anticlockwise or stop rapidly.

Again, the enable/inhibit input is used for a free running stop – it turns off all four transistors of

the bridge when low. A very rapid stop may be achieved by reversing the current, though this requires more careful design to stop the motor dead. In practice a tachometer dynamo and closed loop control are usually necessary. Like the previous circuit, this configuration is suitable for motors with currents up to 1A (L293/L293E) or 2A (L298N).

The motor speed in these examples can be controlled by switching the drivers with pulse width modulated squarewaves. This approach is particularly suitable for microcomputer control.

For unidirectional drive with a single channel the PWM control signal can be applied to either the channel input or the appropriate enable input. In both cases the recirculation path is through the suppression diode and motor, giving a fairly slow decay. From a practical point of view it is preferable to control the channel input because the circuit response is faster. This is very convenient because each channel has an independent input.

The situation is different for bidirectional motors driven by a bridge. In this case the two alternatives have different effects. If the channel inputs are driven by the PWM signal, with suitable logic, the

recirculation path is through a diode, the motor and a transistor (figure 7a), giving a slow decay. On the other hand, if the enable input is controlled the recirculation path is from ground to supply through two diodes and the winding. This path gives a faster decay (figure 7b).

Figure 8 shows a practical example of PWM motor speed control. This circuit includes the oscillator and modulator and allows independent regulation of the speeds of the two motors. The channel inputs are used to control the direction.

An interesting feature of this circuit is that it takes advantage of the threshold of the enable/inhibit input to economise on comparators. The TBA820M audio amplifier generates triangle waves, the DC level of which is varied from 0 to 5V by means of P1 and P2.

Since the switching threshold of the L293's enable/inhibit inputs is roughly 2V the duty cycle of the output current (and hence the motor speed) is controlled by the setting of the potentiometer.

In this circuit the switching frequency is set by R1/C1 and the amplitude of the oscillator signal is set by the divider R2/R3.

Fig. 7a - If the current shown by the solid line is interrupted by bringing A low the current recirculates round the dotted path. Decay is slow.

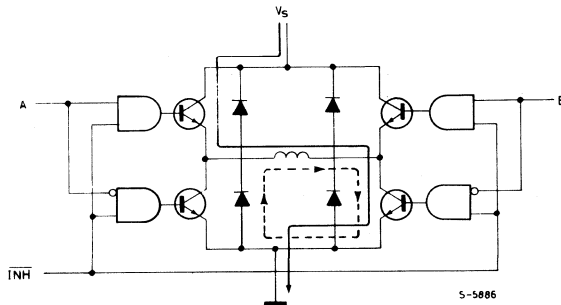


Fig. 7b - If the enable input is brought low to interrupt the current indicated by the solid line the current recirculates from ground to V_s and the decay is faster.

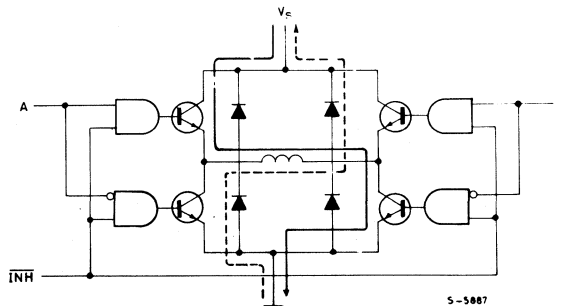
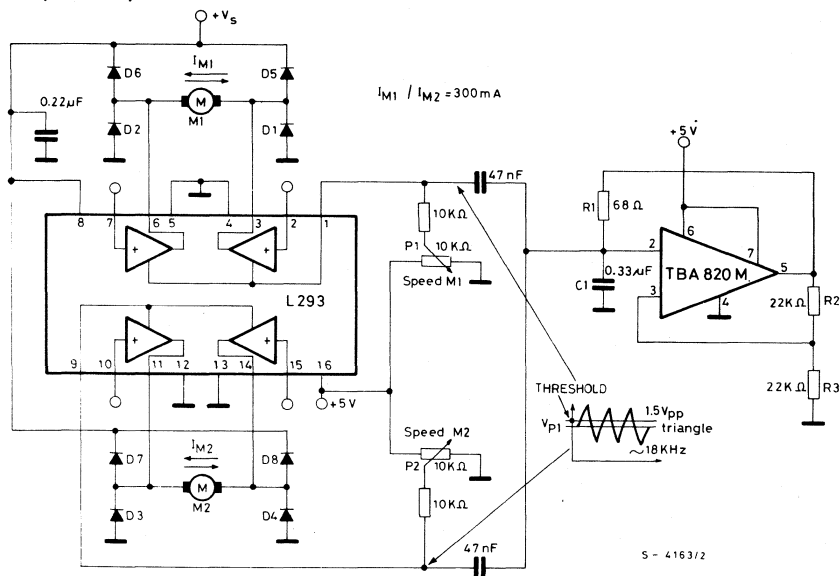


Fig. 8 - This circuit illustrates PWM control of the motor speed. The speed of each motor is controlled independently.



STEPPER MOTOR DRIVING

Monolithic bridge drivers are extremely useful for stepper motor driving because they simplify the use of bipolar motors. This is an important point since a bipolar stepper motor costs less than an equivalent unipolar motor (it has fewer windings) and gives more torque per unit volume, other things being equal.

The basic configuration for bipolar stepper motor driving is shown in figure 9. In this example it is assumed that a suitable translator (phase sequence generator) is connected to the four channel inputs.

Either an L293 or an L298N can be used in this circuit; an L293E would be wasted compared to an L293 because load current regulation, and hence the sense resistor connection, is not used.

But load current regulation is highly desirable to exploit the performance characteristics of the motor. Using an L293E or L298N this can be implemented by adding an LM339 quad comparator as shown in figure 10.

This is another circuit that requires an external translator but it provides independent PWM chopper regulation of the current in each winding.

Looking at motor phase one, the comparator output is initially high, enabling the bridge through pin 1.

The current in the motor winding rises until the voltage across the sensing resistor R2 produces a voltage at the inverting input of the comparator equal to the voltage on the non-inverting input (370 mV). This value is produced by the divider R10/R11 and by the hysteresis determined by R6 and R8.

At this point the comparator switches, disabling the bridge. The current in the winding recirculates through D5 and D6 until the voltage across R2 falls below the lower threshold of the comparator. The comparator then switches again and the cycle repeats.

Fig. 9 - A single device can be used to drive a two phase bipolar stepper motor.

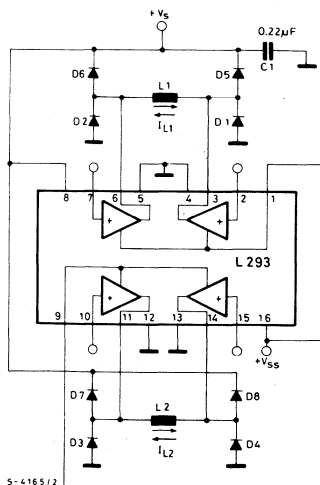
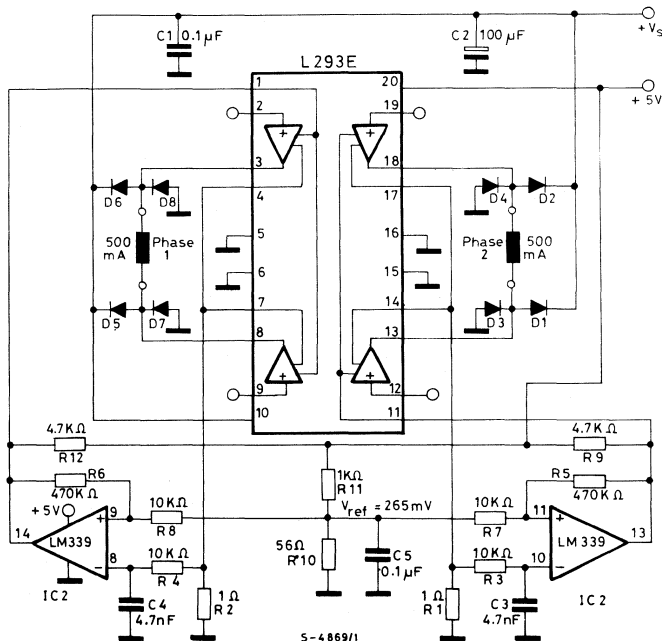


Fig. 10 – Two comparators provide chopper current regulation in this bipolar stepper motor drive circuit.



The peak current in each winding is determined by V_{ref} (in this case it is 0.5A) and the switching rate – and hence the average current – depends on the hysteresis of the comparator and R4C4. With the component values shown the switching frequency is roughly 20 kHz.

The figure 10 circuit uses only half of the LM339 quad comparator. With the addition of a few extra passive components we can take advantage of the spare comparators to implement short circuit protection. Figure 11 shows how this is done.

As before, comparators 1 and 2 regulate the current in the windings but in this case the connection is different because the inhibit/enable inputs are used for the short circuit protection. The PWM choppers act on the channel inputs through the four clamp diodes D9, D10, D11 and D12. This is a simple trick which allows us to use the channel inputs both for the step sequencing and the choppers.

Comparators 3 and 4 realize the short circuit protection function. Again looking at phase one, comparator 3 operates as a flip flop. Its output is connected to the bridge enable inputs (pins 1 and 11) and is normally high, enabling the drivers. If the output current (sensed by RS1) reaches double the nominal value the comparator CP3 switches, inhibiting the two bridges.

The comparator remains in this state until the V_{SS}

supply (5V) is interrupted. The outputs of comparators 3 and 4 are ORed together so that a short circuit on one phase disables both bridges.

For this circuit V_A should be less than 300 mV (V_A is the voltage on the + input of CP1). From the value chosen for V_A and the desired phase current the sense resistor RS1 (and RS2) is chosen. The current ripple should be at least 30 mA to avoid spurious triggering of CP1 and CP2.

The component values indicated are for a motor with a resistance of 37 Ω /phase, inductance of 80 mH/phase and a current of 280 mA/phase. V_{ref} is 243 mV giving $V_A = 274$ mV when the output is high and 243 mV when the output is low. Since $RS1 = 1\Omega$ the current in the winding reaches 274 mA peak and has a ripple of roughly 30 mA. The switching frequency depends on the hysteresis of the comparators and the motor characteristics. For this example the frequency is about 15 kHz.

Stepper motor drive circuits can be simplified using the L297 stepper motor controller which contains a translator to generate the phase sequences plus a dual PWM chopper to regulate the phase currents.

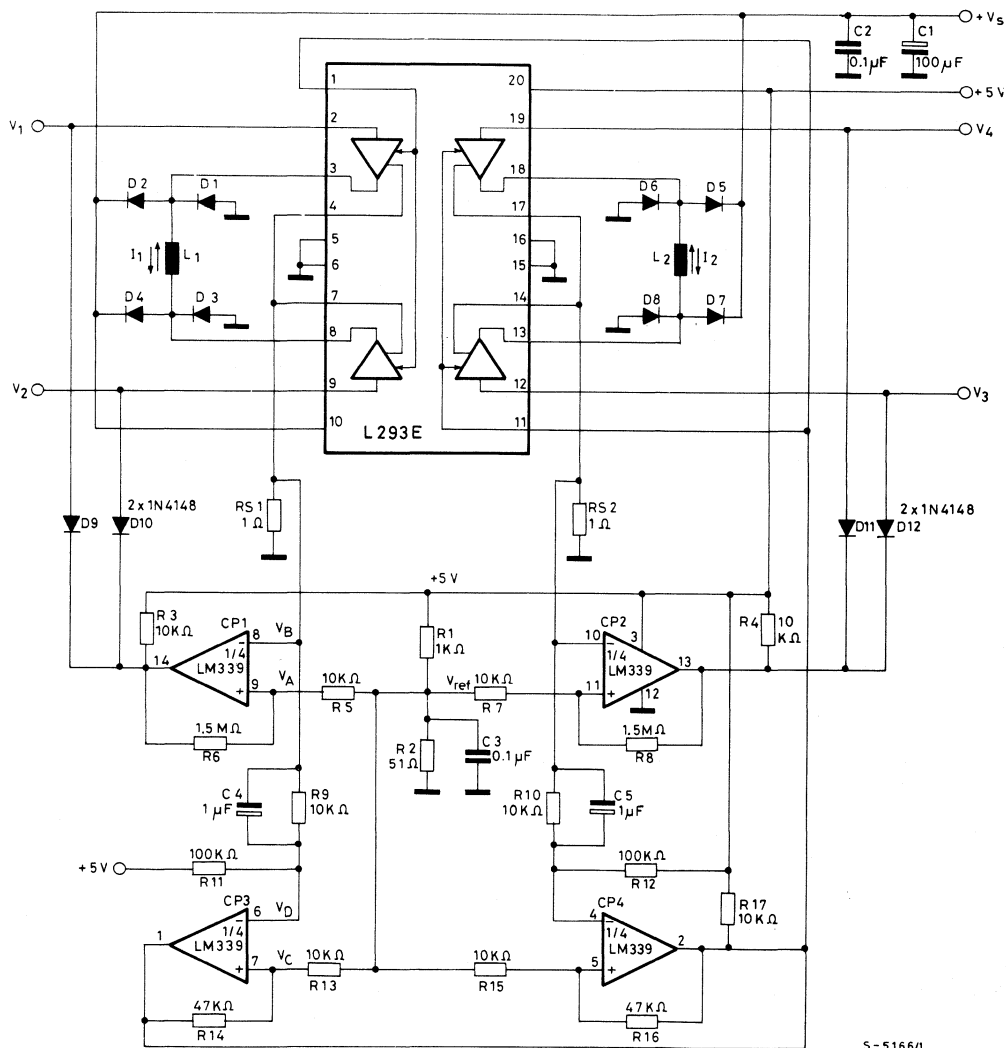
The L297 connects directly to the L293E or L298N as shown in figure 12. This example drives a bipolar stepper motor with winding currents up to 2.5A. For lower currents an L293E is used and more powerful motors can be driven by two L298N's with paralleled bridges, giving up to 3.5A.

In this configuration the motor is controlled through the L297. A step clock moves the motor one increment, the CW/CCW input controls the direction and the HALF/FULL input selects half step or normal operation. The input V_{ref} is connected to a suitable voltage reference and sets the

peak winding current in the motor. The choppers in the L297 can operate on the phase lines or the inhibit lines, depending on the state of the logic input called CONTROL.

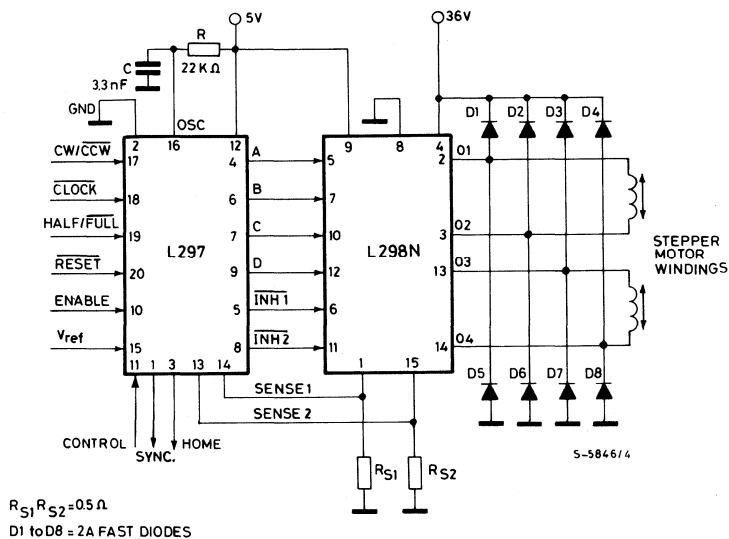
For a more detailed description of the L297 see "Introducing the L297 Stepper Motor Controller".

Fig. 11 - With a quad comparator both current regulation and short circuit protection can be obtained.



S-5166/1

Fig. 12 - An L297 stepper motor controller and a L298N driver together from a complete microprocessor-to-stepper motor interface. This circuit drives bipolar stepper motors with winding currents up to 2A.



SWITCH-MODE DRIVERS FOR SOLENOID DRIVING

This design guide describes the operation and applications of the L294 and L295 switch-mode solenoid drivers. Integrating control circuitry and power stage on the same chip, these devices replace complex discrete circuits, bringing space and cost savings.

Many applications, particularly in computer peripherals, require a high power, fast solenoid driver circuit. In the past these circuits have been realised with discrete components because the high powers required precluded the use of monolithic technology.

SGS has overcome this problem with a new high power bipolar technology that uses an innovative implanted isolation technique. This technology is used to fabricate two switchmode solenoid driver chips, the L294 and L295, which both incorporate high power output stages and control circuitry. Both circuits are designed for efficient switchmode

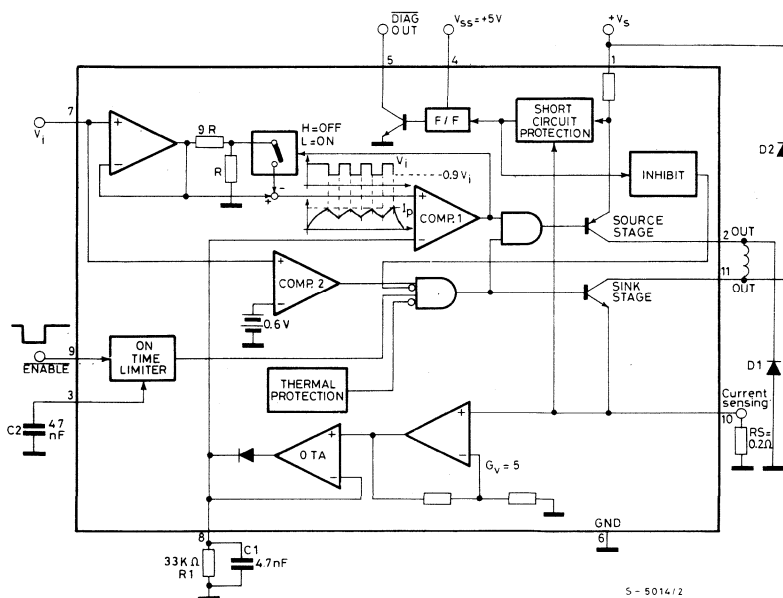
operation and are mounted in SGS' Multiwatt® plastic package.

THE L294 SOLENOID DRIVER

The L294 is designed for solenoid driving applications where both very high speed and high current are essential; needle and hammer driving in printer mechanisms, for example. It delivers 4A with supply voltages up to 46V, handling effective powers up to 180W.

Shown in figure 1, the L294 is controlled by a TTL – level logic input and the peak load current is

Fig. 1 - Internal block diagram of the L294 switchmode solenoid driver.



programmed by a reference voltage applied to the pin labelled V_i .

Internal switchmode control circuitry regulates the solenoid current by turning the output stage on and off repeatedly to keep the load current between the programmed peak value, I_p , and a lower limit of $0.9 I_p$.

Other features of the L294 include thermal shut-down, output short circuit protection, overdriving protection and a latched diagnostic output. This output indicates fault conditions such as a short circuit solenoid.

CIRCUIT OPERATION

In most applications the L294 is used with a fixed reference voltage (V_i) and the solenoid is controlled by negative-going pulses on the $\overline{\text{ENABLE}}$ input. When the $\overline{\text{ENABLE}}$ input is active (low level), the output stage is enabled and the load current rises as shown in figure 2.

The load current is sensed by an external resistor (R_s) in the emitter of the sink stage. Through the op amp and transconductance amplifier (OTA), the sensed voltage charges an external RC network (R1C1) which determines the switching characteristics of the device.

The voltage across this RC network is compared with the voltage V_i , which fixes the output peak current. When the current has reached the programmed peak value this comparator switches, turning off the output source stage and closing a switch which reduces the voltage on the non-inverting input to $0.9 V_i$. The load current now recirculates in D1. The voltage on pin 8 falls with a time constant determined by R1C1 or the load characteristics, whichever is the longest. In other

word, R1C1 sets the minimum recirculation time constant.

When the voltage across R1C1 has fallen to the $0.9 V_i$ threshold the comparator switches on, turning the output stage back on and restoring the V_i comparison threshold.

The output source stage is switched in this way, regulating the load current, until the $\overline{\text{ENABLE}}$ input goes high again. At this point the output stage is disabled — both source and sink — and the load current recirculates through D1 and D2 to ensure a fast decay. By varying the voltage V_i the peak load current can be programmed to any value in the range 0.6A to 4A. This feature can be exploited to implement two-level current control if the fixed reference is replaced by a switched reference as shown in figure 3.

Fig. 2 - Output current waveforms of the L294. The output current is regulated by switching between a peak value, I_p , and a lower limit of $0.9 I_p$.

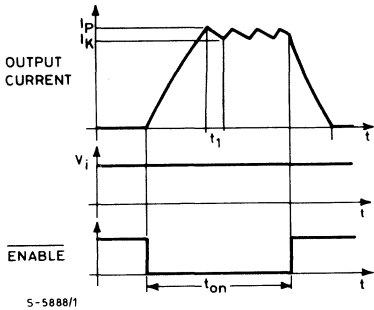


Fig. 3 - Two level current control can be implemented by switching V_i between two values.

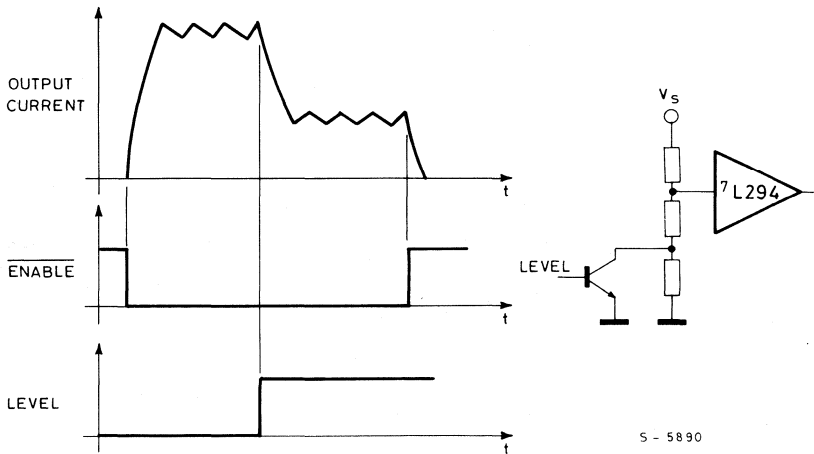
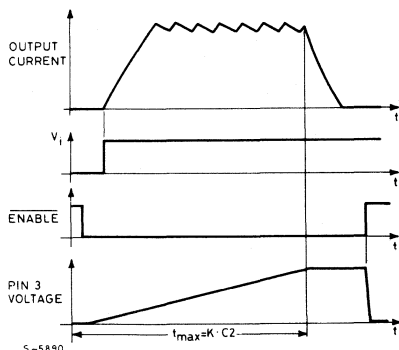


Fig. 4 - On-time limiter waveforms. After a period defined by C2 the output is disabled regardless of the state of ENABLE, protecting against overdriving.



PROTECTION

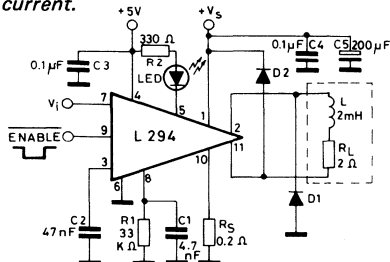
To protect the load and the L294 from overdriving an on-time limiter inhibits the output stage in-

dependently of the $\overline{\text{ENABLE}}$ input if the duration of the input pulse exceeds a period set by the external capacitor C2 (figure 4). This circuit is reset by taking the $\overline{\text{ENABLE}}$ input high. The on-time limiter can be disabled by grounding pin 3.

Protection against overheating is incorporated in the form of a thermal shutdown circuit which disables the output stage when the junction temperature exceeds 150°C. The circuit restarts when the temperature has fallen about 20°C.

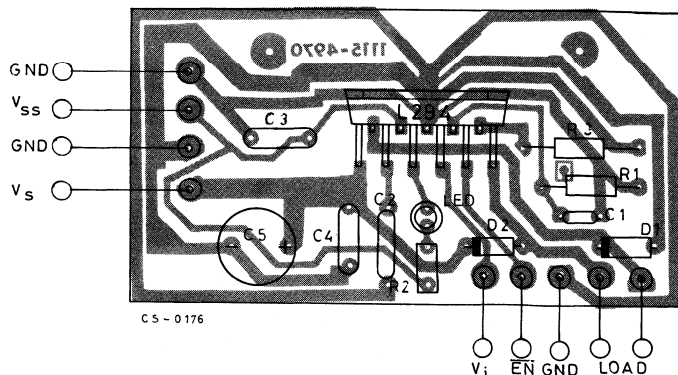
The L294 is also protected against short circuits to ground, to supply and across the load. Triggered when the source stage current exceed 5A or the sink stage current exceed $1V/R_s$, the short circuit protection block inhibits the output stage and sets a flip flop which is supplied by a separate supply voltage V_{ss} . This flip flop is connected to the diagnostic output and signals that all is not well — a shorted solenoid, for example. The diagnostic flip flop is reset by removing the supply V_s . A LED can be connected to the diagnostic output as shown in figure 5. If the diagnostic function is not required the V_{ss} supply can be omitted. The short circuit protection, however, still functions, even without V_{ss} .

Fig. 5 - Standard solenoid driving application of the L294. Pin 7 must be connected to a suitable reference voltage to set the peak current.



D1 : 3A Fast Diode } $t_{rr} \leq 200ns$ S-9
D2 : 1A Fast Diode }

Fig. 6 – Suggested printed circuit board layout for the application circuit of figure 5.



R1C1 determines the minimum value of t_1 (see figure 2), which is given by $t_1 \geq 0.1 \times R1C1$. C1 must be in the range 2.7 – 10 nF to ensure stability of the amplifier OTA. R1 must be at least 10 kΩ to give sufficient gain for OTA. The standard application circuit of figure 5 has a switching frequency of about 10 kHz.

The recirculation diodes should be fast types and rated at 3A (D1) and 1A (D2). If the full 4A capability of the L294 is not used these can be reduced.

A high initial peak and low holding current can be obtained with the circuit shown in figure 7a. This example supplies a current peak for about 10 ms.

The peak current, I_{OEX} , (see figure 7a) is found from:

$$I_{OEX} = \frac{V_z}{5} \cdot \frac{R_2}{R_s} \cdot \frac{1}{R_1 + R_2}$$

V_z is the zener voltage. The zener and R5 can be omitted if a regulated 5V supply is available for point A.

The holding current, I_{hold} , is found from:

$$I_{hold} = \frac{V_z}{5} \cdot \frac{(R_2 // R_4)}{R_s} \cdot \frac{1}{R_1 + (R_2 // R_4)}$$

The duration of the peak is determined by R3C1 and is increased by raising R3 or C1.

Typical component values are listed in the table below:

	$I_{OEX} = 4A$ $I_{HOLD} = 1A$	$I_{OEX} = 2.5A$ $I_{HOLD} = 0.5A$
R1	10 kΩ	10 kΩ
R2	47 kΩ	27 kΩ
R3	150 kΩ	150 kΩ
R4	2.7 kΩ	1.5 kΩ
R5	0.2 Ω (1W)	0.27 Ω (0.5W)
D1	3A	1.5A
D2	0.5A	0.5A
C1	0.2 μF	0.2 μF

Fig. 7a - Application circuit for two level current control. This circuit generates a high peak current for a period determined by R3C1 then a lower holding current.

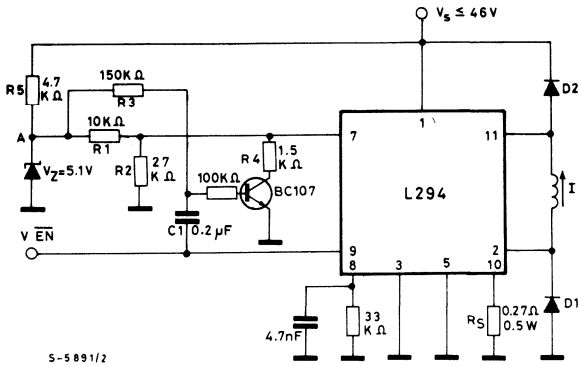


Fig. 7b - Output current waveform obtained with the circuit of fig. 7a.

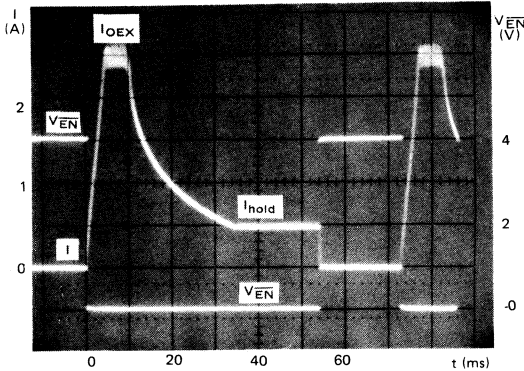


Figura 8 — Pin functions of the L294.

N°	FUNCTION
1	Solenoid supply voltage V_s (12–46V).
2	Output, source stage.
3	On-time limiter time constant. A capacitor to ground sets delay period (120 000 x C2 seconds). On-time limiter is disabled by grounding this pin.
4	Supply input (5V) for diagnostic flip flop.
5	Diagnostic output, open collector. Signals intervention of latched short circuit protection. Reset by removing pin 1 supply.
6	Ground.
7	V_i reference input. Peak output current is proportional to V_i . Transconductance is 1A/V for $R_S = 0.2 \Omega$ and $V_i \geq 600$ mV.
8	Timing. A parallel RC network from this pin to ground sets the minimum recirculation time constant. The capacitor must be 2.7–10 nF to ensure stability. The resistor must be greater than 10 k Ω .
9	<u>ENABLE</u> . TTL-compatible logic input that controls the solenoid current. The solenoid is driven when this input is at a low level. The on-time limiter overrides enable.
10	Connection for load current sense resistor.
11	Output, sink stage.

THE L295 DUAL SWITCHMODE DRIVER

The L295 is a dual switchmode solenoid driver which handles up to 2.5A per channel at voltages up to 46V — a total effective power handling of 220W. Compared to the L294 it offers a more economical solution when 2.5A is sufficient because there are two drivers per chip. Like the L294 it features switchmode regulation of the output current and thermal shutdown. Additionally it has a separate logic supply input so that the logic can be run at a lower voltage, reducing dissipation.

Intended for inductive load driving, the L295 is particularly suitable for solenoids and stepper motors. One L295 drives two solenoids and two

L295s can drive the four phases of a unipolar stepper motor or the two phases of a bipolar stepper motor in bridge configuration.

Each channel of the L295 is controlled by a TTL-level digital input and the peak load current is programmed, independently for each channel, by a voltage reference input. A chip enable input is also provided to disable both channels together.

INSIDE THE L295

Internally the L295 (figure 9) bears little resemblance to the L294. Looking at channel one, when the V_{IN1} input goes high the output transistors Q1 and Q2 are switched on (the enable input $\overline{EN}$ is assumed to be active, i.e. low). The current in the load then rises exponentially, as shown in figure 10, until the voltage across the external sense resistor R_{S1} reaches the current program reference voltage V_{ref1} .

The comparator COMP1 switches and sets the flip flop FF1 which turns off the source transistor Q1. The load current now recirculates through D2–Q2– R_{S1} and decays.

What happens next is determined by the oscillator components R and C on pin 9. If these components are present the flip flop is reset by the next clock pulse before the current decays very far. The output stage is therefore turned on again and the load current rises.

When it reaches the peak value COMP1 switches again, setting the flip flop and disabling the output stage. This process is repeated, regulating the load current until V_{in1} goes low. The output stage is then disabled and the current falls off rapidly, recirculating through D1 and D2 (figure 10).

If the oscillator components are omitted and pin 9 grounded the current simply decays slowly until V_{in1} goes low. The output stage is then disabled and the load current recirculates through D1 and D2. This case is illustrated by the waveforms of figure 11. Note that in this case the peak current level is controlled.

Unlike the L294, the switching frequency of the current regulation loop is determined by the oscillator components R and C (the L294 is also affected by the load). Typically, the switching frequency will be 10–30 kHz. Another difference between the two devices is that the L294 gives a constant ripple, the L295 does not.

TWO LEVEL CONTROL

Since the peak load current is programmed by the reference voltage (for each channel), two level current control can be obtained by switching between two reference voltages. A high V_{ref} is selected initially to give a high initial current peak. Then, after a suitable interval, V_{ref} is reduced to give the lower holding current (figure 12). Two level current control is very useful for solenoids which require a high initial current peak for fast actuation.

Fig. 9 - Internal block diagram of the L295 dual switchmode driver.

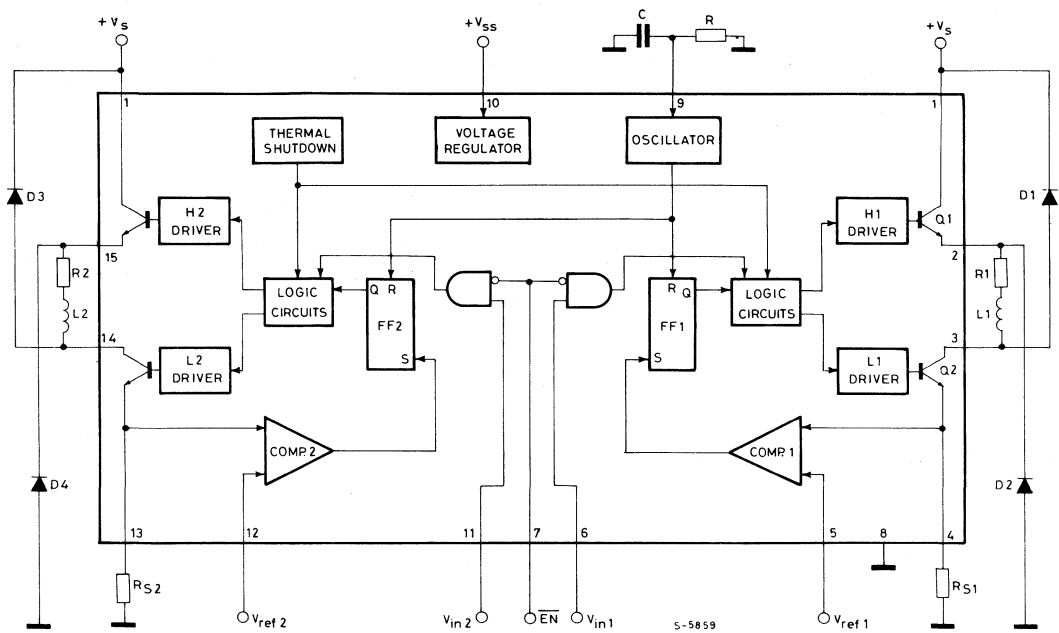


Fig. 10 - Waveforms illustrating normal operation of the L295.

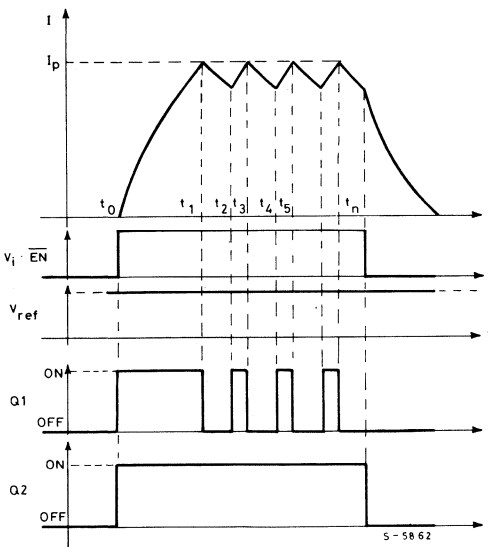


Fig. 11 - When the oscillator components are omitted and pin 9 grounded the L295 delivers a simple current peak to the load.

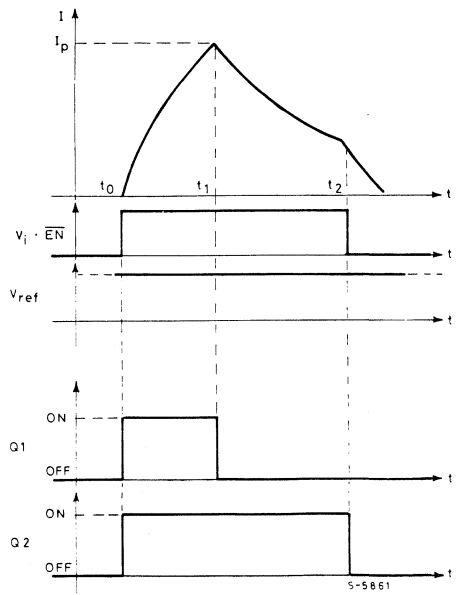
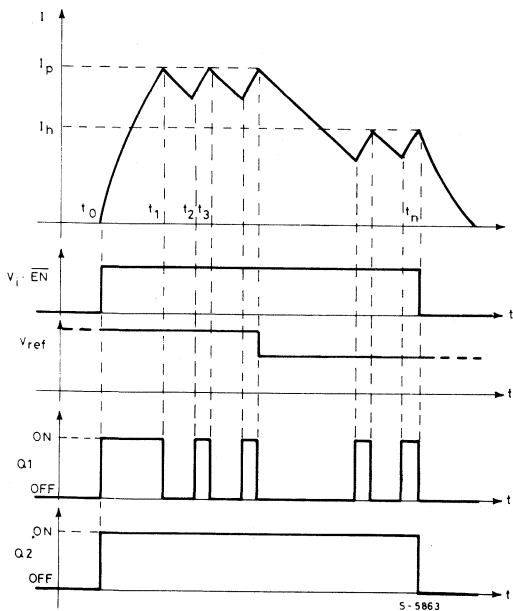


Figure 13 – Pin functions of the L295.



The basic application circuit of the L295 is shown in figure 14. A suitable layout is given in figure 15.

If the V_{ref} inputs are left open circuit the L295 assumes an internal default value of 2.5V giving a peak current of $2.5/R_s$ amperes.

Two L295s could also be used to drive a bipolar stepper motor in systems where a translator already exists.

N°	FUNCTION
1	Solenoid supply voltage, V_s (12-46V).
2	Channel one output, source stage.
3	Channel one output, sink stage.
4	RS_1 . Sense resistor connection, channel one.
5	V_{ref1} . A voltage on this pin sets peak current of channel one. If this pin is left open or connected to V_{ss} a default V_{ref} of 2.5V is assumed. An externally applied V_{ref} must be in the range 0.2 to 2V.
6	V_{in1} . Logic input for channel one. Driver is active when V_{in1} is high and $\overline{EN}$ low.
7	$\overline{EN}$. Chip enable (active low). When high both channels are disabled.
8	Ground.
9	Oscillator timing network. This pin is grounded to produce a single peak.
10	V_{ss} . Logic supply voltage, internally regulated. (4.75 - 10V).
11	V_{in2} . Logic input for channel two. Driver is active when V_{in2} is high and $\overline{EN}$ low.
12	V_{ref2} . Voltage input, controls peak current of channel two. If left open or connected V_s an internal 2.5V reference is assumed. An externally applied V_{ref} must be in the range 0.2 to 2V.
13	RS_2 . Sense resistor connection, channel two.
14	Channel two output, sink stage.
15	Channel two output, source stage.

Fig. 14 – Typical application circuit of the L295. R1L1 and R2L2 are solenoids.

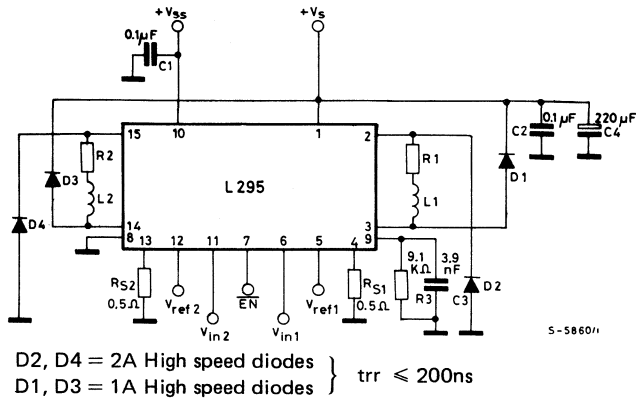


Fig. 15 – Suggested printed circuit board layout for the circuit of figure 14.

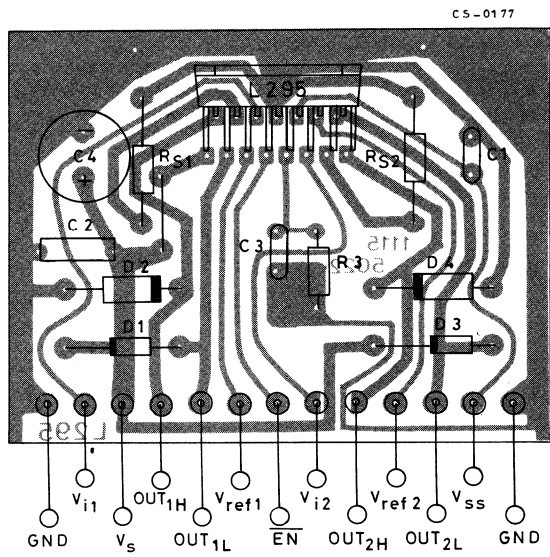


Fig. 16 – Nomogram for the selection of values for the oscillator components, RC.

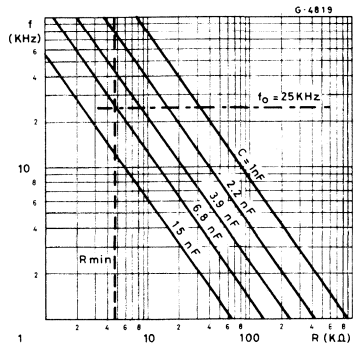
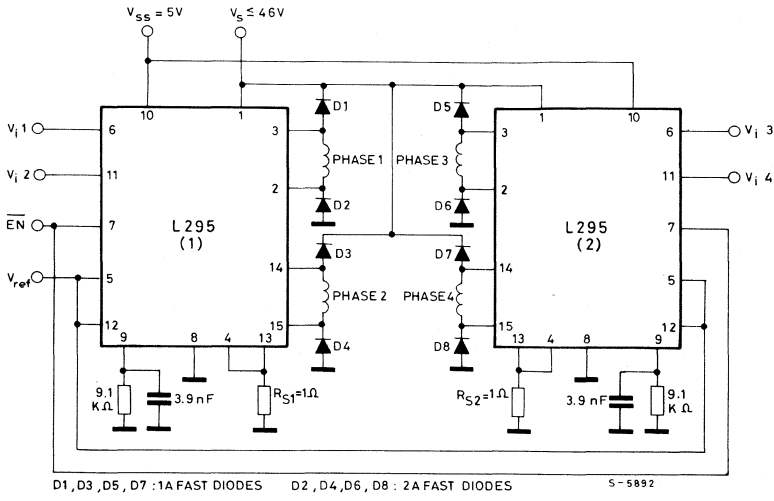


Fig. 17 - Two L295s, connected as shown, can be used to drive a four phase unipolar stepper motor.



SPEED CONTROL OF DC MOTORS WITH THE L292 SWITCH-MODE DRIVER

Power dissipation in DC motor drive systems can be reduced considerably with an L292 switchmode driver. This application guide describes two speed control systems based on this device; one voltage controlled and one controlled by a 6-bit binary word. Both examples are designed for 60W motors equipped with tacho dynamos.

The L292 is a monolithic power IC which functions effectively as a power transconductance amplifier. It delivers a load current proportional to an input voltage, handling up to 2A at 18-36V with a bridge output stage. Completely self-contained, it incorporates internal switchmode circuitry and all the active components to form a current feedback loop.

The L292 is designed primarily for use with an L290 and L291 in DC motor servopositioning applications. However, the L292 can be useful in a wide range of applications as the two examples here show. The first is a simple tachometer feedback circuit, the speed of which is controlled by a DC voltage; direction is controlled by the polarity of this voltage. The second circuit is controlled digitally and includes an L291 D/A converter.

SYSTEM WITH DC CONTROL

In this system the control quantity is a dc voltage variable between

$$+ V_{iM} \text{ and } - V_{iM}$$

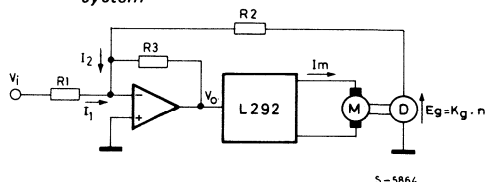
Since the quantity under control is the speed of the motor, it is required that it varies linearly in function of the control voltage.

A simplified circuit diagram of the system is shown in fig. 1.

The current I_1 , proportional to the set voltage V_i , and the current I_2 , proportional to the speed of the motor, are fed to the sum point of the error amplifier. Assuming that the motor does not drain current, the system is in a steady-state condition whenever $I_1 = -I_2$; as a matter of fact, in this case the output from the error amplifier V_o is OV. During transients, the voltage V_o will assume a value $V_o = -R3(I_1 + I_2)$ and consequently, since the L292 integrated circuit operates as a transconductance (G_m), a mean current $I_m = G_m \cdot V_o$

will flow in the motor determining an acceleration proportional to it.

Fig. 1 - Simplified circuit diagram of DC control system



Calculation of R1, R2, R3

Let us call:

V_{iM}	the maximum control voltage value
n_M	the maximum speed allowed for the motor
K_g	voltage constant of the dynamo

By imposing that the balance condition be met in correspondence to the maximum rotation speed the following equation is obtained:

$$I_1 = -I_2 ; \quad \frac{V_{iM}}{R1} = - \frac{K_g \cdot n_M}{R2}$$

Since R2 is the impedance which the tachometer dynamo is loaded on to and its value is recommended by the manufacturer, it is possible from the previous relationship to determine the value of R1.

Resistor R3 determines the system gain. It's best to keep the gain as high as possible (and consequently R3 as high as possible) to obtain a high response speed of the system, even for small variations in the control voltage. On the other hand, an excessive gain would cause excessive overshoot around the balance conditions at the end of transients. Consequently, a trade-off must be made between the two opposing requirements in select-

ing the final gain. The value for R3 should be theoretically determined by studying the transfer function, by knowing the electrical and mechanical constants of the motor as well as the load applied to it.

A complete diagram of the circuit actually realized is shown in fig. 2, while fig. 3, shows the characteristic $n = f(V_i)$ obtained.

Resistor R2 drawn in the simplified circuit diagram has been split here in two parts and, in addition, a capacitor has been interposed to ground to filter the signal coming from the tachometer dynamo.

The curve n. 1 in fig. 3 refers to the operation of the motor in no-load condition, with a current drain of 200 mA; the curve n. 2 refers to a motor loaded so as to drain a current of 1A. By disregarding the discontinuity around the origin, it can be noted that the characteristics are linear over the whole control voltage range.

By analyzing the curves around the origin, it can be noted that the motor stands still as long as the input signal does not exceed a certain threshold

level, which is as much higher as the current drained by the motor is higher.

Let us call G_m the transconductance of L292, and I the starting current of the motor; the voltage which must be available at the input of L292 in order that the motor starts turning is:

$$V_o = \frac{I}{G_m} \text{ with } G_m = 220 \frac{\text{mA}}{\text{V}} \text{ (typical value)}$$

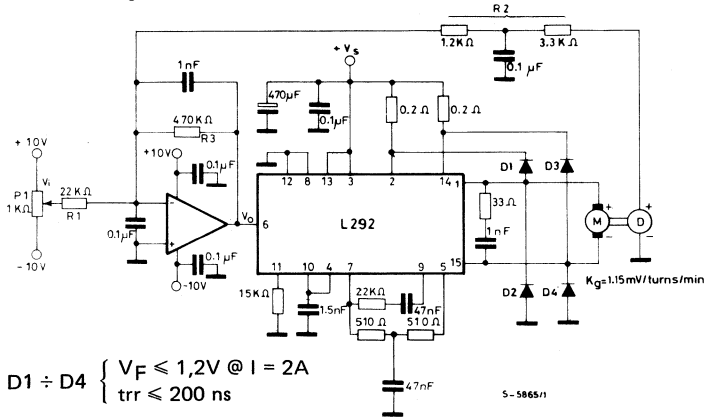
The corresponding control voltage will be:

$$V_i = V_o \cdot \frac{R1}{R3} = \frac{I}{G_m} \cdot \frac{R1}{R3}$$

and it is as much lower as the gain of the error amplifier is higher.

The presence of a control voltage interval in which the motor stands still, can be useful when it is required that, for a certain position of potentiometer P1 (see fig. 2), the motor speed be zero. An other method to hold the motor still is to use the inhibits of L292, for instance by grounding pin 13.

Fig. 2 - Complete circuit diagram



$$D1 \div D4 \left\{ \begin{array}{l} V_F \leq 1,2V @ I = 2A \\ trr \leq 200 ns \end{array} \right.$$

It can be noted from fig. 3 that, by keeping the control voltage V_i constant, the speed varies according to the motor current drain.

Let us call ΔI the current variation; the voltage variation required at the input of L292 is

$$\Delta V_o = \frac{\Delta I}{G_m}$$

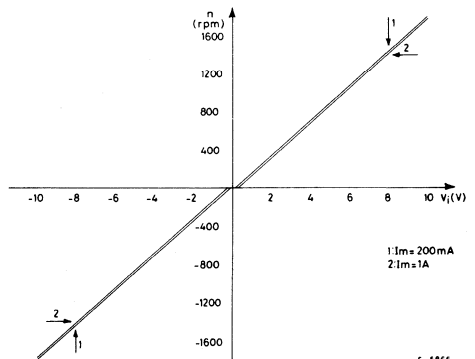
since the control voltage is constant, to generate this ΔV_o it is necessary that the rotation speed be varied by a quantity Δn such as to have:

$$K_g \cdot \Delta n \cdot \frac{R3}{R2} = \Delta V_o = \frac{\Delta I}{G_m}$$

$$\Delta n = \frac{\Delta I}{G_m K_g} \cdot \frac{R2}{R3}$$

(ΔI shall be taken with its sign)

Fig. 3 - Output characteristics of the circuit in fig. 2

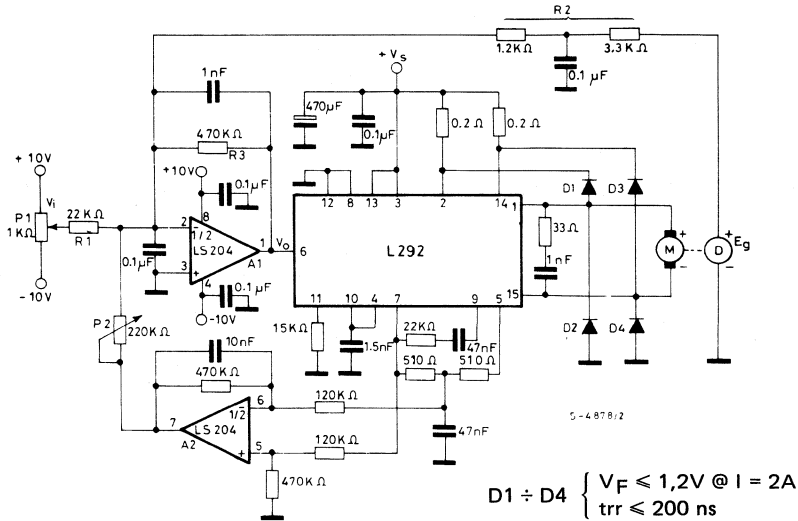


In this case too, the variation Δn is as much lower as the error amplifier gain is higher. With the circuit shown in fig. 2 Δn is approximately 30 turns/min. with $\Delta I = 800 \text{ mA}$, $\Delta n = 0.037 \text{ turns/mA}$.min approx.

variation in the number of turns in function of motor current. The problem is to "sense" the current flowing through the motor and to send a current proportional to it to the sum point of the error amplifier. The complete circuit which includes, beside the voltage feed-back loop, also a current feed-back loop, is illustrated in fig. 4.

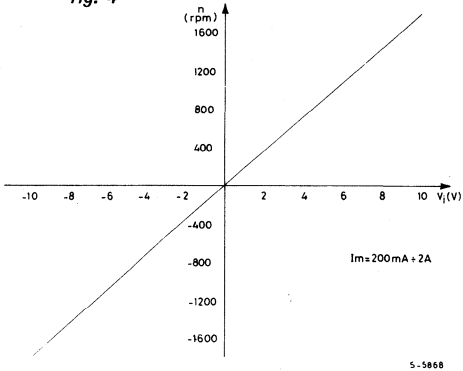
It is possible to adopt a circuit which prevents the

Fig. 4 - Complete circuit with current feedback



In the integrated circuit L292, a current proportional to the mean current drained by the motor flows between pin 5 and pin 7. An operational amplifier amplifies the voltage drop provoked by this current across a 510 Ω resistor and sends a current to the sum point which is consequently proportional to the mean current in the motor, the value of which can be made vary by acting on potentiometer P2. By properly adjusting P2, a condition can be achieved in which the speed does not change when the current drained by the motor varies.

Fig. 5 - Output characteristic of the circuit in fig. 4



The discontinuity around the origin, which was present in the previous circuit (fig. 2), is practically negligible in the circuit shown in fig. 4.

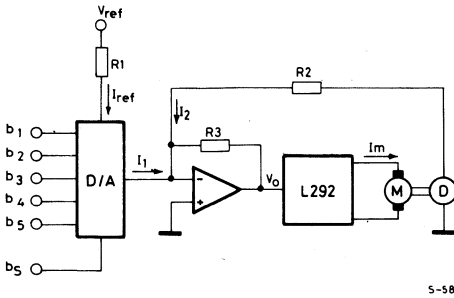
The characteristic $n = f(V_i)$ relevant to the circuit of fig. 4 is shown in fig. 5, and this characteristic does not substantially change over the whole range of currents allowed by the L292 (up to 2A). In the circuit described above if the motor stall condition is requested, it is preferable to act on the inhibits of the integrated circuit L292, for instance by grounding pin 13, instead of adjusting potentiometer P1: as a matter of fact, the exact position of this potentiometer is difficult to obtain, since the characteristic crosses the axis V_i in one only point (this means that n is only 0 for a very narrow interval of V_i).

SYSTEM WITH DIGITAL CONTROL

In this system the speed information is given to the circuit by a binary code made up of 5 information bits plus one sign bit, which determines whether the movement shall be clockwise or counter-clockwise. For the circuit implementation, the integrated circuits L291 (which includes a D/A converter and two operational amplifiers) and L292 are used.

A simplified circuit diagram is shown in fig. 6.

Fig. 6 - Simplified circuit diagram (digital control)



dition (no current drained by the motor), it must be:

$$I_1 = -I_2$$

By imposing the balance condition at the maximum speed, one obtains: $I_1 \max = -I_2 \max$

$$\frac{V_{ref}}{R1} \cdot \frac{31}{16} = -\frac{K_g n_M}{R2}$$

where

K_g = dynamo's voltage constant
 n_M = maximum speed preset for the motor.

The current value I_1 depends on the value of I_{ref} and on the value of inputs b_1 through b_5 , where its sign depends on the b_5 input. The maximum value for I_1 , which is obtained whenever inputs b_1 through b_5 are low, is:

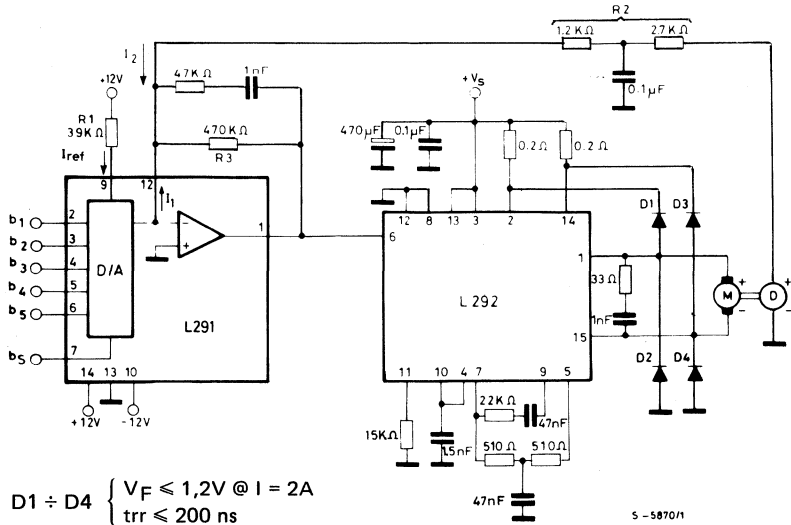
$$I_1 \max = I_{ref} \frac{31}{16} = \frac{V_{ref}}{R1} \cdot \frac{31}{16}$$

In order to have the system in a steady state con-

The current I_{ref} , and consequently the ratio $V_{ref}/R1$, must lie within a certain range imposed by the D/A converter actually used. In our case, this range is 0.3 to 1 mA. The values of $R1$ and $R2$ can be determined from the previous relationship. The same considerations made in the description of the DC control system apply for the selection of $R3$.

A complete diagram of the circuit implemented is indicated in fig. 7, while the input versus output characteristics is shown in fig. 8.

Fig. 7 - Complete circuit diagram



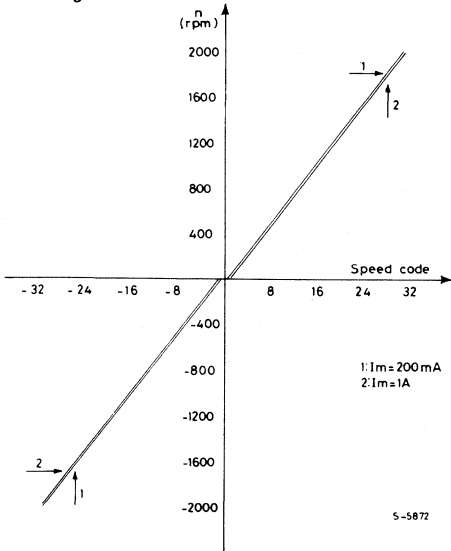
$$D1 \div D4 \begin{cases} V_F \leq 1.2V @ I = 2A \\ trr \leq 200 ns \end{cases}$$

In the graph of fig. 8 the rotation speed of the motor is represented on ordinates, while the decimal speed code, corresponding to the binary code applied to inputs b_1 through b_5 , is represented on abscissae.

The abscissa 1 corresponds to the minimum speed code, i.e. input b_1 low and remaining inputs high, since the least significant input is b_1 and the active status of inputs is low. The abscissa 31 corresponds to the maximum speed code, i.e. all inputs

b_1 through b_5 low. The negative abscissae have been obtained by changing the status of the b_5 input. The graph in fig. 8 should have been made up of a number of dots; these dots have been joined together with an uninterrupted line for convenience. This graph has the same features as the graph in fig. 3, i.e. the curve features a discontinuity around the origin, and it lowers as long as the motor current drain increases. In this case too, the circuit in fig. 7 can be modified in order to

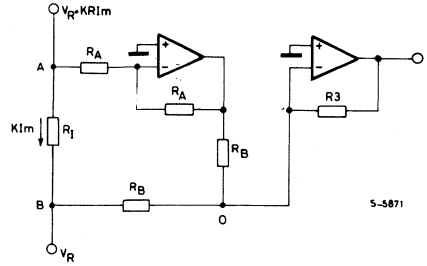
Fig. 8 - Output characteristic of the circuit in fig. 7



prevent that the speed vary in function of the motor load, by adding a current loop in the control circuit, by using the remaining operational amplifier available in the integrated circuit L291.

Since this amplifier has only the inverting input available, while the non-inverting input is grounded, a circuit arrangement as schematically shown in fig. 9 has been adopted in order to have an output signal referred to ground, given an input signal referred to a reference voltage (in L292) of approximately 8V.

Fig. 9 - Translator circuit



Resistors R_A and R_B must be high-precision resistors in order to have output 0 with no I_m current present. In the practical implementation, resistors with an accuracy of 5% are used and the ends of a potentiometer are interposed between resistors R_B and the output to the sum point of the error amplifier is made through the cursor. The gain of this current loop is proportional to the ratio R_3/R_B . A complete circuit diagram is shown in fig. 10.

Since, for reasons of gain, resistor R_B must be 27 k Ω and, if connected to pin 7 of L292, should have subtracted too much current by thus affecting the correct operation of L292, it has been connected to pin 11, having the same potential as pin 7. Consequently, the resistance value between pin 11 and ground has been modified, in order to maintain the switching frequency of L292 unchanged. In order to have a correct adjustment of potentiometer P1, it is enough to set the O speed code (b_1 through b_5 high) and turn the cursor until the motor stops.

The input versus output characteristic obtained with the circuit of fig. 10 is indicated in fig. 11.

Fig. 10 - Complete circuit with current feedback

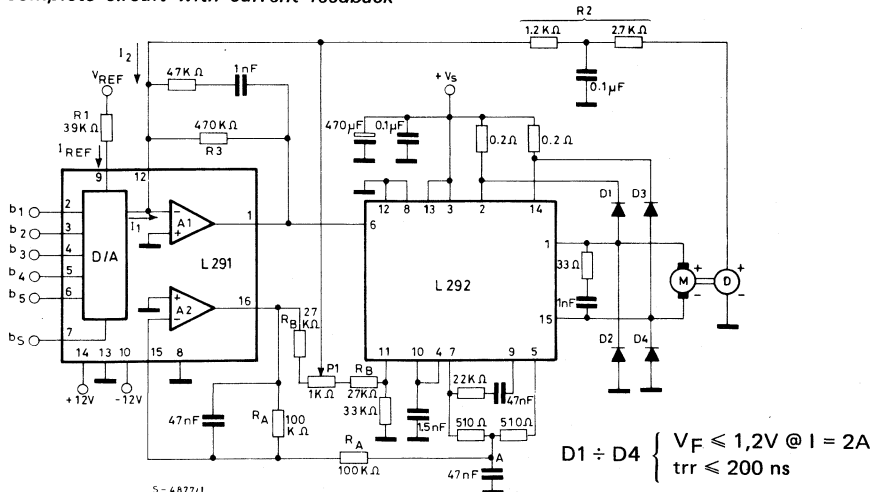
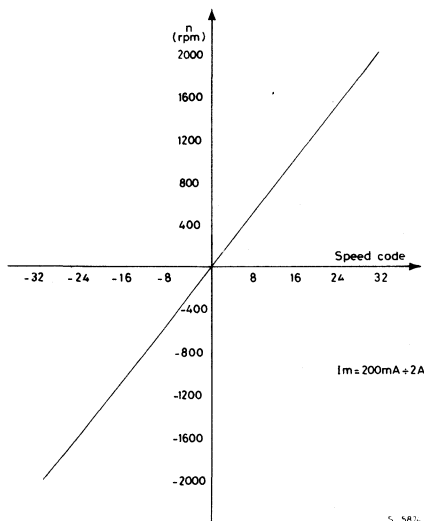


Fig. 11 - Output characteristic of the circuit in fig. 10



RESPONSE TO INPUT STEP

Measurements have been taken on the circuits described in the previous paragraphs, in order to analyze how the motor speed varies when a step variation is imposed to the input.

For the system DC control, the control voltage has been changed from 0 to the maximum value V_{iM} and down to 0 again. For the digital system the speed code has been changed from 0 (b_1 through b_5 high) to the maximum value (b_1 through b_5 low) and down to 0 again. When the control quantity changes from 0 to the maximum value, the output voltage of the error amplifier (V_o , fig. 1 and fig. 6) assumes its maximum value, since the feed-back signal coming from the tachometer dynamo initially 0. In these conditions, L292 supplies the motor with the maximum current (2A) and maintains it until the motor speed is sufficiently close to the maximum value.

Since the motor is powered from a constant current, it moves with a constant acceleration and consequently its speed grows linearly from 0 up to the maximum value over the time interval t_a . The time needed for the motor to reach the maximum speed also depends, besides the current, on the electrical and mechanical characteristics of the motor and on the moment of inertia of the load applied to the motor. When the control quantity changes from the maximum value to 0, the output of the error amplifier V_o assumes the maximum value, but with an opposite sign with respect to the previous case, and the current flowing in the motor is also reversed and tends to brake it, by making the speed linearly decrease from the maximum value down to 0 over the time period t_f .

The no-load characteristics, relevant to the motor used for the previous tests, are shown in fig. 12. The times t_a and t_f are not equal to each other, which circumstance is basically due to the frictions which, during the acceleration phase, oppose increase of speed, while during the deceleration phase they contribute to make the speed decrease. As a matter of fact, from the movement equation:

$$J \ddot{\Theta} + D \dot{\Theta} + T_f = K_T I_M$$

where:

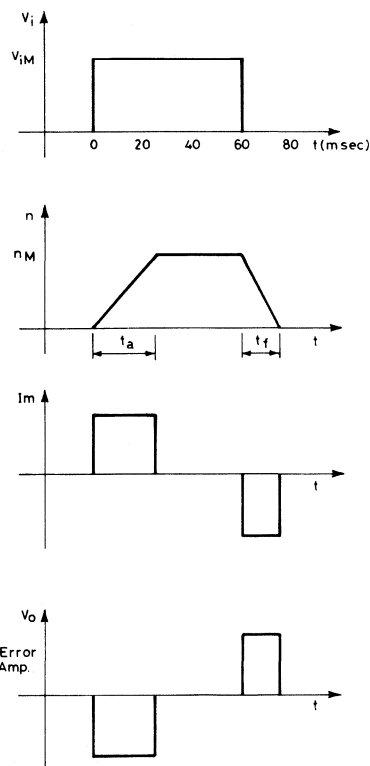
- J = System moment of inertia
- D = Coefficient of viscous friction
- T_f = Braking couple
- K_t = Motor constant
- $\dot{\Theta}$ = Angular speed
- $\ddot{\Theta}$ = Angular acceleration

and by disregarding the term $D\dot{\Theta}$, one obtains:

$$\ddot{\Theta} = \frac{K_T \cdot I_M - T_f}{J}$$

where from it can be seen that $|\ddot{\Theta}|$ is greater if I_M is negative.

Fig. 12 - Pulse response



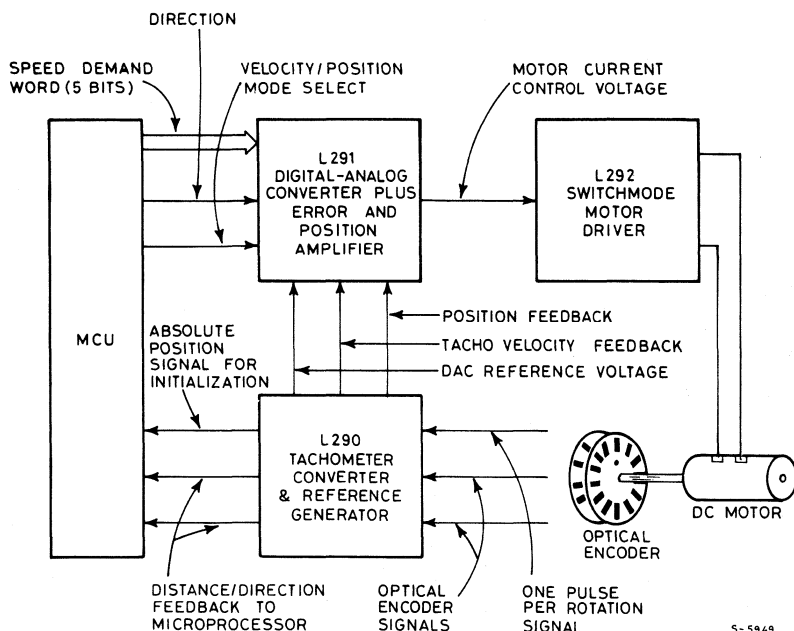
A DESIGNER'S GUIDE TO THE L290/L291/L292 DC MOTOR SPEED/POSITION CONTROL SYSTEM

The L290, L291 and L292 together form a complete microprocessor-controlled DC motor servopositioning system that is both fast and accurate. This design guide presents a description of the system, detailed function descriptions of each device and application information.

The L290, L291 and L292 are primarily intended for use with a DC motor and optical encoder in the configuration shown schematically in figure 1. This system is controlled by a microprocessor, or micro-computer, which determines the optimum speed profile for each movement and passes appropriate commands to the L291, which contains the system's D/A converter and error amplifiers. The

L291 generates a voltage control signal to drive the L292 switchmode driver which powers the motor. An optical encoder on the motor shaft provides signals which are processed by the L290 tachometer converter to produce tacho voltage feedback and position feedback signals for the L291 plus distance/direction feedback signals for the control micro.

Fig. 1 - The L290, L291 and L292 form a complete DC motor servopositioning system that connects directly to microcomputer chips.



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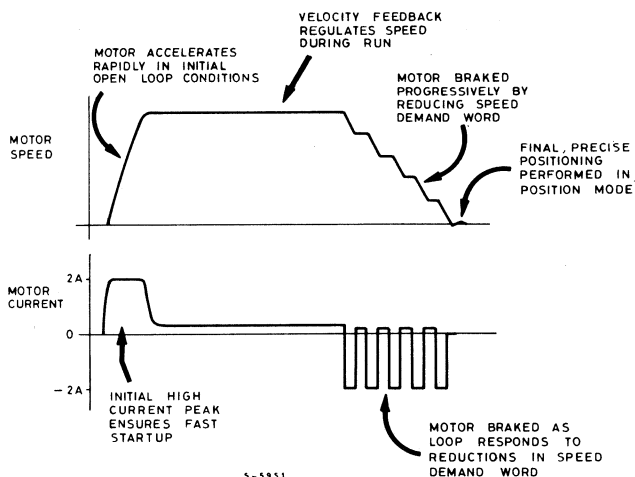
The system operates in two modes to achieve high speed and accuracy: closed loop speed control and closed loop position control. The combination of these two modes allows the system to travel rapidly towards the target position then stop precisely without ringing.

Initially the system operates in speed control mode. A movement begins when the microcomputer applies a speed demand word to the L291, typically calling for maximum speed. At this instant the motor speed is zero so there is no tacho feedback and the system operates effectively in open loop mode (see figure 2). In this condition a high current peak — up to 2A — accelerates the motor rapidly to ensure a fast start.

As the motor accelerates the tacho voltage rises and the system operates in closed loop speed mode, moving rapidly forwards the target position. The microcomputer, which is monitoring the optical encoder signals (squared by the L290), reduces the speed demand word gradually when the target position is close. Each time the speed demand word is reduced the motor is braked by the speed control loop.

Finally, when the speed code is zero and the target position extremely close, the micro commands the system to switch to position mode. The motor then stops rapidly at the desired position and is held in an electronic detent.

Fig. 2 - The system operates in two modes to achieve high speed and accuracy. Tachometer feedback regulates the speed during a run and brakes the motor towards the end. Position feedback allows a precise final positioning.



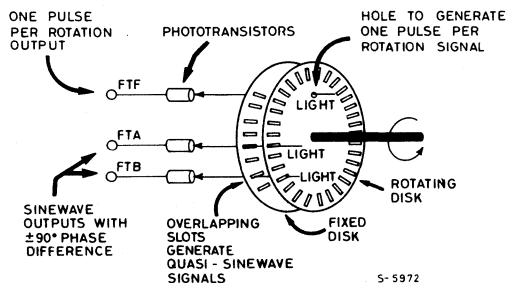
OPTICAL ENCODER

The optical encoder used in this system is shown schematically in figure 3. It consists of a rotating slotted disk and a fixed partial disk, also slotted.

Light sources and sensors are mounted so that the encoder generates two quasi-sinusoidal signals with a phase difference of $\pm 90^\circ$. These signals are referred to as FTA and FTB. The frequency of these signals indicates the speed of rotation and the relative phase difference indicates the direction of rotation. An example of this type is the Sensor Technology STRE 1601, which has 200 tracks. Similar types are available from a number of manufacturers including Sharp and Eleprint.

This encoder generates a third signal, FTF, which consists of one pulse per rotation. FTF is used to find the absolute position at initialization.

Fig. 3 - The system operates with an optical encoder of the type shown schematically here. It generates two signals 90° out of phase plus a one pulse-per-rotation signal.



THE L290 TACHOMETER CONVERTER

The L290 tachometer converter processes the three optical encoder signals FTA, FTB, FTF to generate a tachometer voltage, a position signal and feedback signals for the microprocessor. It also generates a reference voltage for the system's D/A converter.

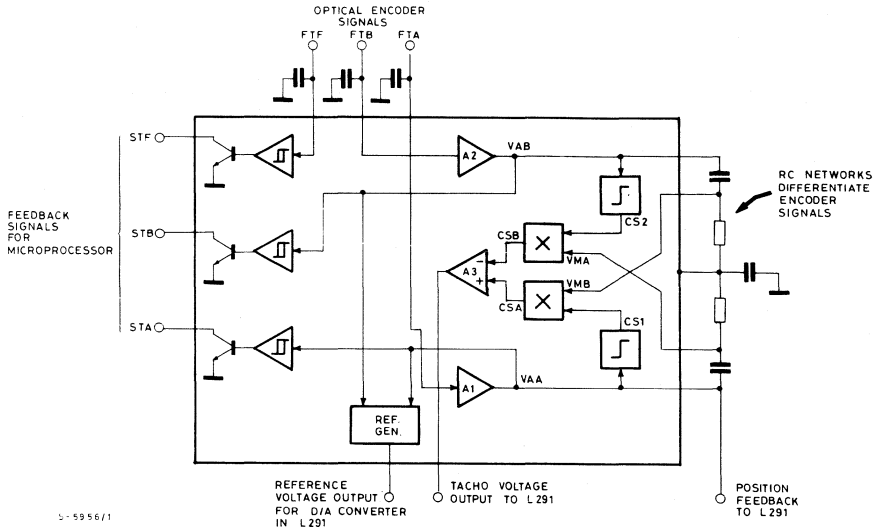
Analytically, the tacho generation function can be expressed as:

TACHO =

$$\frac{dV_{AB}}{dt} \cdot \frac{FTA}{|FTA|} - \frac{dV_{AA}}{dt} \cdot \frac{FTB}{|FTB|}$$

In the L290 (block diagram, figure 4) this function is implemented by amplifying FTA and FTB in A1 and A2 to produce V_{AA} and V_{AB} . V_{AA} and V_{AB} are differentiated by external RC networks to give the signals V_{MA} and V_{MB} which are phase

Fig. 4 - The L290 processes the encoder signals, generating a tacho voltage and position signal for the L291 plus feedback signals for the microprocessor. Additionally, it generates a reference voltage for the L291's D/A converter.



shifted and proportional in amplitude to the speed of rotation. V_{MA} and V_{MB} are passed to multipliers, the second inputs of which are the sign of the other signal before differentiation.

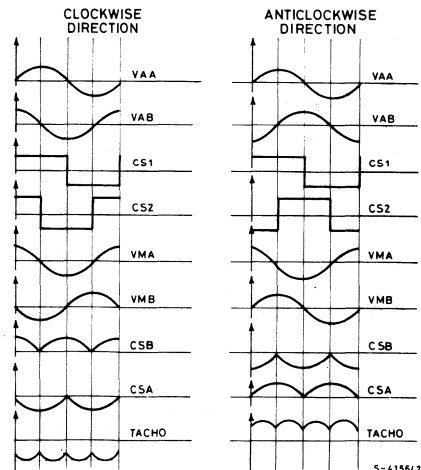
The sign ($\frac{FTA}{|FTA|}$ or $\frac{FTB}{|FTB|}$) is provided by the comparators CS1 and CS2. Finally, the multiplier outputs are summed by A3 to give the tacho signal. Figure 5 shows the waveforms for this process.

This seemingly complex approach has three important advantages. First, since the peaks and nulls of CSA and CSB tend to cancel out, the ripple is very small. Secondly, the ripple frequency is the fourth harmonic of the fundamental so it can be filtered easily without limiting the bandwidth of the speed loop. Finally, it is possible to acquire tacho information much more rapidly, giving a good response time and transient response.

Feedback signals for the microprocessor, STA, STB and STF, are generated by squaring FTA, FTB and FTF. STA and STB are used by the micro to keep track of position and STF is used at initialization to find the absolute position.

Position feedback for the L291 is obtained simply from the output of A1.

Fig. 5 - These waveforms illustrate the generation of the tacho voltage in the L290. Note that the ripple is fourth harmonic. The amplitude of TACHO is proportional to the speed of rotation.



The L290 also generates a reference voltage for the L291's D/A converter. This reference is derived from V_{AA} and V_{AB} with the function:

$$V_{ref} \equiv |V_{AA}| + |V_{AB}|$$

Since the tacho voltage is also derived from V_{AA} and V_{AB} it follows that the system is self compensating and can tolerate variations in input levels, temperature changes and component ageing with no deterioration of performance.

THE L291 D/A CONVERTER AND AMPLIFIERS

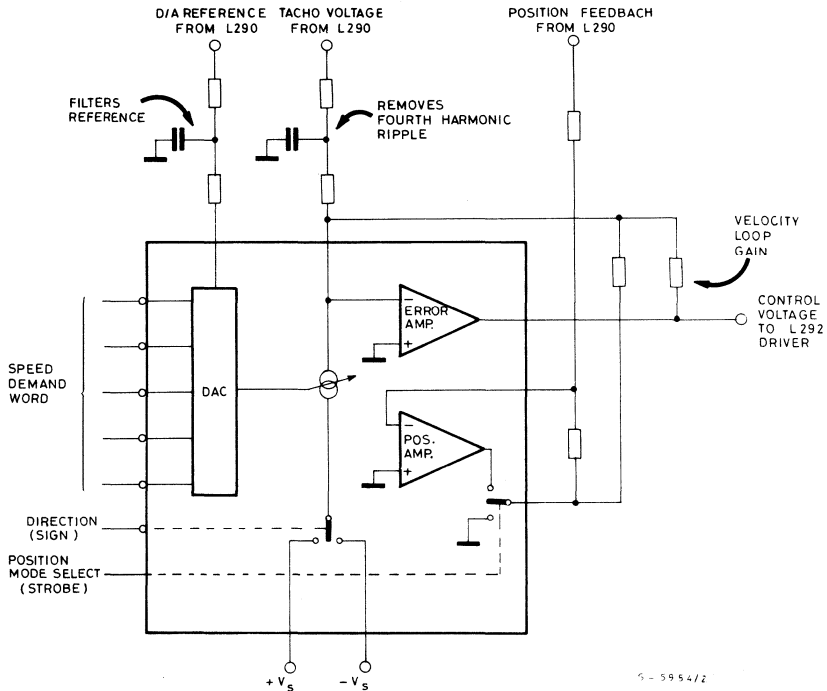
The L291, shown in figure 6, links the system to

the micro and contains the system's main error amplifier plus a position amplifier which allows independent adjustment of the characteristics of the position loop.

It contains a five bit D/A converter with switchable polarity that takes its reference from the L290. The polarity, which controls the motor direction, is controlled by the micro using the SIGN input.

The main error amplifier sums the D/A converter output and the tacho signal to produce the motor drive signal ERRV. The position amplifier is provided to allow independent adjustment of the position loop gain characteristics and is switched in/out of circuit to select the mode. The final position mode is actually 'speed plus position' but since the tacho voltage is almost zero when position mode is selected the effect of the speed loop is negligible.

Fig. 6 - The L291 links the system to the microprocessor. It contains the system DA converter, main error amplifier and position amplifier.



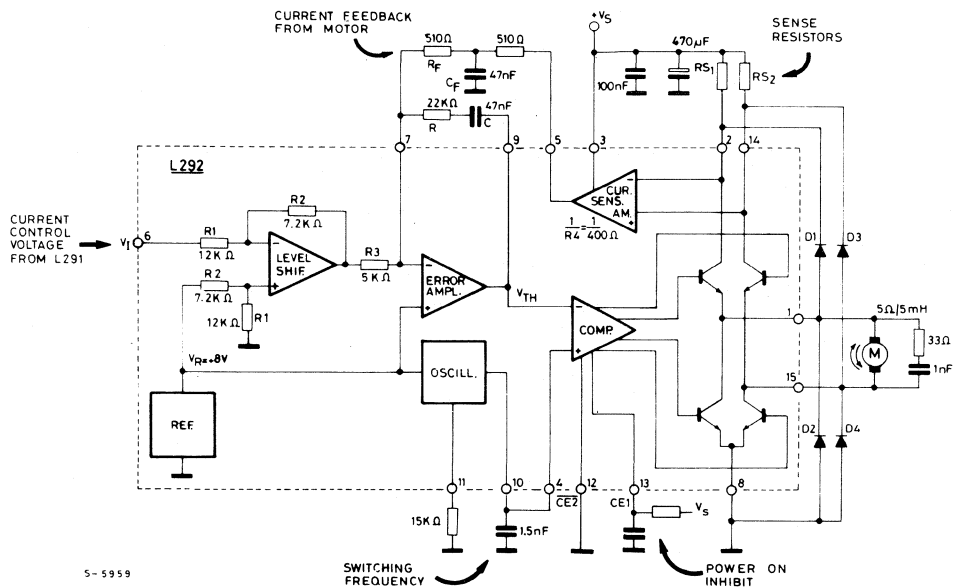
THE L292 SWITCHMODE MOTOR DRIVER

The L292 can be considered as a power transconductance amplifier — it delivers a motor current proportional to the control voltage (ERRV) from the L291. It drives the motor efficiently in switchmode and incorporates an internal current feedback loop to ensure that the motor current is always proportional to the input control signal.

The input control signal (see block diagram, figure 7) is first shifted to produce a unipolar signal (the L292 has a single supply) and passed to the error amplifier where it is summed with the current feedback signal. The resulting error signal is used to modulate the switching pulses that drive the output stage.

External sense resistors monitor the load current, feeding back motor current information to the error amplifier via the current sensing amplifier.

Fig. 7 - The L292 switchmode driver receives a control voltage from the L291 and delivers a switchmode regulated current to the motor.



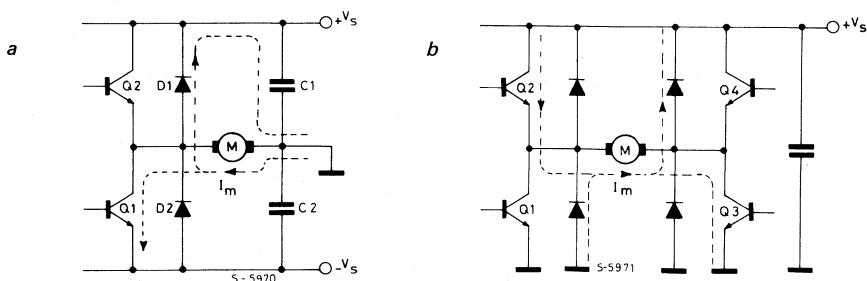
The L292 incorporates its own voltage reference and all the functions required for closed loop current control of the motor. Further, it features two enable inputs, one of which is useful to implement a power on inhibit function.

The L292's output stage is a bridge configuration capable of handling up to 2A at 36V. A full bridge stage was chosen because it allows a supply voltage to the motor effectively twice the voltage allowed if a half bridge is used. A single supply was chosen to avoid problems associated with pump-back energy.

In a double supply configuration, such as the example in figure 8a, current flows for most of the time through D1 and Q1. A certain amount of power is thus taken from one supply and pumped back into the other. Capacitor C1 is charged and its voltage can rise excessively, risking damage to the associated electronics.

By contrast, in a single supply configuration like figure 8b the single supply capacitor participates in both the conduction and recirculation phases. The average current is such that power is always taken from the supply and the problem of an uncontrolled increase in capacitor voltage does not arise.

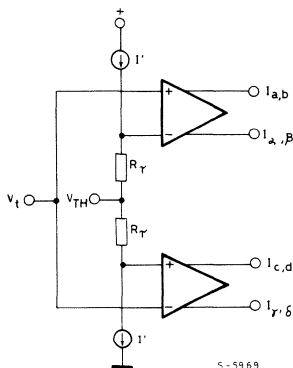
Fig. 8 - A simple push pull output (a) needs a split supply and the device can be damaged by the voltage built up on C1. The L292 has a bridge output to avoid these problems. Only one supply is needed and the voltage across the single capacitor never rises excessively. Moreover, the motor can be supplied with a voltage up to twice the voltage allowed with a half bridge.



A problem associated with the system used in the L292 is the danger of simultaneous conduction in both legs of the output bridge which could destroy the device. To overcome this problem the comparator which drives the final stage consists of two separate comparators (figure 9). Both receive the same V_t , the triangular wave from the oscillator, signal but on opposite inputs.

The other two inputs are driven by V_{TH} , the error amplifier output, shifted by plus or minus $R_T I'$. This voltage shift, when compared with V_t , results in a delay in switching from one comparator to the other.

Fig. 9 - The L292's final comparator actually consists of two comparators. This configuration introduces a delay to prevent simultaneous conduction of two legs.

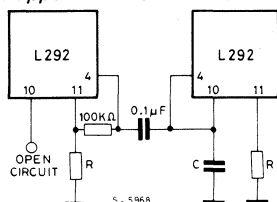


Consequently there will always be a delay between switching off one leg of the bridge and switching on the other. The delay τ is a function of the integrated resistor R ($1.5 \text{ k}\Omega$) and an external capacitor $C17$ connected to pin 10 which also fixes the oscillator frequency. The delay is given by:

$$\tau = R\tau \quad \text{C17}$$

In multiple L292 configurations (in a typewriter, for example, there may be two systems) it is desirable to synchronise the switching frequencies to avoid intermodulation. This can be done using the configuration shown in figure 10.

Fig. 10 - Ground plane switching noise and modulation phenomena are avoided in multi-L292 systems by synchronizing the chopper rate with this RC network.

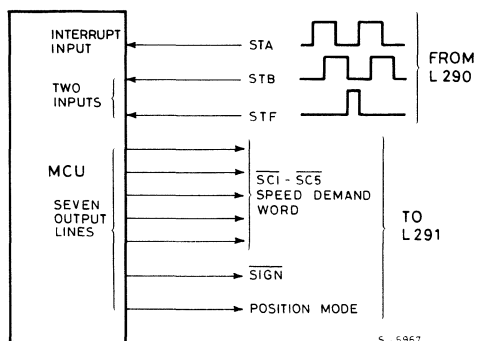


SOFTWARE AND INTERFACING TO THE MICRO

In a typical system the L290/1/2 system is connected to the control microcomputer through ten I/O lines: seven outputs and three inputs.

The outputs are all connected to the L291 D/A converter and consist of the five bit speed demand word, SIGN (which sets the direction) and the speed/position mode select line. Position feedback for the micro comes from the L290 tachometer and consists of the signals STA, STB (the squared encoder outputs) plus the one-pulse-per-rotation signal, STF (figure 11).

Fig. 11 - In a typical system the L290/L291/L292 combination is linked to the micro through seven output lines, two inputs and an interrupt input.



To follow the motor position the micro counts the STA pulses to measure the distance travelled and compares the phase of STA and STB to sense the direction. The most convenient way to do this is to connect the STA line to an interrupt input. An interrupt service routine will then sample STB and increment or decrement the position count depending on the relative phase difference: $+90^\circ$ if STB is high: -90° if STB is low.

It could be argued that the micro doesn't need to sense the direction of the rotation because it controls the direction. In practice, however, it is better to sense the direction to allow for the possibility that the motor may be moved by externally applied forces.

For each movement the micro calculates the distance to be travelled and determines the correct direction. It then sets the L291 to velocity feedback mode, sets the director appropriately and sets the speed demand word for maximum speed (possibly less if the move is very short).

By means of the STA interrupt service routine it follows the changing position, reducing the speed demand word to brake the motor when the target position is very close. Finally, the micro orders the L291 to switch to position loop control for the final precise positioning.

Fig. 12 - Complete application circuit of the system.

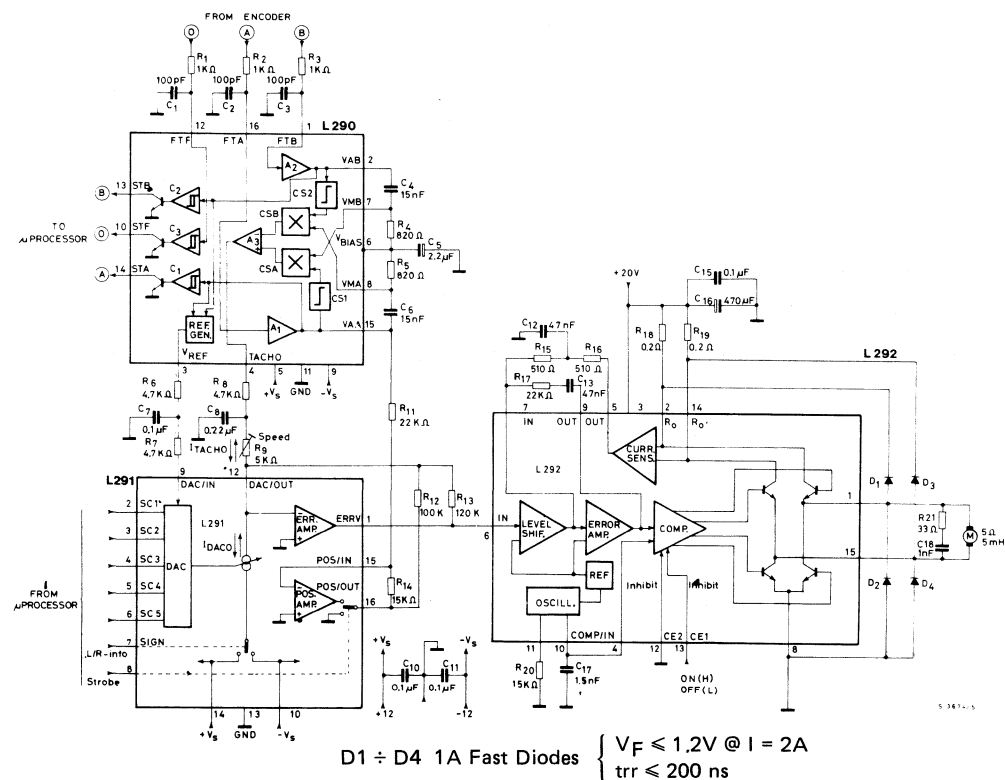


Fig. 13 – P.C. board and component layout (1:1 scale)

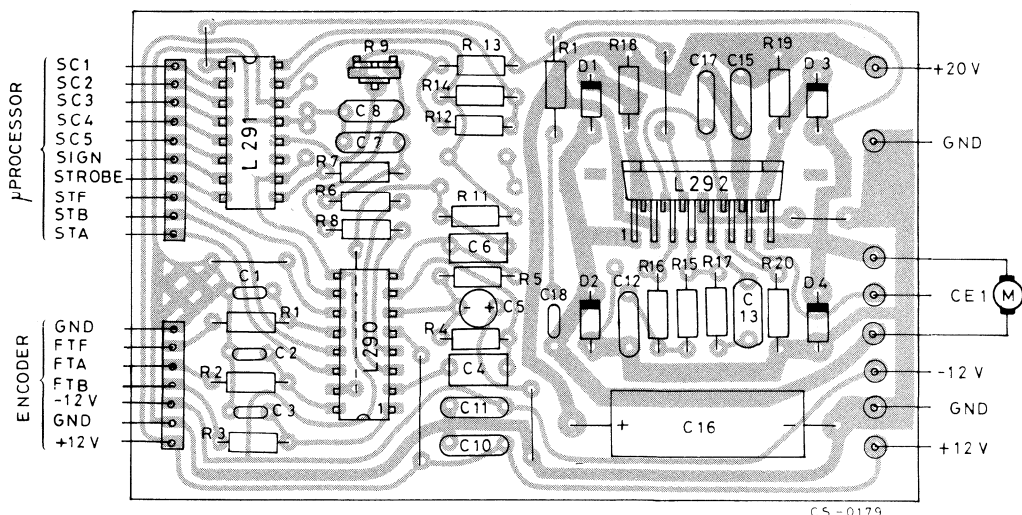


Fig. 14

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
R1, R2, R3	1 k Ω	To filter the noise on the encoder signals	Offset voltage increase (V_{AA}, V_{AB})	
R4, R5	820 Ω	Differentiator network	Tacho offset and tacho signal increase	Tacho offset increase Tacho signal decrease
R6, R7	4,7k Ω	To set the D/A input current	D/A input current decrease	D/A input current increase
R8	4.7k Ω	To set the motor speed	Motor speed increase	Motor speed decrease
R9	5k Ω	To adjust the motor speed	Danger of oscillation $R9 \leq R13/10$	
R11	22k Ω	To set the position loop gain	– Position loop gain decrease	– Position loop gain increase – Danger of oscillation of the motor shaft
R12	100k Ω	To set the position loop gain	– Position loop gain decrease	– Position loop gain increase – Danger of oscillation of the motor shaft
R13	120k Ω	To set the speed loop gain	– Speed loop gain increase	– Speed loop gain decrease
R14	15k Ω	To set the position loop gain	– Position loop gain increase – Danger of oscillation of the motor	– Position loop gain decrease
R15, R16	510 Ω	To filter the feedback current	Danger of output saturation of the current sensing amplifier $R15 + R16 \leq 3.3k\Omega$	
R17	22k Ω	To set the gain of the err. amplifier	Increase of the gain at high frequencies	Danger of oscillations $R17 > 5.6k\Omega$
R18, R19	0.2 Ω	To set the transconductance value of the L292	Transconductance decrease (R18, R15). $I_m \leq 0.44V$	Transconductance increase
R20	15k Ω	To set the oscillator frequency	Oscillator frequency decrease	Oscillator frequency increase. $R20 \geq 8.2k\Omega$
R21	33 Ω	Compensation network		Increase of the peak current in the output transistors during the commutations
C1, C2, C3	100 pF	To filter the noise on the encoder signals	Bandwidth reduction of the low pass filter	Bandwidth increment of the low pass filter
C4, C6	15 nF	Differentiator network	Tacho signal increase	Tacho signal decrease
C5	2.2 μF	By-pass capacitor	Larger set-up time after power on	Reduced by-pass effect at low frequencies
C7	0.1 μF	Low-pass filter for the D/A input current		Increase of the current ripple at low speed
C8	0.22 μ	– Low pass filter for the tacho signal – To determine the dominant pole of the speed loop	Bandwidth reduction of the speed loop	Low filtering at low speed, causing noise on the motor
C10, C11	0.1 μF	Supply by-pass capacitor		Danger of oscillations
C12	47 nF	To filter the feedback current	– Lower value of the damping factor – Danger of oscillations	– Higher value of dumping factor
C13	47 nF	To set the gain of the error amplifier $C13 \cdot R17 = L_M/R_M$		
C15	0.1 μF	Supply by-pass capacitor		Danger of oscillations
C16	470 μF	Supply by-pass capacitor		Ripple increment on the supply voltage
C17	1.5 nF	To set the oscillator frequency and the dead time of the output transistors	– Oscillation frequency reduction – Dead time increment	– Oscillation frequency increment. – Dead time reduction
C18	1 nF	Compensation network		Danger of oscillations
D1, D2, D3, D4	1A Fast diodes	Recirculation diodes		

Where the optical encoder rotates more than once the 'one-pulse-per-rotation' signal is not sufficient. An example of this is the carriage positioning servo of a computer printer. In this case the simplest solution is to fit a microswitch on one of the endstops. First the motor is run backwards slowly until the carriage hits the endstop. Then it moves forward until the STF signal is detected. The beauty of this solution is that the endstop micro-switch does not need to be positioned accurately.

Figure14 explains what each component does and what happens if it is varied. Maximum and minimum values are also indicated where appropriate.

The circuit shown in figure 16 is suitable for motor currents up to 50A at voltages to 150V. Two supplies are used; 24V for the L292 and LS141 and 150V for the external transistors and motor. This circuit too behaves just like an L292, except for the higher power, and connects to the L290 and L291 as usual.

The motor current is given by:

$$I_m = \frac{V_{in} \times 120 \times 10^{-6} R}{R_s}$$

where $R_s = R_{s1} = R_{s2} = 12 \times 10^{-3} \Omega$

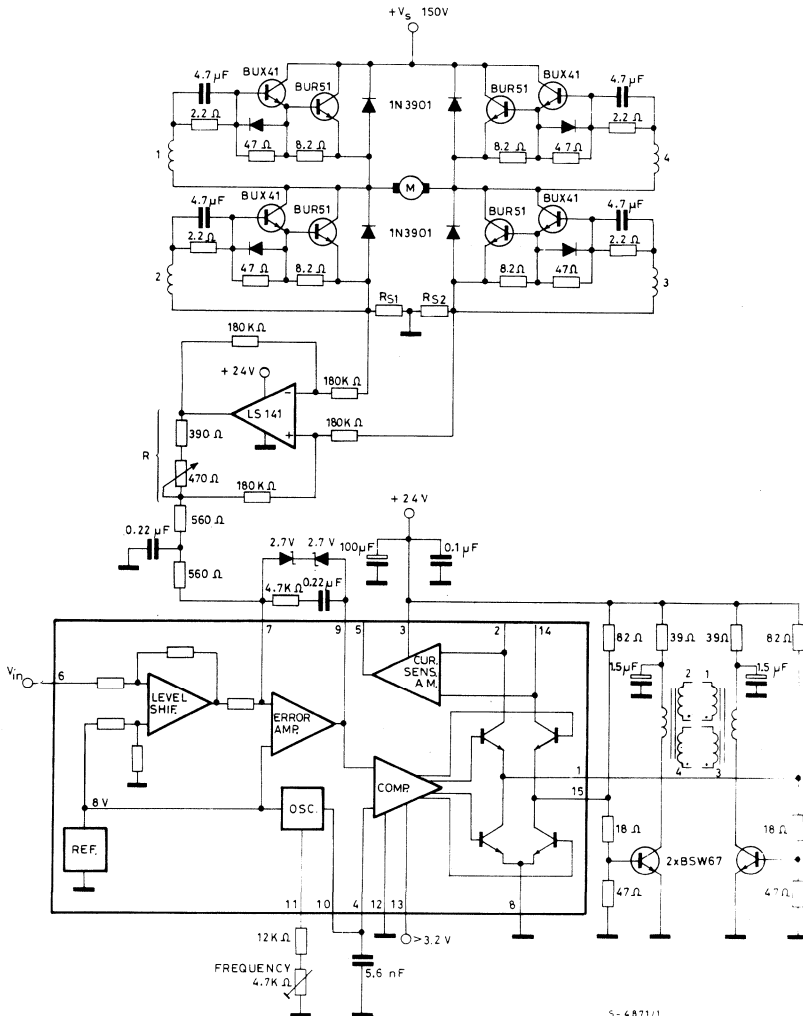
and

$$390 \Omega < R < 860 \Omega$$

This gives a range of transconductance values (I_m/V_{in}) from 3.0 A/V ($R = 390\Omega$) to 8.6 A/V ($R = 860\Omega$).

In this circuit the L292 drives two transformers whose secondaries drive the power transistors. The coil ratio of the transformers is 1:20. To limit the duty cycle at which the transformers operate from 15% to 85%, two zener diodes are inserted between pin 7 and pin 9 of the L292. The LS141 op amp supplies current feedback from the transistor bridge to the L292.

Fig. 16 - For higher voltages and currents-up to 150V at 50A - this circuit can be used. It connects to the L290 and L291, behaving just like and L292.



DESIGN CONSIDERATIONS

The application circuit of figure 12 will have to be adapted in most cases to suit the desired performance, motor characteristics, mechanical system characteristics and encoder characteristics. Essentially this adaptation consists of choosing appropriate values for the ten or so components that determine the characteristics of the L290, L291 and L292.

The calculations include:

- Calculation of maximum speed and acceleration; useful both for defining the control algorithm and setting the maximum speed.
- Calculation of R8 and R9 to set maximum speed.
- Laplace analysis of system to set C8, R11, R12, R13 and R14.
- Laplace analysis of L292 loop to set the sensing resistors and C12, C13, R15, R16, R17.
- Calculation of values for C4 and C6 to set max level of tach signal.
- Calculation of values for R6 and R7 to set D/A reference current.
- Calculation of R20 to set desired switching frequency.

MAXIMUM ACCELERATION

For a permanent magnet DC motor the acceleration torque is related to the motor current by the expression:

$$T_a + T_f = K_T I_m$$

where:

- I_m is the motor current
 K_T is the motor torque constant
 T_a is the acceleration torque
 T_f is the total system friction torque

The acceleration torque is related to angular acceleration and system inertia by:

$$T_a = (J_m + J_{oe} + J_L) a$$

where:

- J_m is the moment of inertia of the motor
 J_{oe} is the moment of inertia of the encoder
 J_L is the moment of inertia of the load
 a is the angular acceleration.

In a system of this type the friction torque T_f is normally very small and can be neglected. Therefore, combining these two expressions we can find the angular acceleration from:

$$a = \frac{K_T}{J_m + J_{oe} + J_L} \cdot I_m$$

It follows that for a given motor type and control loop the acceleration can only be increased by increasing the motor current, I_m .

The characteristics of a typical motor are given in figure 17. From this table we can see that:

$$K_T = 4.3 \text{ N cm/A} \quad (6.07 \text{ oz.in./A})$$

$$J_m = 65 \text{ g} \cdot \text{cm}^2 \quad (0.92 \times 10^{-3} \text{ oz.in.s}^2)$$

We also know that the maximum current supplied by the L292 is 2A and that the moment of inertia of the STRE1601 optical encoder, J_{oe} , is $0.3 \times 10^{-4} \text{ oz.in.s}^2$.

The moment of inertia of the load J_L , is unknown but assume, for example, that $J_{oe} + J_L \cong 2 J_m$. Therefore the maximum angular acceleration is:

$$a = \frac{6.07 \times 2}{2 \times 0.92 \times 10^{-3}} = 6597.8 \text{ rad/s}^2$$

Fig. 17 - The characteristics of a typical DC motor.

Motor - Parameter	Value
$U_{BB} (V_s)$	18V
C. emf. K_E	4.5 mV/min ⁻¹
N_o (without load)	3800 rpm
I_{om} (without load)	190 mA
T_f (friction torque)	0.7 N cm
K_T (motor constant)	4.3 N cm/A
Amature moment of inertia	65 g. cm ²
R_M of the motor	5.4 Ω
L_M of the motor	5.5 mH

MAXIMUM SPEED

The maximum speed can be found from:

$$V_{S \text{ min}} = 2 V_{CEsat} + R_S I_m + K_e \Omega + R_m I_m$$

where:

- $E = K_e \Omega$ is the internally generated voltage (EMF)
 K_e is the motor voltage constant
 Ω is the rotation speed of the motor.

For example, if $V_{S \text{ min}} = 20V$

$$2 V_{CEsat} + R_S I_m = 5V \text{ (from L292 datasheet)}$$

$$R_m I_m = 10.8V \text{ (} R_m = 5.4 \Omega \text{)}$$

we obtain:

$$K_e \Omega (E) = 4.2V$$

and

$$\Omega = \frac{4.2V}{4.5 \text{ mV/min}^{-1}} = 933.3 \text{ rpm} = 97.74 \text{ rad/s}$$

The STRE1601 encoder has 200 tracks so this speed corresponds to:

$$V = \Omega \frac{200}{60} = 3111.1 \text{ tracks/s.}$$

The time taken to reach maximum speed from a standing start can be found from

$$\Delta t = \frac{\Omega}{a} = \frac{97.74 \text{ rad/s}}{6597.8 \text{ rad/s}^2} = 14.8 \text{ ms}$$

We can also express the acceleration in terms of tracks/s²:

$$K = \frac{V}{\Delta t} = \frac{3111.1 \text{ tracks/s}^2}{14.8 \text{ ms}} = 210209.5 \text{ tracks/s}^2$$

Therefore the number of tracks necessary to reach the maximum system speed for our example is:

$$p = \frac{V^2}{2K} = 23 \text{ tracks}$$

This information is particularly useful for the programmer who writes the control software.

SETTING THE MAXIMUM SPEED

The chosen maximum speed is obtained by setting the values of R6, R7, R8, R9, C4 and C6 (all shown on the application circuit, figure 12). This is how it's done:

The first step is to calculate R6 and R7, which define the DAC current reference. From the L291 datasheet we know that I_{ref} , the DA converter current reference, must be in the range 0.3 mA to 1.2 mA.

Choosing an I_{ref} of roughly 0.5 mA, and knowing that V_{ref} (the L290s reference output) is typically 5V, it follows that:

$$R6 + R7 = \frac{V_{ref}}{I_{ref}} = 10 \text{ k}\Omega$$

Therefore we can choose $R6 = R7 = 4.7 \text{ k}\Omega$ (5% tolerance).

Substituting the minimum and maximum values of V_{ref} (from the L290 datasheet) and the resistance variations we can now check that the variation of I_{ref} in the worst cases is acceptable.

$$I_{ref \text{ min}} = \frac{V_{ref \text{ min}}}{(R6 + R7) \text{ max}} = 0.46 \text{ mA}$$

$$I_{ref \text{ typ}} = \frac{V_{ref \text{ (typ)}}}{4.7 \text{ k} + 4.7 \text{ k}} = 0.53 \text{ mA}$$

$$I_{ref \text{ max}} = \frac{V_{ref \text{ max}}}{(R6 + R7) \text{ min}} = 0.62 \text{ mA}$$

These values are within the 0.3 mA to 1.2 mA limits.

Now that the reference current is defined we can calculate values for R8 and R9 which define the tacho current at the summing point.

The full scale output current of pin 12 of the L291 (the D/A converter output) is:

$$I_o = 1.937 I_{ref}$$

which is typically 1.02 mA.

The worst case output current is when I_{ref} is at a maximum (0.62 mA) and the I_{out} error is maximum (+ 2%):

$$I_o = 0.62 \times 1.937 \times 1.02 = 1.22 \text{ mA}$$

This less than the 1.4 mA maximum value for I_{out} specified in the L291 datasheet.

Assuming that the maximum DC voltage at the TACHO output of the L290 (pin 4) is 7V (this is the tacho voltage generated at the maximum system speed), we can find the sum of R8 and R9;

$$R8 + R9 = \frac{V_{tacho \text{ DC}}}{I_o \text{ typ}} = \frac{7}{1.02} = 6.85 \text{ k}\Omega$$

Therefore we choose $R8 = 4.7 \text{ k}\Omega$ and a 5 k Ω trimmer for R9. R9 is used to adjust the maximum speed.

We can now calculate the ripple voltage and maximum tacho voltage:

$$V_{\text{ripple pp}} = \frac{\pi}{4} (\sqrt{2}-1) V_{tacho \text{ DC}} \cong 2.3 V_{pp}$$

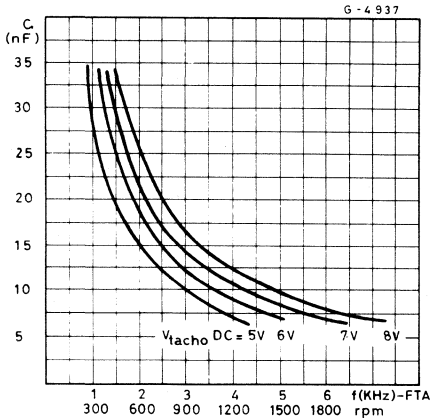
$$V_{tacho \text{ max}} = \frac{\pi}{4} \sqrt{2} V_{tacho \text{ DC}} \cong 7.8 V_p$$

This value is within the voltage swing of the tacho amplifier ($\pm 9V$); that means the choice of $V_{tacho \text{ DC}} = 7V$ is correct.

At this point we know the values of R6, R7, R8 and R9. The maximum speed can now be set by choosing values for C4 and C6 which form the differentiation networks on the L290. These values depend on the number of tracks of the optical encoder. For the STRE1601 encoder the capacitor values can be found from figure 18. These curves show how the capacitor values is related to frequency (encoder rotation speed) for different tacho voltages and maximum speed. The example values are $V_{tacho \text{ DC}} = 7V$ and maximum speed = 3111 tracks/sec therefore the value for C4 and C6 is 15 nF.

The values of R4 and R5 must be 820 Ω to minimize the offsets.

Fig. 18 - C4 and C6 value versus rotation speed for various maximum tacho voltage values.



LAPLACE ANALYSIS OF THE SYSTEM

Suitable values for the components R11, R12, R13, R14 and C8 can be found from a Laplace analysis of the system. Figure 19 shows a simplified block diagram of the system which will be useful for the analysis.

The analysis is based on the angular speed Ω and on the motor position θ . The motor is represented, to a first approximation, by the current I_m and by the acceleration torque, T_a , which drives an inertial load J.

There are two conversion factors, K_{sp} and K_θ . They link the mechanical parameters (position and speed) with the equivalent feedback signals for the two loops. The values of K_{sp} and K_θ are determined by the encoder characteristics and the gain parameters of the integrated circuits. The open-loop and closed-loop gains are fixed by four external resistors:

- R_{ref} — fixes the reference current ($R_6 + R_7$)
- R_{speed} — fixes the speed loop gain ($R_8 + R_9$)
- R_{pos} — controls the position loop gain (R_{12})
- R_{err} — controls the system loop gain (R_{13}).

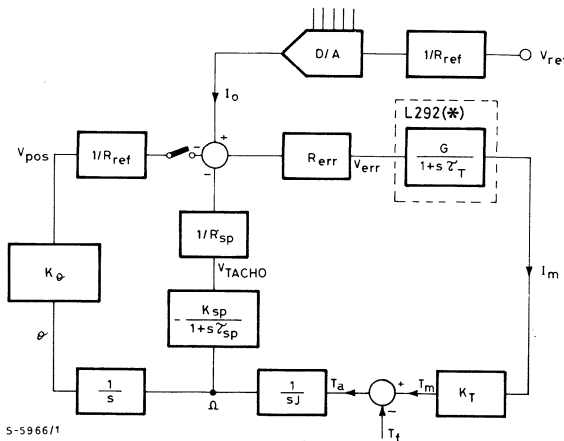
The stability both of the speed loop and of the speed-position loop are defined by external components.

The fundamental characteristics of the speed control system can thus be determined by the designer.

τ_{sp} is the time constant that determines the dominant pole of the speed loop and is determined by C8, R8 and R9

$$\tau_{sp} = C_8 \frac{R_8 R_9}{R_8 + R_9}$$

Fig. 19



(*) See L292 datasheet for an accurate analysis of this block.

List of terms

s : Laplace variable
 K_T : Motor torque constant
 T_a : Acceleration torque
 T_f : Total system friction torque
 J : Total moment of inertia ($J = J_{oe} + J_m + J_L$).
 Ω : Speed

θ : Angular position
 K_{sp} : Conversion factor that links the motor rotation speed and the TACHO signal.
 K_T : Conversion factor that links the motor position and the V_{pos} signal.

SETTING THE L292 COMPONENTS

The sensing resistor and feedback loop component values for the L292 can be calculated easily using the following formulae. A detailed Laplace analysis of this block is given on the L292 datasheet.

a) Sense resistors. $R_s = R18 = R19$

$$\frac{I_m}{V_i} = \frac{R2}{R1} \frac{R4}{R3} \cdot \frac{I}{R_s}$$

$$\Rightarrow R_s = \frac{R2}{I_m} \frac{R4}{R1} \frac{V_i}{R3}$$

(These resistors are all inside the L292).

where:

I_m is the motor current

V_i is the input voltage corresponding to I_m .

For example, $I_m = 2A$, $V_i = 9.1V$, resistor values as in figure 7 (L292 internal block diagram)

$$R_s = \frac{0.044}{I_m} V_i = 0.2 \Omega$$

b) R17, R15, R16, C12, C13

$$G_{mo} = \frac{2 V_s}{R_m V_R}$$

V_s = L292 supply voltage

R_m = motor resistance

V_R = L292 reference voltage

and

$$\xi = \sqrt{\frac{R4 C13}{4 R15 C12 G_{mo} R_s}}$$

$R4$ = L292 internal resistor (400 Ω)

$R_s = R18 = R19$

A good choice for ξ is $1/\sqrt{2}$. Substituting this value, G_{mo} and the values of $R4$ and R_s :

$$\xi^2 = \frac{1}{2} = \frac{400 C13}{4 R15 C12 \times 0.2}$$

$$\Rightarrow \frac{1000 C13}{R15 C12} = 1$$

Also
$$f_T = \frac{0.9}{2 \pi R15 C12}$$

Assuming that f_T is 3 kHz, another recommended value:

$$R15 C12 \cong 47 \times 10^{-6} \text{ s}$$

Therefore we can find C13 :

$$1000 C13 \cong 47 \times 10^{-6}$$

$$\Rightarrow C13 = 47 \text{ nF}$$

Since
$$\frac{L_m}{R_m} = R17 C13$$

$$R17 = \frac{L_m}{C13 R_m}$$

For the example motor $L_m = 5 \text{ mH}$, $R_m = 5.4 \Omega$ therefore:

$$R17 = \frac{L_m}{C13 R_m} = 22 \text{ k}\Omega$$

From $R15 C12 \cong 47 \times 10^{-6} \text{ s}$, choosing a value of $R15$; 510 Ω , we have:

$$C12 = 82 \text{ nF}$$

Also, $R16 = R15 = 510 \Omega$.

DEAD TIME

C17 sets the switching delay of the L292 which protects against simultaneous conduction. The delay is:

$$\tau = R_T C17$$

and R_T is an internal 1.5k resistor. The suggested 1.5 nF value gives a switching delay of about 2.25 μs . This is more than adequate because the transistors have a switch off delay of only 0.5 μs .

SWITCHING FREQUENCY

The switching frequency is set by C17 and R20:

$$f_{osc} = \frac{1}{2 R20 C17}$$

R20 must be at least 8.2 k Ω and is varied to set the frequency: the value of C17 is imposed by dead time requirements. Typically the frequency will be 15-20 kHz.

It should be outside the audio band to reduce noise but not to high or efficiency will be impaired. The maximum recommended value is 30 kHz.

CURRENT RIPPLE

To reduce dissipation in the motor and the peak output current the ripple, ΔI_m , should be less than 10% of the maximum current.

Since
$$\Delta I_m = \frac{V_s}{L_m} \cdot \frac{T}{2}$$

$$\left(\frac{T}{2}\right) = \text{half period of oscillator}$$

and

$$\Delta I_m = 0.1 I_{m \max}$$

$$\Rightarrow 0.1 I_{m \max} = \frac{V_s}{2f L_{M \min}}$$

$$\Rightarrow L_{M \min} = \frac{5 V_s}{f I_{m \max}}$$

Therefore there is a minimum inductance for the motor which may not always be satisfied. If this is the case, a series inductor should be added and the value is found from:

$$L_{\text{series}} = \frac{5 V_s}{f I_{m \max}} - L_M$$

EFFICIENCY AND POWER DISSIPATION

Neglecting the losses due to switching times and the dissipation due to the motor current, the efficiency of the L292's bridge can be found from:

$$\eta = 1 - \frac{\Delta t_1}{\Delta t_1 - \Delta t_2} \cdot \frac{V_{\text{sat}}}{V_s} - \frac{\Delta t_1}{\Delta t_1 - \Delta t_2} \cdot \frac{V_{\text{over}}}{V_s}$$

where:

- $V_{\text{over}} \cong 2V (2 V_{BE} + R_S I_m)$
- $V_{\text{sat}} \cong 4V (2 V_{CE\text{sat}} + 3 V_{BE})$
- $\Delta t_1 =$ transistor conduction period
- $\Delta t_2 =$ diode conduction period.

If $\Delta t_1 \gg \Delta t_2$ and $V_s = 20V$ we obtain:

$$\eta = 1 - \frac{4}{20} = 80\%$$

In practice the efficiency will be slightly lower as a results of dissipation in the signal processing circuit (about 1W at 20V) and the finite switching times (about 1W).

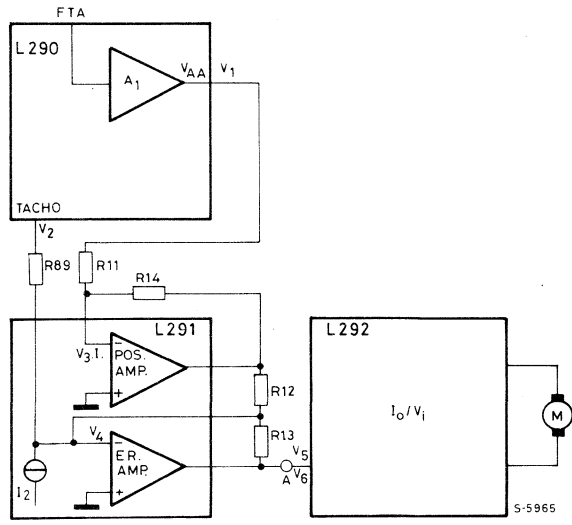
If the power transferred to the motor is 40W, the 80% efficiency implies 10W dissipated in the bridge and a total dissipation of 12W. This gives an actual efficiency of 77%. Since the L292's Multiwatt package can dissipate up to 20W it is possible to handle continuous powers in excess of 60W.

POSITION ACCURACY

The main feature of the system L290, L291, L292 is the accurate positioning of the motor. In this section we will analyse the influence of the offsets of the three ICs on the positioning precision.

When the system is working in position mode, the signal FTA coming from the optical encoder, after suitable amplification, is sent to the summing point of the error amplifier (L291). If there were no offset and no friction, the motor would stop in a position corresponding to the zero crossing of the signal FTA, and then at the exact position required. With a real system the motor stops in a position where FTA has such a value to compensate the offsets and the friction; as a consequence there is a certain imprecision in the positioning. The block diagram, fig. 20, shows the parts of the 3 ICs involved in the offsets. First we will calculate the amount of the offsets at the input of the IC L292 (point A of fig. 20).

Fig. 20



L290

The offset of the TACHO signal, V₂, is the main cause of the imprecision of the positioning. Another offset in L290 is V₁, the output offset voltage of A1. The contribution at point A is:

$$V_{1A} = V_1 \cdot \frac{R_{14}}{R_{11}} \cdot \frac{R_{13}}{R_{12}}$$

$$V_{2A} = V_2 \cdot \frac{R_{13}}{R_{89}}$$

L291

In this IC there are the following offsets:

V₃ = input offset voltage of the position amplifier

I₁ = input bias current of the position amplifier

I₂ = output offset current of the D/A converter plus ER.AMP bias current

V₄ = input offset voltage of the error amplifier.

Their contribution at point A is:

$$V_{3A} = V_3 \cdot (1 + \frac{R_{14}}{R_{11}}) \cdot \frac{R_{13}}{R_{12}}$$

$$V_{I1A} = I_1 \cdot R_{14} \cdot \frac{R_{13}}{R_{12}}$$

$$V_{I2A} = I_2 \cdot R_{13}$$

$$V_{4A} = V_4 (1 + \frac{R_{13}}{R_{12} // R_{89}})$$

L292

Referring to this IC we must consider the input offset voltage V₅. Moreover, we call V₆ the input voltage that must be applied to the L292 to keep the motor in rotation, i.e. to compensate the dynamic friction. V₆ is not an offset voltage, but has the same effects, and for this reason we have to put it together with the offsets.

$$V_{5A} = V_5 \quad \frac{I_o}{V_i} = \text{Transconductance of L292}$$

$$V_{6A} = V_6 = \frac{I_6}{\left[\frac{I_o}{V_i}\right]} \quad I_6 = \text{Motor current necessary to compensate the dynamic friction}$$

The total offset voltage referred to point A is given by the sum of all the precedent terms:

$$V_A = V_{1A} + V_{2A} + V_{3A} + V_{I1A} + V_{I2A} + V_{4A} + V_{5A} + V_{6A}$$

The amplitude of the signal FTA necessary to compensate the offset V_A is:

$$V_{FTA} = V_A \cdot \frac{R_{12}}{R_{13}} \cdot \frac{R_{11}}{R_{14}} \cdot \frac{1}{A_1}$$

Calling V_M the maximum value of the signal FTA, the phase error of the system is:

$$\alpha = \sin^{-1} \frac{V_{FTA}}{V_M}$$

If α_c is the phase between two consecutive characters, (it may be equal 360° or multiple of it) the percentage error in the character positioning is:

$$\epsilon = \frac{\alpha}{\alpha_c} \cdot 100$$

In these calculations we have not considered how the precision of the signal FTA, coming from the optical encoder, influences the positioning error. The percentage value of the pitch accuracy must be added to ε to have the total percentage error in the character positioning. Any DC offset of the mean value of the signal FTA must be multiplied by A₁ and added to V₁ to obtain its effect on the error.

NUMERICAL EXAMPLE

In this numerical example we will calculate the precision of the positioning in the worst case, i.e. with all the offsets at the max value. The values of the external components are taken from the application circuit. (fig. 12).

R₁₁ = 22K R₁₂ = 100K R₁₃ = 120K R₁₄ = 15K
R₈₉ = R₈ + R₉ = 6K

From the data sheets of the three ICs we can find:

V₁ = 55 mV V₂ = 80 mV V₃ = 4.5 mV

V₄ = 2 mV V₅ = 350 mV

I₁ = 0.3 μA I₂ = 0.4 μA

A_{1 min} = 22 dB = 12.6

$$\frac{I_o}{V_i} \text{ min} = 205 \frac{\text{mA}}{\text{V}}$$

$$V_{Mmin} = 0.4V$$

For I₆ we will consider the value I₆ = 50 mA

$$V_{1A} = 55 \cdot 10^{-3} \cdot \frac{15}{22} \cdot \frac{120}{100} = 45 \text{ mV}$$

$$V_{2A} = 80 \cdot 10^{-3} \cdot \frac{120}{6} = 1.6V$$

$$V_{3A} = 4.5 \cdot 10^{-3} (1 + \frac{15}{22}) \cdot \frac{120}{100} = 9.1 \text{ mV}$$

$$V_{I1A} = 0.3 \cdot 10^{-6} \cdot 15 \cdot 10^3 \cdot \frac{120}{100} = 5.4 \text{ mV}$$

$$V_{I2A} = 0.4 \cdot 10^{-6} \cdot 120 \cdot 10^3 = 48 \text{ mV}$$

$$V_{4A} = 2 \cdot 10^{-3} \cdot (1 + \frac{120}{5.6}) = 44.9 \text{ mV}$$

$$V_{5A} = 350 \text{ mV}$$

$$V_{6A} = \frac{50}{205} = 244 \text{ mV}$$

$$V_A = 2.346 \text{ V}$$

$$V_{FTA} = 2.329 \cdot \frac{100}{120} \cdot \frac{22}{15} \cdot \frac{1}{12.6} = 0.228 \text{ V}$$

$$\alpha = \sin^{-1} \frac{0.226}{0.4} \cong 35^\circ$$

If we consider an optical encoder with 200 tracks/turn and a daisy wheel with 100 characters, the phase between two consecutive characters is $\alpha_c = 720^\circ$, and then the maximum percentage error we can have is.

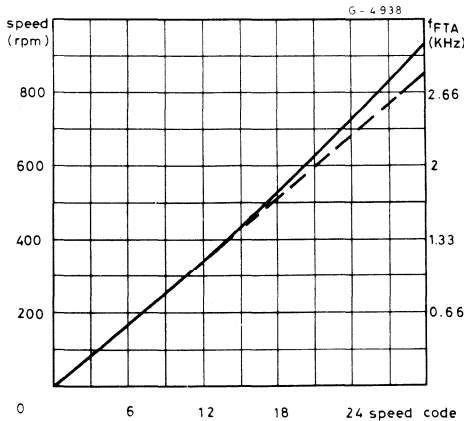
$$\epsilon = \frac{35}{720} \cdot 100 \cong 4.8\%$$

From this numerical example we can see that the main contribution to the positioning error is given by the offset of the TACHO signal (V_{2A}), other big contributions are given by the input offset voltage of L292 (V_{5A}) and by the voltage necessary to compensate the dynamic friction of the motor (V_{6A}). This last term is only determined by the motor and can also have greater values.

The error we have calculated is the maximum possible and it happens when all the offsets have the max value with the same sign, i.e. with a probability given by the product of the single probabilities. Considering as an example every offset has a probability of 1% to assume the max value, the probability the error assumes the max value is:

$$P = (10^{-2})^7 = 10^{-14}$$

Fig. 21

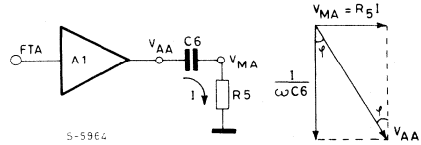


SPEED ACCURACY

If we consider the complete system with L290-L291-L292 driving a DC MOTOR with optical

encoder, we can note the speed of the motor is not a linear function of the speed digital code applied to L291. The diagram of fig. 21 shows this function and it is evident that the speed increases more than a linear function, i.e. if the speed code doubles, the speed of the motor becomes more than the double. The cause of this non linearity is the differentiator network R4 C4 and R5 C6 (see fig. 22) that has not an ideal behaviour at every frequency.

Fig. 22



$$1) V_{MA} = V_{AA} \sin \varphi$$

$$\varphi = \tan^{-1} \omega R5 C6 \quad \omega = 2 \pi f$$

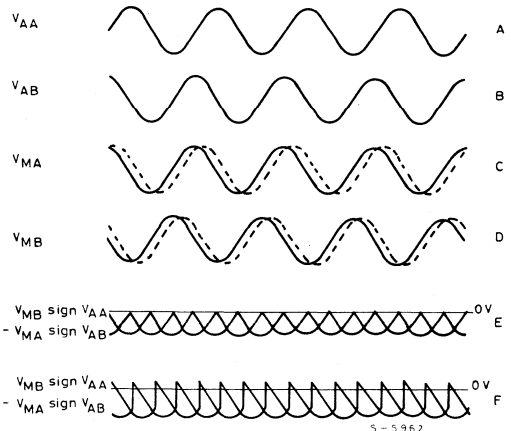
$$2) V_{MA} = V_{AA} \sin \tan^{-1} \omega R5 C6$$

$$f = \text{frequency of the signal FTA}$$

This last relation gives the amplitude of the signal V_{MA} ; it is evident there is not a linear function between V_{MA} and ω , like $V_{MA} = K\omega$ and the difference is greater if the product $\omega R5 C6$ doesn't respect the disequation $\omega R5 C6 \ll 1$, i.e. at high frequencies.

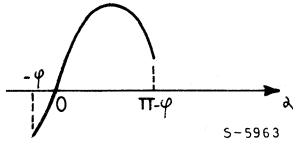
The phase angle between V_{MA} and V_{AA} should be 90° and then $\varphi = 0$, in our case φ increases with the frequency according to the equation $\varphi = \tan^{-1} \omega R5 C6$, and influences the amplitude of the output signal TACHO. In fig. 23 are shown the waveforms that contribute to generate the TACHO signal. A and B are the signals V_{AA} and V_{AB} in phase with the input signals FTA and FTB. C and

Fig. 23



D are the signals V_{MA} and V_{MB} : the continue line indicate the ideal case, in fact the phase between V_{MA} and V_{AA} is 90° ; the dotted line is referred to the real case in which the phase is lower than 90° . By adding the two signals shown in E we obtain the TACHO signal, whose expression is:

Fig. 24



$$V_{TACHO} = V_{MB} \cdot \text{sign } V_{AA} - V_{MA} \cdot \text{sign } V_{AB}$$

The signals in E are referred to the ideal case, the ones in F to the real case. It is possible to demonstrate the mean value of the TACHO signal in the real case is lower than the one we could have with an ideal differentiator network and this explains why in fig. 21 the speed of the motor increases more than a linear function. The mean value of the waveforms F is (fig. 24).

$$3) V_m = \int_{-\varphi}^{\pi-\varphi} K1 \sin \alpha d\alpha = \frac{2 K1}{\pi} \cos \varphi$$

Since the waveforms E are half sinewaves, the mean value is

$$4) V'_m = \frac{2 K1}{\pi}$$

We can conclude that two causes contribute to give a TACHO signal lower than the theoretical one, both due to the differentiator network:

- a) the amplitude of the signal V_{MA} is lower than $V_{MA} = K\omega$ and we can call ϵ_1 the relative percentage error.

$$\epsilon_1 = \frac{\sin \text{tg}^{-1} \omega R5 C6 - \omega R5 C6}{\omega R5 C6} \cdot 100$$

- b) the mean value of the signals $V_{MA} \cdot \text{sign } V_{AB}$ and $V_{MB} \cdot \text{sign } V_{AA}$ is lower than the theoretical one because there is a shift in the phase of the signals V_{MA} and V_{MB} . The relative percentage error only due to the shift of the phase is

$$\epsilon_2 = (\cos \varphi - 1) \cdot 100 \quad \varphi = \text{tg}^{-1} \omega R5 C6$$

The total percentage decrease of the TACHO signal is given with a good approximation by the sum of ϵ_1 and ϵ_2 .

Example:

Consider:

$f = 3000 \text{ Hz}$ corresponding to

$$n = \frac{3000}{200} \cdot 60 = 900 \text{ rpm of the motor if 200 are the tracks/turn of the encoder}$$

$$\epsilon_1 \cong -2.6\% \text{ with } R5 = 820 \Omega \\ C6 = 15 \text{ nF}$$

$$\epsilon_2 \cong -2.6\%$$

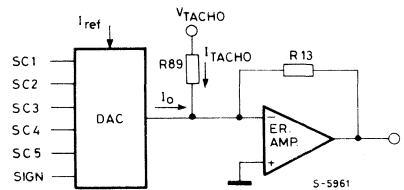
$$\epsilon_3 \cong \epsilon_1 + \epsilon_2 \cong -5.2\%$$

From the diagram of fig. 21 we note that at a speed of 900 rpm corresponds a theoretical speed of 855 rpm with a percentage difference of about 5.2%.

SPEED ACCURACY DUE TO THE D/A CONVERTER

To analyse the influence of the DAC precision on the speed accuracy we will refer to the following (fig. 25).

Fig. 25



The value of the output current of the DAC I_O depends on I_{ref} and on the digital code defined by the inputs SC1-SC5, while its direction depends on the value of the SIGN input, the max theoretical value of I_O , obtained with SC1-SC5 low, is:

$$I_{OM} = \pm \frac{31}{16} I_{ref}$$

The motor will run at a speed corresponding to the following value of the TACHO signal:

$$V_{TACHO} = -I_{OM} \cdot R89 = \pm \frac{31}{16} I_{ref} \cdot R89$$

This last relation is true if we don't consider the motor friction and the offsets. Consider now the possible spreads we can have in the motor speed due to the DAC. If we call I_{OM1} the value of the max output current I_O corresponding to the SIGN LOW and I_{OM2} the one corresponding to the SIGN HIGH, the percentage error we have in the max speed from the positive to the negative value is:

$$\epsilon_4 = \frac{I_{OM1} + I_{OM2}}{I_{OM}} \cdot 100$$

Note that we have consider the sum of I_{OM1} and I_{OM2} because they have opposite signs. This kind of error is principally due to a different gain of the DAC between the two conditions of the SIGN LOW and HIGH. An equal difference of I_{OM1} and I_{OM2} , from I_{OM} ($|I_{OM1}| - |I_{OM2}| = |I_{OM2}| - |I_{OM1}|$) doesn't constitute a speed error because this shift from the theoretical value can be compensated by adjusting the resistor R89 that is formed by a fixed resistor in series with a potentiometer.

With the guaranteed values on the L291 data sheet we can calculate for €4 the max value:

$$\epsilon 4 = \frac{21 \mu A}{1.4 \text{ mA}} \cdot 100 = 1.5\%$$

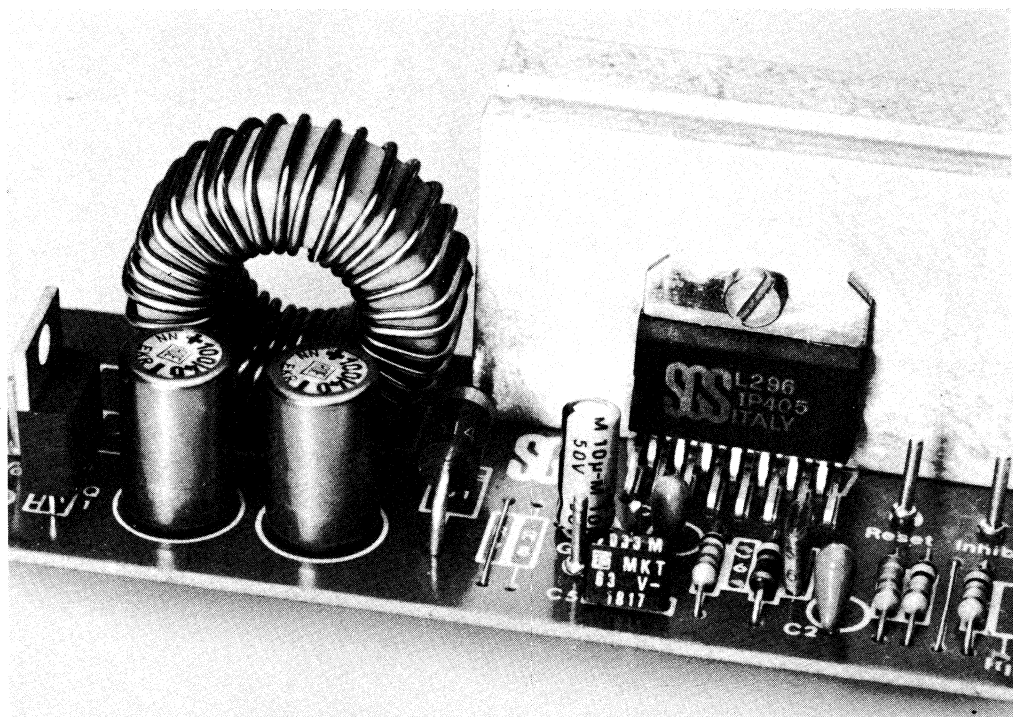
Another characteristic of a D/AC is the linearity, that in our case is better than $\pm 1/2$ LSB. This value is sufficient to guarantee the monotonicity of I_O , and then of the speed of the motor, as a function of the input digital code. The precision of $\pm 1/2$ LSB implies a spread of the speed at every configuration of the input code of $\pm 1.61\%$ referred to the maximum speed. The max percentage error we can have is then greater at low level speed ($\pm 50\%$ at min speed) and has its minimum value at the maximum speed (1.61%).

ACCURACY DUE TO THE ENCODER

The amplitude of the signals FTA and FTB determines the value of the TACHO signal. This amplitude must be constant on the whole range of the frequency, otherwise it is not possible to have a linear function between the TACHO signal and the frequency. The spread of the amplitudes of the two signals FTA and FTB between several encoder can be compensated by adjusting the potentiometer R9 (see fig. 12). The phase between the two signals should be 90° . If there is a constant difference from this value, a constant factor reduction of the TACHO signal results that can be compensated with the potentiometer R9. If the difference from 90° is random, also the reduction of the TACHO signal is random in the same way, and by means of R9 it is possible to compensate only the mean value of that reduction.

DESIGNING WITH THE L296 MONOLITHIC POWER SWITCHING REGULATOR

A cost-effective replacement for costly hybrids, the SGS L296 Power Switching Regulator delivers 4A at an output voltage of 5.1V to 40V and includes many popular supply features. This comprehensive application guide explains how the device operates and how it is used. Typical application circuits are also presented.



The SGS L296 is the first monolithic switching regulator in plastic package which includes the power section. Moreover, the circuit includes all the functions which make it specially suited for microprocessor supply.

Before the introduction of L296, which realizes the step down configuration, this function was implemented with discrete power components driven by integrated PWM regulator circuits (giving a maximum output current of 300 to 400 mA) or with hybrid circuits. Both of these solutions are characterized by a low efficiency of the power transistor. For this reason it is generally necessary to operate at frequencies in the 20kHz to 40 kHz range. Of the two alternatives discrete solutions are usually less expensive because they do not include as many functions as the L296.

With the new L296 regulator the driving problem of the power control stage has been eliminated. Besides a higher overall efficiency, it is therefore also possible to operate directly at frequencies as high as 100 kHz. At 200 kHz the device still operates (further reducing the cost of the L and C external components) when a reduction of a few percent in efficiency is acceptable.

The device delivers a maximum current of 4A to the load, at an output voltage adjustable from 5.1 to 40V; the maximum operating input voltage is 46V. The high voltage and the high current capabilities of the device are a result of the special technology used and the special care taken in designing the power transistor. Essential requirements for a good power transistor are high gain and high current levels, low saturation voltage and good second breakdown robustness. To achieve high gain at high current levels, the power transistor has to be designed to maximize the emitter's perimeter/area ratio.

In the L296 power transistor, realized with a high voltage (50V) process, current densities in the magnitude order of 10 mA/Mi² are achieved.

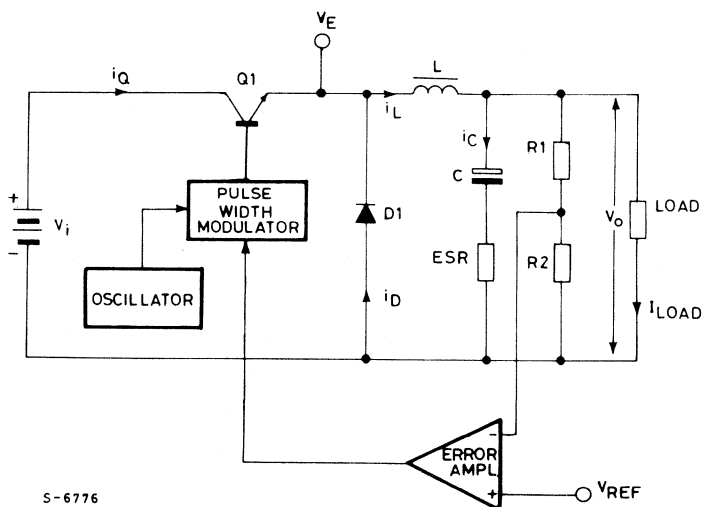
In its most complete configuration, in which all the available functions are being used, a significant reduction of the external component count is achieved compared with discrete component solution.

The L296 is mounted in a MULTIWATT® plastic package with 15 pins, minimizing the cost per watt and allowing a low thermal resistance of 3°C/W between junction and package and of 35°C/W between junction and ambient. This thermal resistance (including the contact resistance) is comparable to that of the more costly metal TO-3 packages.

THE STEP-DOWN CONFIGURATION

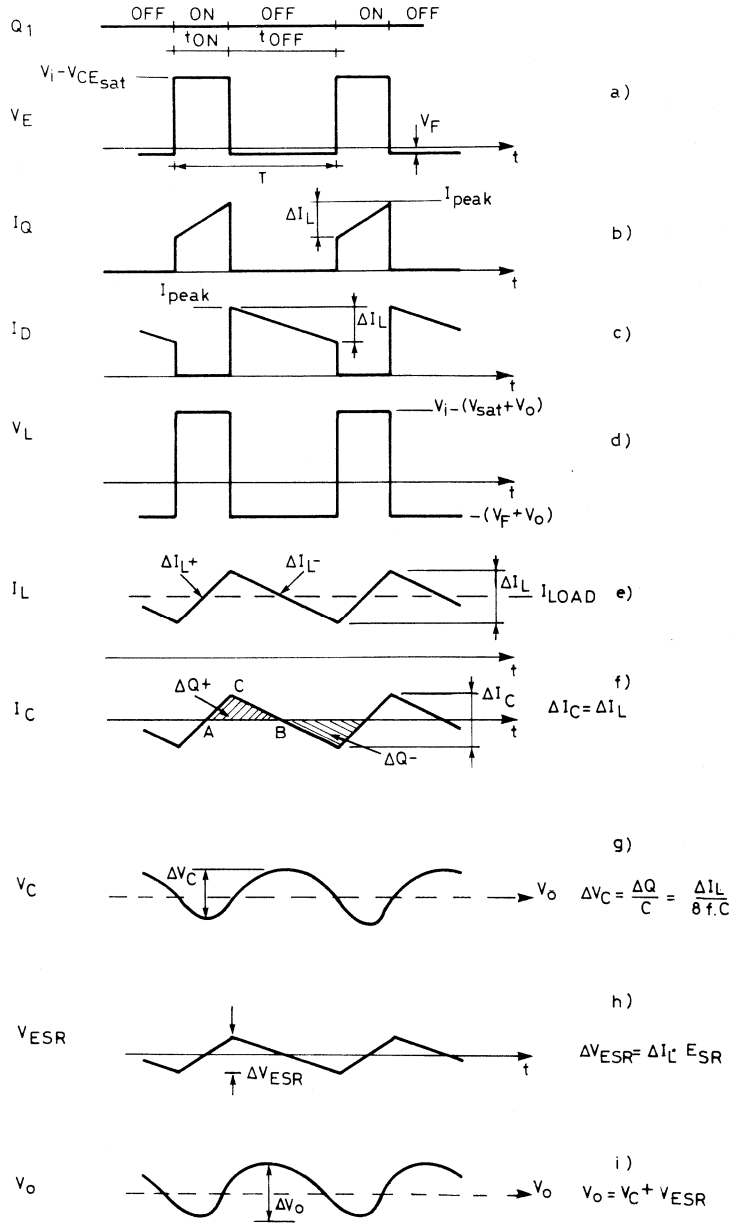
Fig. 1 shows the simplified block diagram of the circuit realizing the step-down configuration. This circuit operates as follows: Q1 acts as a switch at the frequency f and the ON and OFF times are suitably controlled by the pulse width modulator circuit. When Q1 is saturated, energy is absorbed from the input which is transferred to the output through L. The emitter voltage of Q1, V_E , is $V_i - V_{sat}$ when Q is ON and $-V_F$ (with V_F the forward voltage across the D diode as indicated) when Q1 is OFF. During this second phase the current circulates again through L and D. Consequently a rectangular-shaped voltage appears on the emitter of Q1 and this is then filtered by the L-C-D network and converted into a continuous mean value across the capacitor C and therefore across the load. The current through L consists of a continuous component, I_{LOAD} , and a triangular-shaped component superimposed on it, ΔI_L , due to the voltage across L.

Fig. 1 — The basic step-down switching regulator configuration.



S-6776

Fig. 2 – Principal circuit waveforms of the fig. 1 circuit.



S-6788

Fig. 2 shows the behaviour of the most significant waveforms, in different points of the circuit, which help to understand better the operation of the power section of the switching regulator. For the sake of simplicity, the series resistance of the coil has been neglected. Fig. 2a shows the behaviour of the emitter voltage (which is practically the voltage across the recirculation diode), where the power saturation and the forward V_F drop across the diode are taken into account.

The ON and OFF times are established by the following expression:

$$V_O = (V_i - V_{sat}) \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

Fig. 2b shows the current across the switching transistor. The current shape is trapezoidal and the operation is in continuous mode. At this stage, the phenomena due to the catch diode, that we consider as dynamically ideal, are neglected. Fig. 2c shows the current circulating in the recirculation diode. The sum of the currents circulating in the power and in the diode is the current circulating in the coil as shown in fig. 2e. In balanced conditions the ΔI_L^+ current increase occurring during T_{ON} has to be equal to the ΔI_L^- decrease occurring during T_{OFF} . The mean value of I_L corresponds to the charge current.

The current ripple is given by the following formula:

$$\begin{aligned} \Delta I_L^+ &= \Delta I_L^- = \frac{(V_i - V_{sat}) - V_O}{L} T_{ON} = \\ &= \frac{V_O + V_F}{L} T_{OFF} \end{aligned}$$

It is a good rule to respect to $I_{O_{MIN}} \geq I_L/2$ relationship, that implies good operation in continuous mode. When this is not done, the regulator starts operating in discontinuous mode. This operation is still safe but variations of the switching frequency may occur and the output regulation decreases.

Fig. 2d shows the behaviour of the voltage across coil L . In balanced conditions, the mean value of the voltage across the coil is zero. Fig. 2f shows the current flowing through the capacitor, which is the difference between I_L and I_{LOAD} .

In balanced conditions, the mean current is equal to zero, and $\Delta I_C = \Delta I_L$. The current I_C through the capacitor gives rise to the voltage ripple.

This ripple consists of two components: a capacitive component, ΔV_C , and a resistive component, ΔV_{ESR} , due to the ESR equivalent series resistance of the capacitor. Fig. 2g shows the capacitive component ΔV_C of the voltage ripple, which is the integral of a triangular-shaped current as a function of time. Moreover, it should be observed that $v_C(t)$ is in quadrature with $i_C(t)$ and therefore with the voltage V_{ESR} . The quantity of charge ΔQ^+ supplied to the capacitor is given by the area enclosed by the ABC triangle in fig. 2f:

$$\Delta Q = \frac{1}{2} \cdot \frac{T}{2} \cdot \frac{\Delta I_L}{2}$$

which therefore gives:

$$\Delta V_C = \frac{Q}{C} = \frac{\Delta I_L}{8fc}$$

Fig. 2h shows the voltage ripple V_{ESR} due to the resistive component of the capacitor. This component is $v_{ESR}(t) = i_C(t) \cdot ESR$. Fig. 2i shows the overall ripple V_O , which is the sum of the two previous components. As the frequency increases ($> 20 \text{ kHz}$), which is required to reduce both the cost and the sizes of L and C , the V_{ESR} component becomes dominant. Often it is necessary to use capacitors with greater capacitance (or more capacitors connected in parallel) to limit the value of ESR within the required level.

We will now examine the stepdown configuration in more detail, referring to fig. 1 and taking the behaviour shown in fig. 2 into account.

Starting from the initial conditions, where $Q = ON$, $v_C = V_O$ and $i_L = i_D = 0$, using Kirckoff second principle we may write the following expression:

$$V_i = v_L + v_C \quad (V_{sat} \text{ is neglected against } V_i).$$

$$V_i = L \frac{di_L}{dt} + v_C = L \frac{di_L}{dt} + V_O \quad (1)$$

which gives:

$$\frac{di_L}{dt} = \frac{(V_i - V_O)}{L} \quad (2)$$

The current through the inductance is given by:

$$i_L = \frac{(V_i - V_O)}{L} t \quad (3)$$

When V_i , V_O , and L are constant, i_L varies linearly with t . Therefore, it follows that:

$$\Delta I_L^+ = \frac{(V_i - V_O) T_{ON}}{L} \quad (4)$$

When Q is OFF the current through the coil has reached its maximum value, I_{peak} and because it cannot vary instantaneously, the voltage across the coil is inverted and the diode D becomes forward biased to allow the recirculation of the current through the load.

When Q switches OFF, the following situation is present:

$$v_C(t) = V_O, \quad i_L(t) = i_D(t) = I_{peak}$$

And the equation associated to the following loop may be written:

$$V_F + L \frac{di_L}{dt} + v_C = 0 \quad (5)$$

where:

$$V_C = V_O$$

$$\frac{di_L}{dt} = -(V_F + V_O)/L$$

It follows therefore that:

$$i_L(t) = -\frac{V_F + V_O}{L} t \quad (7)$$

The negative sign may be interpreted with the fact that the current is now decreasing. Assuming that V_F may be neglected against V_O , during the OFF time the following behaviour occurs:

$$i_L = \frac{V_O}{L} t \quad (8)$$

therefore:

$$\Delta i_L^- = \frac{V_O}{L} T_{OFF} \quad (9)$$

But, because

$$\Delta i_L^+ = \Delta i_L^- \quad \text{it follows that :}$$

$$\frac{(V_i - V_O) T_{ON}}{L} = \frac{V_O T_{OFF}}{L}$$

which allows us to calculate V_O :

$$V_O = V_i \frac{T_{ON}}{T_{ON} + T_{OFF}} = V_i \frac{T_{ON}}{T} \quad (10)$$

where T is the switching period.

Expression (10) links the output voltage V_O to the input voltage V_i and to the duty cycle. The relationship between the currents is the following:

$$i_{DC} = i_{O_{DC}} \cdot \frac{T_{ON}}{T}$$

EFFICIENCY

The system efficiency is expressed by the following formula:

$$\eta\% = \frac{P_O}{P_i} 100$$

$$\text{where } P_O = V_O I_O \quad (\text{with } I_O = I_{LOAD})$$

is the output power to the load and P_i is the input

power absorbed by the system. P_i is given by P_O , plus all the other system losses. The expression of the efficiency becomes therefore the following :

$$(6) \quad \eta = \frac{P_O}{P_O + P_{sat} + P_D + P_L + P_q + p_{sw}} \quad (12)$$

DC LOSSES

P_{sat} : saturation losses of the power transistor Q.
These losses increase as V_i decreases.

$$P_{sat} = V_{sat} \cdot I_O \frac{T_{ON}}{T} = V_{sat} I_O \frac{V_O}{V_i} \quad (13)$$

where $\frac{T_{ON}}{T} = \frac{V_O}{V_i}$ and V_{sat} is the power transistor saturation at current I_O .

P_D : losses due to the recirculation diode. These losses increase as V_i increases, as in this case the ON time of the diode is greater.

$$P_D = V_F I_O \frac{V_i - V_O}{V_i} = V_F I_O (1 - \frac{V_O}{V_i}) \quad (14)$$

where V_F is the forward voltage of the recirculation diode at current I_O .

P_L : losses due to the series resistance R_S of the coil

$$P_L = R_S I_O^2 \quad (15)$$

P_q : losses due to the stand-by current and to the power driving current:

$$P_q = V_i I'_{3q} + V_i I''_{3q} \frac{T_{ON}}{T} \quad (16)$$

where being:

$$\frac{T_{ON}}{T} = \frac{V_O}{V_i} \quad \text{it follows that :}$$

$$P_q = V_i I'_{3q} + V_O I''_{3q} \quad \text{in which :}$$

$$I'_{3q} = I_{3q} \quad \text{at 0\% duty cycle}$$

$$I''_{3q} = I_{3q}(100\% \text{ d.c.}) - I_{3q}(0\% \text{ d.c.})$$

SWITCHING LOSSES

p_{sw} : switching losses of the power transistor:

$$p_{sw} = V_i I_O \frac{t_r + t_f}{2T}$$

The switching losses of the recirculation diode are

neglected (which are anyway negligible) as it is assumed that diode is used with recovery time much smaller than the rise time of the power transistor.

We can neglect losses in the coil (it is assumed that ΔI_L is very small compared to I_o) and in the output capacitor, which is assumed to show a low ESR.

Calculation of the inductance value, L

Calculating T_{ON} and T_{OFF} through (4) and (9) respectively it follows that:

$$T_{ON} = \frac{\Delta I_L^+ \cdot L}{V_i - V_o} \quad T_{OFF} = \frac{\Delta I_L^- \cdot L}{V_o}$$

But because:

$$T_{ON} + T_{OFF} = T \quad \text{and} \quad \Delta I_L^+ = \Delta I_L^- = \Delta I_L,$$

it follows that:

$$\frac{\Delta I_L \cdot L}{V_i - V_o} + \frac{\Delta I_L \cdot L}{V_o} = T$$

Calculating L, the previous relation becomes:

$$L = \frac{(V_i - V_o) V_o}{V_i \Delta I_L} T \quad (18)$$

Fixing the current ripple in the coil required by the design (for instance 30% of I_o), and introducing the frequency instead of the period, it follows that:

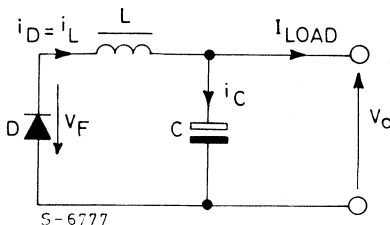
$$L = \frac{(V_i - V_o) V_o}{V_i \cdot 0.3 \cdot I_o \cdot f} \quad \text{where L is in Henry and f in Hz}$$

Calculation of the output capacitor C

From the output node in fig. 3 it may be seen that the current through the output capacitor is given by:

$$i_c(t) = i_L(t) - I_o$$

Fig. 3 – Equivalent circuit showing recirculation when Q_1 is turned off.



From the behaviour shown in fig. 2 it may be calculated that the charge current of the output capacitor, within a period, is $\Delta I_L/4$, which is supplied for a time $T/2$. It follows therefore that:

$$\Delta V_C = \frac{\Delta I_L}{4C} \frac{T}{2} = \frac{\Delta I_L T}{8C} = \frac{\Delta I_L}{8fC} \quad (19)$$

but, remembering expression (4):

$$\Delta I_L^+ = \frac{(V_i - V_o) T_{ON}}{L} \quad \text{and} \quad T_{ON} = \frac{V_o}{V_i} T$$

therefore equation (19) becomes:

$$\Delta V_C = \frac{(V_i - V_o) V_o}{8 V_i f^2 L C}$$

Finally, calculating C it follows that:

$$C = \frac{(V_i - V_o) V_o}{8 V_i \Delta V_C f^2 L} \quad (20)$$

where: L is in Henrys
C is in Farads
f is in Hz

Finally, the following expression should be true:

$$ESR_{max} = \frac{\Delta V_{Cmax}}{\Delta I_L} \quad (21)$$

It may happen that to satisfy relation (21) a capacitance value much greater than the value calculated through (20) must be used.

TRANSIENT RESPONSE

Sudden variations of the load current give rise to overvoltages and undervoltages on the output voltage. Since $i_c = C(dv_c/dt)$ (22), where $dv_c = \Delta V_o$, the instantaneous variation of the load current ΔI_o is supplied during the transient by the output capacitor. During the transient, also current through the coil tends to change its value.

Moreover, the following is true:

$$v_L = L \frac{di_L}{dt} \quad (23) \quad \text{where} \quad di_L = \Delta I_o.$$

$$v_L = V_i - V_o \quad \text{for a load increase}$$

$$v_L = V_o \quad \text{for a load decrease}$$

Calculating dt from (22) and (23) and equalizing, it follows that:

$$L \frac{di_L}{v_L} = C \frac{dv_c}{i_c}$$

$$\Delta V_o = \frac{L \Delta I_o^2}{C(V_i - V_o)} \quad (24) \quad \text{for } +\Delta I_o$$

$$\Delta V_o = \frac{L \Delta I_o^2}{C V_o} \quad (25) \quad \text{for } -\Delta I_o$$

DEVICE DESCRIPTION

Fig. 4 shows the package in which the device is mounted and the pin function assignments. The internal structure of the device is shown in fig. 5. Each block will now be examined.

The device is provided with an internal stabilized power supply that, besides supplying the reference voltage of 5.1V for the whole system, also supplied the internal analog blocks. Special features of the voltage reference are its accuracy, temperature stability and high line rejection. Through zener-zap trimming, the voltage is within $\pm 2\%$ limits.

Fig. 4 – Pin assignments of the L296.

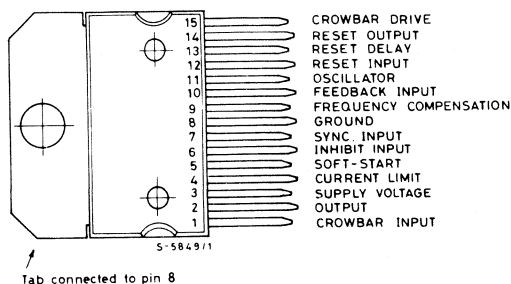
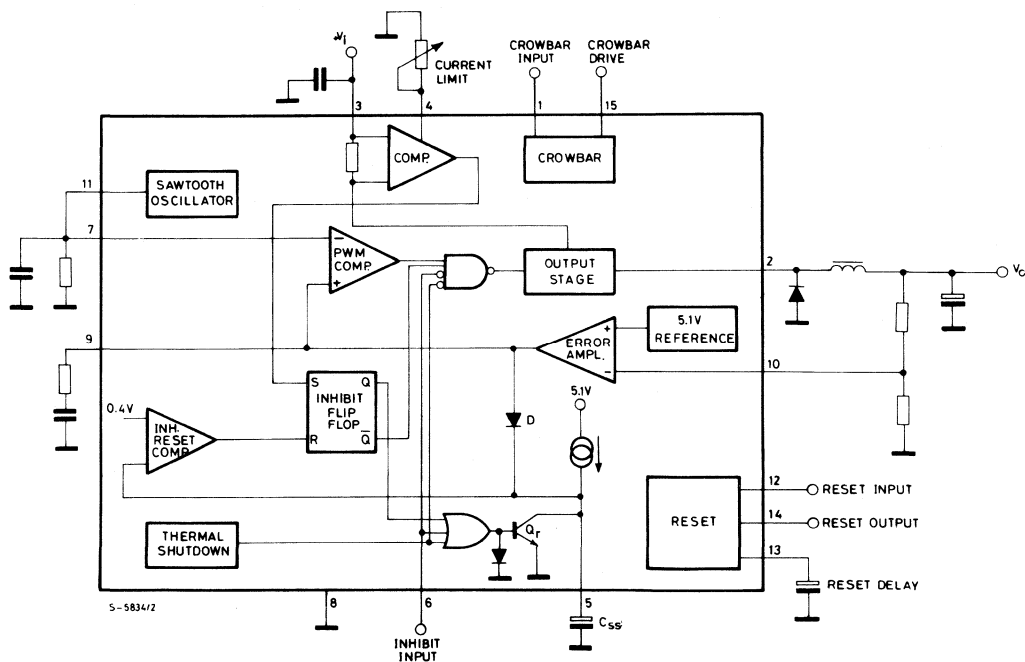


Fig. 5 – Block diagram of the L296. In addition to the basic regulation loop the device includes functions such as reset, crowbar and current limiting.



OSCILLATOR

The oscillator block generates the saw-tooth waveform that sets the switching frequency of the system. This signal, compared with the output voltage of the error amplifier, generates the PWM signal to be sent to the power output stage. The saw-tooth, whose amplitude is between 1.2V and 3.2V, is generated by charging rapidly the C_{osc} capacitor which then discharges across the R_{osc} resistance. As shown in fig. 6, the oscillator is realized by a comparator (with grounded compatible input) with hysteresis whose thresholds are 1.2V and 3.2V respectively. The C_{osc} capacitor and the R_{osc} resistance are connected to the non-inverting input of the comparator which set the oscillating frequency is fixed. When the voltage on pin 11 is less than 3.2V, the switch S_1 is closed and the current generator charges the C_{osc} capacitor rapidly; in this phase S_2 is also closed. As soon as 3.2V is reached the comparator output drives S_2 open (therefore opening S_1 , too); the inverting input voltage is reduced to about 1.2V and the capacitor starts to discharge itself across the R_{osc} resistor (the I_{bias} effect is neglected). When the voltage reaches 1.2V, S_2 and S_1 close again and a new cycle starts. The generated waveform is shown in fig. 7.

To achieve a good accuracy of the switching frequency it is essential to have a charging time of the capacitor which is much smaller than the discharging time. In this way, the oscillation frequency only depends on the external components C_{osc} and R_{osc} . For this reason the capacitor charging current (when S_1 is ON) is typically around 10 mA. For example, with a 2.2 nF capacitor to switch from 1.2V to 3.2V about 400 ns is required, which is negligible compared to the 10 μ s period that occurs when the operation is performed at 100 kHz. The diagrams shown in fig. 8 allow the calculation of the R_{osc} value (R_1 in fig. 8) with C_{osc} as a parameter (C_3 in fig. 8) when the oscillation frequency required for operation has been previously fixed.

Fig. 6 – Internal schematic of the oscillator

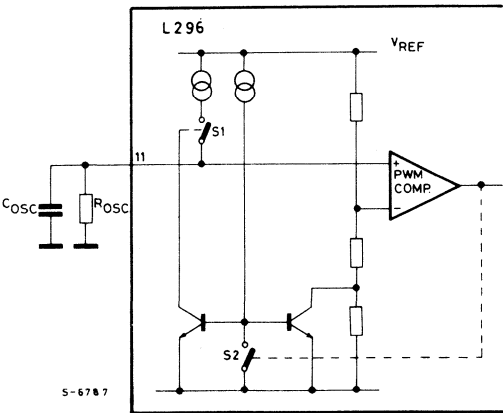


Fig. 7a – Oscillator waveform at pin 11 with $f = 100$ KHz ($R_{osc} = 4.3$ K Ω , $C_{osc} = 2.2$ nF)

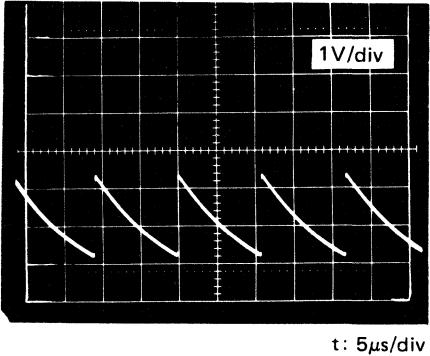


Fig. 7b – Oscillator waveform at pin 11 with $f = 50$ KHz ($R_{osc} = 9.1$ K Ω , $C_{osc} = 2.2$ nF)

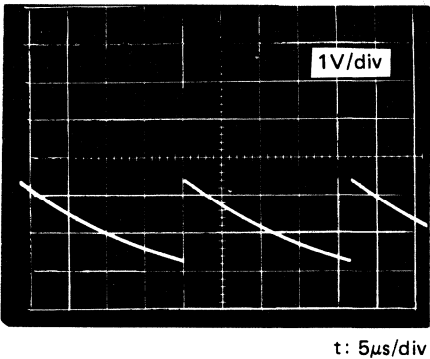


Fig. 8 - Nomogram for the choice of oscillator components.

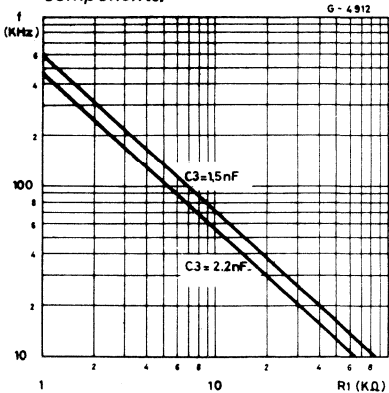


Fig. 8 shows two suggested values for the C_{osc} capacitance. Excessively low capacitance value may give rise to an inaccuracy of the upper threshold

due to the switching delays of the comparator. This inaccuracy is caused by an excessively short rise time of the voltage. A capacitance value too high gives rise to a charging time which is too long compared to the discharging time. An additional inaccuracy cause would be therefore present for the switching frequency, now due to spread of the charge current.

The oscillation frequency is given by the following formula:

$$f_{osc} = \frac{1}{R_{osc} C_{osc}} \quad (26)$$

PWM (see fig. 9)

The PWM signal is generated on the comparator output; the triangular-shaped waveform and the continuous signal coming from the output of the transconductance error amplifier are sent to its inputs. The PWM signal is then transferred to the driving stage of the output power transistor.

SOFT START (see fig. 9)

Soft start is an essential function for correct start-up, to prevent stresses and possible breakdown from occurring in the power transistor and to obtain a monotonically increasing output voltage. In particular, the L296, as it does not have any duty cycle limitation and due to the type of current limitation does not allow the output to be forced to a

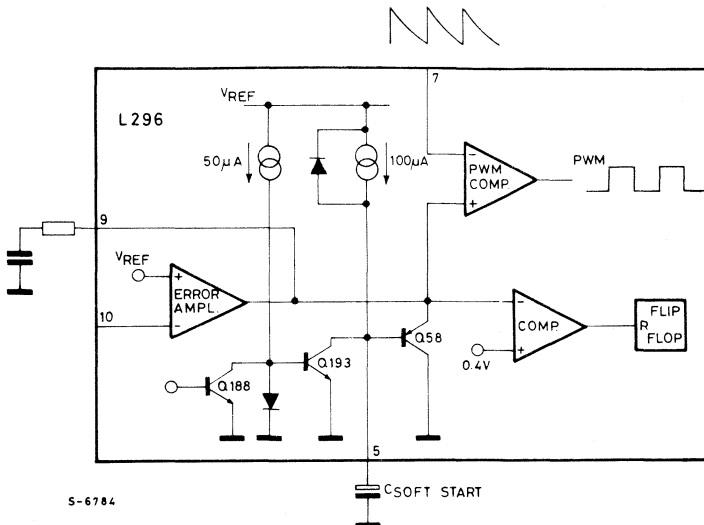
steady state without the aid of the soft-start facility. Soft-start operates at the start-up of the system, after the inhibit has been activated, after an intervention of the current limitation and after the intervention of the thermal protection.

The soft-start function is realized through a capacitor connected to pin 5 which is charged at constant current ($\cong 100\mu A$) up to a value of about V_{REF} . During the charging time, through PNP transistor Q58, the voltage on pin 9 is forced to increase with the same rising speed as on pin 5. Starting from the discharged capacitor condition (pin 5 voltage = 0V) the power transistor is in the OFF condition, as the voltage on pin 9 is smaller than the minimum level of the ramp voltage. As the capacitor is charged, the PWM signal begins to be generated as soon as the error amplifier output voltage crosses the ramp; the power stage starts to switch with steadily increasing duty cycle. This behaviour is shown in fig. 10. As soon as the steady condition is reached the duty cycle sets itself to the right value due to the effect of the feedback network while the soft-start capacitor completes its charging to a value very close to V_{REF} .

The soft-start effect is determined, apart from the switch-on time, when the current limitation operates, due to either an overload or a short circuit, to keep the mean value of the current absorbed by the power supply low.

Moreover from fig. 11 it may be observed that since the voltage on pin 9 can decrease under the minimum ramp level and increase over the maximum level no limitations have been provided on the duty cycle, which therefore may vary between 0 and 100%.

Fig. 9 – Partial internal schematic showing PWM and soft start blocks.



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Fig. 10 — Soft start waveforms. When power is applied, or after an inhibit, the L296's output current rises slowly under control of the soft start circuit.

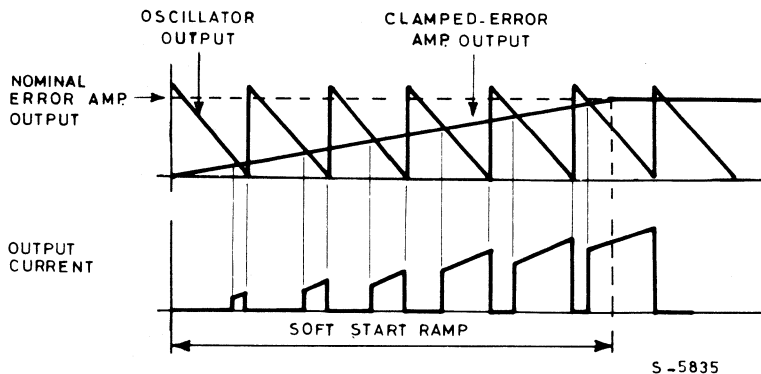
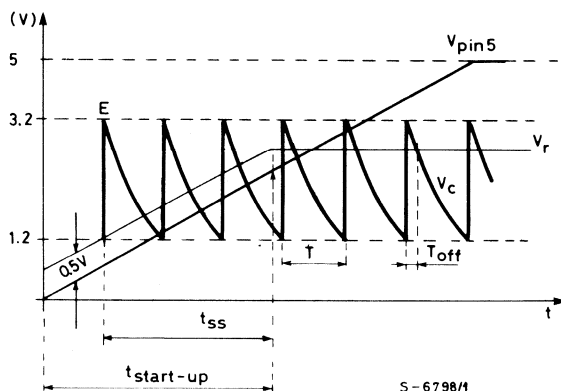


Fig. 11 — Waveform for calculation of duty cycle and soft start time.



CALCULATING THE DUTY CYCLE AND SOFT-START TIME

Assume, for simplicity, that the rising edge of the ramp is instantaneous; V_r is the output voltage of the error amplifier and V_c the ramp voltage (see fig. 11). The PWM comparator block switches when $V_r = V_c$; therefore:

$$V_r = V_c = E e^{-\frac{t}{R_{osc} C_{osc}}}$$

Consequently:

$$t = R_{osc} C_{osc} \ln \frac{E}{V_r}$$

The time obtained from this expression is the T_{OFF} time of the power transistor. The duty cycle d is given by:

$$d = \frac{T_{ON}}{T} = \frac{T - R_{osc} C_{osc} \ln \frac{E}{V_r}}{T} =$$

$$= 1 - \ln \frac{E}{V_r} = \frac{V_o}{V_i}$$

Consequently, starting with the capacitor discharged, the output of the regulator will be at the nominal level when the voltage at the terminal of the capacitor (which is charged by a constant current) has reached $V_r - 0.5V$.

$$t_{\text{start-up}} = \frac{C_{ss} (V_r - 0.5V)}{I_{ss0}}$$

where C_{ss} is the soft-start capacitor and I_{ss0} is the charging current.

Considering as the soft-start time the time required for the soft-start capacitor to charge from (1.2V-0.5V) to $V_r - 0.5V$, gives:

$$t_{ss} = \frac{C_{ss} (V_r - 1.2)}{I_{ss0}} \quad (28)$$

substituting V_r from (27) gives:

$$V_r = E e^{-\left(1 - \frac{V_o}{V_i}\right)}$$

substituting into (28) gives:

$$t_{ss} = \frac{C_{ss}}{I_{ss0}} (E e^{-\left(\frac{V_o}{V_i} - 1\right)} - 1.2)$$

SYNCHRONIZATION

The synchronization function is available on pin 7, this function allows the device to be switched at an externally generated frequency (leaving pin 11 open), or to mutually synchronize several devices, using one of them as master and the others as slave (Fig. 12).

This allows several devices to be operated at the same frequency, avoiding undesirable intermodulation phenomena. The number of mutually synchronizable devices is obviously much greater than the

three devices shown in the figure. It is anyway difficult to establish an exact maximum number of devices, as it depends on different conditions.

The first consideration concerns the accuracy which must be achieved and maintained on the oscillation frequency. Since the bias current on pin 7 is an output current, the sum of all the bias currents must be much smaller than the capacitor discharge current in close proximity to the lower discharge threshold. Therefore, assuming $C_{osc} = 2.2 \text{ nF}$ and $R_{osc} = 4.3 \text{ K}\Omega$, it follows that:

$$\frac{1.2V}{4.3 \text{ K}\Omega} = 280 \mu A$$

Assuming that a 10% variation may be accepted, it follows therefore that the number of synchronizable devices is given by:

$$N = \frac{28 \mu A}{I_{\text{bias max}}}$$

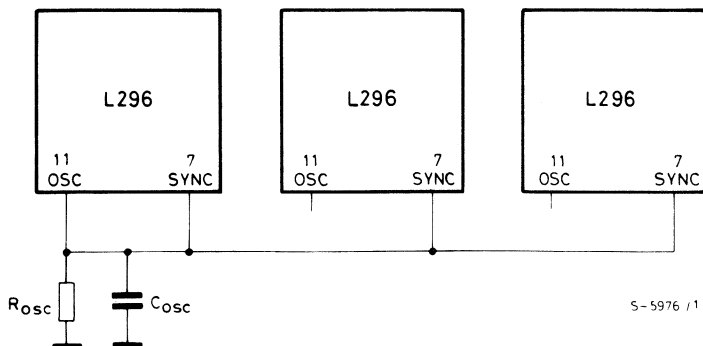
This means that if the overall I_{bias} is too high it may modify the discharging time of the capacitor.

The second consideration concerns the layout design.

In the presence of a great number of devices to be synchronized, the length of the paths may become significant and therefore the distributed inductance introduced along the paths may begin to modify the triangular shaped waveform, particularly the rising edge which is very steep. This effect would affect the devices that are physically located more distant from the master device.

The amplitude of the saw-tooth to be externally connected must be within 0.5V and 3.5V, values also representing the maximum swing of the error amplifier output.

Fig. 12 — In multiple supplies several L296's can be synchronized as shown here.



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CURRENT LIMITATION

The current limitation function has been realized in a rather innovative way to avoid overload condition during the short circuit operation. In fact, while for all the other devices a constant current limitation is implemented by acting on the duty cycle (therefore, in short circuit conditions an output current is equal to the maximum limitation current), the new control approach allows operation in short circuit conditions with a mean current much smaller than the allowed 4A value. Operation of the current limiter will now be described. Refer to the block diagram, fig. 13.

The current which is delivered from the output transistor to the load flows through the current sensing resistor R_S . When the voltage drop on R_S is equal to the offset voltage of the current comparator, the comparator generates a set pulse for the flip-flop, with a delay of about 1 μsec . The purpose of this delay is to avoid triggering of the protection circuit on the current peak that occurs during the recirculation phase. Therefore, the output $\bar{Q}$ goes

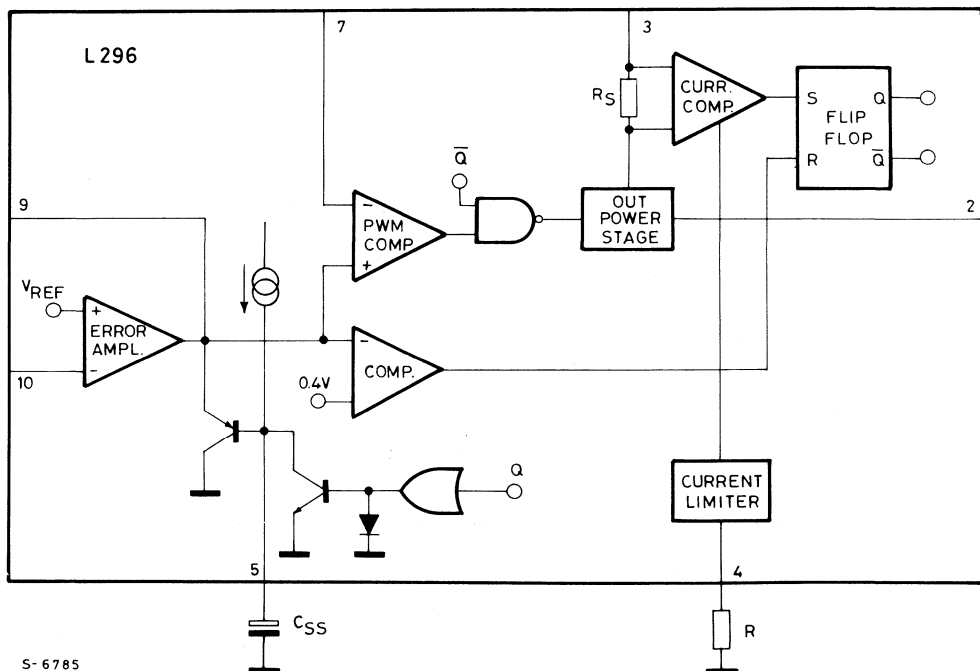
low and the power stage is immediately switched off, while the output Q goes high and acts directly on the soft-start capacitor discharging the soft-start capacitor at a constant current (about 50 μA).

When the voltage on pin 5 reaches 0.4V the comparator triggers, supplying a reset pulse to the flip-flop; from now on, the power stage is enable and the soft-start phase starts again. When the limitation cause, either overload or short circuit, is still present the cycle repeats again. The waveform of the output current on pin 2 is shown in fig. 14.

From fig. 14 it may be observed how this current limitation technique allows the short circuit operation with a very low output current value.

It is possible to reduce the maximum current value by acting on pin 4. On this pin a voltage of about 3.3V is present; by connecting a resistance a constant current, given by $3.3/R$, is sent to ground. This current reduces the offset voltage of the current comparator, therefore anticipating its triggering threshold.

Fig. 13 — Partial schematic showing the current limiter circuit.



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Fig. 14a — Current limiter waveforms.

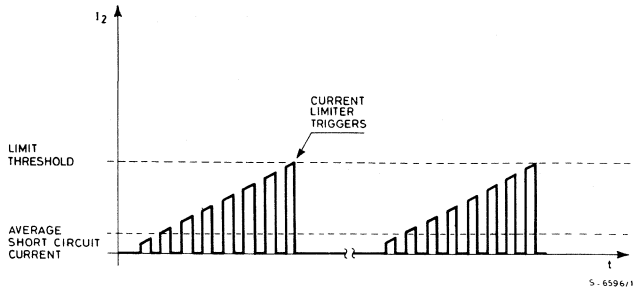


Fig. 14b — Load current in short circuit conditions ($V_i = 40\text{V}$, $L = 300\ \mu\text{H}$, $f = 100\ \text{KHz}$)

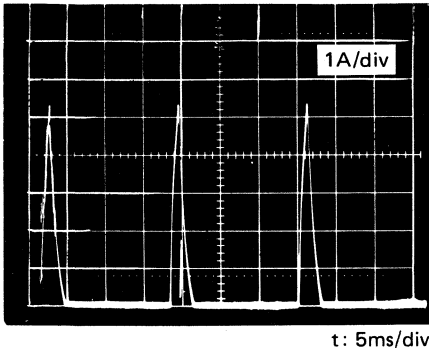
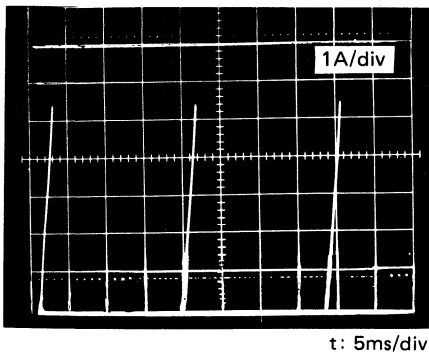


Fig. 14c — Current at pin 2 when the output is short circuited.



RESET

The reset function is of great importance when the device is used to supply microprocessors, logic devices, and so on. This function differentiates the SGS L296 device from all previous devices. The block diagram of the function is shown in fig. 15. A reset signal is generated when the output voltage

is within the limits required to supply the microprocessor correctly.

The reset function is realized through the use of 3 pins: the reset input pin 12, the reset delay pin 13 and the reset output pin 14. When the voltage on pin 12 is smaller than 5V the comparator output is high and the reset capacitor is not charged because the transistor Q is saturated and the voltage on pin 14 is at low level, since Q2 is saturated, too. When the voltage on pin 12 goes above 5V, the transistor Q switches OFF and the capacitor can start to charge through a current generator of about $100\ \mu\text{A}$. When the voltage on pin 13 goes above 4.5V the output of the related comparator switches low and the pin 14 goes high. As the output consists of an open collector transistor, a pull-up external resistance is required. In contrast, when the reset input voltage goes below 5V, less a hysteresis voltage of about 100 mV, the comparator triggers again and instantaneously sets the voltage on pin 14 low, therefore forcing to saturation the Q1 transistor, that starts the rapid discharge of the capacitor. Obviously, the reset delay is again present when the voltage on pin 13 is allowed to go under 4.5V.

To achieve switching operations without uncertainties the two comparators have been provided with an hysteresis of about 100 mV. In every operating condition the reset switching is guaranteed with a minimum reset input of 4.75V, the value required for correct operation of the microprocessor even in the presence of the minimum V_{REF} value.

Normally pin 12 is used connected to pin 10. When it is connected to the output, the function may be more properly called "reset"; on the other hand, when it is connected through resistive divider, to the input voltage, the function is called "power fail". Fig. 16 and fig. 17 show the two possible usages.

The "power-fail" function is used to predict, with a given advance, the drop of the regulator output voltage, due to main failures, which is enough to save the data being processed into protected memory areas. Fig. 18 summarises the reset function operation.

Fig. 15 — Partial schematic showing reset circuit.

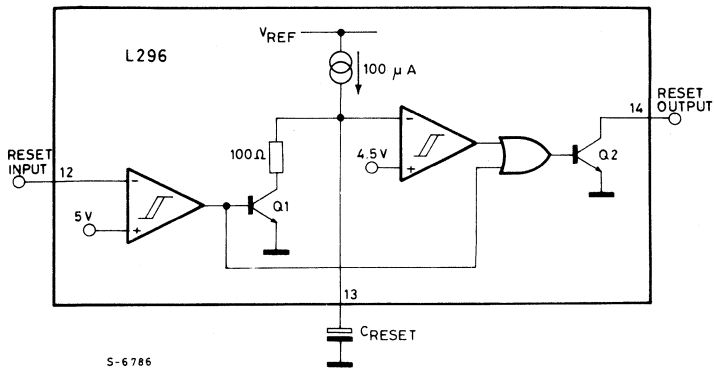


Fig. 16 — For power - on reset the reset block is connected as shown here.

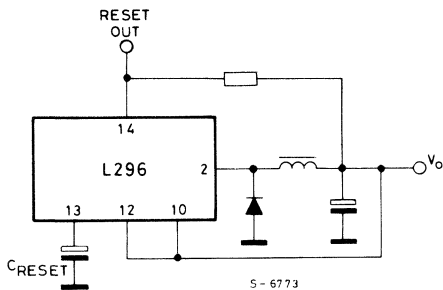


Fig. 17 – To obtain a power fail signal, the reset block is connected like this.

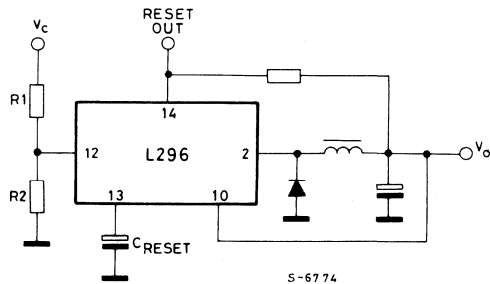
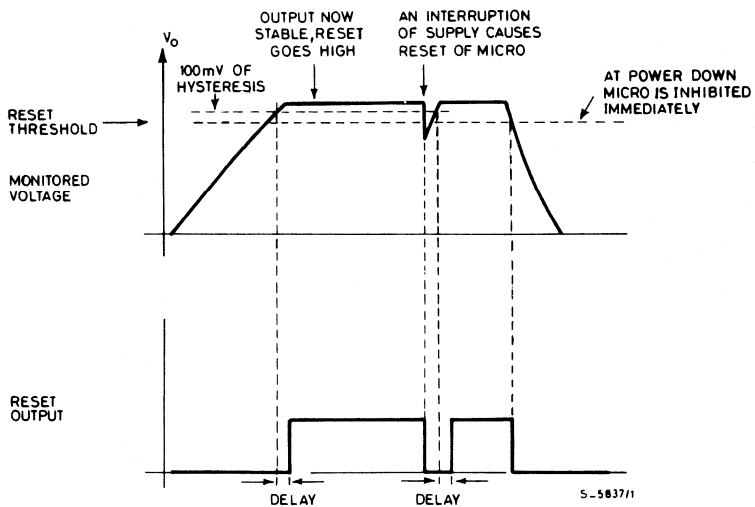


Fig. 18 – Waveform of the reset circuit.



CROWBAR

This protection function is realized by a completely independent block, using pin 1 as input and pin 15 as output. It is used to prevent dangerous overvoltages from occurring when the output exceeds 20% of rated value. Pin 15 is able to output a 100 mA current to be sent to the gate of a SCR which, triggering, short circuits either output or the input. When connected to the input, as the SCR is triggered a fuse in series connected to power supply is blown and to bring the system back to operation manual intervention is requested. Figs. 19, 20 and

21 show the different configurations.

When the voltage on pin 1 exceeds by about 20% the V_{REF} value the output stage is activated, which sends a current to the SCR gate, after a delay of about $5\mu\text{sec}$ to make the system insensitive to low-duration spikes. When activated, the output stage delivers about 100mA; when not activated, it drains about 5 mA and shows a low impedance to the SCR gate to avoid uncorrect triggering due to random noise. If the crowbar function is not used connect pin 1 to ground.

Fig. 19 – Connection of crowbar circuit at output for 5.1V output applications.

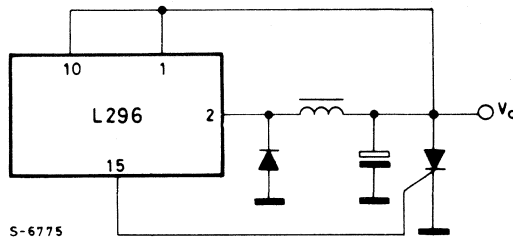


Fig. 20 – Connection of crowbar circuit at output for output voltages above 5.1V.

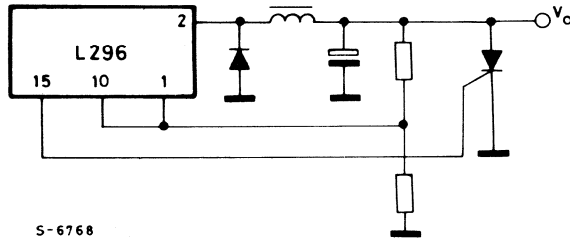
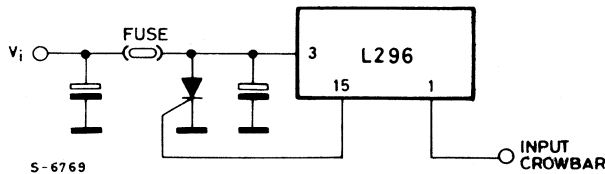


Fig. 21 – Connection of crowbar circuit to protect input. When triggered, the SCR blows the fuse.



INHIBIT

The inhibit input (pin 6) is TTL compatible and is activated when the voltage exceeds 2V and deactivated when the voltage goes under 0.8V. As may be seen in the block diagram, the inhibit acts on the power transistor, instantaneously switching it off and also acts on the soft-start, discharging its capacitor. When the function is unused, pin 6 must be grounded.

THERMAL PROTECTION

The thermal protection function operates when the junction temperature reaches 150°C ; it acts directly on the power stage, immediately switching it off, and on the soft-start capacitor, discharging it. The thermal protection is provided with hysteresis and, therefore, after an intervention has occurred, it is necessary to wait for the junction temperature to decrease of about 30°C below the intervention threshold.

APPLICATIONS

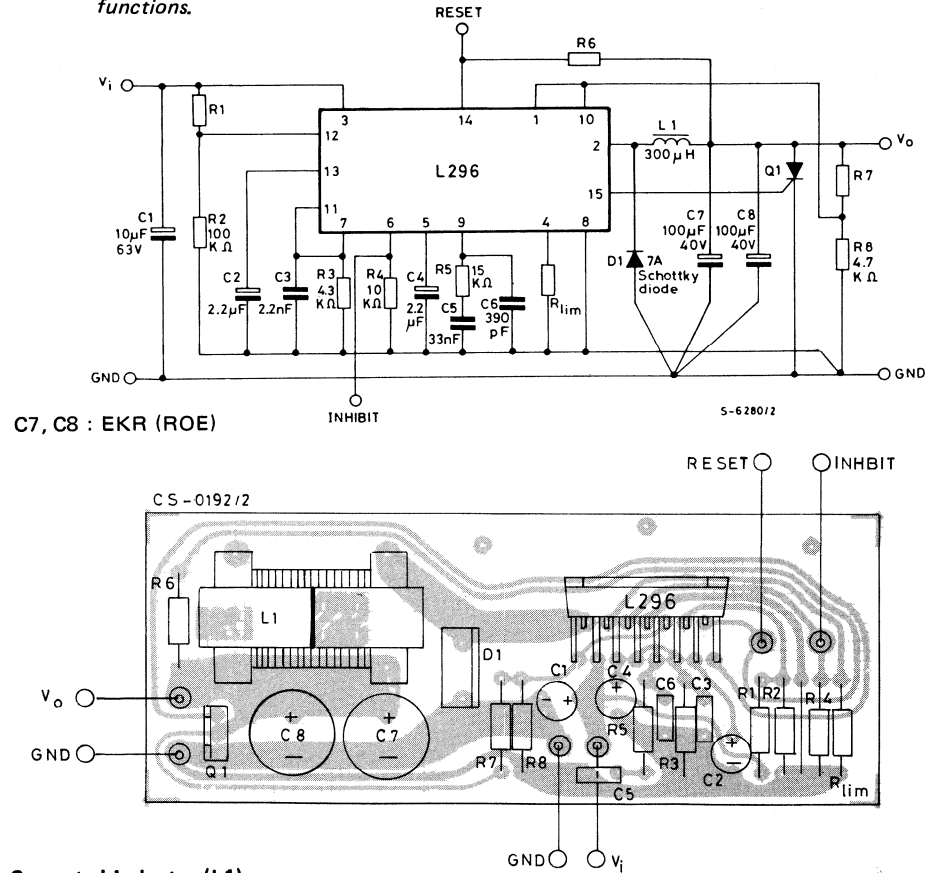
Though the L296 is designed for step-down regulator configurations it may be used in a variety of other applications. We will now examine these possibilities and show how the capabilities of the device may be extended.

In fig. 22 the complete typical application is shown, where all the functions available on the device are being used. This circuit delivers to the load a maximum current of 4A and a voltage which is established by the voltage divider constituted by R₇ and R₈ resistances. The following table is helpful for a quick calculation of some standard output voltages:

Resistor value for standard output voltages		
V _o	R ₈	R ₇
12V	4.7 kΩ	6.2 kΩ
15V	4.7 kΩ	9.1 kΩ
18V	4.7 kΩ	12 kΩ
24V	4.7 kΩ	18 kΩ

To obtain V_o = V_{REF} the pin 10 is directly connected to the output, therefore eliminating both R₇ and R₈. The switching frequency is 100 kHz.

Fig. 22 – Schematic, PCB layout and suggested component values for the evaluation circuit used to characterize the L296. This is a typical stepdown application which exercises all the device's functions.

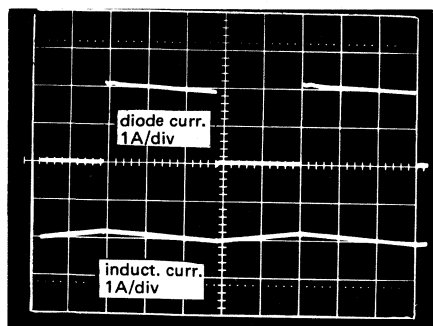
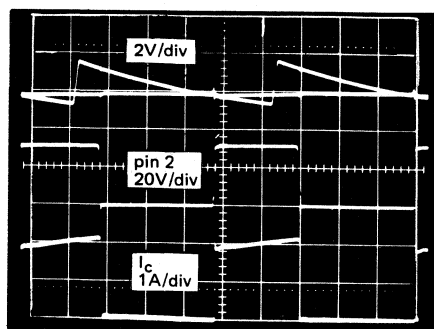


Suggested Inductor (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 – A2MPP	43	1.0 mm.	—
Thomson GUP 20x16x7	65	0.8 mm.	1 mm.
Siemens EC 35/17/10 (B6633& – G0500 – X127)	40	2 x 0.8 mm.	—

VOGT 250 μH Toroidal coil, part number 5730501800

Fig. 23 — Oscilloscope photographs showing main waveforms of the figure 22 circuit.



$t: 2\mu s/div$

The oscilloscope photographs of the main waveforms are shown in fig. 23. The output voltage ripple ΔV_o depends on the current ripple in the coil and on the performance of the output capacitor at the switching frequency (100 kHz). A capacitor suitable for this kind of application must have a low ESR and be able to accept a high current ripple, at the working frequency. For this application the Roederstein EKR series capacitors have been selected, designed for high frequency applications (>200 kHz) and manufactured to show low ESR value and to accept high current ripples. To minimize the effects of ESR, two 100 $\mu F/40V$ capacitors have been connected in parallel. The behaviour of the impedance as a function of frequency is shown in fig. 24.

Also the selection of the catch diode requires special care. The best choice is a Schottky diode which minimizes the losses because of its smaller forward voltage drop and greater switching frequency rate. A possible limitation comes from the backward voltage, that generally reaches 40V max.

When the full input voltage range of the device is required in this application it is possible to use super fast diodes with 35 to 50 ns rated recovery time, where no more problems on the backward voltage occur (on the other hand, they show a greater forward voltage). The use of slower diodes,

with $trr = 100$ ns or more is not recommended; The photographs in fig. 25 show the effects on the power current and on the voltage on pin 2, due to the diodes showing different speeds. Diodes showing trr greater than 35-50 ns will reduce the overall efficiency of the system, increasing the power dissipated by the device.

The third component requiring care is the inductor. Fig. 22a shows the part numbers of some types used for testing. Besides having the required inductance value, the coil has to show a very high saturation current.

Therefore, a correct dimensioning requires a saturation current above the maximum value of I_{2L} , the current limit threshold.

To achieve high saturation with ferrite cores an air gap between the two core halves must be provided; the air gap causes a leakage flux which is radiated in the surrounding space. To better limit this phenomenon "pot cores" may be used, whose geometry is such to better limit the flux radiated to the outside.

Using toroidal cores, for instance of Magnetic 58930-A2 moly-permalloy kind, both the requirements of high saturation and low leakage flux are satisfied. The saturation is softer than the saturation shown by the ferrite materials. The air gap is not concentrated in one area, but is finely distributed along the whole core; this gives the low leakage flux value.

Careful selection of the external components therefore allows the realization of a power supply system whose benefits are significant when compared to a system with the same performance but realized with the linear technique.

Fig. 24 — Typical impedance/frequency curves for EKR capacitors.

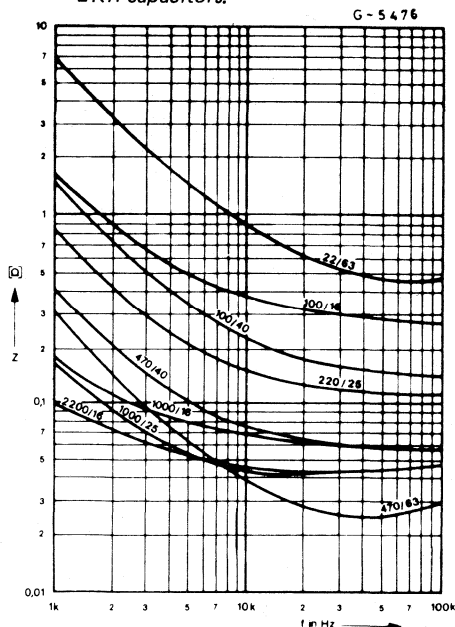
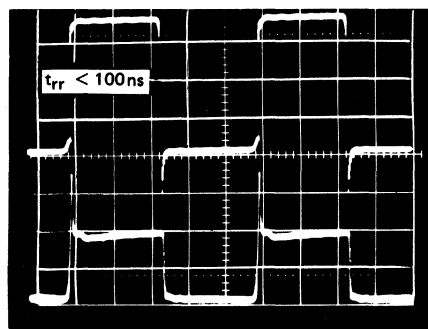
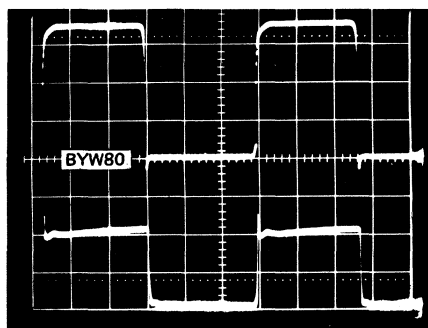
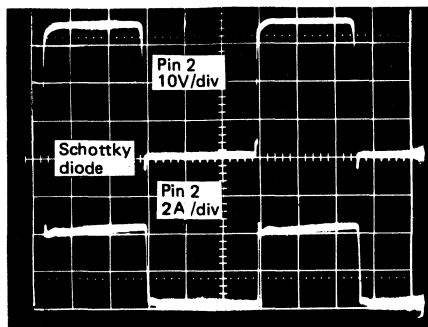


Fig. 25 – Oscilloscope photographs showing the waveforms obtained with diodes having different t_{rr} values.



t: 2μs/div

SWITCHING vs LINEAR

Switching regulators are more efficient than linear types so the transformer and heatsink can be smaller and cheaper. But how much can you gain?

We can estimate the savings by comparing equivalent linear and switching regulators. For example, suppose that we want a 4A/5V supply.

Linear

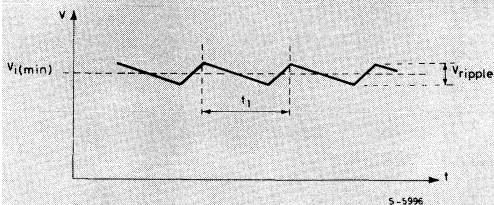
For a good linear regulator the minimum dropout

will be at least 5V at 4A. The minimum input voltage is given by:

$$V_{i \min} = V_o + V_{\text{drop}} + \frac{1}{2} V_{\text{ripple}}$$

where:

$$V_{\text{ripple}} \simeq \frac{I_o t_1}{C} = \frac{4 \times 8 \times 10^{-3}}{10 \times 10^{-3}} = 3.2V$$



(a good approximation is 8 ms for t_1 at mains frequency of 50Hz and 10.000 μF for C, the filter capacitor after the bridge). Therefore $V_{i \min} \simeq 10.6V$. Since operation must be guaranteed even when the mains voltage falls 20%, the nominal voltage on load at the terminals of the regulator must be:

$$V_{\text{nom}} = \frac{V_{i \min}}{0.8} = \frac{10.6}{0.8} = 13.25V$$

To allow even a small margin we have to choose:

$$V_{\text{nom}} = 14V$$

The power that the series element must dissipate is therefore:

$$P_d = (V_{\text{nom}} - V_o) I_o = 36W$$

and a heatsink will be necessary with a thermal resistance of:

$$R_{\text{th heats.}} = 0.8^\circ\text{C/W}$$

and the transformer must supply a power of:

$$P_{\text{diss}} = 14 \times 4 = 56W$$

It must therefore be dimensioned for:

$$P_D = \frac{56}{0.9} = 62VA$$

Switching (L296)

Assuming the same nominal voltage (14V), the L296 data sheet indicates that the power dissipated in this case is only 7W. And this power is dissipated in two elements; the L296 itself and the recirculation diode.

It follows that the transformer must be roughly 30VA and the heatsink thermal resistance about 11°C/W.

	Linear	Switching
Transformer	62 VA	30 VA
Heatsink	0.8 °C/W	11 °C/W

This comparison shows that the L296 switching regulator allows a saving of roughly 50% on the cost of the transformer and an impressive 80-90% on the cost of the heatsink. Considering also the extra functions integrated by the L296 the total cost of active and passive components is roughly the same for both types.

Finally, it is important to note that a lower power dissipation means that the ambient temperature in the regulator enclosure can be lower – particularly when the circuit is enclosed in a box – with all the

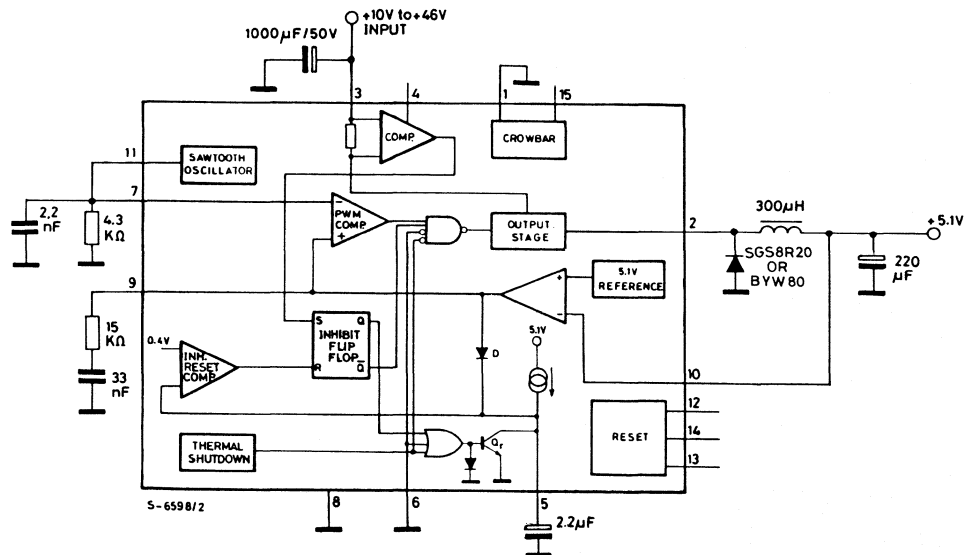
advantages cooler operation brings.

If for some reason it is necessary to use higher supply voltages the switching technique, and hence the L296, becomes even more advantageous.

LOW COST APPLICATION AND PREREGULATOR

Fig. 26 shows the low cost application of a 4A and $V_o = 5.1V$ power supply. A minimum amount of essential external components is required, which are necessary for correct operation. It is impossible to save other components, specially the soft-start capacitor. Without soft-start, the system cannot reach the steady state and there is also a serious risk of damaging the device.

Fig. 26 – A minimal component count 5.1V/4A supply.



This application is very well suited not only as a low-cost power supply, but also as pre-regulator for post-regulators distributed in different circuit points, or even on different boards (Fig. 27). The post-regulators may be selected among the low-drop types, like L4805 and L387 for example, still obtaining a high efficiency, combined with an excellent regulation. The use of L387 device allows us to use also the reset function, useful to power a microprocessor.

POWER SUPPLY COMPLETE WITH TRANSFORMER

Fig. 28 shows a power supply complete of transformer, bridge and filter, with regulation on the output voltage from 5.1V to 15V.

As already stated above, the output capacitors have to show some speciale features, like low ESR and high current ripple, to obtain low voltage ripple

values and high reliability. The input filter capacitors must not be neglected because they have to show excellent features, too, having to supply a pulsed current, required by the device at the switching frequency. The current ripple is rather high, greater than the load current. For this application, two parallel connected 3300 µF/50V EYF (ROE) capacitors have been used.

POWER SUPPLY WITH MAINS SWITCHING PREREGULATOR

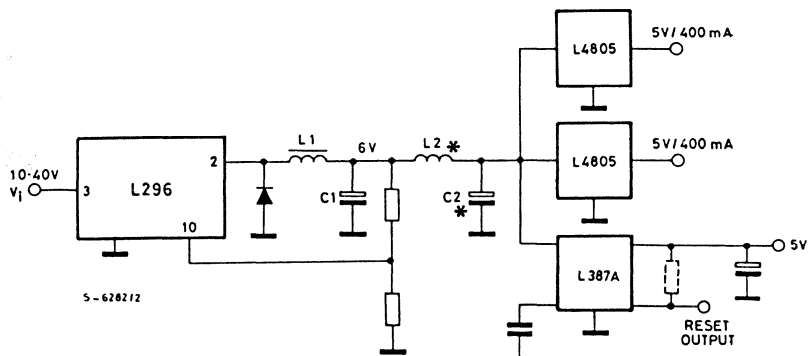
When it is desirable to eliminate the 50/60 Hz transformer – in portable or volume-limited equipment – a mains preregulator can be added to reduce the input voltage to a level acceptable for the L296.

In this case the pre-regulator circuit is connected to the primary of the transformer which now operates at the switching frequency and is therefore smaller and lighter.

Using a UC3840 which includes the feed-forward function it is possible to compensate mains variation within wide limits. The secondary voltage is therefore only affected by load variations. Using one or more L296s as postregulators, feedback to the pri-

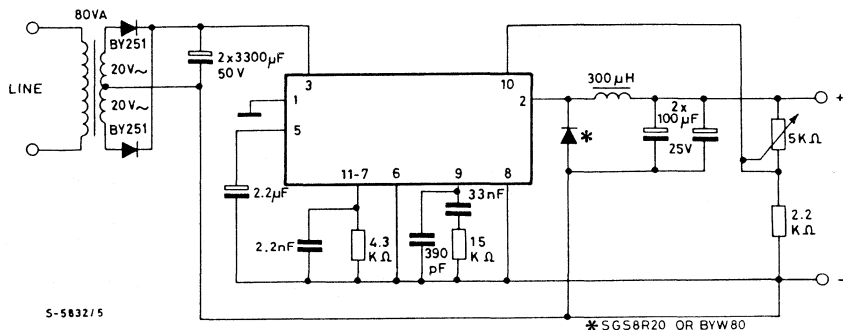
mary is no longer necessary, reduces the complexity and cost of the transformer which needs only a single secondary winding. Fig. 28A shows a multi-output supply with a mains preregulator.

Fig. 27 — The L296 may also be used as a preregulator in distributed supply systems.



(*) L2 and C2 are necessary to reduce the switching frequency spikes.

Fig. 28 — A typical variable supply showing the mains transformer.



$V_o = 5.1$ to $15V$

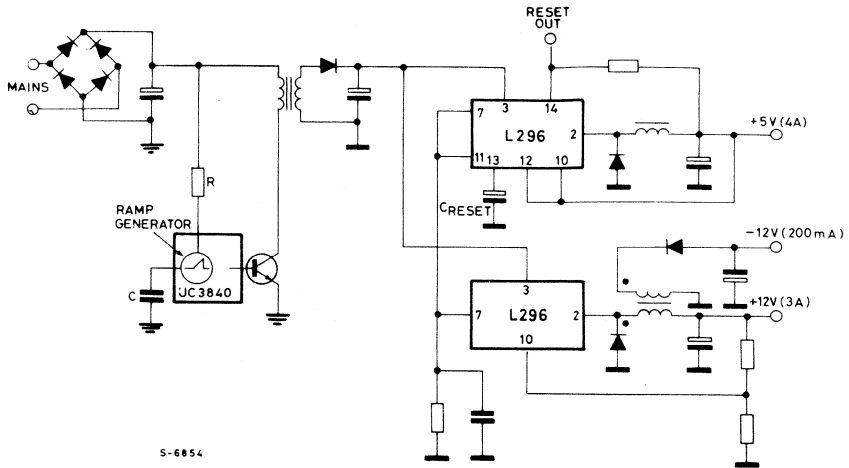
$I_o = 4A$ max. (min. load current = $100mA$)

ripple $\leq 20mV$

load regulation ($1A$ to $4A$) = $10mV$ ($V_o = 5.1V$)

line regulation ($220V \pm 15\%$ and to $I_o = 3A$) = $15mV$ ($V_o = 5.1V$)

Fig. 28A — A multiple output supply using a switching preregulator rather than a mains transformer.



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POWER SUPPLY WITH 0 – 30V ADJUSTABLE VOLTAGE

When output voltages lower than 5V are required, the circuit shown in fig. 29 may be used.

Calibration is performed by grounding the P1 slider. Acting on P2, the current which flows through the 10 kΩ resistor is fixed at approximately 2.5 mA to obtain an output voltage of 30V. The equivalent circuit is shown in fig. 30.

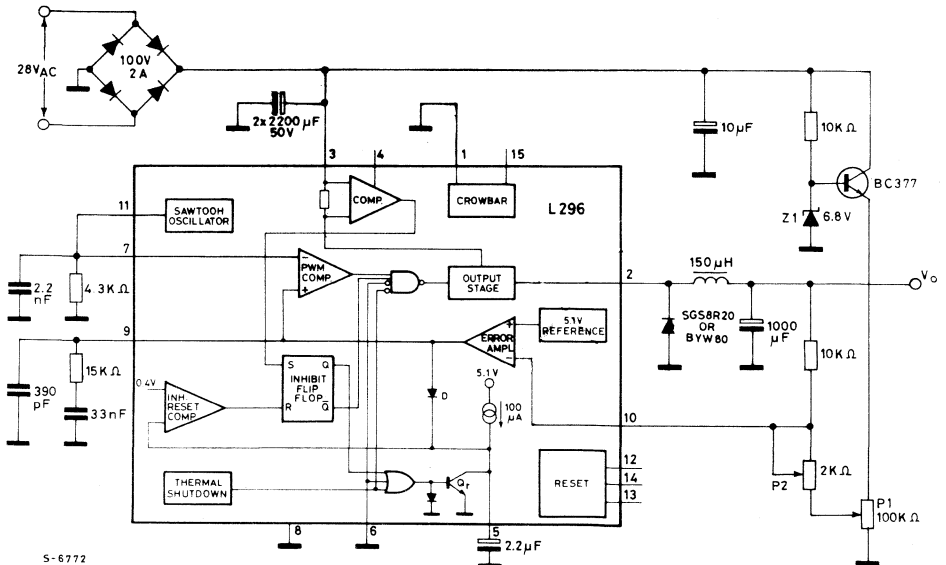
Acting now on the slider of P1, the current flow-

ing through the divider may be varied. The new equivalent circuit is shown in fig. 31.

Reducing the current flowing, also the voltage drop across the 10 kΩ resistance is reduced, together with V_O . When the current reaches zero, it follows that $V_O = V_{REF}$. When the voltage on the slider of P1 exceeds V_{REF} , the current start to flow in opposite direction and V_O begins to decrease below 5V.

When $I_1 \times 10K\Omega = V_{REF}$ it follows that $V_O = 0$.

Fig. 29 — Variable 0-30 V supply illustrating how output voltages below 5.1V are obtained.



S-6772

Fig. 30 — When setting up the figure 29 circuit the slider of P1 is grounded, giving the equivalent circuit shown here, and P2 adjusted to give an output voltage of 30 V.

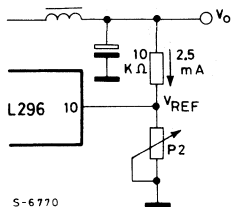


Fig. 31 — Partial schematic showing output voltage adjustment of figure 29.

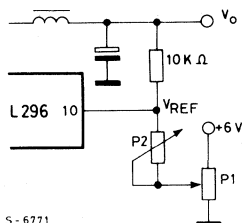
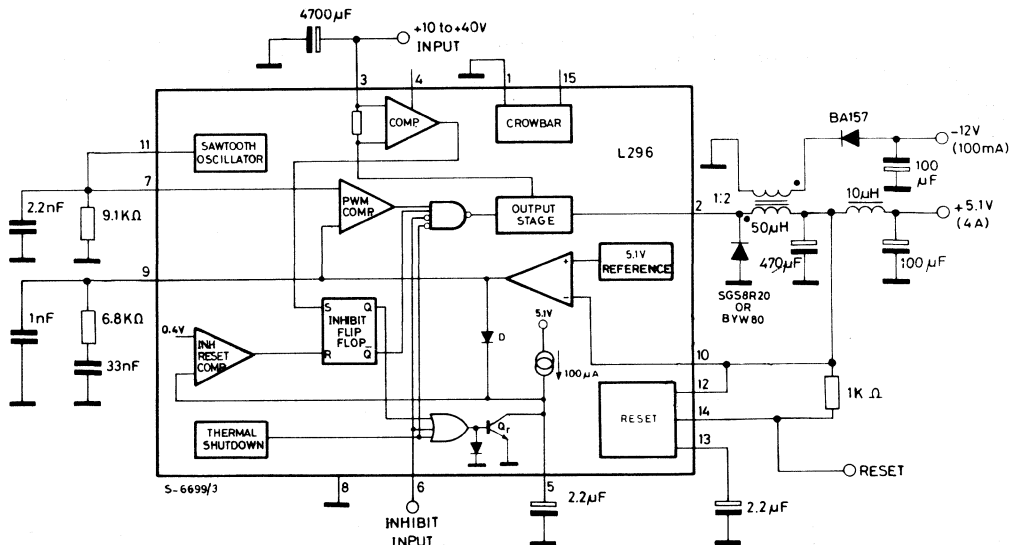


Fig. 32 — Dual output regulator showing how an additional winding can be added to the inductor to generate a secondary output.



PERSONAL COMPUTER POWER SUPPLY

Using two mutually synchronized devices it is possible to obtain a four output power supply suitable for power a microprocessor system.

$V_{O1} = 5.1V/4A$
 $V_{O2} = 12V/2.5A$ (up to 4A)
 $V_{O3} = -5V/0.2A$
 $V_{O4} = -12V/0.2A$

DUAL OUTPUT REGULATOR

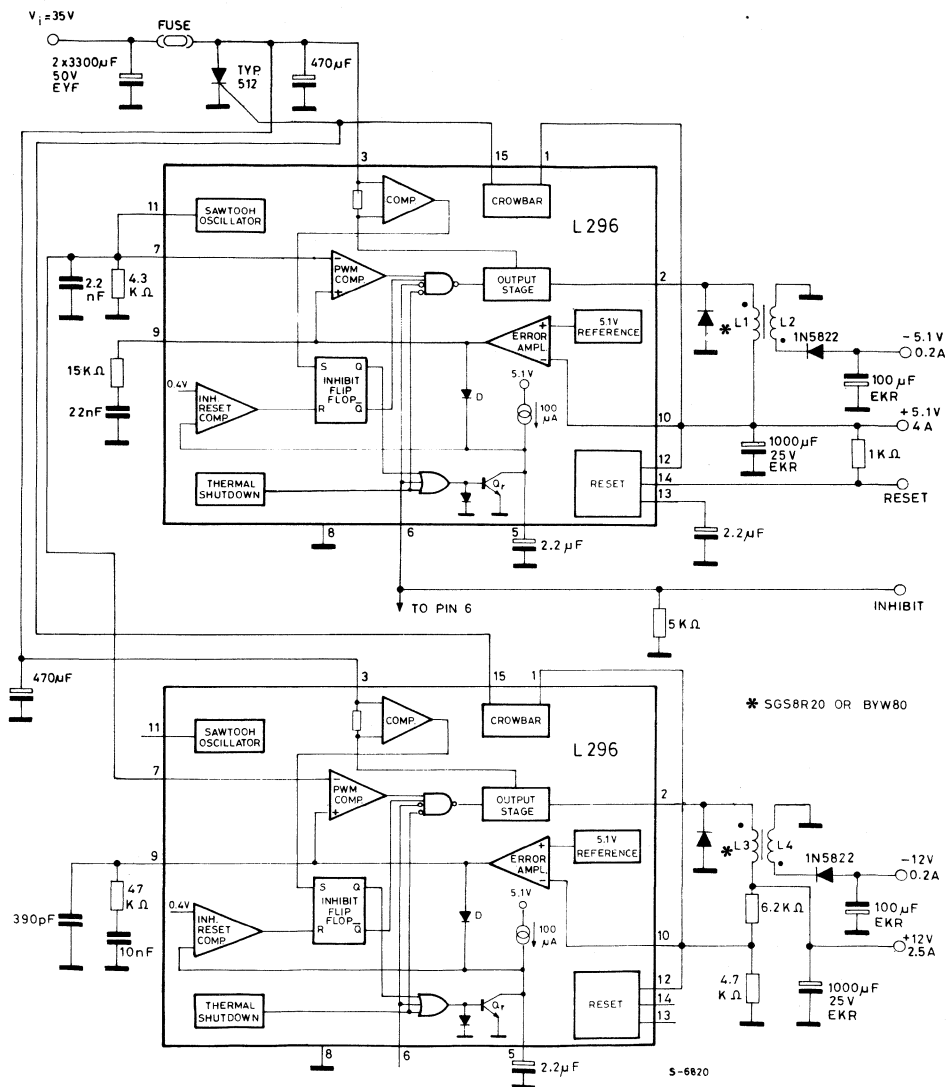
The application shown in fig. 32 is specially interesting because it provides two output voltages. The first voltage, the main one, is directly controlled by the feedback circuit. The second voltage is obtained through an auxiliary winding.

It often happens, when microprocessors, logic devices etc., have to be power supplied, that a main 5V output and an auxiliary +12V or -12V output are required, the latter with lower current requirements ($100 \div 200$ mA) and a stabilization level not excessively high. As the auxiliary power supply is obtained through a completely separated winding, it is possible to obtain either a positive or negative voltage (compared to the main voltage or also a completely isolated voltage. With V_i variable between 20V and 40V, $V_o = 5.1V$ and $I_o = 2.5A$, the auxiliary -12V/0.2A voltage is within a $\pm 2\%$ tolerance.

The schematic diagram is shown in fig. 33. The 5V output is also provided with the reset function, that is available also for the 12V output.

The feedback is direct, no other external component is used and no calibration is therefore required. An output is obtained with the accuracy of the reference voltage ($\pm 2\%$). For the 12V output, by using a resistive divider with 1% resistance an output is obtained whose spread is within $\pm 4\%$.

Fig. 33 — Microcomputer supply with 5V, -5V, 12V and -12V outputs.



The two devices are mutually synchronized not to give rise to intermodulation which could generate unpleasant noise and, at the same time, a further component saving is achieved.

The crowbar function is implemented on both 5V and 12V outputs, using a single SCR connected to the input. The latter, by discharging to ground the electrolytic filter capacitors, blows the fuse connected in series with the devices power supply. In this way, should a faulty be present on either of the main outputs, the supply is switched off for whole system.

To inhibit both the devices with a single input signal, it is possible to connect the two inhibit inputs (pin 6) together; the 5KΩ resistance is used when the inhibit input is left open. If this input is not used it must be grounded.

As may be noted in the diagram, to obtain the two auxiliary voltages is very simple and cost-effective.

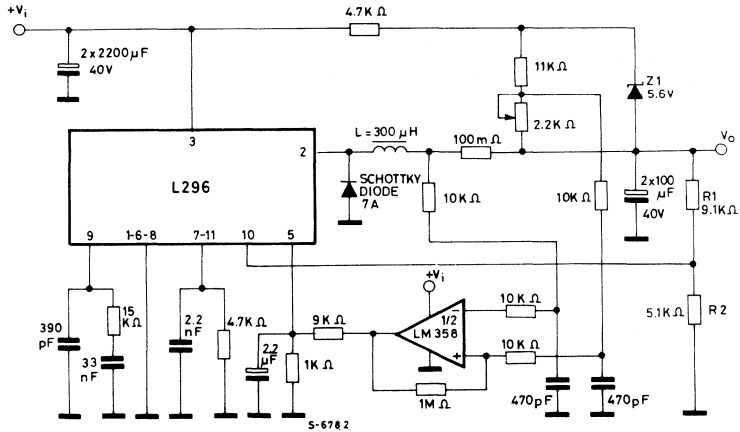
It is suggested that the diodes are fast types ($t_{rr} < 50$ nsec); should slower diodes be required some more turns have to be added to the auxiliary winding.

BATTERY CHARGER

When the device has to be used as current generator it is necessary to avoid the internal current limiter is operated. Fig. 34 shows the circuit realizing constant current limitation. In this way it is possible to obtain a 6V, 12V and 24V battery charger. For each of these voltages a max. current of 4A is avail-

able, which is large enough for batteries up to 40-45 Ah (for 12V type). With reference to the electric diagram through the $2K\Omega$ potentiometer the max output current is set, while through the $R_1 - R_2$ output divider the voltage is set. (R_1 may be replaced by either a potentiometer or a 3 position switch, to directly obtain the three 6V, 12V and 24V voltages).

Fig. 34 — Battery charger circuit illustrating how the device is used to regulate the output current.



HIGHER INPUT VOLTAGE

Since a maximum input voltage of 46V (operating value) may be applied to the device the diagram shown in fig. 35 may be used when it is necessary to exceed this limit.

This system is particularly useful when operating at low output voltages. In this case a mean current I_{DC} which has a low value when compared to I_o is obtained. In fact, since $V_o = V_i (T_{ON}/T)$ and $V_o I_o = V_i I_{DC}$ (assuming the device has an ideal efficiency), it follows that $I_{DC} = I_o (T_{ON}/T)$.

Assuming to be:

$$V_o = 5V \quad I_o = 4A \quad \text{and} \quad V_3 \approx 37V,$$

it follows that:

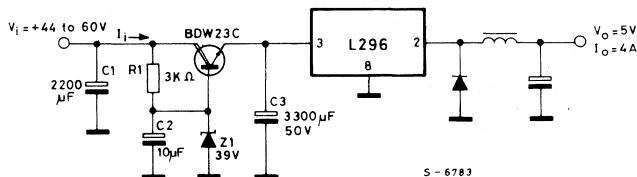
$$T_{ON}/T = V_o/V_i = \frac{5}{37} = 0.135$$

$$I_{DC} = 4 \times 0.135 = 0.54A.$$

With input voltage 50V and $I_o = 4A$, the external transistor dissipates about 7W. High good efficiency is still achieved, around 74%; in the real case, considering also the device losses, an efficiency around 62% is achieved.

During output short circuits the external transistor is not overloaded because in this condition I_{DC} reduces to values lower than 100mA. It is not possible to realize this application with series post-regulator because the efficiency would be unacceptably low.

Fig. 35 — The maximum input voltage can be raised above 46V by adding a transistor as shown here.



MOTOR CONTROL

The L296 is also suitable for use in motor controls applications. Fig. 36 shows how to use the device to drive a motor with a maximum power of about 100W and provided with a tachometer generator for a good speed control.

HIGHER CURRENT REGULATORS

It is possible to increase the output current to the load above 4A through the use of an external power transistor. Fig. 37 shows a suitable circuit. The frequency is around 40 kHz to prevent the device from losing excessive power due to switching on the external power.

The circuits shown in fig. 38 and fig. 39 show how current limitation may be realized in two different ways: through a sensing resistor connected in series with the collector of the external power transistor or through a current transformer.

In the first case, the sensing resistor is a low value resistor able to withstand the maximum load current required. The V_{CE} of the power transistor is higher than its V_{CEsat} : when the resistor is connected in series to the collector V_{CE} is reduced; consequently since the overall dissipated power is constant, the power dissipated by the sensing resistor is subtracted from that dissipated by the power transistor. The values indicated in figs. 38 and 39 realize adjustable current limitation for load currents around 10A.

Fig. 36 — With a tacho dynamo supplying feedback the L296 can be used as a motor speed controller.

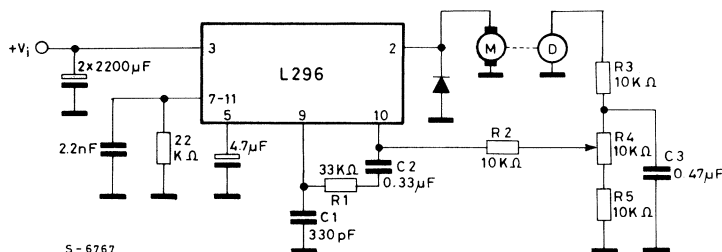


Fig. 37 — The output current may be increased by adding a power transistor as shown in this circuit.

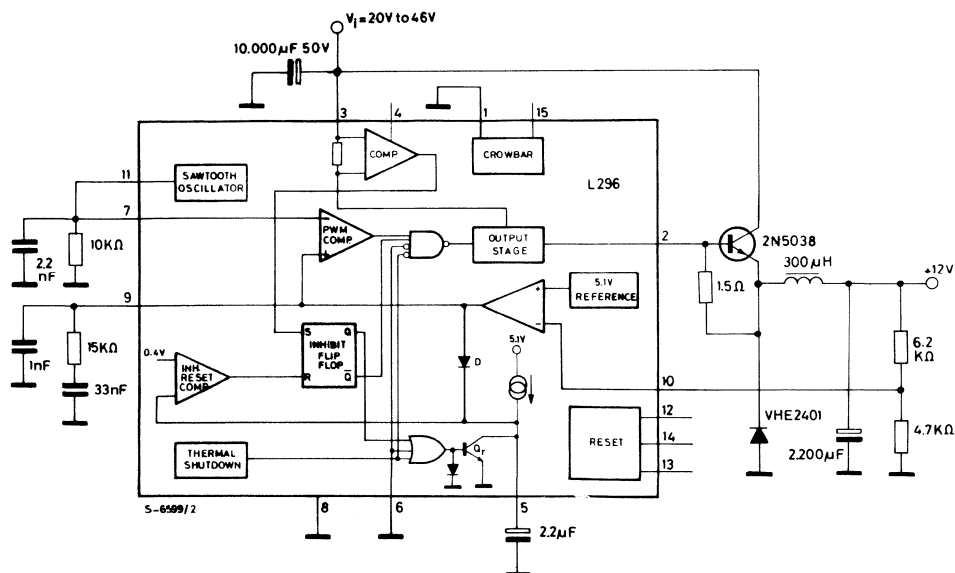


Fig. 38 — This circuit shows how current limiting for the external transistor is obtained with a sensing resistor.

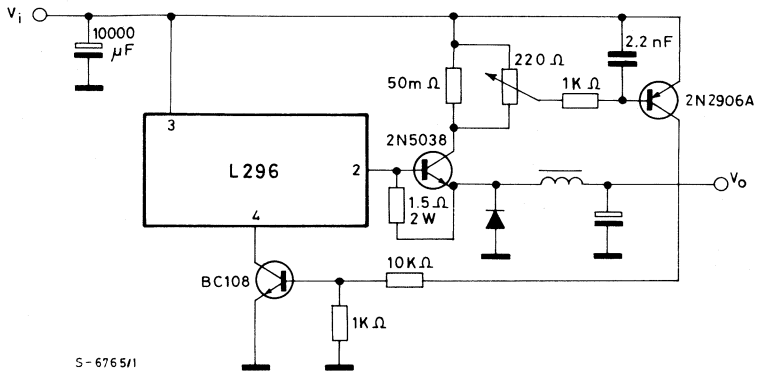
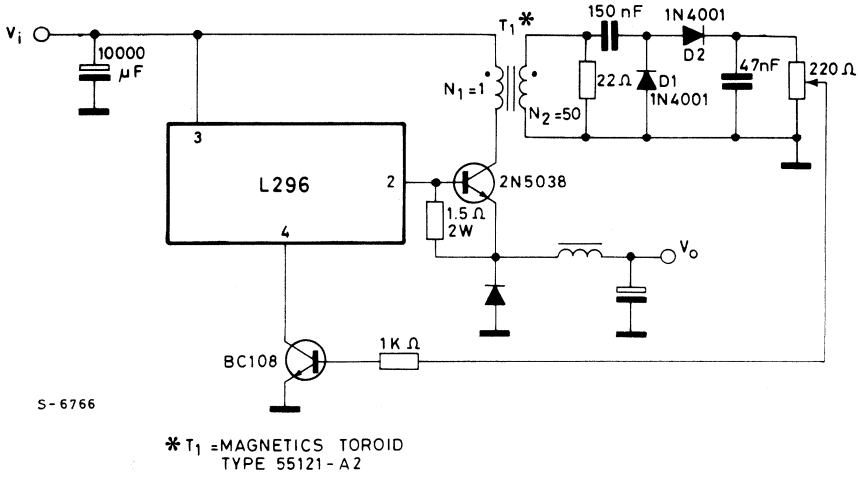


Fig. 39 — A small transformer is used in this example for current limiting.



STEP-UP CONVERTER

With the L296 it is also easy to realize a step-up converter, by using a MOS power transistor. Fig. 40 shows the electric diagram of the step-up converter. The frequency is 100 kHz, operation is in discontinuous mode and the device internal current limiter is used. Therefore no other external protection is required.

The input voltage could be a 12V car battery, from which an output voltage of 35V may be obtained. Lower output voltage values may be obtained by reducing the value of R₇.

DESCRIPTION OF OPERATION

Fig. 41 shows the diagram of the circuit realizing the step-up configuration.

When the transistor Q1 is ON, the inductance L charges itself with a current given by:

$$i_L = \frac{V_i}{L} t$$

The peak current in the coil is:

$$I_{peak} = \frac{V_i}{L} T_{ON}$$

Fig. 40 — A step-up converter using a power MOS transistor.

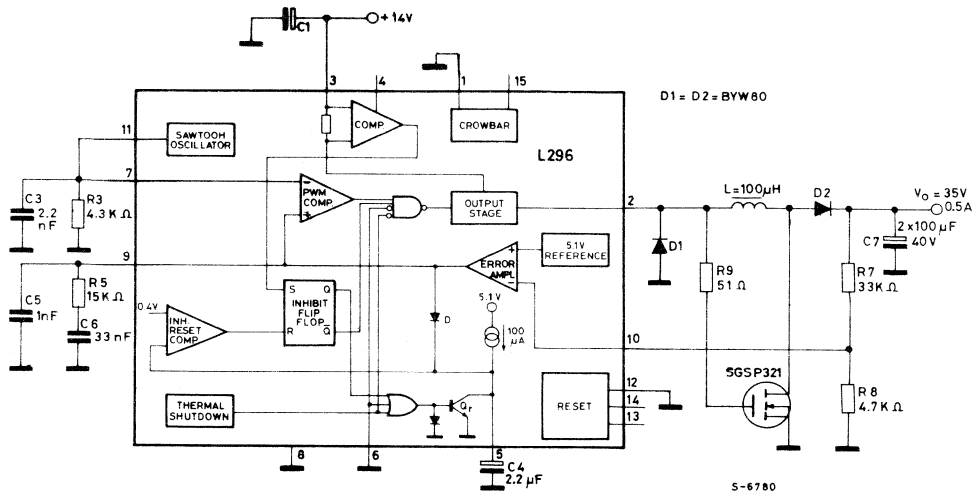
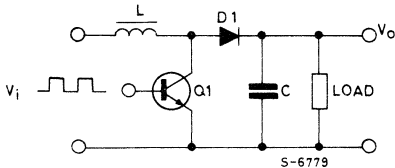


Fig. 41 — Basic schematic for step-up configurations.



In this configuration, unlike the step-down configuration, the peak current is not strictly related to the load current. The energy stored in the coil is successively discharged across the load when the transistor switches OFF. To calculate the I_o load current, the following procedure may be used:

$$\frac{1}{2} L I_{\text{peak}}^2 = V_o I_o T$$

$$I_o = \frac{L I_{\text{peak}}^2}{2 V_o T} = \frac{V_i^2 T_{\text{ON}}^2}{2 L V_o T}$$

For a greater output power to be available, the internal limitation must be replaced by an external circuit to protect the external power devices and to limit the current peak to a convenient value. A dual comparator (LM393) with hysteresis is used to avoid uncertainties when the current limitation operates. The electric diagram is shown in fig. 42.

LAYOUT CONSIDERATIONS

Both for linear and switching power supplies when the current exceeds 1A a careful layout becomes important to achieve a good regulation. The problem becomes more evident when designing switching regulators in which pulsed currents are over imposed on dc currents. In drawing the layout, therefore, special care has to be taken to separate ground paths for signal currents and ground paths for load currents, which generally show a much higher value.

When operating at high frequencies the path length becomes extremely important. The paths introduce distributed inductances, producing ringing phenomena and radiating noise into the surrounding space.

The recirculation diode must be connected close to pin 2, to avoid giving rise to dangerous extra negative voltages, due to the distributed inductance.

Fig. 43 and fig. 44 respectively show the electric diagram and the associated layout which has been realized taking these problems into account. Greater care must be taken to follow these rules when two or more mutually synchronized devices are used.

[illegible]

Suggested Inductor (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 – A2MPP	43	1.0 mm.	—
Thomson GUP 20x16x7	65	0.8 mm.	1 mm.
Siemens EC 35/17/10 (B663& – G0500 – X127)	40	2 x 0.8 mm.	—

VOGT 250 μ H Toroidal coil, part number 5730501800

Resistor values for standard output voltages		
V _o	R8	R7
12V	4.7 k Ω	6.2 k Ω
15V	4.7 k Ω	9.1 k Ω
18V	4.7 k Ω	12 k Ω
24V	4.7 k Ω	18 k Ω

HEATSINK DIMENSIONING

The heatsink dissipates the heat produced by the device to prevent the internal temperature from reaching values which could be dangerous for device operation and reliability.

Integrated circuits in plastic package must never exceed 150 °C even in the worst conditions. This limit has been set because the encapsulating resin has problems of vitrification if subjected to temperatures of more than 150 °C for long periods or of more than 170 °C for short periods. In any case the temperature accelerates the ageing process and therefore influences the device life; an increase of 10° C can halve the device life. A well designed heatsink should keep the junction temperature between 90° C and 110° C. Fig. 45 shows the structure of a power device. As demonstrated in thermodynamics, a thermal circuit can be considered to be an electrical circuit where R_1 , R_2 represent the thermal resistance of the elements (expressed in °C/W) (see fig. 46).

Fig. 45

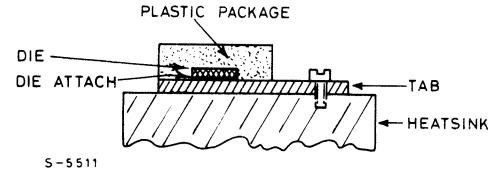
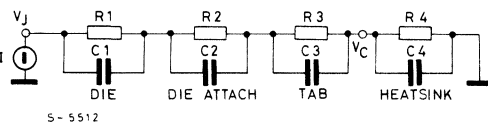


Fig. 46

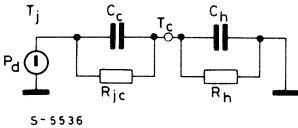


- C1, C2 are the thermal capacitance (expressed in °C/W)
- I is the dissipated power
- V is the temperature difference with respect to the reference (ground)

This circuit can be simplified as shown in fig. 47, where:

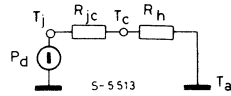
- Cc is the thermal capacitance of the die plus that of the tab.
- Ch is the thermal capacitance of the heatsink
- Rjc is the junction case thermal resistance
- Rh is the heatsink thermal resistance

Fig. 47



But since the aim of this section is not that of studying the transistors, the circuit can be further reduced as shown in figure 48.

Fig. 48



If we now consider the ground potential as ambient temperature, we have:

$$\begin{aligned} T_j &= T_a + (R_{jc} + R_h) P_d & a) \\ R_h &= \frac{T_j - T_a - R_{jc} P_d}{P_d} & b) \\ T_c &= T_a + R_h P_d & c) \end{aligned}$$

Thermal contact resistance depends on various factors such as the mounting, contact area and planarity of the heatsink. With no material between the device and heatsink the thermal resistance is around 0.5 °C/W; with silicone grease roughly 0.3 °C/W and with silicone grease plus a mica insulator about 0.4 °C/W. See fig. 49. In application where one external transistor is used together, the dissipated power must be calculated for each component. The various junction temperatures can be calculated by solving the circuit shown in fig. 50. This applies if the dissipating elements are fairly close with respect to the dissipator dimensions, otherwise the dissipator can no longer be considered as a concentrated constant and the calculation becomes difficult. This concept is better explained by the graph in fig. 51 which shows the case (and therefore junction) temperature variation as a function of the distance between two dissipating elements with the same type of heatsink and the same dissipated power. The graph in fig. 51 refers to the specific case of two elements dissipating the same power, fixed on a rectangular aluminium plate with a ratio of 3 between the two sides. The temperature jump will depend on the total dissipated power and on the devices geometrical positions. We want to show that there exists an optimal position between the two devices:

$$d = \frac{1}{2} \cdot \text{side of the plate}$$

Fig. 49

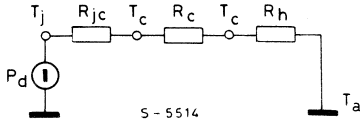


Fig. 50

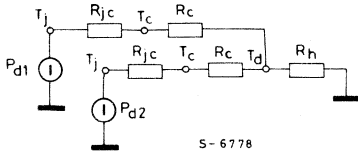


Fig. 52 shows the trend of the temperature as a function of the distance between two dissipating elements whose dissipated power is fairly different (ratio 1 to 4). This graph may be useful in application with two L296 synchronized.

Fig. 51

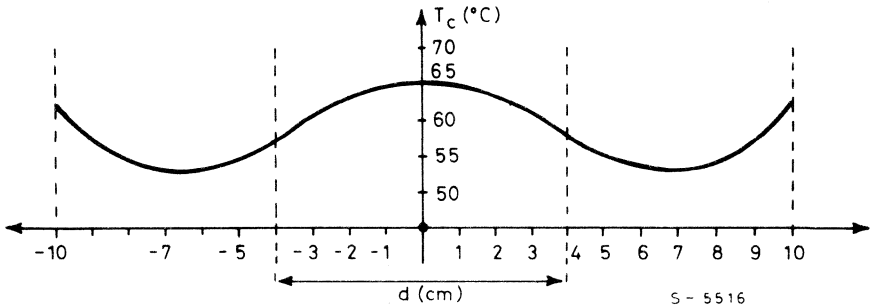
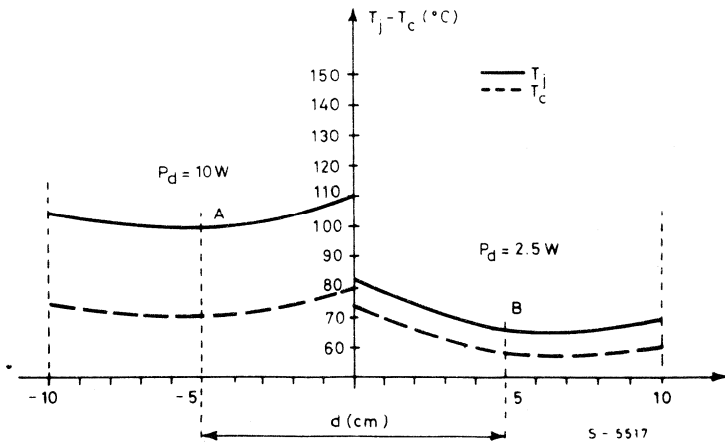


Fig. 52



APPENDIX A: CALCULATING SYSTEM STABILITY

This section is intended to help the designer in the calculation of the stability of the whole system.

Figure A1 shows the entire control system of the switching regulator.

The problem which arises immediately is the transfer function of the PWM block and output stage, which is non-linear. If this function can be considered linear the analysis is greatly simplified.

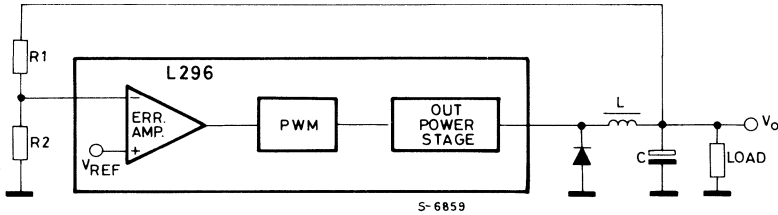
Since the circuit operates at a constant frequency and the internal logic is fairly fast, the error introduced by assuming that this function is linear is minimized. Factors which could contribute to the non-linearity are an excessive delay in the output power transistor, ringing and parasitic oscillations

generated in the power stage and non-linearity introduced by magnetic part.

In the case of the L296, in which the power transistor is internal and driven by well-controlled and efficient logic, the contribution to non-linearity is further reduced.

For the assumption of linearity to be valid the cut-off frequency of the LC filter must be much lower than the switching frequency. In fact, switching operation introduces singularities (poles) at roughly half the switching frequency. Consequently, as long as the LC filter is still dominant, its cut-off frequency must be at least an order of magnitude lower than the switching frequency. This condition is not, however, difficult to respect. The characteristics of LC filter affect the output voltage waveforms; is generally much less than an order of magnitude below the switching frequency.

Fig. A1 — The control loop of the switching regulator.



GAIN OF THE PWM BLOCK AND OUTPUT STAGE

The equation which links V_O to V_i is:

$$V_O = V_i \frac{T_{ON}}{T}$$

A variation ΔT_{ON} in the conduction time of the switching transistor causes a corresponding variation in the output voltage, ΔV_O , giving:

$$\frac{\Delta V_O}{\Delta T_{ON}} = \frac{V_i}{T}$$

Indicating with V_r the output voltage of the error amplifier, and with V_{ct} the amplitude of the ramp (the difference between the maximum and minimum values), T_{ON} is zero when V_r is at the minimum value and equal to T when V_r is at a maximum. Consequently:

$$\frac{\Delta T_{ON}}{\Delta V_r} = \frac{T}{V_{ct}}$$

The gain is given by:

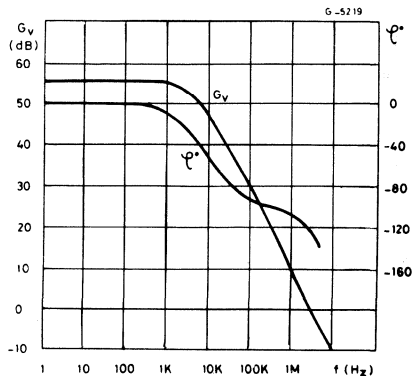
$$\frac{\Delta V_O}{\Delta V_r} = \frac{V_i}{V_{ct}}$$

Since V_{ct} is absolutely constant the gain of the PWM block is directly proportional to the supply voltage V_i .

ERROR AMPLIFIER

The error amplifier is a transconductance amplifier (it transforms a voltage variation at the input into a current variation at the output). It is used in open loop configuration inside the main control loop and its gain and frequency response are determined by a compensation network connected between its output and ground.

Fig. A2 — Open loop frequency and phase response of error amplifier.



In the application a series RC network is recommended which gives high system gain at low frequency – to ensure good precision and mains ripple rejection and a lower gain at high frequencies to ensure stability of the system. Figure A2 shows the gain and phase curves of the uncompensated error amplifier.

The amplifier has one pole at about 7 kHz and a phase shift which reaches about -90° at frequencies around 1 MHz.

The introduction of a series network $R_C C_C$ between the output and ground modifies the circuit as shown in figure A3.

Figure A4 shows the gain and phase curves of the compensated error amplifier.

Fig. A3 – Compensation network of the error amplifier.

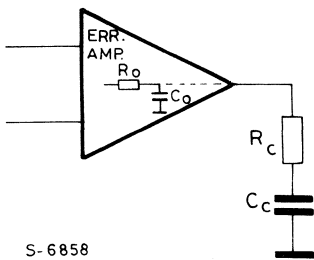
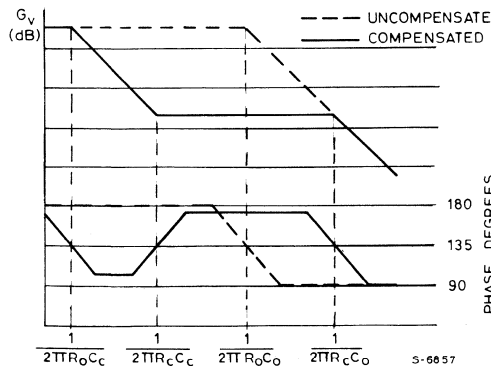


Fig. A4 – Bode plot showing gain and phase of compensated error amplifier.



CALCULATING THE STABILITY

For the stability calculation refer to the block diagram shown in figure A5.

The transfer functions of the various blocks are rewritten as follows.

The simplified transfer function of the compensated error amplifier is:

$$G_{EA} = g_m Z_C = g_m \frac{1 + s R_C C_C}{s C_C} \quad (g_m = \frac{1}{2500})$$

The DC gain must be considered equal to

$$A_o = g_m R_o$$

PWM block and output stage:

$$G_{PWM} = \frac{V_i}{V_{ct}}$$

LC FILTER:

$$G_{LC} = \frac{1 + s C \cdot ESR}{s^2 LC + s C ESR + 1}$$

where ESR is the equivalent series resistance of the output capacitor which introduces a zero at high frequencies, indispensable for system stability. Such a filter introduces two poles at the angular frequency.

$$\omega_o = \frac{1}{\sqrt{LC}}$$

Refer to the literature for a more detailed analysis.

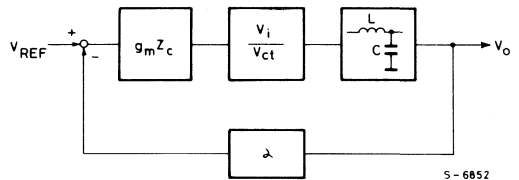
Feedback: consists of the block labelled α

$\alpha = 1$ when $V_o = V_{REF}$ (and therefore $V_o = 5.1V$)

and

$$\alpha = \frac{R_2}{R_1 + R_2} \quad \text{when } V_o > V_{REF}$$

Fig. A5 – Block diagram used in stability calculation



To analyse the stability we will use a Bode diagram. The values of L and C necessary to obtain the required regulator output performance, once the frequency is fixed, are calculated with the following formulae:

$$L = \frac{(V_i - V_o) V_o}{V_i f \Delta I_L}$$

$$C = \frac{(V_i - V_o) V_o}{8 L f^2 \Delta V_o}$$

Since this filter introduces two poles at the angular frequency

$$\omega_o = \frac{1}{\sqrt{LC}}$$

we place the zero of the $R_C C_C$ network in the same place:

$$\omega_z = \frac{1}{R_C C_C}$$

Taking into account also the gain of the PWM block, the Bode plot of figure A6 is obtained.

The slope where the curve crosses the axis at 0 dB is about 40dB/decade therefore the circuit is unstable.

Taking into account now the zero introduced by the equivalent series resistance (ESR) of the output capacitor, we have further condition for dimensioning the $R_c C_c$ network. Knowing the ESR (which is supplied by the manufacturer for the quality components) we can determine the value of R_c so that the axis is crossed at 0dB with a single slope. The zero introduced by the ESR is at the angular frequency:

$$\omega_{zESR} = \frac{1}{ESR \cdot C}$$

The overall Bode diagram is therefore as shown in figure A7.

Fig. A6 — Bode plot of system taking filter and compensation network into account.

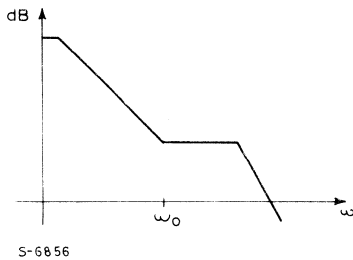
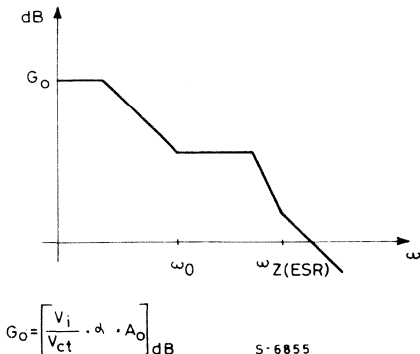


Fig. A7 — Bode plot of complete system taking into consideration the equivalent series resistance of the output capacitor.



$$G_0 = \left[\frac{V_i}{V_{ct}} \cdot d \cdot A_0 \right] \text{dB}$$

DC GAIN AND LINE REGULATION

Indicating the open-loop gain of the error amplifier with A_o , the overall open-loop gain of the system is:

$$A_t = A_o \frac{V_i}{V_{ct}} \cdot \frac{R_2}{R_1 + R_2}$$

When $V_o = V_{REF}$, the gain becomes:

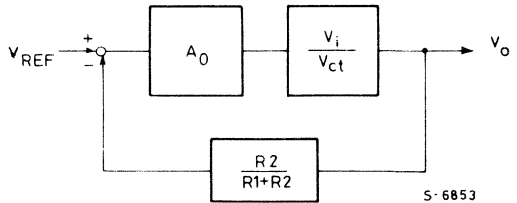
$$A_t = A_o \frac{V_i}{V_{ct}}$$

Considering the block diagram of figure A8 and calculating the output variation ΔV_o caused by a variation of V_i , from the literature we obtain:

$$\frac{\Delta V_o}{V_o} = \frac{\frac{\Delta V_i}{V_i}}{\frac{A_o V_i}{V_{ct}} \cdot \frac{R_2}{R_1 + R_2}}$$

This expression is of general validity. In our case the percentage variation of the reference must be added by vector addition.

Fig. A8 — Block diagram for calculation of line regulation.



APPENDIX B: REDUCING INTERFERENCE

The main disadvantage of the switching technique is the generation of interference which can reach levels which cause malfunctions and interfere with other equipment.

For each application it is therefore necessary to study specific means to reduce this interference within the limits allowed by the appropriate standards.

Among the main sources of noise are the parasitic inductances and capacitances within the system which are charged and discharged fastly. Parasitic capacitances originate mainly between the device case and the heatsink, the windings of the inductor and the connection wires. Parasitic inductances are

generally found distributed along the strips of the printed circuit board.

Fast switching of the power transistors tends to cause ringing and oscillations as a result of the parasitic elements. The use of a diode with a fast reverse recovery time (t_{rr}) contributes to a reduction in the noise flowing by the current peak generated when the diode is reverse biased.

Radiated interference is usually reduced by enclosing the regulator in a metal box.

To reduce conducted electromagnetic interference (or radio frequency interferences — RFI) to the levels permitted a suitably dimensioned filter is added on the supply line. The best method, generally, to reduce conducted noise is to filter each output terminal of the regulator. The use of a fixed switching frequency allows the use of a filter with a relatively narrow bandwidth. For off-line switching regulators this filter is usually costly and bulky. In contrast, if the device is supplied from a 50/60 Hz transformer the RFI filter problem is greatly reduced.

Tests have been carried out at the laboratories of Roederstein to determine the dimensions of a mains supply filter which satisfies the VDE 0871/6.78, class B standard. The measurements (see figs. B1 and B2) refer to the application with the L296 supplied with a filtered secondary voltage of about 30V, with $V_o = 5.1V$ and $I_o = 4A$. The switching frequency is 100 kHz.

Figure B1 shows the results obtained by introducing on the transformer primary a $0.01 \mu F/250V \sim$ class X capacitor (type ERO F1772-310-2030). To reduce interference further below the limit set by the standards an additional inductive filter must be added on the primary of the transformer.

Figure B2 shows the curves obtained by introducing this inductive filter (type ERO F1753-210-124).

Measurements have also been performed beyond 30 MHz; the maximum value measured is still well below the limit curve.

Fig. B1 — EMI measurements with a capacitor connected across the primary transformer with screen grounded (A) and floating (B)

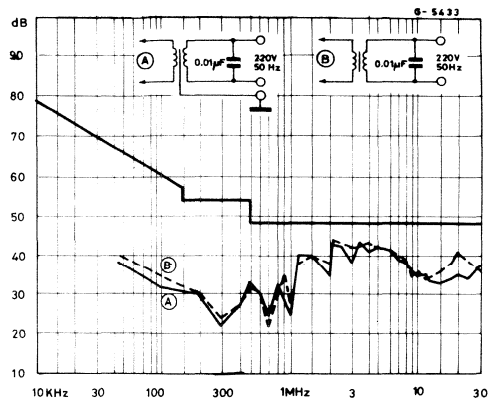
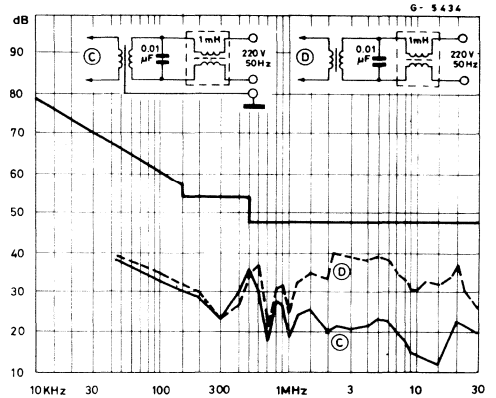
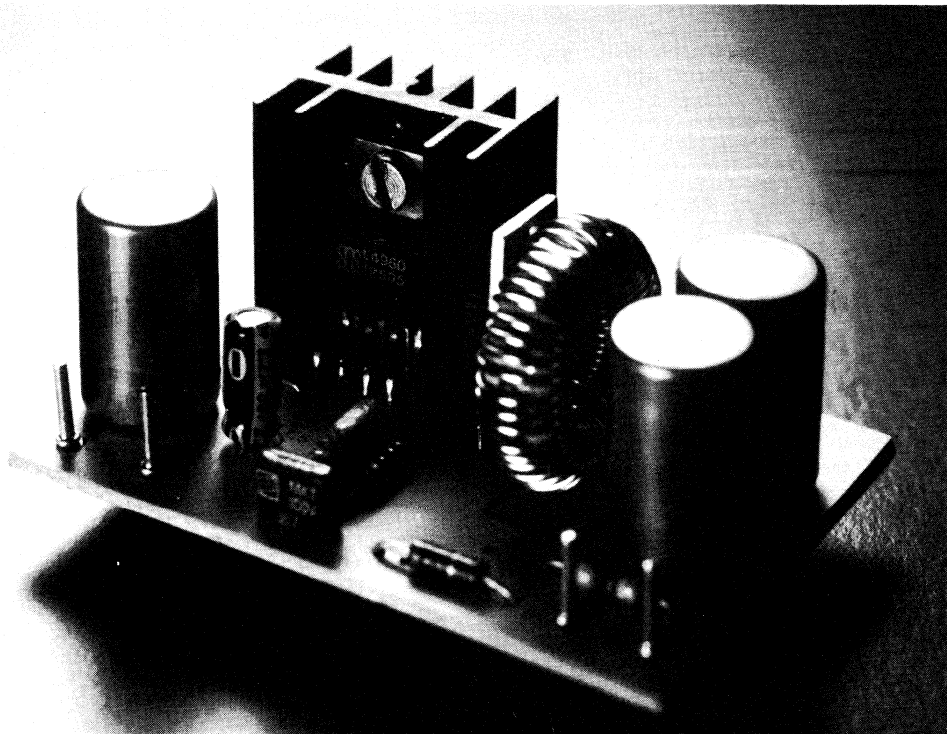


Fig. B2 — EMI results with the addition of an inductive filter on the mains input.



DESIGNING MULTIPLE-OUTPUT POWER SUPPLIES WITH THE L296 AND L4960

Multiple output supplies can be realized simply and economically using the SGS L296 and L4960 high power switching regulators. This note describes several practical circuits of this type.



Most of the switching regulators produced today have multiple outputs. The output voltages most frequently used – at least for powers up to 50W – are +5V, -5V, +12V and -12V. In these supplies the 5V output is normally the output which delivers the highest current and requires the highest precision. For the other voltages – particularly the negative outputs – less precision ($\pm 5\%$ to $\pm 7\%$) is usually sufficient. Often, however, for high current 12V outputs better stabilization and greater precision (typically $\pm 4\%$ – the output tolerance of an L7800 series linear regulator) are required.

Multiple output supplies which satisfy these requirements can be realized using the SGS L296 and L4960 high power switching regulator ICs. Several practical supply designs are described below to illustrate how these components are used to build compact and inexpensive multi-output supplies.

DUAL OUTPUT 15W SUPPLY

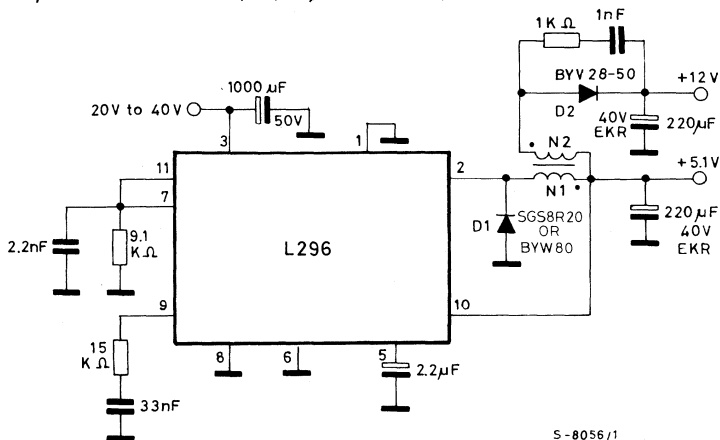
$V_{O1} = 5V/3A$, $V_{O2} = 12V/150mA$

A single L296 is used in this application to produce two outputs. The application circuit, Figure 1, illustrates how the second output (12V) is obtained by adding a second winding to the output inductor. Energy is transferred to the secondary during the recirculation period when the internal power device of the L296 is OFF.

Since the 12V output is not separated from the 5V output fewer turns are necessary for the second winding, therefore less copper is needed and load regulation is improved.

In applications of this type it is a good rule to ensure that the power drain on the auxiliary output is no more than 20-25% of the power delivered by the main output.

Fig. 1 - Dual output DC-DC converter (5V/3A, 12V/150mA)



Transformer: magnetics 58930, N1 = 30 turns, N2 = 40 turns

Table 1 shows the performance obtained with this dual output supply. This circuit operates at a switching frequency of 50KHz.

TABLE 1

Parameter		V _{O1}	V _{O2}	Unit
Output voltage I _{O1} = 3A	V _i = 30V I _{O2} = 150mA	5.120	12.089	[V]
Output ripple		70	40	[mV]
Line regulation I _{O1} = 3A	20V ≤ V _i ≤ 40V I _{O2} = 150mA	15	30	[mV]
Line regulation I _{O1} = 700mA	20V ≤ V _i ≤ 40V I _{O2} = 100mA	15	10	[mV]
Load regulation I _{O1} = 700mA → 3A	V _i = 30V I _{O2} = 150mA	10	130	[mV]
Load regulation I _{O1} = 700mA	V _i = 30V I _{O2} = 100 → 150mA	0	40	[mV]
Load regulation I _{O1} = 3A	V _i = 30V I _{O2} = 100 → 150mA	0	40	[mV]
Efficiency	V _i = 30V V _{O1} = 5.120V I _{O1} = 3A V _{O2} = 12.089V I _{O2} = 150mA	75		%

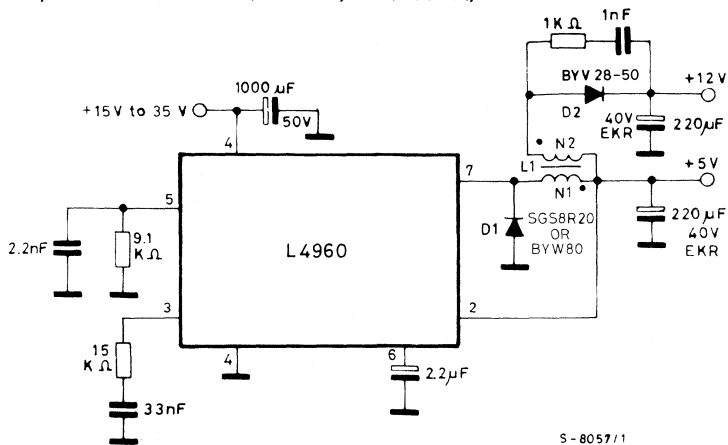
DUAL OUTPUT 7.5W SUPPLY

$$V_{O1} = 5V/1.5A, \quad V_{O2} = 12V/100mA$$

The same technique - adding a secondary winding - can also be used to produce an economical and

simple dual output supply with the L4960, a device containing the same control loop blocks as the L296 and a 2A output stage. (Fig. 2). Though this circuit costs very little the performance obtained (see Table 2) is more than satisfactory. The switching frequency is 50kHz.

Fig. 2 - Dual output DC-DC converter (5V/1.5A, 12V/100mA)



Transformer: magnetics 58206, $N_1 = 30$ turns, $N_2 = 40$ turns

TABLE 2

Parameter		V _{O1}	V _{O2}	Unit
Output voltage I _{O1} = 1.5A	V _i = 25V I _{O2} = 100mA	5.050	12.010	[V]
Output ripple		50	30	[mV]
Line regulation I _{O1} = 1.5A	15V ≤ V _i ≤ 35V I _{O2} = 100mA	7	75	[mV]
Line regulation I _{O1} = 500mA	15V ≤ V _i ≤ 35V I _{O2} = 50mA	7	60	[mV]
Load regulation I _{O1} = 0.5A → 1.5A	V _i = 25V I _{O2} = 100mA	3	100	[mV]
Load regulation I _{O1} = 500mA	V _i = 25V I _{O2} = 50mA → 100mA	0	55	[mV]
Load regulation I _{O1} = 1.5A	V _i = 25V I _{O2} = 50mA → 100mA	0	50	[mV]
Efficiency	V _i = 25V I _{O1} = 1.5A I _{O2} = 100mA	78		%

TRIPLE OUTPUT 15W SUPPLY

$$V_{O1} = 5V/3A, V_{O2} = 12V/100mA, V_{O3} = -12V/100mA$$

Figure 3 shows how to obtain two auxiliary outputs ($\pm 12V$) which are isolated from the 5V output. For this output power range an L296 is

used,

To ensure good tracking of the 12V and -12V outputs the secondary outputs in this application should be bifilar wound.

This circuit operates at 50KHz and gives the performance indicated in Table 3.

Fig. 3 - Triple output DC-DC converter (5V/3A, 12V/100mA, -12V/100mA)

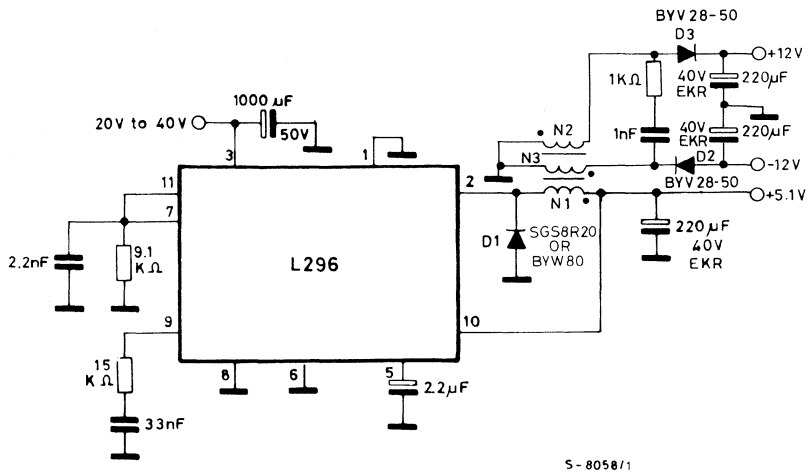


TABLE 3

Parameter	V_{O1}	V_{O2}	V_{O3}	Unit
Output Voltage $I_{O1} = 3A$ $V_i = 30V$ $I_{O2} = I_{O3} = 100mA$	5.057	12.300	-12.300	[V]
Output ripple	80	30	30	[mV]
Line regulation $I_{O1} = 700mA$ $20 \leq V_i \leq 40V$ $I_{O2} = I_{O3} = 100mA$	15	60	60	[mV]
Line regulation $I_{O1} = 3A$ $20 \leq V_i \leq 40V$ $I_{O2} = I_{O3} = 100mA$	18	100	100	[mV]
Load regulation $I_{O1} = 0.7 \rightarrow 3A$ $V_i = 30V$ $I_{O2} = I_{O3} = 100mA$	4	150	150	[mV]
Load regulation $I_{O1} = 3A$ $V_i = 30V$ $I_{O2} = 100mA$ $I_{O3} = 50 \rightarrow 100mA$	0	125	52	[mV]
Load regulation $I_{O1} = 3A$ $V_i = 30V$ $I_{O3} = 100mA$ $I_{O2} = 50 \rightarrow 100mA$	0	50	120	[mV]
Efficiency	76			%

TRIPLE OUTPUT 7.5W SUPPLY

$V_{O1} = 5V/1.5A$, $V_{O2} = 12V/50mA$, $V_{O3} = -12V/50mA$

For lower output powers, the L296 in the previous application may be replaced by an L4960 as shown in Figure 4. The performance of this circuit is indicated in Table 4.

Fig. 4 - Triple output DC-DC converter (5V/1.5A, 12V/50mA, -12V/50mA)

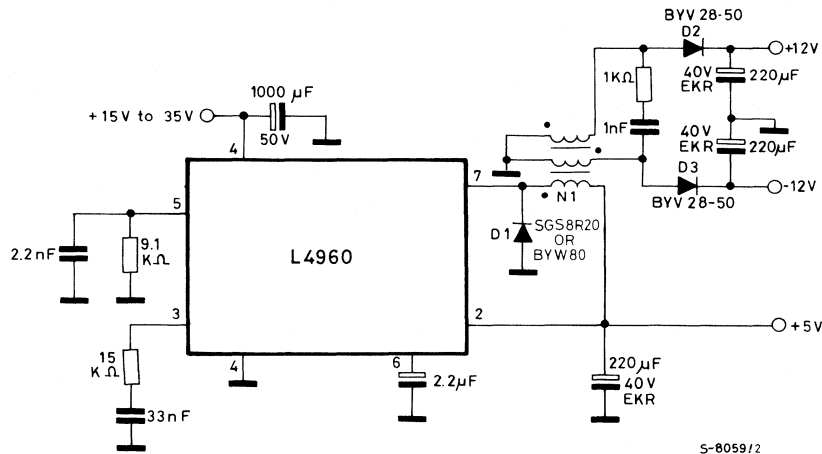


TABLE 4

Parameter		V _{o1}	V _{o2}	V _{o3}	Unit
Output Voltage I _{o1} = 1.5A	V _i = 25V I _{o2} = I _{o3} = 50mA	5.040	12.020	-12.020	[V]
Output ripple		60	30	30	[mV]
Line regulation I _{o1} = 500mA	15 ≤ V _i ≤ 35V I _{o2} = I _{o3} = 50mA	5	80	80	[mV]
Line regulation I _{o1} = 1.5A	15 ≤ V _i ≤ 35V I _{o2} = I _{o3} = 50mA	4	60	60	[mV]
Load regulation I _{o1} = 0.5 → 1.5A	V _i = 25V I _{o2} = I _{o3} = 50mA	5	120	120	[mV]
Load regulation I _o = 1.5A I _{o3} = 20 → 50mA	V _i = 25V I _{o2} = 50mA	0	15	50	[mV]
Load regulation I _{o1} = 1.5A I _{o2} = 20 → 50mA	V _i = 25V I _{o3} = 100mA	0	50	15	[mV]
Efficiency		70			%

THE L296 AND L4960 HIGH POWER SWITCHING REGULATORS

The SGS L296 is a monolithic stepdown switching regulator assembled in the 15-pin Multiwatt package. Operating with supply input voltages up to 46V it provides a regulated 4A output variable from 5.1V to 40V.

Internally the device is equipped with current limiter, soft start and reset (or power fail) functions, making it particularly suitable for supplying microprocessors and logic.

The precision of the L296's internal reference ($\pm 2\%$) eliminates the need for external dividers or trimming to obtain a 5V output.

The synchronization pin allows synchronous operation of several devices at the same frequency to avoid generating undesirable beat frequencies.

The L4960 is a similar device assembled in the 7-lead Heptawatt package. Like the L296 it has a maximum input voltage of 46V and it provides a regulated output voltage variable from 5V to 40V with a maximum load current of 2.5A. Current limiting, soft start and thermal protection functions are included.

The thermal protection circuit in both the L296 and L4960 has a hysteresis of 30°C to allow soft restarting after a fault condition.

THE STEP DOWN CONFIGURATION

Figure 5 shows the basic structure of a step down switching regulator. The transistor Q is used as a switch and the ON and OFF times are determined by the control circuit.

When Q is saturated current flows from the supply, V_i , to the load through the inductor L. Neglecting the saturation voltage of Q, $V_e \approx V_i$.

When Q is OFF, current continues to flow in the inductor L, in the same direction, forcing the diode into conduction immediately therefore V_e is negative. In these conditions the load current flows through L and D.

The average value of the current in the inductor is equal to the load current. In the inductor a triangular current ripple equal to ΔI_L is added to this average current.

During the time when Q is ON this ripple is :

$$\Delta I_L = \frac{(V_i - V_o) T_{ON}}{L}$$

and when Q is off it is:

$$\Delta I_L = \frac{V_o \cdot T_{OFF}}{L}$$

Equating these expression and assuming that the transistor and diode are ideal we obtain :

$$V_o = V_i \cdot \frac{T_{ON}}{T} \quad \begin{array}{l} T_{ON} \text{ is the conduction time} \\ \text{of the transistor} \end{array}$$

T is the oscillator period

The absolute average current in the supply is therefore :

$$I_{ioc} = I_o \cdot \frac{T_{ON}}{T}$$

Once the working frequency and desired ripple current have been fixed the value of the inductor L is given by :

$$L = \frac{(V_i - V_o) V_o}{V_i f \Delta I_L}$$

and the value of the capacitor C required to give the desired output voltage ripple (ΔV) is :

$$C = \frac{(V_i - V_o) V_o}{8 L f^2 \Delta V_o}$$

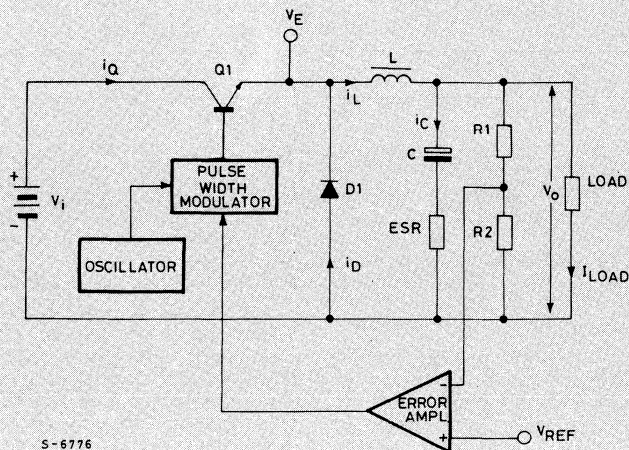
This capacitor must have a maximum ESR given by :

$$ESR_{MAX} = \frac{\Delta V_o}{\Delta I_L}$$

And, finally, the minimum load current, I_{OMIN} , must be :

$$I_{OMIN} = \frac{\Delta I_L}{2} = \frac{(V_i - V_o) V_o}{2 V_i f L}$$

Fig. 5 - Basic STEP-DOWN configuration



S-6776

30W DC-DC CONVERTER

Designing power supplies in the 30-40W range is becoming increasingly difficult because it is here that there is the greatest need to maintain performance levels and reduce costs. The application proposed here is very competitive because it exploits new ICs to reduce size, number of components and assembly costs.

This solution, the DC-DC converter, compares very favourable with off-line switching supplies in terms

of cost. DC-DC converters can, in fact, be realized even by designers with little experience and allows the convenience of working with low voltages. Off-line switching supplies are only preferable when the weight and size of the mains transformer in a DC-DC converter would be excessive.

In this circuit, figure 6 two devices are used, an L296 and an L4960. The L296 is used, to supply a 5V output with a current of 3A and the auxiliary -5V/100mA output and the L4960 is used to provide the 12V/1.5A output and the auxiliary -12V/100mA output.

Fig. 6 - Multioutput DC-DC converter with L296 and L4960 (5V/3A, 12V/1.5A, -12V/100mA, -5V/100mA)

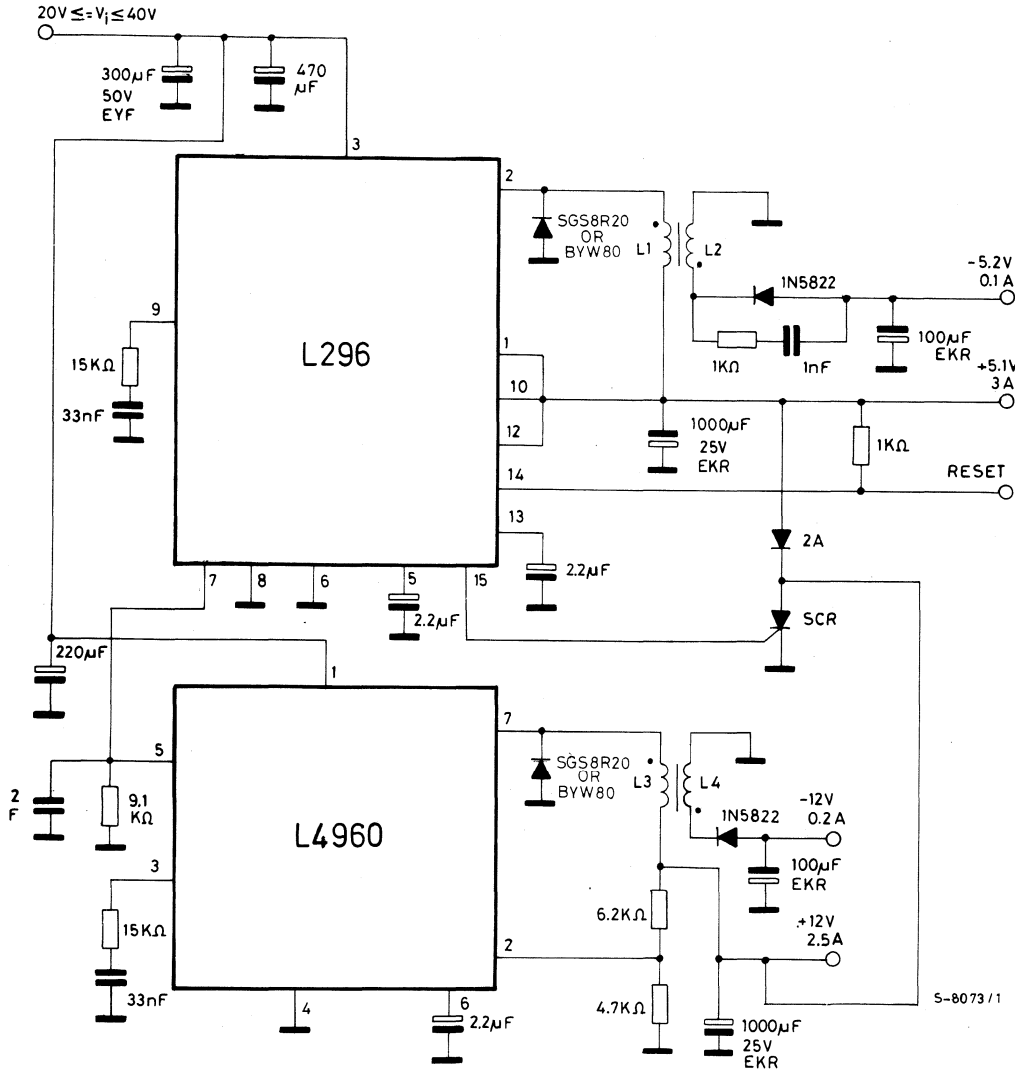


Table 5 shows the performance obtained with this power supply.

TABLE 5

Parameter		V _{O1}	V _{O2}	V _{O3}	V _{O4}	Unit
Output Voltage I _{O1} = 3A I _{O2} = 100mA	V _I = 30V I _{O3} = 1.5A I _{O4} = 100mA	5.080	-5010	11.96	12.00	[V]
Output ripple		50	30	50	40	[mV]
Line regulation I _{O1} = 1A I _{O3} = 0.5A	20 ≤ V _I ≤ 40V I _{O2} = 100mA I _{O4} = 100mA	13	15	10	20	[mV]
Load regulation I _{O1} = 1A to 3A	V _I = 30V I _{O2} = 100mA	8	90			[mV]
I _{O3} = 0.5 to 1.5A	I _{O4} = 100mA			3	80	[mV]
Load regulation I _{O1} = 3A	V _I = 30V I _{O2} = 50 → 100mA	0	100			[mV]
I _{O3} = 1.5A	I _{O4} = 50 → 100mA			0	100	[mV]
Load regulation I _{O1} = 1A	V _I = 30V I _{O2} = 50 → 100mA	0	35			[mV]
I _{O3} = 0.5A	I _{O4} = 50 → 100mA			0	90	[mV]
Line regulation I _{O1} = 3A	20 ≤ V _I ≤ 40V I _{O2} = 100mA	15	45			[mV]
I _{O3} = 1.5A	I _{O4} = 100mA			15	40	[mV]

This application illustrates how two devices may be synchronized. Note also that the reset circuit is used in this case to monitor the output voltage (see figure 7).

If a power fail function is required in place of the reset function the Figure 6 circuit should be modified as shown in Figure 8.

Fig. 7 - Reset output waveforms

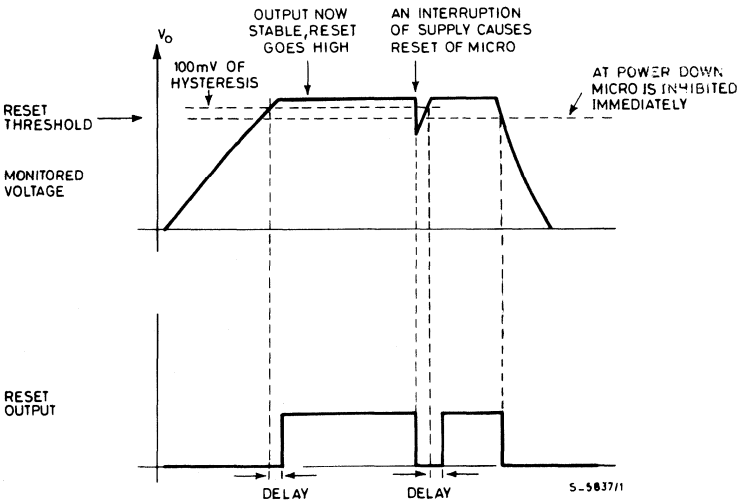
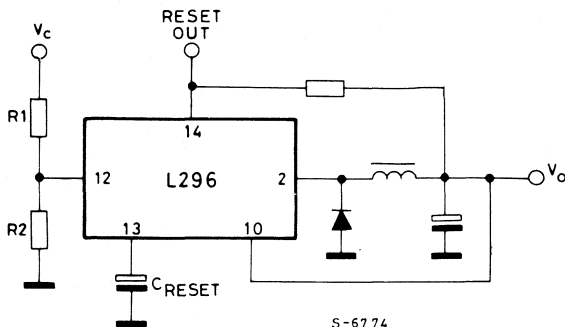


Fig. 8

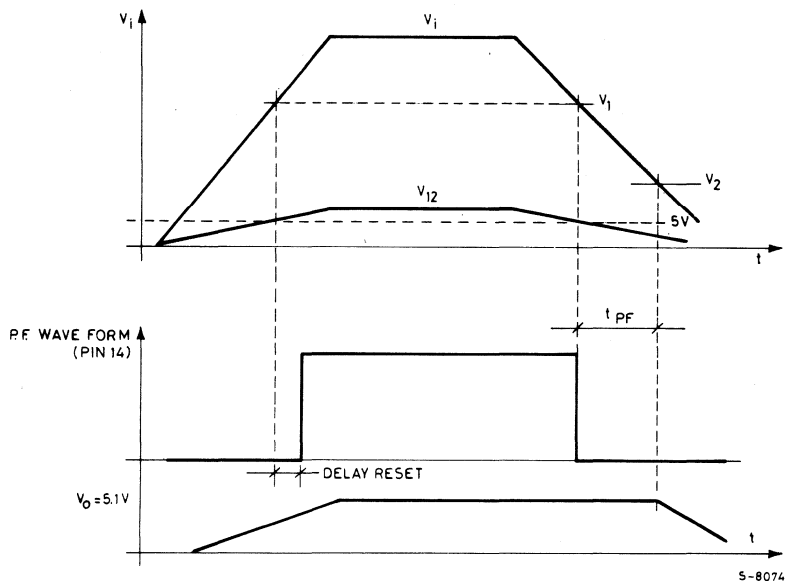


CALCULATING THE POWER FAIL TIME

The 'power fail time' is defined as the time from when the power fail output (pin 14) goes low to

the time when the input voltage falls to the minimum level required to maintain the regulated output (see Figure 9). From this definition we can evaluate the energy balance.

Fig. 9



The energy which the filter capacitor C supplies to the operating device while it discharges is:

$$E = 1/2C (V_1^2 - V_2^2) \quad (1)$$

The load drains a power of $P_o = V_o I_o$. Taking into consideration the average efficiency η (derived with the input between V_1 and V_2), the power to be supplied at the input of the device is:

$$P_{o2} = \frac{P_o}{\eta}$$

Equating the expressions (1) and (2) gives:

$$1/2C (V_1^2 - V_2^2) = \frac{P_o}{\eta} \cdot t_{PF}$$

where V_1 is the input voltage at which the voltage on pin 12 reaches 5V (through the divider R_1/R_2); V_2 is the maximum input voltage below which the device no longer regulates.

Rearranging this expression to obtain C:

$$(2) \quad C = \frac{2 P_o t_{PF}}{\eta (V_1^2 - V_2^2)}$$

EXAMPLE - Suppose that $V_o = 5V$, $I_o = 3A$, $T_{pf} = 10ms$ and $V_1 = 35V$. Fixing $V_1 = 25V$ and $V_2 = 10V$ we obtain:

$$C = \frac{2 P_o t_{PF}}{\eta (V_1^2 - V_2^2)} = \frac{2 \times 15 \times 10^{-3}}{0.75 (25^2 - 10^2)} = 760\mu F$$

We therefore choose a capacitor of $1000\mu F$.

CROWBAR

The L296 includes an internal crowbar function; the only external component needed is an SCR. The intervention threshold of this block is fixed internally at $\pm 20\%$ of the nominal value of the internal reference.

In the Figure 6 circuit the SCR is triggered by an overvoltage on the 5V output (usually the most important output to monitor) and shortcircuits to ground the 5V output and, through the diode which connects the two outputs, the 12V output.

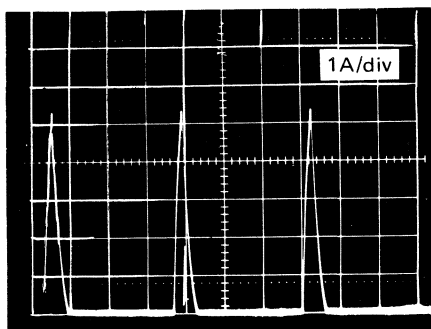
Since the internal current limiter in the device is designed to function as shown in Figure 10 (that is, with pulsed output current) the SCR turns off in the gap between pulses and is re-activated gain if, when the device restarts softly, the fault condition has not been eliminated. But if the fault no longer exists the SCR remains OFF and the output voltage returns to the normal value.

If the designer prefers the supply to remain off after the SCR has been activated the circuit can be modified as shown in Figure 11. In this modification, when the SCR is triggered a very high current flows in the fuse, blowing it.

Since the filter capacitor can have a high value and be charged to high voltages the choice of SCR is important. The type used in this circuit - the TYP512 - is a plastic packaged SCR able to handle 12Arms and 300A for 10ms. The maximum forward and reverse voltages are about 50V.

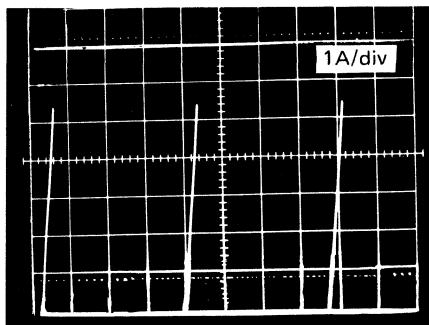
If the crowbar circuit is not used it is advisable to connect pin 1 to ground or pin 10.

Figs 10- Load current in short circuit conditions ($V_i = 40V$, $L = 300\mu H$, $f = 100KHz$)



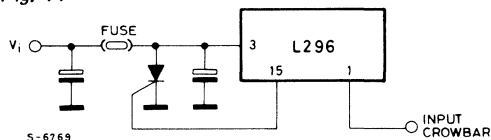
t: 5ms/div

Current at pin 2 when the output is short circuited.



t: 5ms/div

Fig. 11



DUAL REGULATORS SIMPLIFY MICRO SYSTEM SUPPLY DESIGN

Combining two 5V regulators and a reset circuit on a single chip, special purpose regulator chips simplify the design of power supplies for microprocessor systems incorporating battery backup RAMs or shadow-type NV RAMs.

Power supplies for microprocessor systems are often complicated by the need to take care of the special requirements of non-volatile read/write memory. Where battery backup CMOS RAMs are used, for example, it is important to ensure that the RAMs are disabled when the primary supply is removed. And when shadow-type NV memory is included the backup transfer must be initiated and completed when the supply is interrupted. Designed specifically for such applications, the SGS L4901, and L4902 dual voltage regulators combine two 5V regulators plus a reset circuit on a single chip, simplifying the designer's task.

Assembled in the SGS Heptawatt [TM] 7-lead package, the L4901 and L4902 contain separate voltage regulators rated at 5V/300mA (the "V1" output) and 5V/400mA (the "V2" output).

Both the V1 and V2 regulators have an output voltage precision of $\pm 2\%$ and include protection against output short circuits and 60V input transients. Also included on the chip is a reset circuit

with externally programmable timing which depends on the input voltage and the output of the V1 regulator.

Functionally, the two devices are identical except that the L4901 has separate inputs to the two regulators and the L4902 has a common input plus a disable input which controls the V2 output. (Fig. 1)

Generally the V1 regulator is used to supply circuits which must be powered continuously — volatile memory, a time-of-day clock and so on — while the V2 output supplies other 5V circuits which may be powered down when the equipment is inactive.

The V1 output features a very low leakage current at the output — less than $1\mu\text{A}$ — to allow the use a backup battery. The V1 regulator also features a low quiescent current at the input (0.6mA typical) to minimize battery drain in applications where the V1 regulator is permanently connected to a battery supply.

Fig. 1a - TWO 5V OUTPUTS — The L4901 Dual Regulator provides 300mA and 400mA 5V outputs and includes a microprocessor reset function. This device is ideal for microprocessor systems with battery backup or shadow RAM.

Fig. 1b - DISABLE INPUT — The L4902 is similar to the L4901 but also features a disable input for the V2 regulator.

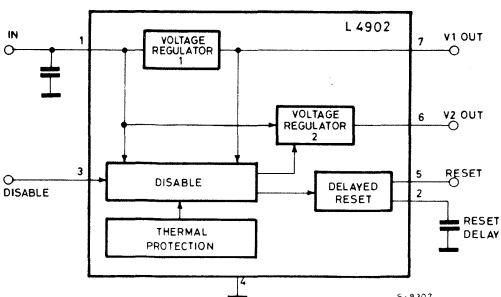
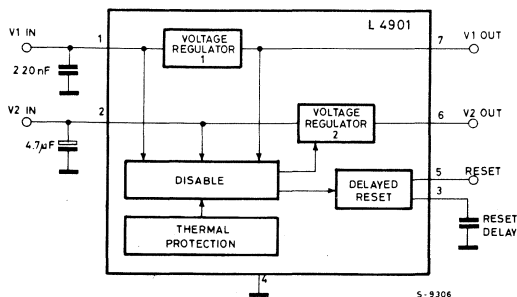
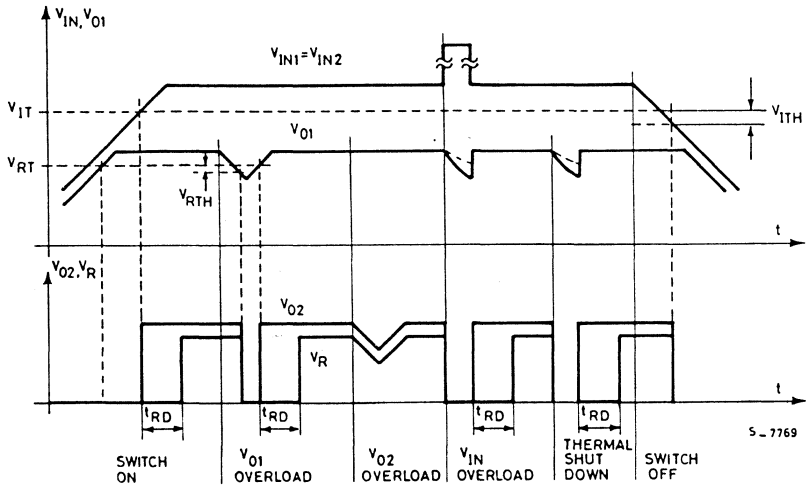


Fig. 2 - WAVEFORMS — An important feature of the L4901 series regulators is that the reset circuit monitors the input voltage.



VERSATILE DEVICES

The L4901 and L4902 are versatile devices which simplify the supply circuitry of many systems and can be used in a number of different ways.

One possibility, outlined in figure 3, is to connect the V1 regulator permanently to a battery to supply a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory. In this example the V2 output supplies non-essential 5V circuits. A typical use of this scheme is in trip computers or car radios with programmable tuning.

An alternative, shown in figure 4, is to use the L4901 with a backup battery on the V1 output to maintain a CMOS clock and a standby-type NMOS microcomputer chip. In this case the main on/off switch disconnects both the V1 and V2 regulators from the battery.

Figure 5 illustrates how the L4902's disable input

may be used in a CMOS microcomputer application. In this example the V2 output, supplying non-essential circuits, is turned off under control of the microprocessor circuit. Configurations of this type are used in products where the "OFF" switch is part of a keypad scanned by a micro which operates continuously, even in the "OFF" state.

The L4901 is also ideal for microcomputer systems using battery backup CMOS static RAMs. As shows in figure 6 the V1 output supplies the CMOS RAMs and the V2 output supplies the microprocessor plus other 5V circuits. The L4901's reset output is used both to reset the Z80 and, through the M74HC138 address decoder, to ensure that the RAMs are disabled as soon as the main supply voltage starts to fall. Note that the M74HC138 is supplied from the backup battery.

Fig. 3 - LOW QUIESCENT CURRENT at the V1 input makes the L4901 useful in applications like this where the V1 regulator is always connected to the battery.

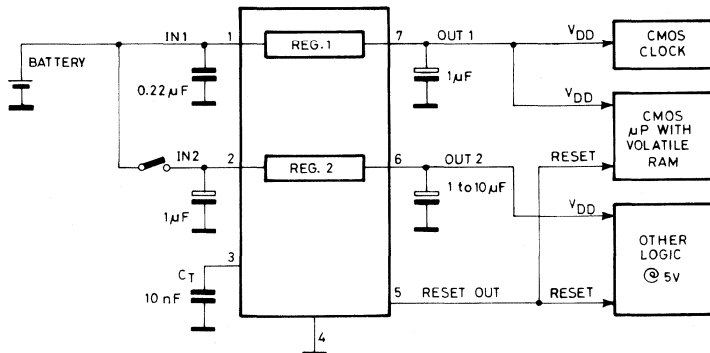


Fig. 4 - LOW LEAKAGE at the V1 output makes the L4901 ideal for battery backup operation.

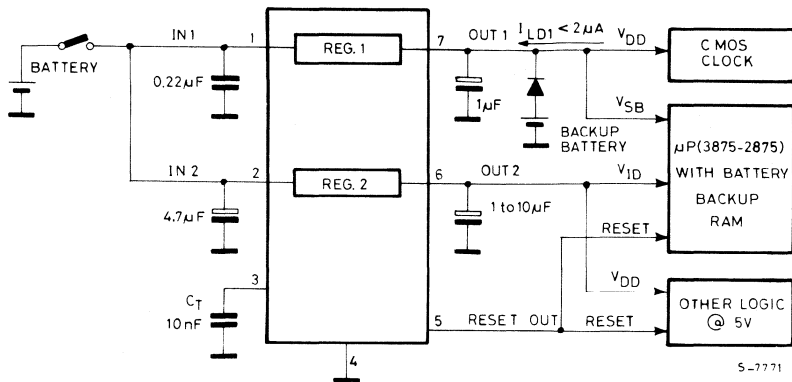
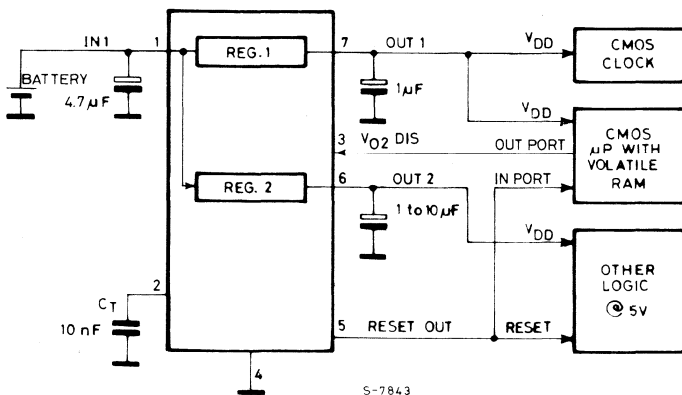


Fig. 5 - STANDBY — The L4902 can be used in applications where the supply is connected permanently and the disable function used to turn off non-essential circuits in the standby state.



It is important to make sure that the RAMs are disabled because the lithium cells used as backup batteries have a high internal resistance. If the RAMs were not forced into the low consumption standby state the battery voltage could drop so low that memory contents are corrupted. Moreover, to prevent latch up, no input of a CMOS RAM should ever be higher than the supply voltage.

IDEAL FOR SHADOW MEMORIES

Another interesting application for the L4902 is supplying a shadow-ram microcomputer chip like the SGS M38SH72 where a fast non-volatile memory is backed up on-chip by a slow EEPROM (figure 7). For these chips it is important to ensure that the backup command is generated when the

supply is removed, a function which the L4902's reset output can perform. Since the L4902's reset function depends on the INPUT voltage the power fail condition is sensed early enough to guarantee that the backup transfer will be successful.

In figure 7 the reset output is forced low when the input voltage falls below 6.3V or when the V1 output goes below 4.8V. This allows 10µs for the backup transfer (with 10µF capacitors) which is more than sufficient.

Similarly, the L4902 can be used with shadow-type RAMs such as the Xicor X2201. In the figure 8 circuit a capacitor on the V1 input ensures that the X2201 is powered during the transfer operation. When the input voltage is removed or goes below 6.3V the L4902's reset output, connected to

the 8085's TRAP input, forces the execution to a service routine which saves the state of the machine in the RAM then issues a backup command. The V2 output drops immediately while the 680μF capacitor on the V1 input provides enough energy to keep the X2201 running for the 10ms needed to complete the backup transfer. The low consumption of the V1 regulator allows the use of a relatively small capacitor for this function.

ADDING A WATCHDOG

By adding a few components and two Schmitt

trigger gates a watchdog function can be added to the L4902 (figure 9). Normally an output port of the micro will supply a software-generated pulse at least every 10ms. If something has gone wrong in the software or hardware and these pulses are missing the disable input will be activated after a period set by R1.C1, disabling all the circuitry connected to the V2 output of the L4902. The disable period could be useful to prevent spurious operation of motors and solenoids while the control processor is malfunctioning.

Fig. 6 - CMOS RAMs — The L4901 is useful in systems with battery backup CMOS RAMs because the reset output can be used to ensure that the RAM chips are disabled to reduce battery drain when the main supply is removed.

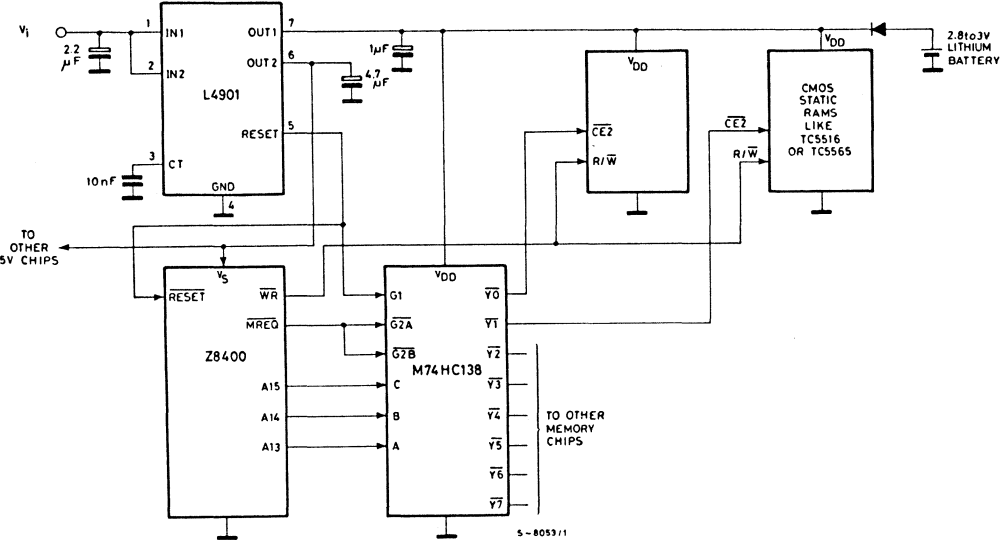


Fig. 7 - NV MEMORY μCs — The L4902 is also useful for supplying chips like the SGS M38SH72 single-chip micro with NV memory. In this application the reset circuit initiates the RAM-to-shadow transfer.

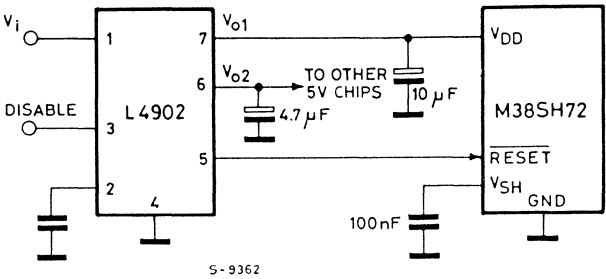


Fig. 8 - SHADOW RAMs — The L4901's reset function also serves in systems using shadow type NV RAMs like the X2201 to ensure that the backup transfer is executed correctly.

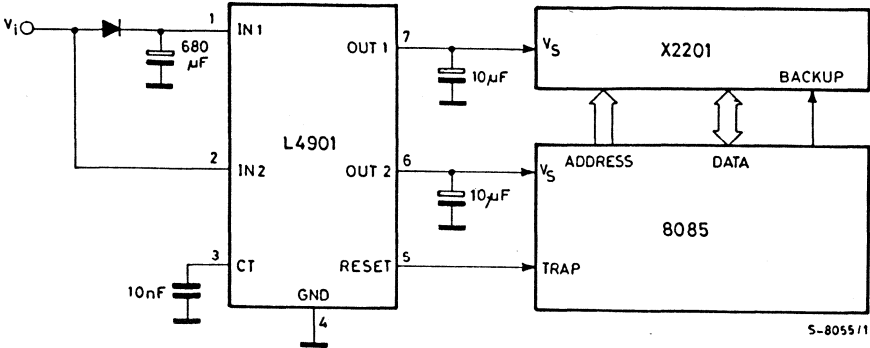
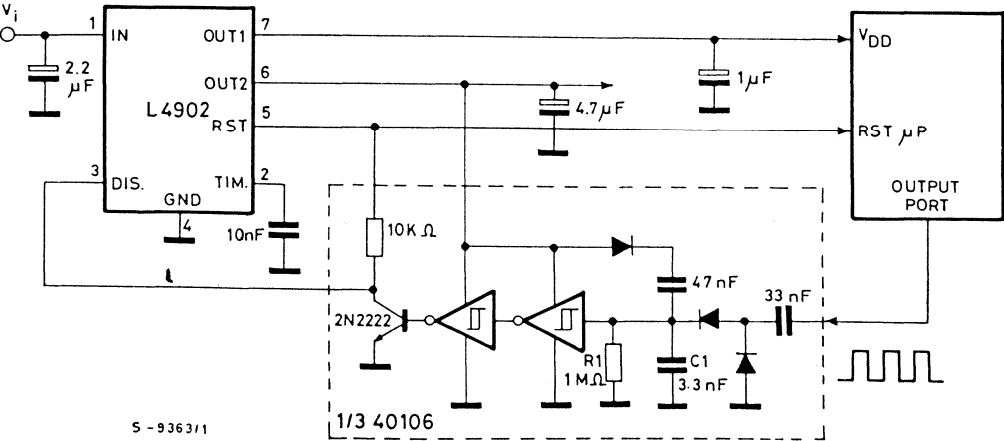


Fig. 9 - With a CMOS Schmitt trigger and a few components a watchdog function can be added for critical applications.



UC3842 PROVIDES LOW-COST CURRENT-MODE CONTROL

The fundamental challenge of power supply design is to simultaneously realize two conflicting objectives: good electrical performance and low cost. The UC3842 is an integrated pulse width modulator (PWM) designed with both these objectives in mind. This IC provides designers an inexpensive controller with which they can obtain all the performance advantages of current-mode operation. In addition, the UC3842 is optimized for efficient power sequencing of off-line converters and for driving increasingly popular POWERMOS.

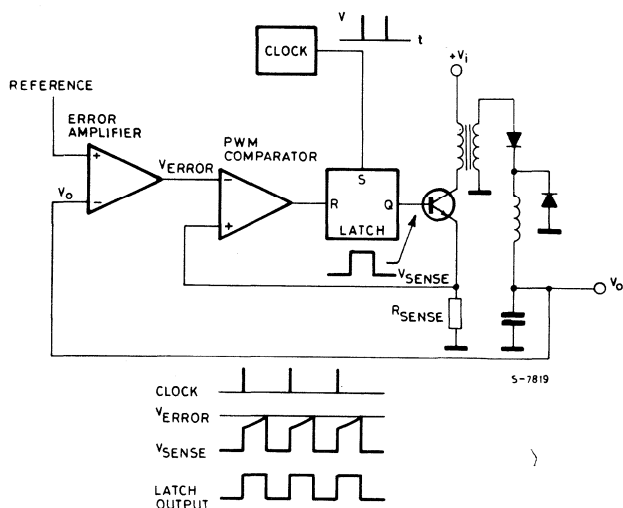
This application note gives a functional description of the UC3842 and suggests how to incorporate the IC into practical power supplies. A review of current-mode control and its benefits is included and methods of avoiding common pitfalls dis-

cussed. The final section presents designs of two power supplies utilizing UC3842 control.

CURRENT-MODE CONTROL

Figure 1 shows the two-loop current-mode control system in a typical buck regulator application. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. In this way the error signal actually controls peak inductor current. This contrasts with conventional schemes in which the error signal directly controls pulse width without regard to inductor current.

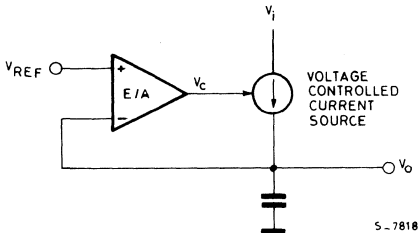
Fig. 1 - Two-loop current-mode control system



Several performance advantages result from the use of current-mode control. First, an input voltage feed-forward characteristic is achieved; i.e., the control circuit instantaneously corrects for input voltage variations without using up any of the error amplifier's dynamic range. Therefore, line regulation is excellent and the error amplifier can be dedicated to correcting for load variations exclusively.

For converters in which inductor current is continuous, controlling peak current is nearly equivalent to controlling average current. Therefore, when such converters employ current-mode control, the inductor can be treated as an error-voltage-controlled-current-source for the purposes of small-signal analysis. This is illustrated by Figure 2. The two-pole control-to-output frequency response of these converters is reduced to a single pole (filter capacitor in parallel with load) response.

Fig. 2 - Inductor looks like a current source to small signals



One result is that the error amplifier compensation can be designed to yield a stable closed-loop converter response with greater gain-bandwidth than would be possible with pulse-width control, giving the supply improved small-signal dynamic response to changing loads. A second result is that the error

amplifier compensation circuit becomes simpler and better behaved, as illustrated in Figure 3. Capacitor C_i and resistor R_{iz} in Figure 3a add a low frequency zero which cancels one of the two control-to-output poles of non-current-mode converters. For large-signal load changes, in which converter response is limited by inductor slew rate, the error amplifier will saturate while the inductor is catching up with the load. During this time, C_i will charge to an abnormal level. When the inductor current reaches its required level, the voltage on C_i causes a corresponding error in supply output voltage. The recovery time is $R_{iz} C_i$, which may be milliseconds. However, the compensation network of Figure 3b can be used where current-mode control has eliminated the inductor pole. Large-signal dynamic response is then greatly improved due to the absence of C_i .

Fig. 3 - Required error amplifier compensation for continuous inductor current designs using (a) Duty-cycle control and (b) Current-mode control.

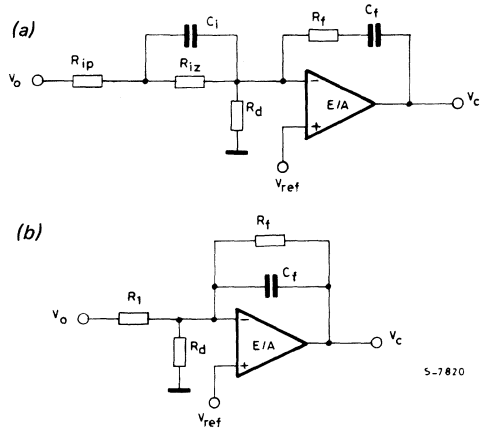
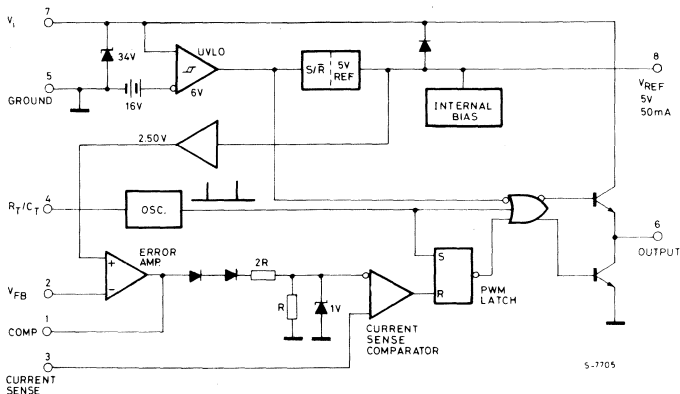


Fig. 4 - UC3842 block diagram



Current limiting is simplified with current-mode control. Pulse-by-pulse limiting is, of course, inherent in the control scheme. Furthermore, an upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

Finally, current-mode controlled power stages can be operated in parallel with equal current sharing. This opens the possibility of a modular approach to power supply design.

FUNCTIONAL DESCRIPTION

A block diagram of the UC3842 appears in Figure 4. This IC will operate from a low impedance DC source of 10V to 30V. Operation between 10V and 16V requires a start-up bootstrap to a voltage greater than 16V in order to overcome the under-voltage lockout. V_{CC} is internally clamped to 34V for operation from higher voltage current-limited sources ($I_{CC} \leq 30\text{mA}$).

Under-Voltage Lockout (UVLO)

This circuit insures that V_{CC} is adequate to make the UC3842 fully operational before enabling the output stage. Figure 5a shows that the UVLO turn-on and turn-off thresholds are fixed internally at 16V and 10V respectively. The 6V hysteresis prevents V_{CC} oscillations during power sequencing. Figure 5b shows supply current requirements. Start-up current is less than 1mA for efficient bootstrapping from the rectified input of an off-line converter, as illustrated by Figure 6. During normal circuit operation, V_{CC} is developed from auxiliary winding W_{AUX} with D_1 and C_{IN} . At start-up, however, C_{IN} must be charged to 16V through R_{IN} . With a start-up current of 1mA, R_{IN} can be as large as $100\text{k}\Omega$ and still charge C_{IN} when $V_{AC} = 90\text{V RMS}$ (low line). Power dissipation in R_{IN} would then be less than 350mW even under high line ($V_{AC} = 130\text{V RMS}$) conditions.

During UVLO, the UC3842 output driver is biased to a high impedance state. However, leakage currents (up to $10\mu\text{A}$), if not shunted to ground, could pull high the gate of a POWERMOS. A $100\text{k}\Omega$ shunt, as showing in Figure 6, will hold the gate voltage below 1V.

Fig. 5 (a) - Under-voltage lockout and (b) supply current requirements.

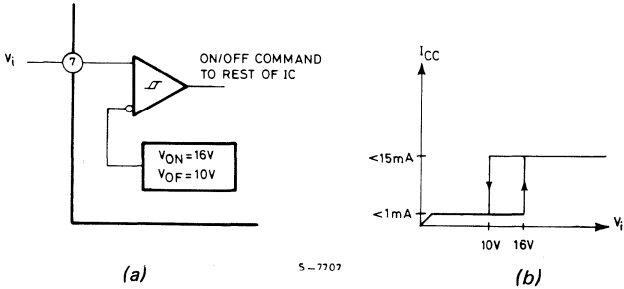
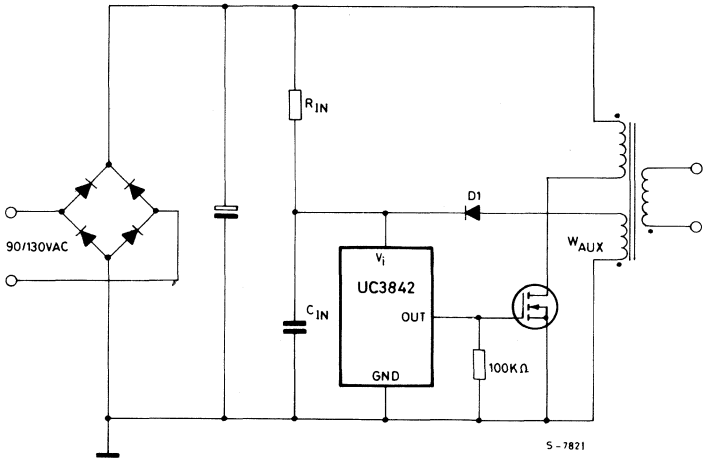


Fig. 6 - Providing power to the UC3842



Oscillator

The UC3842 oscillator is programmed as shown in Figure 7a. Oscillator timing capacitor C_T is charged from V_{REF} (5V) through R_T , and discharged by an internal current source. Charge and discharge times are given by:

$$t_c \approx 0.55 R_T C_T$$

$$t_d \approx R_T C_T \ln \left(\frac{0.0063 R_T - 2.7}{0.0063 R_T - 4.0} \right)$$

frequency, then, is: $f = \frac{1}{t_c + t_d}$

For $R_T > 5k\Omega$, t_d is small compared to t_c , and:

$$f \approx \frac{1}{0.55 R_T C_T} \approx \frac{1.8}{R_T C_T}$$

During the discharge time, the internal clock signal blanks the output to the low state. Therefore, t_d limits maximum duty cycle (D_{MAX}) to:

$$D_{MAX} = \frac{t_c}{t_c + t_d} = 1 - \frac{t_d}{\tau}$$

where: $\tau = 1/f =$ switching period.

The timing capacitor discharge current is not tightly controlled, so t_d may vary somewhat over temperature and from unit to unit. Therefore, when very precise duty cycle limiting is required, the circuit of Figure 7b is recommended.

One or more UC3842 oscillators can be synchronized to an external clock as shown in Figure 8. Noise immunity is enhanced if the free-running oscillator frequency ($f = 1/(t_c + t_d)$) is programmed to be $\sim 20\%$ less than the clock frequency.

Fig. 7 (a) – Oscillator timing connections and (b) circuit for limiting duty cycle.

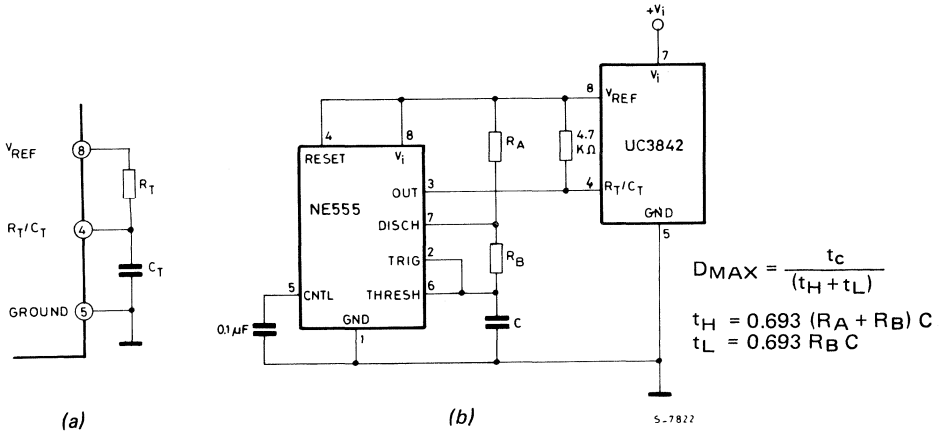
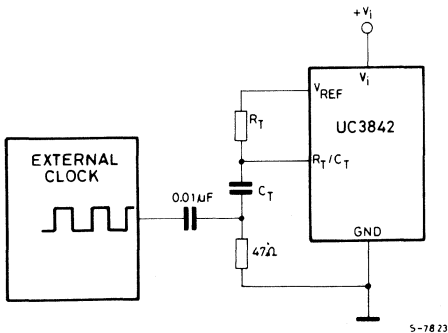


Fig. 8 – Synchronization to an external clock



Error Amplifier

The error amplifier (E/A) configuration is shown in Figure 9. The non-inverting input is not brought out to a pin, but is internally biased to $2.5V \pm 2\%$. The E/A output is available at pin 1 for external compensation, allowing the user to control the converter's closed-loop frequency response.

Figure 10a shows an E/A compensation circuit suitable for stabilizing any current-mode controlled topology except for flyback and boost converters operating with continuous inductor current. The feedback components add a pole to the loop transfer function at $f_p = 1/2\pi R_f C_f$. R_f and C_f are chosen so that this pole cancels the zero of the output filter capacitor ESR in the power circuit. R_1 and R_f fix the low-frequency gain. They are chosen to provide as much gain as possible while still allowing the pole formed by the output filter capacitor and load to roll off the loop gain to

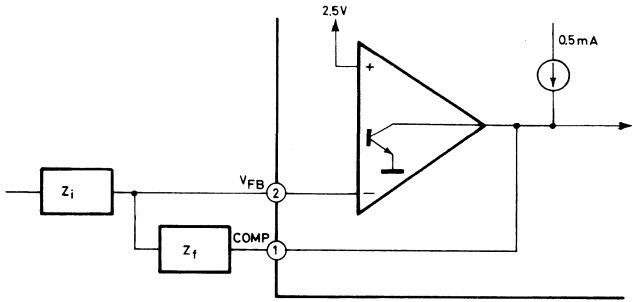
unity (0dB) at $f \approx f_{\text{switching}}/4$. This technique insures converter stability while providing good dynamic response.

Continuous-inductor-current boost and flyback converters each have a right-half-plane zero in their transfer function. An additional compensation pole is needed to roll off loop gain at a frequency less than that of the RHP zero. R_p and C_p in the circuit of Figure 10b provide this pole.

The E/A output will source 0.5mA and sink 2mA. A lower limit for R_f is given by:

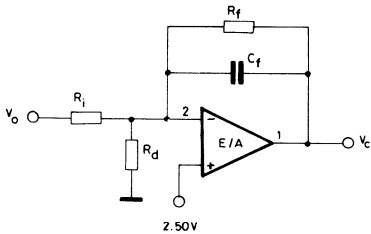
$$R_{f(\text{MIN})} \approx \frac{V_{\text{E/A OUT (MAX)}} - 2.5\text{V}}{0.5\text{mA}} = \frac{6\text{V} - 2.5\text{V}}{0.5\text{mA}} = 7\text{k}\Omega$$

Fig. 9 – UC3842 error amplifier

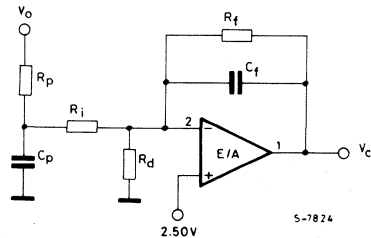


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Fig. 10- (a) Error amplifier compensation addition pole and (b) needed for continuous inductor-current boost ad flyback.



(a)



(b)

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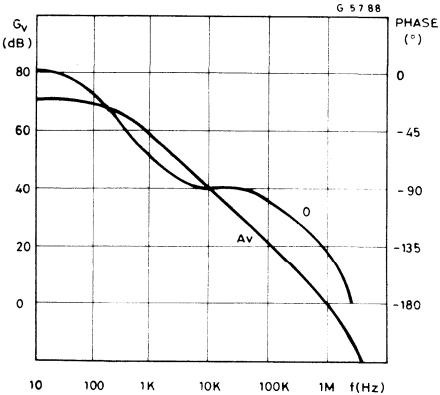
E/A input bias current ($2\mu\text{A}$ max) flows through R_i , resulting in a DC error in output voltage (V_o) given by:

$$\Delta V_o(\text{MAX}) = (2\mu\text{A}) R_i$$

It is therefore desirable to keep the value of R_i as low as possible.

Figure 11 shows the open-loop frequency response of the UC3842 E/A. The gain represent an upper limit on the gain of the compensated E/A. Phase lag increases rapidly as frequency exceeds 1MHz due to second-order poles at $\sim 10\text{MHz}$ and above.

Fig. 11 – Error amplifier open-loop frequency response



Current Sensing and Limiting

The UC3842 current sense input is configured as shown in Figure 12. Current-to-voltage conversion is done externally with ground-referenced resistor R_s . Under normal operation the peak voltage across R_s is controlled by the E/A according to

the following relation:

$$V_{R_S(pk)} = \frac{V_C - 1.4V}{3}$$

where: V_C = control voltage = E/A output voltage.

R_S can be connected to the power circuit directly or through a current transformer, as Figure 13 illustrates. While a direct connection is simpler, a transformer can reduce power dissipation in R_S , reduce errors caused by the base current, and provide level shifting to eliminate the restraint of ground-referenced sensing. The relation between V_C and peak current in the power stage is given by:

$$i_{(pk)} = N \left(\frac{V_{R_S(pk)}}{R_S} \right) = \frac{N}{3R_S} (V_C - 1.4V)$$

where: N = current sense transformer turns ratio.
= 1 when transformer not used.

For purposes of small-signal analysis, the control-

to-sensed-current gain is:

$$\frac{i_{(pk)}}{V_C} = \frac{N}{3R_S}$$

When sensing current in series with the power transistor, as shown in Figure 13, current waveform will often have a large spike at its leading edge. This is due to rectifier recovery and/or interwinding capacitance in the power transformer. If unattenuated, this transient can prematurely terminate the output pulse. As shown, a simple RC filter is usually adequate to suppress this spike. The RC time constant should be approximately equal to the current spike duration (usually a few hundred nanoseconds).

The inverting input to the UC3842 current-sense comparator is internally clamped to 1V (Figure 12). Current limiting occurs if the voltage at pin 3 reaches this threshold value, i.e. the current limit is defined by:

$$i_{MAX} = \frac{N \cdot 1V}{R_S}$$

Fig. 12 – Current sensing

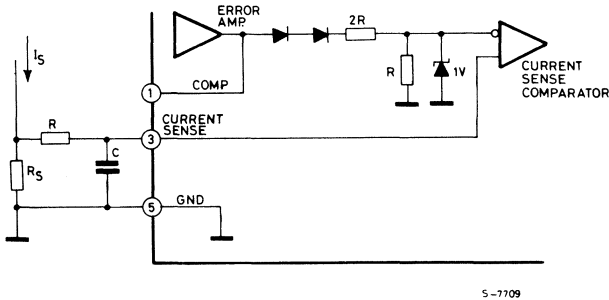
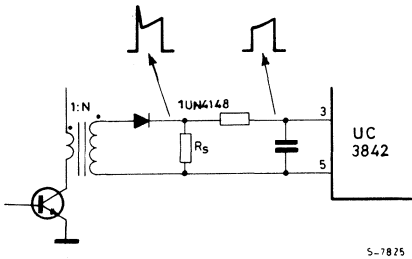


Fig. 13 – Transformer-coupled current sensing

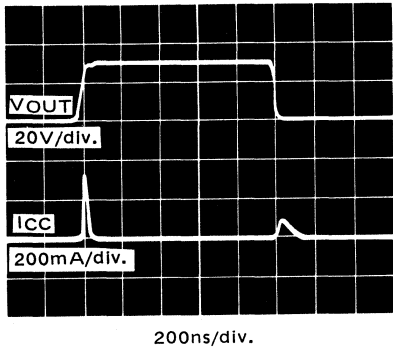


Totem-Pole Output

The UC3842 has a single totem-pole output. The output transistors can be operated to $\pm 1A$ peak current and $\pm 200mA$ average current. The peak current is self-limiting, so no series current-limiting resistor is needed when driving a power MOS gate.

Cross-conduction between the output transistors is minimal, as Figure 14 shows. The average added power due to cross-conduction with $V_i = 30V$ is only 80mW at 200kHz.

Fig. 14 – Output cross-conduction



Figures 15-17 show suggested circuits for driving POWERMOS and bipolar transistors with the UC3842 output. The simple circuit of Figure 15 can be used when the control IC is not electrically isolated from the power MOS. Series resistor R_1 provides damping for a parasitic tank circuit formed by the power MOS input capacitance and any series wiring inductance. Resistor R_2 shunts output leakage currents ($10\mu\text{A}$ maximum) to ground when the under-voltage lockout is active. Figure 16 shows an isolated power MOS drive circuit which is appropriate when the drive signal must be level-shifted or transmitted across an isolation boundary. Bipolar transistors can be driven effectively with the circuit of Figure 17. Resistors R_1 and R_2 fix the on-state base current. Capacitor C_1 provides a negative base current pulse to remove stored charge at turn-off.

Fig. 15 – Direct POWERMOS drive

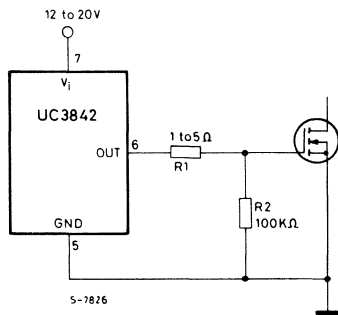


Fig. 16 – Isolated POWERMOS drive

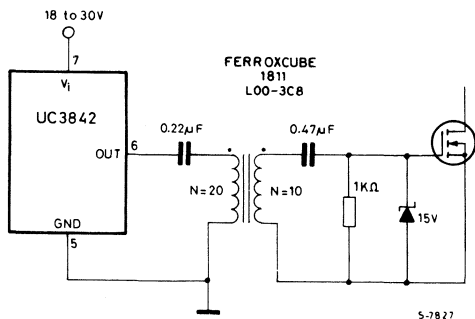
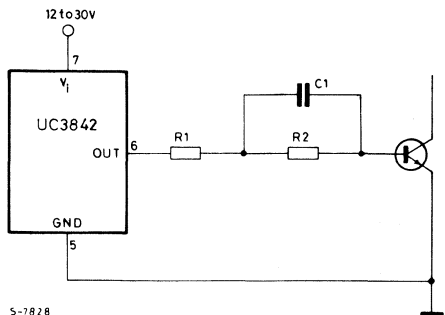


Fig. 17 – Bipolar drive with negative turn-off bias



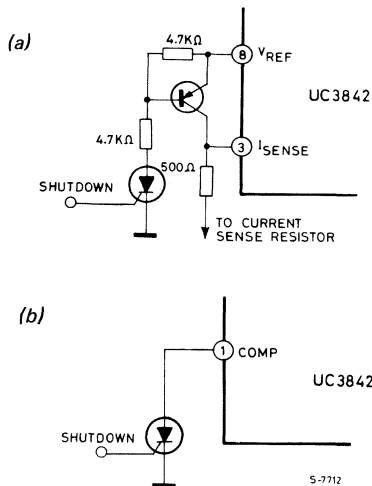
PWM Latch

This flip-flop, shown in Figure 4, ensures that only a single pulse appears at the UC3842 output in any one oscillator period. Excessive power transistor dissipation and potential saturation of magnetic elements are thereby averted.

Shutdown Techniques

Shutdown of the UC3842 can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below 1V. Either method causes the output of the PWM comparator to be high (refer to block diagram, Figure 4). The PWM latch is reset dominant so that the output will remain low until the first clock pulse following removal of the shutdown signal at pin 1 or pin 3. As shown in Figure 18, an externally latched shutdown can be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower under-voltage lockout threshold (10V). At this point all internal bias is removed, allowing the SCR to reset.

Fig. 18 – Shutdown achieved by
a) Pulling pin 3 high
b) Pulling pin 1 Low



AVOIDING COMMON PITFALLS

Current-mode controlled converters can exhibit performance peculiarities under certain operating conditions. This section explains these situations and how to correct them when using the UC3842.

Slope Compensation Prevents Instabilities

It is well documented that current-mode controlled converters can exhibit subharmonic oscillations

when operated at duty cycles greater than 50% .

Fortunately, a simple technique (usually requiring only a single resistor to implement) exists which corrects this problem and at the same time improves converter performance in other respects. This "slope compensation" technique is described in detail in Reference 6. It should be noted that "duty cycle" here refers to output pulse width divided by oscillator period, even in push-pull designs where the transformer period is twice that of the oscillator. Therefore, push-pull circuits will almost always require slope compensation to prevent subharmonic oscillation.

Figure 19 illustrates the slope compensation technique. In Figure 19a the uncompensated control voltage and current sense waveforms are shown as a reference. Current is often sensed in series with the switching transistor for buck-derived topologies. In this case, the current sense signal does not track the decaying inductor current when the transistor is off, so dashed lines indicate this inductor current. The negative inductor current slope is fixed by the values of output voltage (V_O) and inductance (L):

$$\frac{di_L}{dt} = \frac{V_L}{L} = \frac{-V_F - V_O}{L} = \frac{-(V_F + V_O)}{L}$$

where: V_F = forward voltage drop across the free-wheeling diode. The actual slope (m_2) of the dashed lines in Figure 19a is given by:

$$m_2 = \frac{R_S}{N} \cdot \frac{di_L}{dt} = \frac{-R_S (V_F + V_O)}{NL}$$

where: R_S and N are defined as the "Current Sensing" section of this paper.

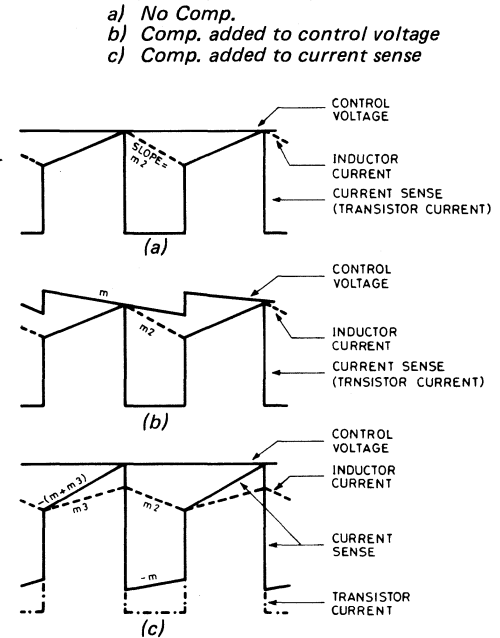
In Figure 19b, a sawtooth voltage with slope m has been added to the control signal. The sawtooth is synchronized with the PWM clock, and practice is most easily derived from the control chip oscillator as shown in Figure 20a. The sawtooth slope in Figure 19b is $m = m_2/2$. This particular slope value is significant in that it yields "perfect" current-mode control; i.e. with $m_2/2$ the average inductor current follows the control signal so that, in the small-signal analysis, the inductor acts as a controlled current source. All current-mode controlled converters having continuous inductor current therefore benefit from this amount of slope compensation, whether or not they operate above 50% duty.

More slope is needed to prevent subharmonic oscillations at high duty cycles. With slope $m = m_2$, such oscillations will not occur if the error amplifier gain ($A_V(E/A)$) at half the switching frequency ($f_s/2$) is kept below a threshold value (Reference 6):

$$A_V(E/A) \bigg|_{\substack{m = m_2 \\ f = f_s/2}} < \frac{\pi^2 C_O}{4\tau}$$

where: C_O = sum of filter and load capacitance
 $\tau = 1/f_s$

Fig. 19 - Slope compensation waveforms:



S-7829

Slope compensation can also improve the noise immunity of a current-mode controlled supply. When the inductor ripple current is small compared to the average current (as in Figure 19a), a small amount of noise on the current sense or control signals can cause a large pulse-width jitter. The magnitude of this jitter varies inversely with the difference in slope of the two signals. By adding slope as in Figure 19b, the jitter is reduced. In noisy environments it is sometimes necessary to add slope $m > m_2$ in order to correct this problem. However, as m increases beyond $m = m_2/2$, the circuit becomes less perfectly current controlled. A complex trade-off is then required; for very noisy circuits the optimum amount of slope compensation is best found empirically.

Once the required slope is determined, the value of R_{SLOPE} in Figure 20a can be calculated:

$$3m = \frac{\Delta V_{RAMP}}{\Delta t_{RAMP}} \cdot A_V(E/A) = \frac{0.7V}{\tau/2} \left(\frac{R_{SLOPE}}{Z_F | f_s} \right) = \frac{1.4}{\tau} \left(\frac{R_{SLOPE}}{Z_F | f_s} \right)$$

$$R_{SLOPE} = \frac{3m \tau}{1.4} (Z_F | f_s) = 2.1 \cdot m \cdot \tau \cdot Z_F | f_s$$

where: $Z_F | f_s$ is the E/A feedback impedance at the switching frequency.

For $m = m_L$: Δt_{RAMP}

$$R_{SLOPE} = 1.7\tau \left(\frac{R_S (V_F + V_O)}{NL} \right) Z_F | f_s$$

Note that in order for the error amplifier to accurately replicate the ramp, Z_F must be constant over the frequency range f_s to at least $3f_s$.

In order to eliminate this last constraint, an alternative method of slope compensation is shown in Figures 19c and 20b. Here the artificial slope is added to the current sense waveform rather than subtracted from the control signal. The magnitude of the added slope still relates to the downslope of inductor current as described above. The requirement for R_{SLOPE} is now:

$$m = \frac{\Delta V_{RAMP}}{\Delta t_{RAMP}} \left(\frac{R_f}{R_f + R_{SLOPE}} \right) = \frac{0.7}{\tau/2} \left(\frac{R_f}{R_f + R_{SLOPE}} \right)$$

$$R_{SLOPE} = \frac{1.4 R_f}{m \tau} - R_f = R_f \left(\frac{1.4}{m \tau} - 1 \right)$$

For $m = m_2$:

$$R_{SLOPE} = R_f \left(\frac{1.4 N L}{R_S (V_F + V_O) \tau} - 1 \right)$$

R_{SLOPE} loads the UC3842 R_T/C_T terminal so as to cause a decrease in oscillator frequency. If $R_{SLOPE} \gg R_T$ then the frequency can be corrected by decreasing R_T slightly. However, with $R_{SLOPE} \lesssim 5R_T$ the linearity of the ramp degrades noticeably, causing over-compensation of the supply at low duty cycles. This can be avoided by driving R_{SLOPE} with an emitter-follower as shown in Figure 21.

Fig. 20 - Slope compensation added (a) to control signal or (b) to current sense waveform

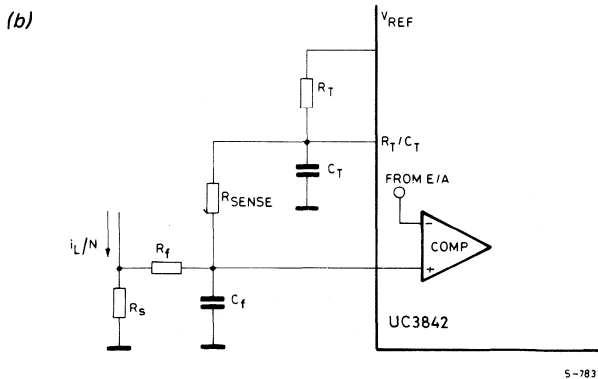
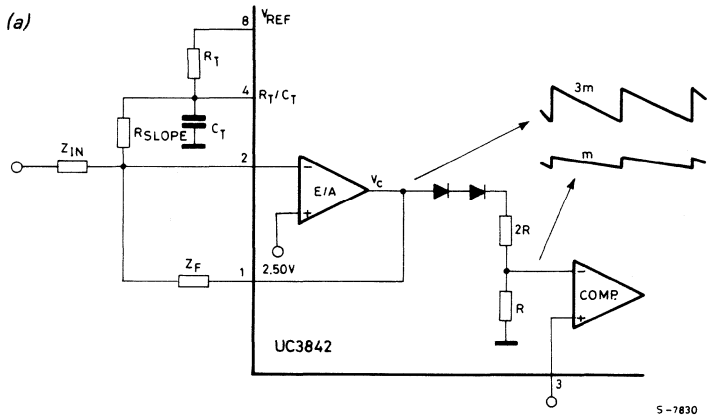
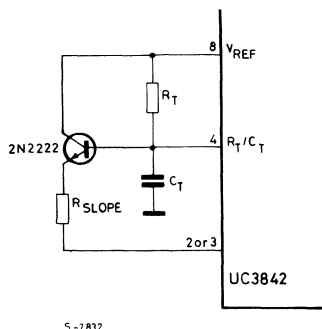


Fig. 21 – Emitter-follower minimizes load at R_T/C_T terminal.



S-7832

Noise

As mentioned earlier, noise on the current sense or control signals can cause significant pulse-width jitter, particularly with continuous-inductor-current designs. While slope compensation helps alleviate this problem, a better solution is to minimize the amount of noise. In general, noise immunity improves as impedance decrease at critical points in a circuit.

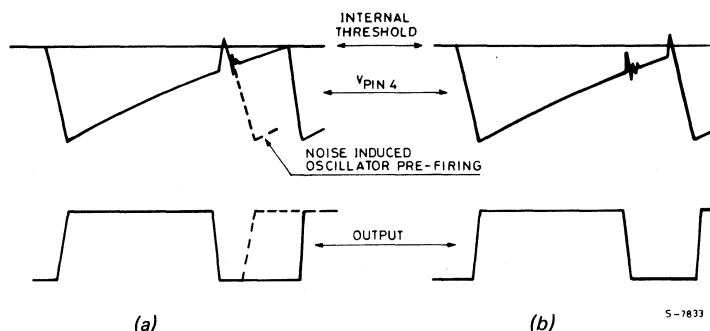
One such point for a switching supply is the ground line. Small wiring inductances between various ground points on a PC board can support common-mode noise with sufficient amplitude to interfere with correct operation of the modulating IC. A copper ground plane and separate return lines for high-current paths greatly reduce common-mode noise. Note that the UC3842 has a single

ground pin. High sink currents in the output therefore cannot be returned separately.

Ceramic bypass capacitors ($0.1\mu\text{F}$) from V_i and V_{REF} to ground will provide low-impedance paths for high frequency transients at those points. The input to the error amplifier, however, is a high-impedance point which cannot be bypassed without affecting the dynamic response of the power supply. Therefore, care should be taken to lay out the board in such a way that the feedback path is far removed from noise generating components such as the power transistor(s).

Figure 22a illustrates another common noise-induced problem. When the power transistor turns off, a noise spike is coupled to the oscillator R_T/C_T terminal. At high duty cycles the voltage at R_T/C_T is approaching its threshold level ($\sim 2.7\text{V}$, established by the internal oscillator circuit) when this spike occurs. A spike of sufficient amplitude will prematurely trip the oscillator as shown by the dashed lines. In order to minimize the noise spike, choose C_T as large as possible, remembering that deadtime increases with C_T . It is recommended that C_T never be less than $\sim 1000\text{pF}$. Often the noise which causes this problem is caused by the output (pin 6) being pulled below ground at turn-off by external parasitics. This is particularly true when driving POWERMOS. A diode clamp from ground to pin 6 will prevent such output noise from feeding to the oscillator. If these measures fail to correct the problem, the oscillator frequency can always be stabilized with an external clock. Using the circuit of Figure 8 results in an R_T/C_T waveform like that of Figure 22b. Here the oscillator is much more immune to noise because the ramp voltage never closely approaches the internal threshold.

Fig. 22 – a) Noise on pin 4 can cause oscillator to pre-trigger
b) With external sync. noise does not approach threshold level



S-7833

Maximum Operating Frequency

Since output deadtime varies directly with C_T , the restraint on minimum C_T (1000pF) mentioned above results in a minimum deadtime capability for the UC3842. This minimum deadtime varies with R_T and therefore with frequency, as shown in Figure 23. Above 100kHz , the deadtime significantly

reduces the maximum duty cycle obtainable at the UC3842 output (also show in Figure 23). Circuits not requiring large duty cycles, such as the forward converter and flyback topologies, could operate as high as 500kHz . Operation at higher frequencies is not recommended because the deadtime become less predictable.

The speed of the UC3842 current sense section poses an additional constraint on maximum operating frequency. A maximum current sense delay of 400ns represents 10% of the switching period at 250kHz and 20% at 500kHz. Magnetic components must not saturate as the current continues to rise during this delay period, and power semiconductors must be chosen to handle the resulting peak currents. In short, above ~250kHz, many of the advantages of higher-frequency operation are lost.

CIRCUIT EXAMPLES

1. Off-Line Flyback

Figure 24 shows a 25W multiple-output off-line flyback regulator controlled with the UC3842. This regulator is low in cost because it uses only two magnetic elements, a primary-side voltage sensing technique, and an inexpensive control circuit. Specifications are listed below.

SPECIFICATIONS:

Input Voltage	95 VAC to 130 VAC (50Hz/60Hz)
Output Voltage:	A. +5V, 5%: 1A to 4A load Ripple voltage: 50mV P-P Max. B. +12V, 3% : 0.1A to 0.3A load Ripple voltage: 100mV P-P Max C. -12V, 3% 0.1A to 0.3A load Ripple voltage: 100mV P-P Max
Line Isolation:	3750V
Switching Frequency:	40kHz
Efficiency @ full load:	70%

Fig. 23 - Deadtime and maximum obtainable duty-cycle vs. frequency with minimum recommended CT.

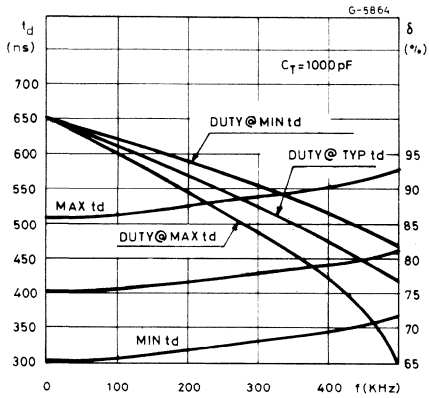
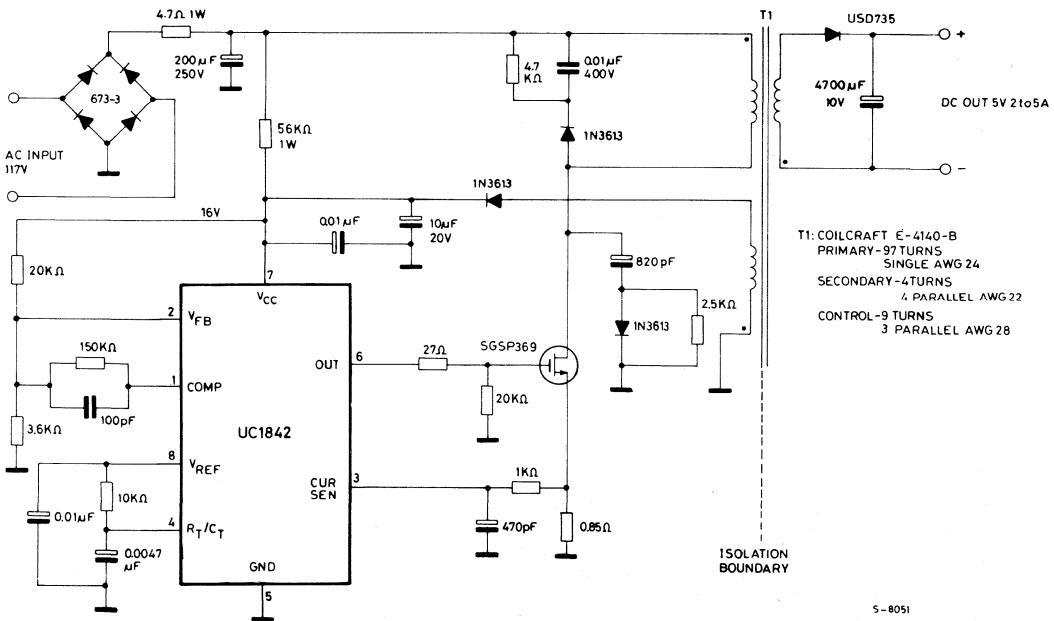


Fig. 24 - 25W off-line flyback regulator



A 25W OFF-LINE FLYBACK SWITCHING REGULATOR

INTRODUCTION

This note describes a low cost switching power supply for applications requiring multiple output voltages, e.g. personal computers, instruments, etc. . . The discontinuous mode flyback regulator used in this application provides good voltage tracking between outputs, which allows the use of primary side voltage sensing. This sensing technique reduces costs by eliminating the need for an isolated secondary feedback loop.

The low cost, (8 pin) UC1842 current mode control chip employed in this power supply provides performance advantages such as:

- 1) Fast transient response
- 2) Pulse by pulse current limiting
- 3) Stable operation

To simplify drive circuit requirements, a TO-220 power MOS SGSP369 is utilized for the power switch. This switch is driven directly from the output of the control chip.

Power Supply Specifications

1. Input voltage: 95VAC to 130VAC (50Hz/60Hz)
2. Output voltage:
 - A. +5V, $\pm 5\%$: 1A to 4A load
Ripple voltage: 50mV P-P Max
 - B. +12V, $\pm 3\%$: 0.1A to 0.3A load
Ripple voltage: 100mV P-P Max
 - C. -12V, $\pm 3\%$: 0.1A to 0.3A load
Ripple voltage: 100mV P-P Max.
3. Line Isolation: 3750V
4. Switching Frequency: 40KHz
5. Efficiency @ Full Load: 70%

Basic Circuit Operation

The 117VAC input line voltage is rectified and

smoothed to provide DC operating voltage for the circuit. When power is initially applied to the circuit, capacitor C2 charges through R2. When the voltage across C2 reaches a level of 16V the output of IC1 is enabled, turning on power MOS Q1.

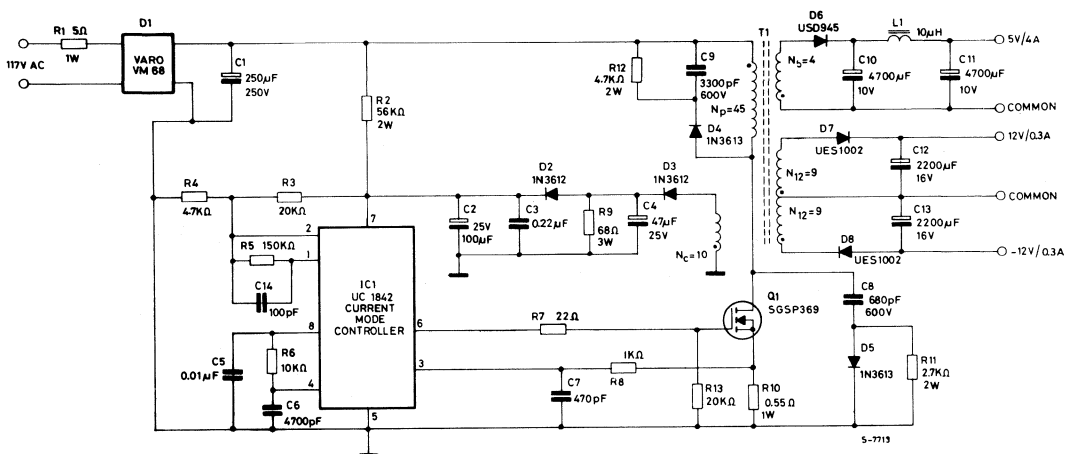
During the on time of Q1, energy is stored in the air gap of transformer (inductor) T1. At this time the polarity of the output windings is such that all output rectifiers are reverse biased and no energy is transferred. Primary current is sensed by a resistor, R10, and compared to a fixed 1V reference inside IC1. When this level is reached, Q1 is turned off and the polarity of all transformer windings reverses, forward biasing the output rectifiers. All the energy stored is now transferred to the output capacitors. Many cycles of this store/release action are needed to charge the outputs to their respective voltages. Note that C2 must have enough energy stored initially to keep the control circuitry operating until C4 is charged to a level of approximately 13V. The voltage across C4 is fed through a voltage divider to the error amplifier (pin 2) and compared to an internal 2.5V reference.

Energy stored in the leakage inductance of T1 causes a voltage spike which will be added to the normal reset voltage across T1 when Q1 turns off. The clamp consisting of D4, C9 and R12 limits this voltage excursion from exceeding the BVDS rating of Q1. In addition, a turn-off snubber made up of D5, C8 and R11 keeps power dissipation in Q1 low by delaying the voltage rise until drain current has decreased from its peak value. This snubber also damps out any ringing which may occur due to parasitics.

Less than 3.5% line and load regulation is achieved by loading the output of the control winding Nc, with R9. This resistor dissipates the leakage energy associated with this winding. Note that R9 must be isolated from R2 with diode D2, otherwise C2 could not charge to the 16V necessary for initial start-up.

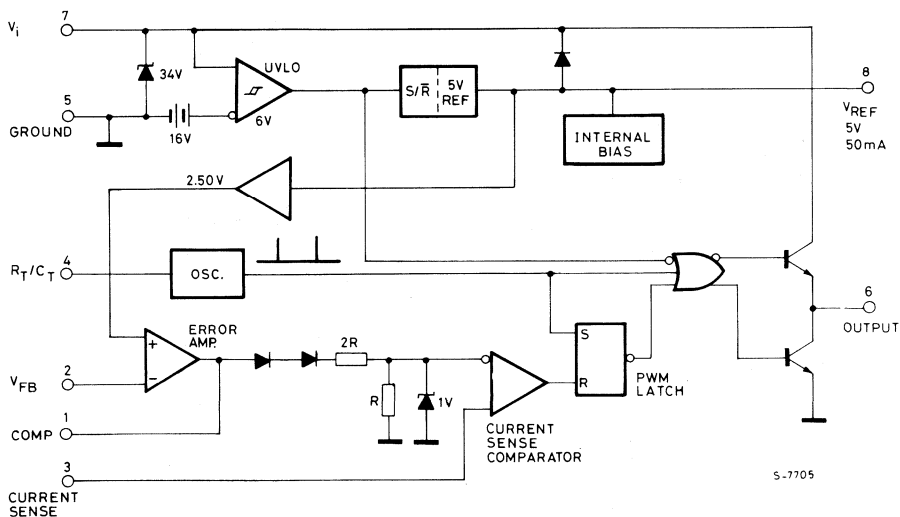
A small filter inductor in the 5V secondary is added to reduce output ripple voltage to less than 50mV. This inductor also attenuates any high frequency noise.

Fig. 1 – 25W off-line flyback regulator



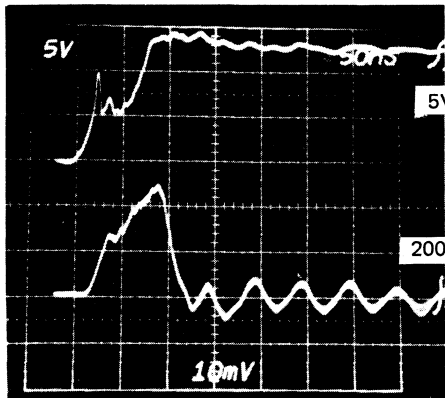
- Notes 1 - All resistors are 1/4W unless noted
2 - See appendix for construction details
3 - L1 = Ferroxcube 204T50-3C8 (Toroid), N° turns: 4, Wire Gauge: 1mm. (18AWG)

Fig. 2 – Block diagram: UC1842 current mode controller

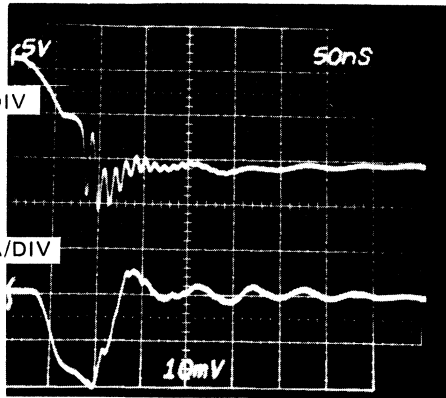


TYPICAL SWITCHING WAVEFORMS

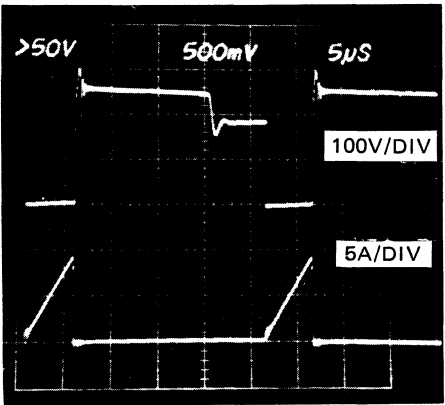
T_{on} - Drive waveforms



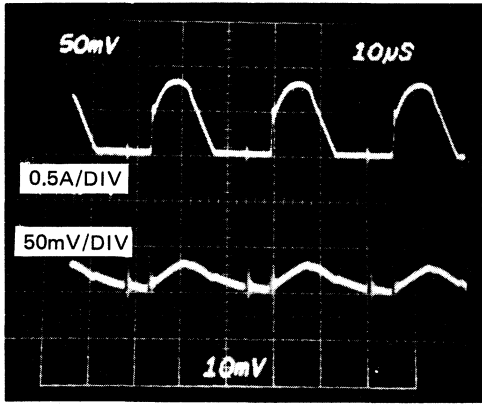
T_{off} - Drive waveforms



Upper trace: Q₁ - Gate to source voltage
Lower trace: Q₁ - Gate current



Upper trace: Q₁ - Drain to source voltage
Lower trace: Primary current - I_D



Upper trace: +5V charging current
Lower trace: +5V output ripple voltage

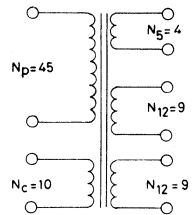
PERFORMANCE DATA

CONDITIONS	5V out	12V out	-12V out
Low Line (95VAC)			
± 12 @ 100mA +5V @ 1.0A 4.0A	5.211 4.854	12.05 12.19	-12.01 -12.14
± 12 @ 300mA +5V @ 1.0A 4.0A	5.199 4.950	11.73 11.68	-11.69 -11.63
Nominal Line (120VAC)			
± 12 @ 100mA +5V @ 1.0A 4.0A	5.220 4.875	12.07 12.23	-12.03 -12.18
± 12 @ 300mA +5V @ 1.0A 4.0A	5.208 4.906	11.73 11.67	-11.68 -11.62
High Line (130VAC)			
± 12 @ 100mA +5V @ 1.0A 4.0A	5.207 4.855	12.06 12.21	-12.02 -12.15
± 12V @ 300mA +5V @ 1.0A 4.0A	5.200 4.902	11.71 11.66	-11.67 11.61
Overall Line and Load Regulation	± 3.5%	± 2.3%	± 2.4%

APPENDIX POWER TRANSFORMER -T1

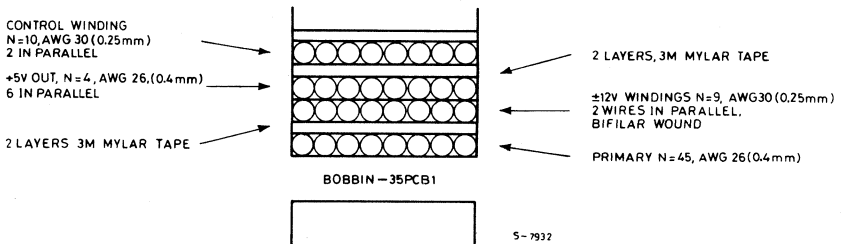
Core: Ferroxcube EC-35/3C8
Gap: 0.25mm. in each outer leg

NOTE: For reduced EMI put gap in center leg only.
Use 0.5mm.



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TRANSFORMER CONSTRUCTION



power switch. This eliminates many of the transitions across the isolation boundary which significantly increase the cost of the magnetics portion of the power supply's budget.

There are two disadvantages to primary control: (1) operating or at least starting, the control electronics from the line voltage (typically 300 VDC), and (2) providing adequate regulation (which requires feedback from the secondary across the isolation boundary). The capability of the UC1840 Control IC to solve these problems while providing all of the regulating, sequencing, monitoring, and protection functions referenced to the primary side, makes this device very attractive.

THE UC1840 CONTROLLER

The overall block diagram of the UC1840, shown in Figure 1, includes the following features:

- (1) Fixed-frequency operation set by user-selected components.
- (2) A variable-slope ramp generator for constant volt-second operation providing open-loop line regulation and minimizing, or in some cases even eliminating, the need for feedback control.
- (3) A drive switch for low current start-up off the high-voltage line.
- (4) A precision reference generator with internal over-voltage protection.

- (5) Complete under-voltage, over-voltage, and over-current protection including programmable shutdown and restart.
- (6) A high-current, single-ended PWM output optimized for fast turn-off of an external power switch.
- (7) Logic control for pulse-commandable or DC power sequencing.

For an understanding of how these individual blocks work together in a typical, medium-power flyback power supply, reference should be made to Figure 2 and the functional description which follows.

UC1840 FUNCTIONAL DESCRIPTION

Power sequencing

A simplified schematic of the UC1840's internal power turn-on circuitry is shown in Figure 3. The key elements of this function are: (1) the Driver Bias Switch, Q3, which keeps the loading on the control voltage line, V_C , to a minimum during start up; (2) the Under-voltage Comparator which also functions as a Start Threshold Detector with programmable hysteresis; and (3) an auxiliary, primary-referenced, low-voltage winding on the main power transformer which provides normal control power after turn-on. The sequence of events is as follows:

Fig. 2 - A fully protected, isolated flyback power supply can be implemented with the UC1840, a high-voltage power switch, the transformer, and a small handful of passive components.

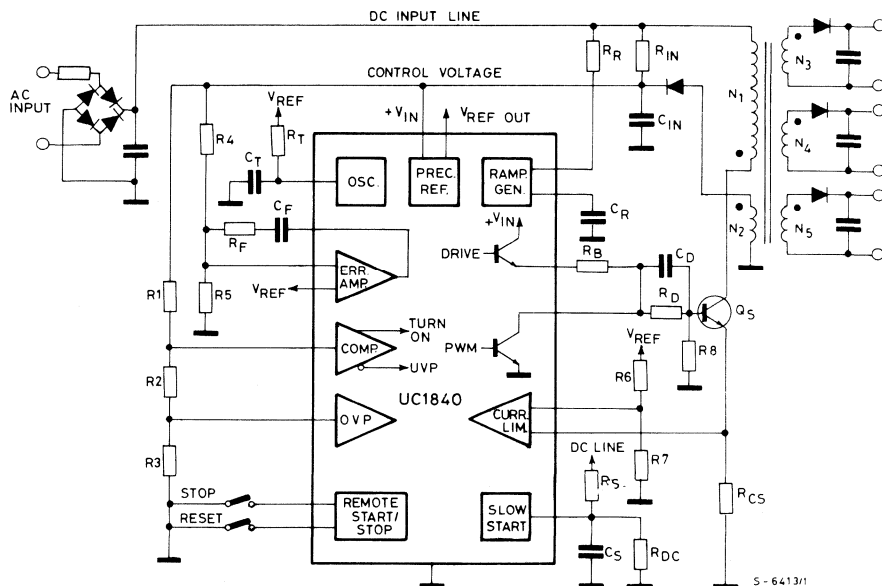
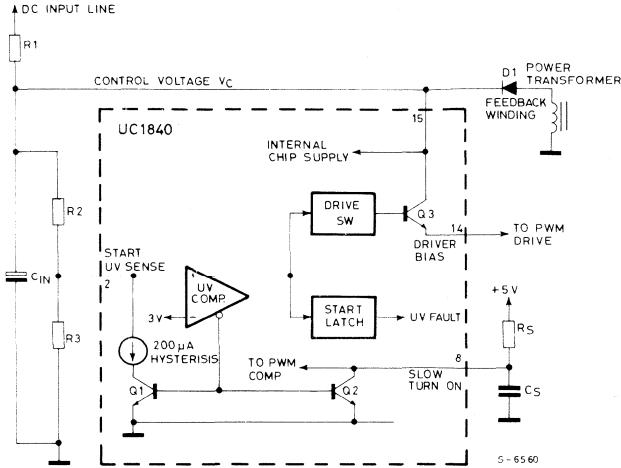


Fig. 3 - The UC1840's start circuitry requires low starting current from the DC input line with normal operating current supplied from a low-voltage feedback winding on the power transformer.



- (1) While the control voltage, V_C , is low enough so that the voltage on pin 2 is less than 3V, the Start/UV Comparator does the following:
 - (a) A 200µA hysteresis current is flowing into pin 2 through Q1 causing an added drop across R2.
 - (b) The drive switch is holding the Driver Bias transistor, Q3, OFF. This insures that the only current required through R1 is the start-up current of the UC1840, plus external dividers (R2, R3, R_S , etc.).
 - (c) The Slow Turn-on transistor, Q2, is ON, holding pin 8 and C_S low.
 - (d) The Start Latch keeps the under-voltage signal from being defined as a fault.

- (2) The start level is defined by:

$$V_C(\text{start}) = 3 \left(\frac{R_2 + R_3}{R_3} \right) + 0.2 R_2.$$

When V_C rises to this level, the Start/UV. Comparator then does the following:

- (a) Turns off Q1, eliminating the 200µA hysteresis current. This allows the voltage on V_C to drop before reaching the under-voltage fault level defined by:

$$V_C(\text{U.V. fault}) = 3 \left(\frac{R_2 + R_3}{R_3} \right)$$

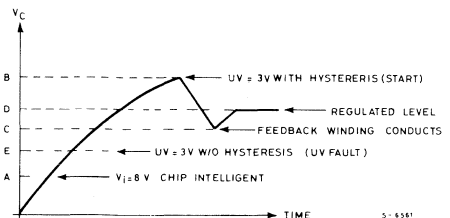
- (b) Sets the Start Latch to monitor for an under-voltage fault.
- (c) Activates Q3 providing Driver Bias to the power switch, pulling the added current out of C_{IN} .
- (d) Turns off Q2 allowing for programmed slow turn-on defined by R_S and C_S .

- (3) A normal start-up occurs with the control voltage, V_C , following the path shown in Figure 4. If the power supply does not start, V_C will fall to an under-voltage fault which will then either initiate a restart attempt or hold the power switch off, depending upon the status of the Reset terminal as defined under Fault Sequencing. If start-up does not occur because of some fault in the Driver Bias line, V_C will continue to rise until the 40V zener across the reference circuit conducts. This will then clamp V_C to that level, protecting the control chip.

After start-up occurs, current will continue to flow in R1 providing a power loss of:

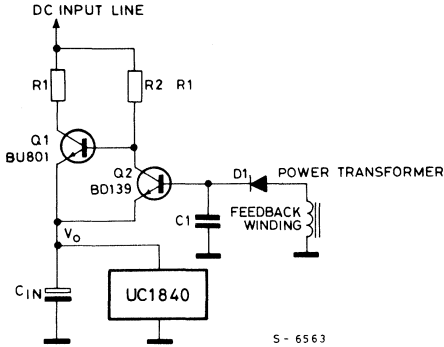
$$P_d = \frac{(V_{\text{line}} - V_C)^2}{R_1}$$

Fig. 4 - Under a normal turn-on, the supply voltage to the UC1840, V_C , would rise lightly loaded to the start level, fall under the turn-on load, and then regulate at some intermediate level.



If this loss is objectionable, it can be reduced more than an order of magnitude by the addition of a two-transistor switch shown in Figure 5. In this circuit, Q1 is initially driven on by current through R2. When the feedback winding starts to conduct through D1, however, Q2 turns on leaving only R2 conducting from the input line.

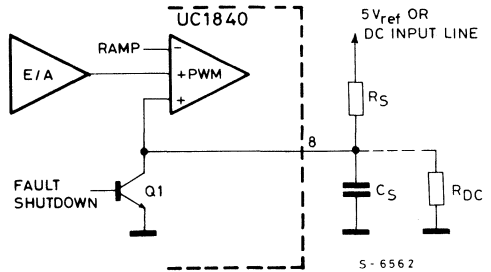
Fig. 5 - The addition of Q1 and Q2 can eliminate the steady-state current through R1 after turn-on. Q2 is selected to pass all control current through its base-emitter junction.



Slow turn-on circuit

The PWM comparator input connected to pin 8 accommodates several programming functions, shown in Figure 6. Since this comparator will only follow the lowest positive input, holding pin 8 low will effectively eliminate a PWM signal, regardless of the status of the Error Amplifier output. Prior to turn-on, and at all times when a fault has been sensed, Q1 is ON, holding pin 8 low.

Fig. 6 - Pin 8 on the UC1840 can be used for both slow turn-on and duty-cycle limiting as well as a PWM shutdown port.

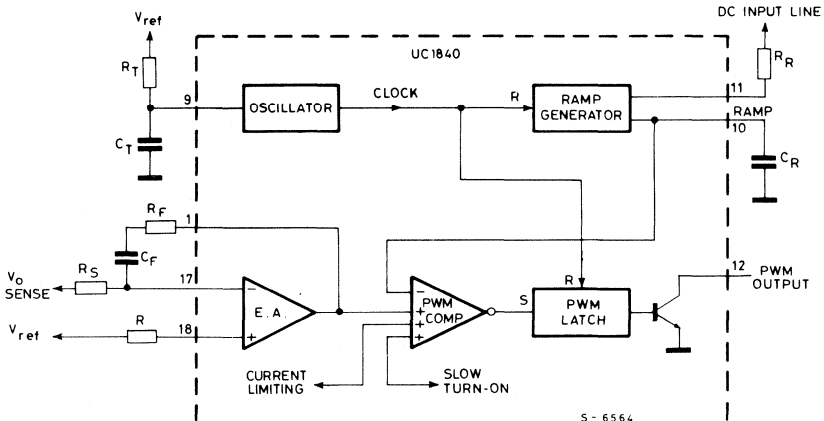


When Q1 turns off, allowing pin 8 to rise with a controlled rate will cause the output pulses to increase from zero to nominal widths at the same rate. This is accomplished by the addition of C_S and a charging source, such as R_S, to the 5V reference.

Note that where starting energy is stored in an input capacitor, the time for PWM turn-on must be less than the time required for the added Driver Bias load current to discharge the input capacitor to the under-voltage fault level. In other words, referring back to Figure 4, the slow turn-on must be faster than the time required for V_C to fall from level B to level E.

Another function of pin 8 is to establish a maximum duty cycle limit. This is achieved by clamping the voltage on pin 8 with a divider formed by adding R_DC to ground. If R_S is taken to the 5V reference, the clamp voltage will be fixed, which is desirable if the ramp slope is also fixed. If the ramp slope is varied with the input line — for constant volt-second operation — then the clamp voltage on pin 8 must also vary. This is readily accomplished

Fig. 7 - The pulse-width modulator within the UC1840 separates the ramp function from the fixed-frequency oscillator.



by connecting R_S to the DC input line. The divider voltage:

$$V_{Pin\ 8} = \left(\frac{R_{DC}}{R_S + R_{DC}} \right) V_{DC\ input}$$

should be equal to the ramp voltage level that yields the desired maximum duty cycle, at the same DC input level.

PWM control

Pulse-Width Modulation within the UC1840 consists of the blocks shown in Figure 7. This architecture, with the possible exception of the separation between the time-base and ramp functions, is fairly conventional. It is described in greater detail in the paragraphs which follow.

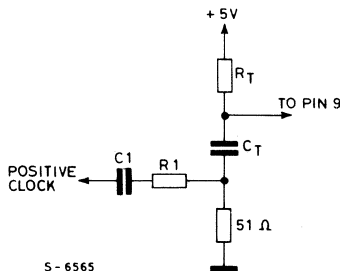
Oscillator

A constant clock frequency is established by connecting R_T from pin 9 to the 5V reference and C_T from pin 9 to ground. The frequency is approximated by:

$$f \approx \frac{1}{R_T C_T}$$

where the value of R_T can range from 1 k Ω to 100K Ω and C_T from 300pF to 0.1 μ F. The best temperature coefficients occur with C_T in the range of 1000 to 3000 pF. Although the clock output pulse is not available external to the UC1840, synchronization to an external clock can still be accomplished with the circuit of Figure 8, where R_1 and C_1 are selected to provide a 0.5V, 200 ns pulse across the 51 Ω resistor, and R_T and C_T define a frequency slightly lower than the synchronizing source.

Fig. 8 – Synchronization to an external time base can be accomplished by adding a 51 Ω resistor in series with C_T .

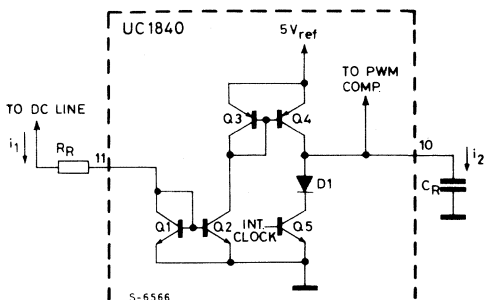


To achieve minimum start-up current, the oscillator is not activated until the input voltage is high enough to give a start command to the drive switch.

Ramp generator

The ramp generator function of the UC1840 is shown in simplified form in Figure 9.

Fig. 9 – Current mirrors Q1–Q4 are used to make the ramp charging current i_2 , linearly proportional to the DC input line.



The NPN and PNP current mirrors provide a charging current to C_R of:

$$i_2 = i_1 = \frac{V_{line} - 0.7V}{R_R} \approx \frac{V_{line}}{R_R}$$

The current mirrors are useful over a current range of 1 μ A to 1mA, but optimum tracking occurs between 30 μ A and 300 μ A. Since the voltage across Q1 is very small, i_2 accurately represents the input line voltage. The ramp slope, therefore, is:

$$\frac{dv}{dt} = \frac{V_{line}}{R_R C_R}$$

The peak voltage across C_R is clamped to approximately 4.2V while the valley, or low voltage, is determined by the on-voltage of the discharge network, D1 and Q5. This is typically 0.7V.

If line sensing is not required, R_R should be connected to the 5V reference for constant ramp slope.

Error amplifier

This is a voltage-mode operational amplifier with an uncommitted NPN differential input stage and an output configuration as shown in Figure 10.

The 1K Ω output resistor, R_O , is used both for short circuit protection and to limit the peak output voltage to less than 4.0V so it cannot rise above the clamped ramp waveform. At sink currents less than 300 μ A, the low output level will be within 200mV of ground but it rises to 1V at higher current levels.

The input common mode range is from 1V to within 2V of the input supply voltage, V_{in} , and thus either input can be connected directly to the 5V reference.

Fig. 10 – The output of the error amplifier operates class A to 300μA, but can source and sink more than 1 mA for fast response.

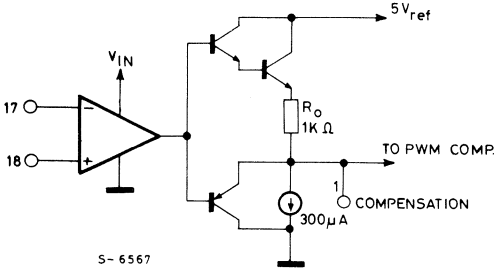


Fig. 11 – The UC1840 error amplifier has a DC gain of 67 dB, a 2 MHz bandwidth, and phase margin of approximately 45°.

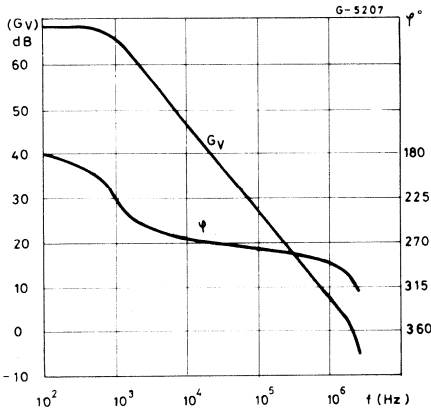
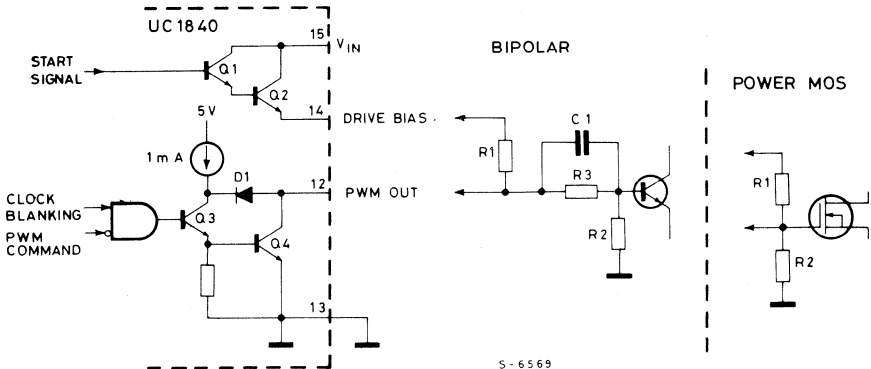


Fig. 12 – Interfacing the UC1840 PWM output stage to either Bipolar or Power MOS switches.



The small signal, open-loop gain characteristics are shown in Figure 11. The amplifier is unity-gain stable and has a maximum slew rate of just under 1V/μs.

PWM comparator and latch

This comparator (see Figure 7) generates the output pulse which starts at the termination of the clock pulse and ends when the ramp waveform crosses the lowest of the three positive inputs. The clock forms a blanking pulse which keeps the maximum duty cycle less than 100%. The PWM latch insures there will be only one pulse per period and eliminates oscillation at comparator cross-over.

PWM output stage

In addition to the PWM output signal on pin 12, the UC1840 also includes an output gating, or arming function as Driver Bias on pin 14. Both functions should be considered together in interfacing to the external high-voltage power switch. These are illustrated in simplified form in Figure 12.

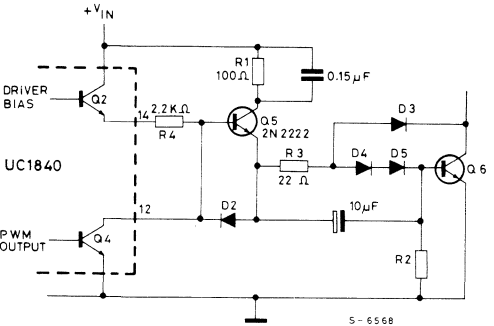
At very low input voltages ($V_{IN} < 3V$), both Q2 and Q4 are OFF. This may necessitate the use of R2, but its value can be high since it does not have to turn the output switch off. It merely holds it in the off state during the early portion of start-up.

Between $V_{IN} = 3V$ and the start threshold (pin 2 = 3V with hysteresis on), Q2 is OFF and Q4 is ON, clamping the power switch off with a low impedance. A start command (UV high) turns on Q2, applying ($V_{IN} - 2V$) to R1. This provides a source for power switch activation; however, since Q4 is still conducting, the current through R1 is shunted to ground and the power switch remains held off.

At the same time Q2 turns on, the clamping transistor at the slow-start terminal, pin 8, turns off allowing the voltage on pin 8 to rise according to the external slow-start time constant described earlier. This allows PWM pulses to begin to activate Q4 — narrow at first and widening to the point where the error amplifier takes command.

The interface between the UC1840 and the primary power switch may be implemented in several different ways to meet varying system requirements. One obvious application is when the use of a bipolar transistor switch requires more drive current than the Driver Bias output can provide. Figure 13 shows a more typical bipolar drive scheme where Q5 has been added to boost the turn-on current with the UC1840 still providing the high speed turn-off. The circuit now serves as a more efficient "totem-pole" driver since Q5 turns off when Q4 conducts. It also illustrates the use of a Baker Clamp to minimize storage time in Q6 and the capacitors for rapid turn-on and high-current pulse turn-off.

Fig. 13 - Adding Q5 as a switched, drive-boost transistor provides added base drive for Q6 while reducing the steady-state current through both Q2 and Q4.



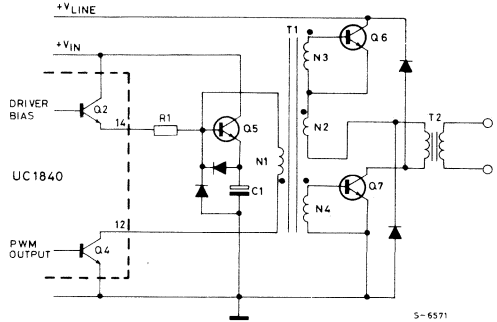
Another application is the two-transistor, off-line, forward converter topology shown in Figure 14. This circuit uses proportional base drive where the UC1840 need only supply a short, turn-off current pulse with transformer regeneration through T1 providing the steady-state drive. The magnetizing current is controlled by R1, with Q5 added to rapidly recharge C1 from which the turn-off current is supplied.

Fault protection

A significant benefit in using the UC1840 is the multi-faceted fault-sensing and programming capability built into the device. With the intent to provide complete control to the power system under all types of potential malfunctions, fault-sensing

circuitry has been included to sense over-voltage, under-voltage, or over-current conditions. Additionally, high-speed, pulse-by-pulse digital current limiting is included as a separate function. The operation of these circuits is described below.

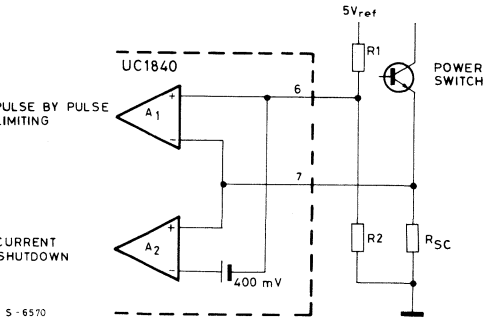
Fig. 14 - Interfacing the UC1840 single PWM output to a two-transistor off-line forward converter which uses proportional base drive.



Current limiting

The current limit comparators have differential inputs for noise rejection but are intended to be used with ground-referenced current sensing as in Figure 15. Comparator A1 is delegated to pulse-by-pulse current limiting. The output of this comparator drives the PWM comparator, where it activates the PWM latch, terminating each pulse when the current sensed by R_{SC} reaches a threshold defined by divider R1, R2, and the 5V reference.

Fig. 15 - Current limiting and overcurrent shut-down are implemented with comparators of different thresholds and a single current sense resistor.



Since V_C is intended to track the supply's output voltage, the addition of a resistor from pin 6 to V_C will provide some foldback to the current limit characteristic. Since comparator A1 has zero offset voltage, it is activated when the voltage across R_{SC} equals that across R2. Comparator A2, with an offset voltage of 400 mV, will activate for over-current shutdown when the voltage across R_{SC} rises to 400 mV higher than the voltage across R2. Since the input bias to both comparators is less than 5 μ A, a low-pass filter for noise rejection may be inserted between R_{SC} and the sense inputs. Activation of comparator A2 is defined as an over-current fault and it triggers the Error Latch. Its operation follows.

Fault sequencing

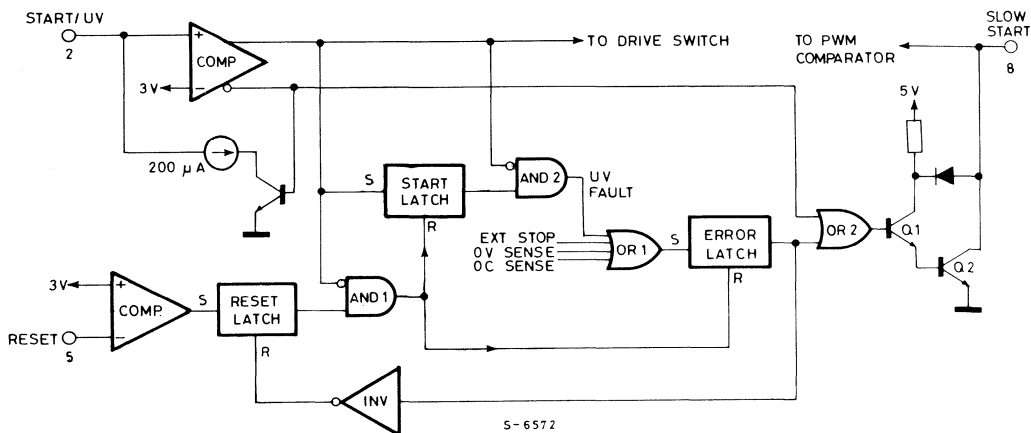
The fault sequencing logic of the UC1840 is shown in Figure 16. Since a fault is defined by this device as an activation of the Error Latch, it makes sense to start here in an attempt to understand this por-

tion of the circuitry. Setting the Error Latch immediately turns on Q1 and Q2, discharging the slow-start capacitor and terminating the PWM output. Note that there is an additional path from the inverted output of the Start/UV comparator through OR2 which keeps pin 8 low. This is to keep the slow-start low during initial turn-on which is not intended to be classified as a fault.

The input to the Error Latch is from OR1 which triggers on signals resulting from four possible events:

- (1) A voltage less than 3V (after prior turn-on) at the Start/UV sense terminal, pin 2.
- (2) A voltage greater than 3V at the Over-Voltage Sense terminal, pin 3.
- (3) A voltage of less than 3V on the Ext. Stop terminal, pin 4.
- (4) An over-current signal resulting in a differential voltage between pins 7 and 6 of greater than 400 mV.

Fig. 16 – Fault sequence logic is designed to insure a complete shutdown and fully controlled restart upon any of four possible fault conditions.



Any of these inputs need only be momentary to set the Error Latch. Transient protection may be necessary to eliminate false triggering, but it can be readily accomplished as all the comparator inputs are high impedances requiring less than 2 μ A of input current, and the 3.0V reference yields a high noise immunity.

The Start Latch can be understood by recognizing that at initial turn-on it is reset with a low output. This prevents AND2 from transmitting a UV fault signal from the Start/UV non-inverting output to the Error Latch. At the start voltage level, defined by a high level on the Start/UV non-inverting output, the Start Latch sets but AND2 still provides no output. Only when the Start/UV input goes low again, with the Start Latch output held high, will AND2 yield an output into the Error Latch.

The status of the Reset terminal, pin 5, determines

what happens after the Error Latch is set. The choices are:

- (1) Latch off and require a recycle of input voltage to restart.
- (2) Continuously attempt to restart.
- (3) Attempt some number of restarts and then latch off.
- (4) Latch off and await a momentary reset pulse to restart.

To examine the operation of the Reset Latch, note that prior to setting the Error Latch, its low output is inverted to hold the reset input to the Reset Latch high. This forces the Reset Latch's output low, regardless of the voltage on pin 5, and, thus, insures no signal out of AND1. With the setting of the Error Latch, the Reset Latch is free to take the

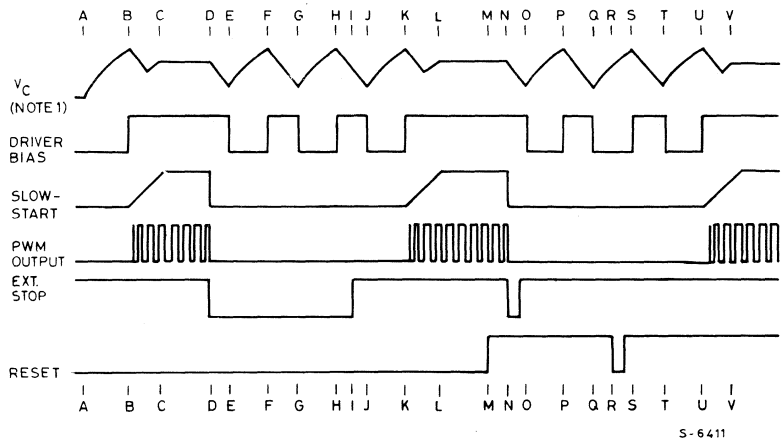
state commanded by pin 5: high if pin 5 is low and vice-versa. The latch allows merely a pulse to set the Reset Latch; the voltage on pin 5 need not be steady state.

With a high Reset Latch output, the Error Latch still does not reset until a low signal is sensed on the Start/UV sense terminal. At that point, AND1 then resets both the Error Latch and the Start Latch re-establishing the initial conditions for a

normal start after fully charging the input capacitor. Of course, if the fault is still present, when the Start/UV input reaches the start level terminating the Error Latch reset signal, this latch will immediately set again.

To aid in the understanding of this logic, Figure 17 gives a pictorial representation of its operation with both steady-state and momentary signals on both the Ext. Stop and Reset terminals.

Fig. 17 - The interrelationship between the functions controlled by the fault sequence logic is illustrated with both static and pulse commands on the ext. stop and reset terminals.



Note 1: V_C represents an analog of the supply output voltage generated by a primary - referenced secondary winding on the power transformer. It is the voltage monitored by the start/UV comparator and in most cases is the supply voltage V_{IN} for the UC1840.

TIME	EVENT
A	INITIAL TURN-ON V _C RISES WITH LIGHT LOAD.
B	START THRESHOLD DRIVER BIAS LOADS V _C .
C	OPERATING PWM REGULATES V _C .
D	STOP INPUT SETS. ERROR LATCH TURNING OFF PWM.
E	UV LOW THRESHOLD. ERROR LATCH REMAINS SET.
F	START TURNS ON DRIVER BIAS BUT ERROR LATCH STILL SET.
G	V _C AND DRIVER BIAS CONTINUE TO CYCLE.
H	
I	STOP COMMAND REMOVED.
J	ERROR LATCH RESET AT UV LOW THRESHOLD.
K	START THRESHOLD NOW REMOVES SLOW-START CLAMP.
L	RETURN TO NORMAL RUN STATE.
M	RESET LATCH SET SIGNAL REMOVED.
N	ERROR LATCH SET WITH MOMENTARY FAULT.
O	ERROR LATCH DOES NOT RESET AS RESET LATCH IS RESET.
P	V _C AND DRIVER BIAS RECYCLE WITH NO TURN-ON.
Q	
R	RESET LATCH IS SET WITH MOMENTARY RESET SIGNAL.
S	V _C MUST COMPLETE CYCLE TO TURN ON.
T	START AND ERROR LATCHES RESET.
U	NORMAL START INITIATED.
V	RETURN TO NORMAL RUN STATE.

If Driver Bias turn-on is used to pump an increment of charge into an integrating capacitor, and that capacitor voltage is applied to the Reset Terminal, some number of retries could be programmed to take place before the Reset voltage rises to 3V, which would then lock the output OFF. Since Driver Bias continues to cycle in the latched-off state, the Reset terminal will remain high until it is either remotely pulled low or the input voltage to the controller is interrupted.

Note that an important element in any restart after a shutdown is the lowering of the voltage at the Start/UV terminal below its UV threshold. While this will occur normally in bootstrap-driven applications, this device can also be used with a constant driving voltage by externally applying a momentary pull-down signal to the Start/UV input after a fault shutdown.

CONCLUSION

With the UC1840, power supply designers now have a device specifically developed for off-line, primary control and one which has addressed the problems of operation under less than "ideal" or normal conditions. Not only does this device make it easier to comply with stringent isolation requirements by requiring a minimum of communication between primary and secondary, but it is also ideally suited for powering systems in remote locations where only a simple transmitted pulse is available for power sequencing.

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50W OFF-LINE SWITCHING POWER SUPPLY USING THE UC3840

INTRODUCTION

This power supply has been designed to provide an easy way to gain familiarity with the operating characteristics of the UC3840 PWM Control Circuit in a practical off-line power supply application. As any switching power supply represents a series of compromises between size, cost, efficiency, performance, and many other variables; no claim is made that this supply optimizes any particular characteristics; only that it provides an easy means to gain an understanding which, hopefully, the designer can use to extrapolate to many specific applications.

This power supply, shown schematically in Fig. 4

implements a 50 watt discontinuous mode flyback power supply with multiple outputs, and features primary-side control with full protection from fault conditions. Additional performance characteristics include simple off-line starting, voltage feed-forward for good line regulation (without feedback across the isolation boundary), pulse-by-pulse current limiting, over- and under-voltage sensing with protective shutdown and automatic restart, and freedom from the need for any circuit adjustments.

For additional information on the operation of the UC3840, reference should be made to TN 168 and data sheet.

POWER SUPPLY SPECIFICATIONS

Input line voltage:	
With 110V jumper:	90 VAC to 130 VAC
With jumper removed:	180 VAC to 260 VAC
Input frequency:	50 or 60 Hz
Switching frequency:	40KHz $\pm$ 10%
Output power:	50W maximum
Output voltages:	5V $\pm$ 5% 12V $\pm$ 5%
Output current:	2.5 to 5A (5V) 1 to 2A (12V)
Line regulation:	5V, 0.07% /V 12V, 0.04% /V
Load regulation:	5V, 2.5%/A 12V, 2.5%/A
Efficiency @ 50 watts	
V _{in} = 90 VAC:	70%
V _{in} = 130 VAC:	65%
Output ripple:	5V @ 5A = 200mV 12V @ 2A = 300mV

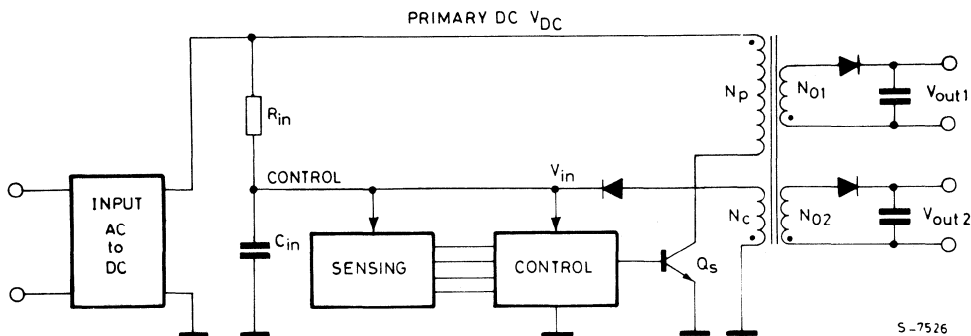
OPERATING PRINCIPLES

In an off-line switching power supply, the input voltage is immediately rectified and filtered, and the resulting DC voltage is chopped at a high frequency. Where 110/220 VAC operation is required, an input voltage doubler configuration is used for 110 VAC input, resulting in a nominal DC input voltage of 310V. The same nominal input voltage is obtained with full wave rectifica-

tion of a 220 VAC line input. High frequency switching allows a very small transformer to be used to efficiently step down to lower output voltages. In the configuration shown in Figure 1 an additional low-voltage winding, N_C , is used to provide continuous operating power for the control and base drive circuits. However, initial energy to start the supply is taken from the line via R_{IN} and C_{IN} . An additional function on N_C is to provide a primary-referenced feedback voltage that is proportional to the output voltages. This feedback voltage is sensed and regulated by the control circuitry, thereby eliminating the need for feedback across the isolated boundary.

The polarity of the transformer windings identifies this configuration as a flyback supply. When transistor Q_5 conducts, all output diodes are reverse biased and the energy is stored in the primary inductance. When Q_5 turns off, the voltage polarity of winding N_p reverses (flies back) and the energy is delivered to the output circuits. This circuit operates in the discontinuous mode in which all the energy stored in the transformer inductance is completely transferred to the load during every cycle, i.e. transformer current goes to zero before the end of each cycle. Although this approach yields higher peak current compared to other topologies, it is usually chosen because of its less stringent requirements on the transformer, its faster transient response, and its easier stabilization. To insure discontinuous operation and core reset, the volt-second product across the transformer primary during reset must be allowed to equal or exceed the volt-seconds applied during the on-time of Q_c .

Fig. 1 – Simplified block diagram of a flyback power supply with primary control



DESIGN CONSIDERATIONS

The following description of the design decisions made for this power supply will be with respect to the complete schematic shown in Fig. 4. No significant theoretical discussion is offered and only nominal values are used in the analysis, but hopefully the equations given can be used to either extrapolate to other design problems or to optimize the supply to a particular characteristics.

Input section

Input bridge D1 rectifies the line voltage while resistors R1 and R2 are used to limit the peak charging current to capacitors C1 and C2. The values for C1 and C2 are usually determined by either the ripple voltage allowable for V_{DC} or the minimum hold-up time.

Ripple calculations are worse-case for the 110V voltage doubler configuration where:

RMS line voltage = 90 to 130 VAC
peak no-load input = 253 to 368 volts.

At the minimum line voltage, each capacitor alternately charges to a peak of 126 volts. Allowing for a total input voltage sag at full load of 50 volts, the minimum capacitor voltage must be held to 92 volts. Since each capacitor must provide one-half the energy requirements of the power supply, the required energy for each line cycle is:

$$W_{in} = \frac{\text{Power out}}{\text{Efficiency} \times \text{Frequency}} = \frac{50}{0.7 \times 60} = 1.2 \text{ Joule}$$

and the capacitor value can be calculated from:

$$\frac{1}{2} W_{in} = \frac{1}{2} C_1 (V_{pk}^2 - V_{min}^2) \text{ or}$$

$$C_1 = \frac{W_{in}}{V_{pk}^2 - V_{min}^2} = \frac{1.2}{126^2 - 92^2} = 162 \mu F$$

If, instead of ripple voltage, we choose the input capacitors to hold the input DC above 200 volts for a least two cycles of line drop-out, then:

$$C_1 = \frac{2 (P_o/2) (\text{no. of cycles drop-out}) 1/f}{\text{Efficiency} (V_{pk}^2 - V_{min}^2)}$$

$$= \frac{2 (25) (2) 1/60}{0.7 (126^2 - 92^2)} = 331 \mu F$$

In this application, 470 μF was picked as a standard size which would allow loose tolerances.

Transformer

A major task with any flyback power supply is the design of the transformer as many tradeoffs are

normally required between regulation, leakage inductance (and corresponding transistor stress), isolation, size, and cost. In this application, the core selected is a Ferroxcube EC35-3C8 which has the following characteristics:

Effective core area, $A_e = 0.84 \text{ cm}^2$
Max flux density, $B_{sat} = 2800 \text{ gauss}$
Bobbin = 35 PC B I

The design starts with a calculation of maximum duty cycle which is defined by the voltage capability of the power switch. This voltage was allocated as follows:

VDC max	= 370V
Reset voltage	= 120V
Leakage inductance spike	= 100V
Max total voltage	= 590V

With a reset voltage of 120V, at minimum input voltage,

$$D_{max} = \frac{120V}{120V + 200V} = 37.5\%$$

The primary inductance can then be calculated as:

$$L_p = \frac{\text{Efficiency}}{2 P_o f} (V_{in \text{ min}} \times D_{max})^2 =$$

$$= \frac{0.7 (200 \times 0.375)^2}{2 \times 50 \times 40 \times 10^3} =$$

$$L_p \approx 1 \text{ mH}$$

The peak current at full load is:

$$I_p = \frac{2 P_o}{\text{eff} (V_{in \text{ min}} \times D_{max})} =$$

$$= \frac{2 \times 50}{0.7 \times 200 \times 0.375} = 1.9 \text{ A}$$

The maximum energy storage requirement within the primary is calculated on the basis of maximum current, in this case assumed to be short circuit current = 120% $\times I_p$ or 2.3A.

$$W = \frac{1}{2} L I_{sc}^2 = \frac{1}{2} (1 \times 10^{-3}) (2.3)^2 = 2.65 \text{ m Joule}$$

The equation defining energy storage in an inductor is:

$$W = \frac{1}{2} \frac{B A_c H_e^2 \times 10^{-8}}{0.4 \pi} \text{ Joules}$$

Therefore,

$$H\ell_e = (0.4\pi) \frac{2W \times 10^8}{BA_c} =$$

$$= \frac{0.4\pi \times 2 \times 2.65 \times 10^{-3} \times 10^8}{2800 \times 0.84} = 282 \text{ Gilberts}$$

Since $H\ell_e = 0.4\pi NI$, on the basis of $I_{sc} = 2.3A$,

$$N_p = \frac{H\ell_e}{0.4\pi I_{sc}} = \frac{282}{0.4\pi \times 2.3} = 98 \text{ turns}$$

The air gap for the core is determined by knowing that

$$H = \frac{B}{\mu} = 2800 \text{ Oersteds}$$

And assuming that with an air gap

$$I_e \approx I_g, \text{ then}$$

$$I_g = 0.4\pi \frac{NI}{H} = \frac{0.4\pi (98) 2.3}{2800} = 0.1 \text{ cm}$$

With the primary turns defined, each secondary can be calculated from:

$$N_s = \frac{N_p (V_o + \text{rectifier } V_f) (1 - D_{\max})}{V_{in} (\min) D_{\max}}$$

With minor adjustments to give an integral number of turns, the final transformer winding specifications are:

First winding — primary — 97 turns, AWG 24

Second winding — 5 volt — 4 turns, 4 parallel AWG 22

Third winding — 12 volt — 9 turns, 2 parallel AWG 22

Last winding — control — 9 turns, AWG 24 evenly spaced along the full bobbin length

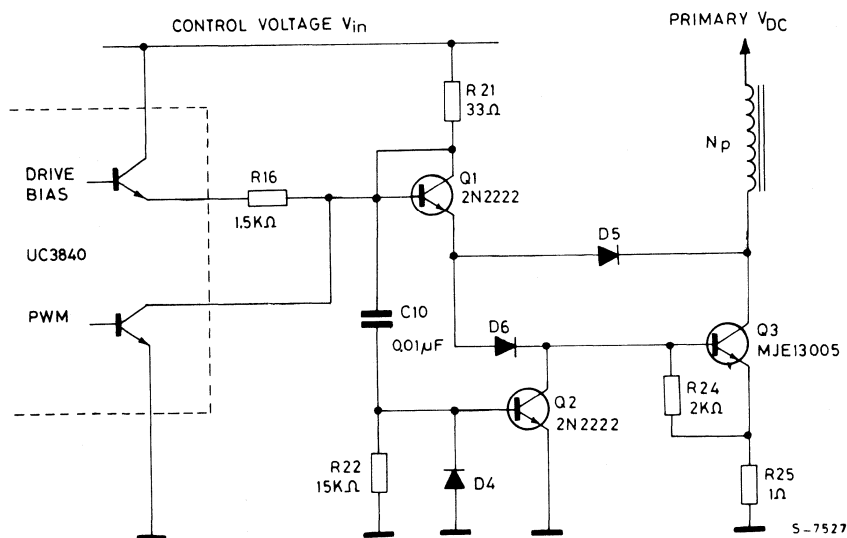
Power switch and drivers

In this application, the peak switch current is 2.3 amps and the peak collector voltage will be approximately 590 volts including the spike caused by leakage inductance. The switching transistor selected is the MJE13005 which has the following characteristics relative to this application:

BV_{ceo}	= 400V
BV_{cer}	= 700V
I_c (cont)	= 4A
h_{fe}	= 8 - 40 @ 2A
t_s	= 1.5μs
t_r	= 0.28μs
t_f	= 0.25μs

While offering inexpensive, high-voltage switching, the MJE13005 needs some support to provide adequate base drive and minimize storage time. This is readily accomplished with the circuitry shown in Figure 2. Prior to obtaining a

Fig. 2 — The high voltage power switch, Q_3 , and its driver interface circuitry



S-7527

start-up signal, the Drive Bias transistor in the UC3840 is off insuring that there is no quiescent current being drawn by any of this interface circuitry. At start-up, the Drive Bias switch turns on providing a pull-up for the UC3840's PWM output. The current through R16 is multiplied by the gain of Q1 to provide a forward base drive in excess of 250mA for the power switch Q3. Diodes D5 and D6 form a Baker clamp to keep Q3 out of hard saturation and improve turn-off, especially at lower collector currents.

Transistor Q2, driven on by the turn-off of Q1, provides a low-impedance path for reverse base current of Q3, and together with the use of the Baker clamp, results in a storage time for Q3 of less than 800nsec.

Snubbing circuits

There are two snubber circuits incorporated into this supply. The network of C12, D7, and R27 is used for load line shaping of transistor Q3 by delaying the voltage rise at the collector of Q3 while the current falls at turn off.

The values for the components in this network are calculated as follows:

$$C12 = \frac{I_{sc} t_f}{2 V_{in(max)}} = \frac{2.3 \times 0.25 \times 10^{-6}}{2 \times 370} \approx 680pF$$

The resistor R27 is selected to discharge C12 with a time constant of one-half the minimum on time, which — under short circuit conditions — is approximately 2.5μs.

$$R27 = \frac{t_{on(min)}}{2C12} = \frac{2.5 \times 10^{-6}}{2 \times 680 \times 10^{-12}} \approx 1.8K\Omega$$

The power dissipated in this resistor is

$$P = \frac{1}{2} C12 (V_{in(max)})^2 f = \frac{1}{2} (680 \times 10^{-12}) (370)^2 40 \times 10^3$$

$$P \approx 2 \text{ watts}$$

The second network of R26, C11, and D2 limits the voltage spike at turn off caused by the leakage inductance of the power transformer. The energy stored in this inductance is transferred into C11 via D2 after the power switch turns off and the voltage rises above the supply plus reset voltage.

C11 is defined by:

$$C11 = \frac{L_e I_{sc}^2}{(V_{reset} + \Delta V_{pp})^2 - V_{reset}^2}$$

Where L_e = Leakage inductance ($\approx 50\mu H$)
 V_{reset} = Reset voltage across transformer (120V)
 V_{pp} = Allowable leakage inductance Voltage spike (100V)

$$\therefore C11 = \frac{50 \times 10^{-6} (2.3)^2}{(120 + 100)^2 - 120^2} = 0.0078 \approx 10nF$$

Resistor R26 is selected to discharge C11 during the remainder of the period leaving a residual voltage equal to the reset voltage at the time turn-off next occurs.

$$R26 = \frac{(V_{reset} + \Delta V_{pp}) 0.63 \tau}{\Delta V_{pp} C11} = \frac{220}{100} \frac{0.63 (25 \times 10^{-6})}{(0.01 \times 10^{-6})} = 3.5K\Omega$$

In this application, R26 was increased to 4.7k due to second order effects such as reverse recovery of D2 which aids in discharging C11.

The power loss in R26 comes from the energy stored in the leakage inductance which is

$$P = \frac{1}{2} L_e I_{sc}^2 f = \frac{1}{2} 50 \times 10^{-6} (2.3)^2 40 \times 10^3$$

$$P \approx 5.3 \text{ watts}$$

but here again, second order effects tend to reduce this value to less than 3 watts in this power supply.

Operating frequency

The frequency is set by R14 and C4 as

$$f = \frac{1}{R_T C_T} = \frac{1}{R_{14} C_4} = \frac{10^3}{12 \times 0.0022} \approx 40kHz$$

Supply start-up

The supply must reliably start with V_{DC} minimum = 250V. The value of R3 + R4 is defined by the total current requirement of the control electronics prior to start. If a start threshold of 12 volts is assumed, total control current is:

UC3840 max	= 7.0mA
R7 + R8	= 0.70mA
R10 + R11	= 0.27mA
C4 charging current	= 0.40mA
R17 + R18	= 0.22mA

$$\text{Total Turn-On Current} = 8.59mA$$

$$\text{and } R3 + R4 = \frac{250 - 12}{8.59} = 27K\Omega$$

Note that R3 and R4 also provide a bleeder path to discharge C1 and C2.

Once start-up is initiated, the control current becomes:

UC3840 max	= 15mA
R16	= 6mA
Q3 Ib (x 0.375 duty cycle)	= 94mA
Total run current	= 115mA

This current must come from C3 until power is available from control winding, N4. This, in conjunction with the start-up time, defines a minimum value for C3.

Although a small soft-start capacitor is incorporated in this supply, its time constant is much shorter than the time to charge the output capacitors with the duty cycle defined by the ramp waveform and the pulse-by-pulse current limit. With the supply fully loaded, start up takes approximately 5msec. During this time, the voltage on C3 cannot fall below the under-voltage threshold.

In defining the start and UV thresholds, one other consideration is the state of the error amplifier. As defined further below, the error amplifier is going to force V_C to 12 volts. If the start threshold is set above this value, the start signal will release the soft-start clamp and arm the driver bias but no PWM output will appear until V_C droops below 12 volts and the output of the error amplifier goes high. To insure soft-start action, the start threshold has been set at 11 volts and the under-voltage level is 8 volts.

Now the value for C3 can be determined from:

$$C3(\min) = \frac{I(\text{start}) \cdot t_{on}}{\Delta V_C}$$

$$= \frac{(115 \times 10^{-3}) (5 \times 10^{-3})}{(11 - 8)} = 192\mu F$$

The start and under-voltage thresholds are defined by R7 and R8 conjunction with the 3 volt threshold and the hysteresis current of the comparator on pin 2 of the UC3840. As the voltage rises on pin2, that pin is sinking 200 μA of current causing an added voltage drop across R7. When pin 2 reaches 3 volts, turn-on is initiated and — at the same time the hysteresis current is removed causing the voltage at pin 2 to jump above 3 volts.

Now, as the power supply attempts to start, the voltage on pin 2 falls and, if it reaches 3 volts from this direction, an under-voltage fault is sensed.

The start voltage at V_C is defined by:

$$V_C(\text{start}) = \frac{3V (R7 + R8)}{R8} + 0.2mA (R7) = 11V$$

while the under-voltage threshold is:

$$V_C (\text{UV fault}) = \frac{3V (R7 + R8)}{R8} = 8V$$

This second equation may be subtracted from the first to yield $R7 = 15K\Omega$, which then defines $R8 = 9.1K\Omega$.

An over-voltage fault in terms of V_{DC} can be calculated by equation:

$$V_{DC} (\text{OV fault}) = 3V \frac{(R5 + R6)}{R6} = 400V, \text{ or}$$

$$R5 = 132 R6$$

Small capacitors (10nF) have been added to both comparator inputs to minimize noise sensitivity.

Feed-forward

This function provides a variable-slope ramp waveform on pin 10 which is one of the inputs to the PWM comparator. This signal is compared with the output from the error amplifier on pin 1, and the pulse width is defined by the time it takes the ramp to rise to the level of the error amplifier's output. If the ramp slope is made proportional to the DC input voltage, a rising input voltage will immediately increase the ramp slope, and correspondingly reduce the pulse width with no change required from the error amplifier's output. The result will be a constant volt-second product delivered to the transformer primary resulting in good open-loop line regulation.

The design procedure used to define the ramp characteristics is to set the ramp slope such that it reaches its peak value at a time equal to the maximum pulse width allowed by the transformer design. This was set at 43% with minimum input voltage and a potential shorted output. The time for the ramp to go from its minimum to maximum value is then:

$$t_{on}(\max) = \frac{0.43}{f} = \frac{0.43}{40 \times 10^3} = 10.75\mu\text{sec}$$

and the slope is:

$$\frac{dv}{dt} (\min) = \frac{V_{pk} - V_{valley}}{t_{on}(\max)}$$

$$= \frac{4.2 - 0.5}{10.75} = 0.344V/\mu\text{sec}$$

and since the slope is determined by:

$$\frac{dv}{dt} = \frac{V_{DC}}{R15 C8}$$

$$\therefore R15 C8 = \frac{200V}{0.34V/\mu s} = 581\mu s$$

With the knowledge that the ramp generator has greatest linearity with currents in the 100μA to 300μA range, we can pick:

$$R15 = 1.5M\Omega \text{ and } C8 \cong 390pF.$$

Duty cycle clamp

The above analysis has provided a maximum duty cycle of 43% at minimum operating voltage. When the AC line voltage is removed, however, the input voltage will fall below 200 volts with the supply still running. As this voltage falls, the ramp slope will reduce and at the same time the error amplifier output will increase in an attempt to maintain regulation. This could extend the pulse width beyond 43% except for the action of the duty cycle clamp divider of R19 and R20 which is set to provide 3.9V at pin 8 with $V_{DC} = 200V$. Therefore, as V_{DC} falls, the voltage on pin 8 will also fall, taking command away from the error amplifier and maintaining a constant pulse width until the Under-Voltage sensing circuit gives a shutdown command.

Voltage control

In this power supply, output voltage regulation is controlled from the primary side by sensing V_C with R10 and R11 and closing a control loop with the error amplifier and 5V reference in the UC3840. The output voltage is then:

$$V_O (5V) = \left(\frac{N2}{N4} \right) V_{ref} \left(\frac{R10 + R11}{R11} \right)$$

Although the UC3840 optimizes this approach by the use of feed-forward which provides first-order automatic line regulation, there will still be inaccuracies caused by inadequate coupling between the windings, IR drops within the windings, and unequal losses in the rectifiers. If greater voltage accuracy is required, the feedback loop must be connected directly to one of the outputs with either an optical coupler or the UC1901 Isolated Feedback Generator used to maintain isolation.

The gain and phase plots for this supply are shown in Figure 3. Overall loop stability is aided by the fact that a discontinuous-mode flyback topology is inherently a single pole system defined by the output load. Its transfer function, excluding the error amplifier, is shown by the dashed curve of Figure 3. The DC gain from the modulator input V_C to the output, V_O , is:

$$\frac{V_O}{V_C} = K \sqrt{\frac{T R_{L \min}}{2L_P}}$$

where K is defined by the feed-forward slope as

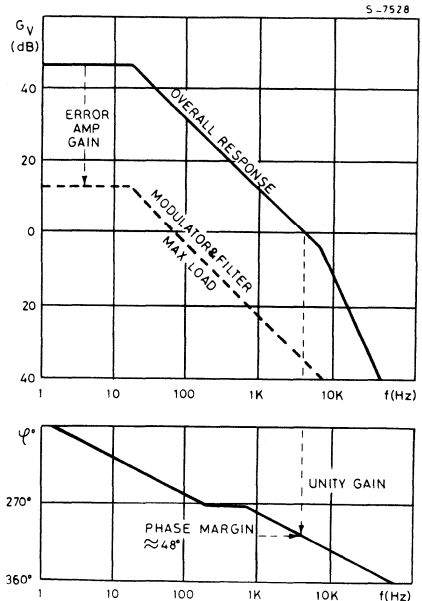
$$K = \frac{(\text{Max duty cycle}) (V_{in \min})}{\text{Ramp peak} - \text{Ramp valley}} = \frac{0.43 \times 200}{4.2 - 0.5}$$

and the minimum load resistance reflected to the primary control supply is:

$$R_{L \min} = \frac{V^2}{P_{O \max}} = \frac{12^2}{50} = 2.88\Omega$$

$$\therefore \frac{V_O}{V_C} = \frac{0.43 \times 200}{4.2 - 0.5} \sqrt{\frac{25 \times 10^{-6} \times 2.88}{2 \times 1 \times 10^{-3}}} = 4.41 = 13\text{db}$$

Fig. 3 – Power supply loop gain and phase



The effective output capacitance, also reflected to the control supply, is:

$$\begin{aligned} C_E &= C14 \left(\frac{N2}{N4} \right)^2 + C13 \left(\frac{N3}{N4} \right)^2 + C3 \\ &= 4700 \left(\frac{4}{9} \right)^2 + 2200 \left(\frac{9}{9} \right)^2 + 200 \\ &= 3328\mu F \end{aligned}$$

The yields an output pole at

$$f_1 = \frac{1}{2\pi R_L C_E} = \frac{10^6}{6.28 (2.88) 3328} = 16.6\text{Hz}$$

The error amplifier is set up for an added DC gain of approximately 35db and a second pole at 8kHz - a frequency well above the overall unity gain point and yet below the roll-off frequency of the error amplifier.

Current limiting

The UC3840 limits current through the power switch, Q3, by sensing the voltage across R25. Pulse-by-pulse current limiting is defined by the divider R17, R18, and the value of R25 as:

$$I_{sc} = \frac{V_{REF} R18}{R25 (R17 + R18)} = \frac{5.0 (10k)}{1\Omega (12k + 10k)} = 2.2 \text{ amps.}$$

If the required pulse width becomes too narrow for the pulse-by-pulse circuitry to respond, the UC3840 contains a second level of protection by initiating a fault shut-down if the voltage across R25 rises to 400mV above the voltage established by R17 and R18 on pin 6. Care must be taken that this threshold is not exceeded by a leading edge spike which might be present on the current waveform.

Fault protection

The UC3840 defines four functions as faults.

- 1. An under-voltage signal on pin 2 (after a start command)
- 2. An over-voltage signal on pin 3
- 3. An external stop command on pin 4
- 4. An over current shut-down from pin 7

Any of these functions will initiate a complete shutdown of the controller with restart defined by the voltage on the reset terminal, pin 5.

If pin 5 is high or open, any fault will latch the supply off and it can only be restarted by reducing the input voltage to zero or by momentarily pulling pin 5 low. Alternatively, grounding pin 5 will cause an automatic restart after any fault shut-down.

CONSTRUCTING THE KIT

It is assumed that the user possesses reasonable electronic assembly skills and therefore detailed

step-by-step instructions have not been considered necessary. Rather, a general assembly procedure is outlined below which, if followed carefully, should offer no problems. Assembly starts by properly orienting the PC board with the assembly drawing shown in Figure 5. This drawing is of the component side of the board - etch side down - with the "Warning - HighVoltage" label at the lower left hand edge.

Test and tie points

Pads have been provided on the PC board for input and output connections and for many internal test points so that complete operation of all portions of the control circuitry can be evaluated. These points are noted in Figure 5 and are listed below:

AC input	(2 pads)
DC input	{ (2 pads each - note that the commons may be separated for alternate polarities)
+ 12V output	
+ 5V output	
H.V. Switching Transistor	(3 pads)

Note: 600V pulses will appear at the collector.

BE CAREFUL OF THIS TEST POINT.

Control Voltage V _C	IC pin 15
Primary Common	IC pin 13 (2 pads)
E/A Compensation	IC pin 1
5.0V Reference	IC pin 16
E/A input	IC pin 17
Drive Bias	IC pin 14
PWM Control	IC pin 12
Ramp Waveform	IC pin 10
S/S Duty Cycle Limit	IC pin 8
Oscillator Frequency	IC pin 9
C/L Limit Sense	IC pin 7
C/L Threshold	IC pin 6
Reset input	IC pin 5
Ext. Stop Input	IC pin 4
OVP Sense Input	IC pin 3
UV/Start Input	IC pin 2

No connections to these points have been included in this kit. It is suggested that the user either supply terminals or solder in small stubs or loops of bus wire so that connections to these test points can easily be made on the component side of the PC board with scope probes or other test instrumentation leads.

Jumpers

There are four jumpers required which are also not included in this kit. Use solid bus wire or a section clipped from the ends of the small resistors. These jumpers are:

- AC input jumper for 110V operation (leave out if 220 VAC is to be used)
- PWM jumper to pin 12
- UV/start jumper to pin 2

Reset jumper on pin 5
(leave out if it is desired to latch the supply off after any fault)

Note that there is nothing connected to pin 4. A low signal here will shut down the supply.

Small signal diodes

The seven small axial lead diodes, D2 through D8 should next be installed insuring correct polarity as shown in Figure 5.

Passive devices

Install the low-power resistors and small capacitors first. Follow with the four high-power resistors, R3, R4, R26 and R27. When inserting R26, keep the body of the resistor $\approx \frac{1}{4}$ inch above the PC board. This resistor will get hot and it is best to have it above, rather than next to C11. At this time, the input diode bridge, D1, and the IC socket can be inserted. Note that pin 1 of the UC3840 is to the front of the PC board.

Large components

Assembly can be completed by installing the remaining components as follows:

- a. Two small signal transistors, Q1 and Q2
- b. Transformer
- c. Electrolytic capacitors: C1, C2, C3, C13 and C14. Check polarity against signs of foil side of PC board.
- d. Power transistor Q3 inserts with its front to the left, or input, inside of the PC board. Insertion is easier if the heat sink is clipped on first.

NOTE: THIS HEAT SINK IS AT THE SAME POTENTIAL AS THE COLLECTOR AND WILL HAVE UP TO 600 VOLTS PRESENT: KEEP IT CLEAR OF OTHER COMPONENTS, TEST LEADS, AND YOUR FINGERS.

- e. Install the 5 volt output rectifier, D9 with its front facing the right, or output side of the board. It also gets a clip-on heat sink.

Check to see that all components are installed and match the drawing of Fig. 5. Insert the UC3840 into the socket.

CHECKOUT PROCEDURES

With the power supply fully assembled, the following checkout procedure is recommended before any input voltage is applied. This procedure is also useful for trouble-shooting a unit which is not operating properly. Checkout will be aided if the user has installed test points at all indicated positions in the PC board. Reference should be made to Figure 5 for test point locations.

1. Insure that there is no AC input voltage applied
2. Double check all connections including diode and capacitor polarities. Insure that the UC3840 is correctly inserted into the socket.
3. Connect a minimum load on one or both outputs equivalent to 25 watts total. i.e., 2Ω on the 5V output and 12Ω on the 12V output. Be careful of the heat from these loads.
4. Install a temporary jumper shorting the base and emitter of Q3 together. Use test points provided on PC board.
5. Connect a 0 to 30 volt, 500mA lab supply to simulate the control voltage, V_C . Connect the positive lead to IC-15 and ground to IC-13. Note that IC-13 will be the ground reference point for all primary side measurements. Set V_C = Zero volts and add a $1k\Omega$, $\frac{1}{2}$ W resistor in shunt across the power supply terminals.
6. Increase V_C to 10 volts and check the following:
 - a. IC-16: should have 5V if the reference is working.
 - b. IC-2: Should be 2.3V if hysteresis current is on.
 - c. IC-14: Should be $< 0.1V$ as Driver Bias is off.
7. Increase V_C to 14 volts and check the following:
 - a. IC-2: Should be 4.7 volts if hysteresis current is off.
 - b. IC-14: Should be 12 volts with Driver Bias on.
 - c. IC-9: Oscillator should show 40kHz exponential waveform.
 - d. Return V_C to Zero volts but leave connected.
8. Apply the high voltage, V_{DC} . This can be done either with a DC lab supply with 300V capability or the input AC line voltage.

A fuse rated at no more than two amps should be in series with the input line to prevent excessive damage in the event of a failure.

NOTE: BE SURE TO USE AN ISOLATION TRANSFORMER WHEN LINE POWER IS USED AS PRIMARY GROUND IS ONE SIDE OF THE LINE.

An AC variac will also be helpful in varying the input voltage.

If a DC power supply is used, connect the positive line to the V_{DC} test point at the top of the board. The negative line will connect to ground on IC-13. Insure that the base-emitter short is still connected to Q3.

9. With V_{DC} = 200 volts, set V_C = 10 volts and check the following:
 - a. IC-14: Should be $< 0.1V$ if Driver Bias is off
 - b. IC-8: Should be $< 0.1V$ if Slow Start clamp is on.
 - c. IC-6: Should be 2.3V to establish current limit threshold.

Fig. 4 — UC3840 PWM control circuit

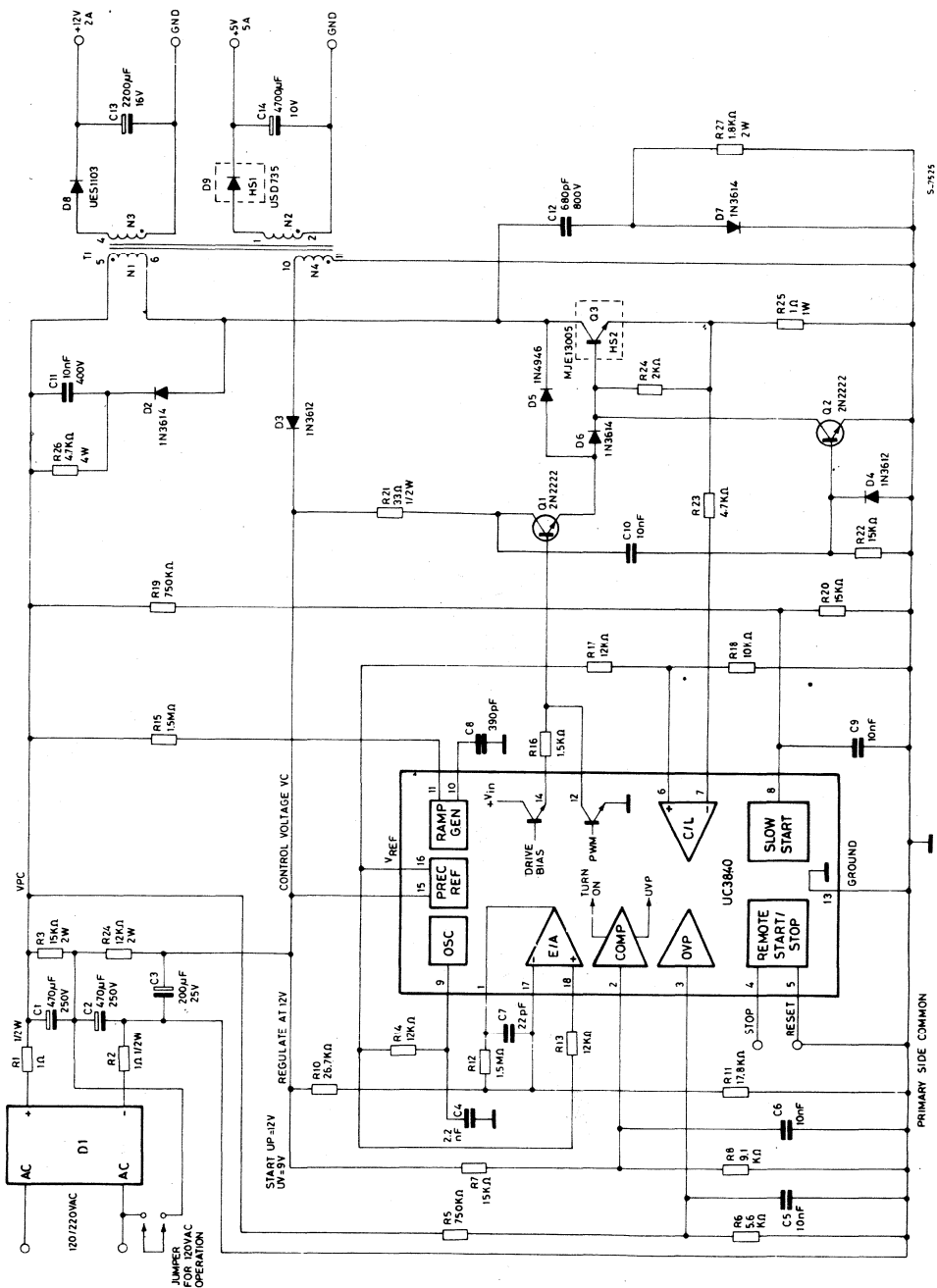
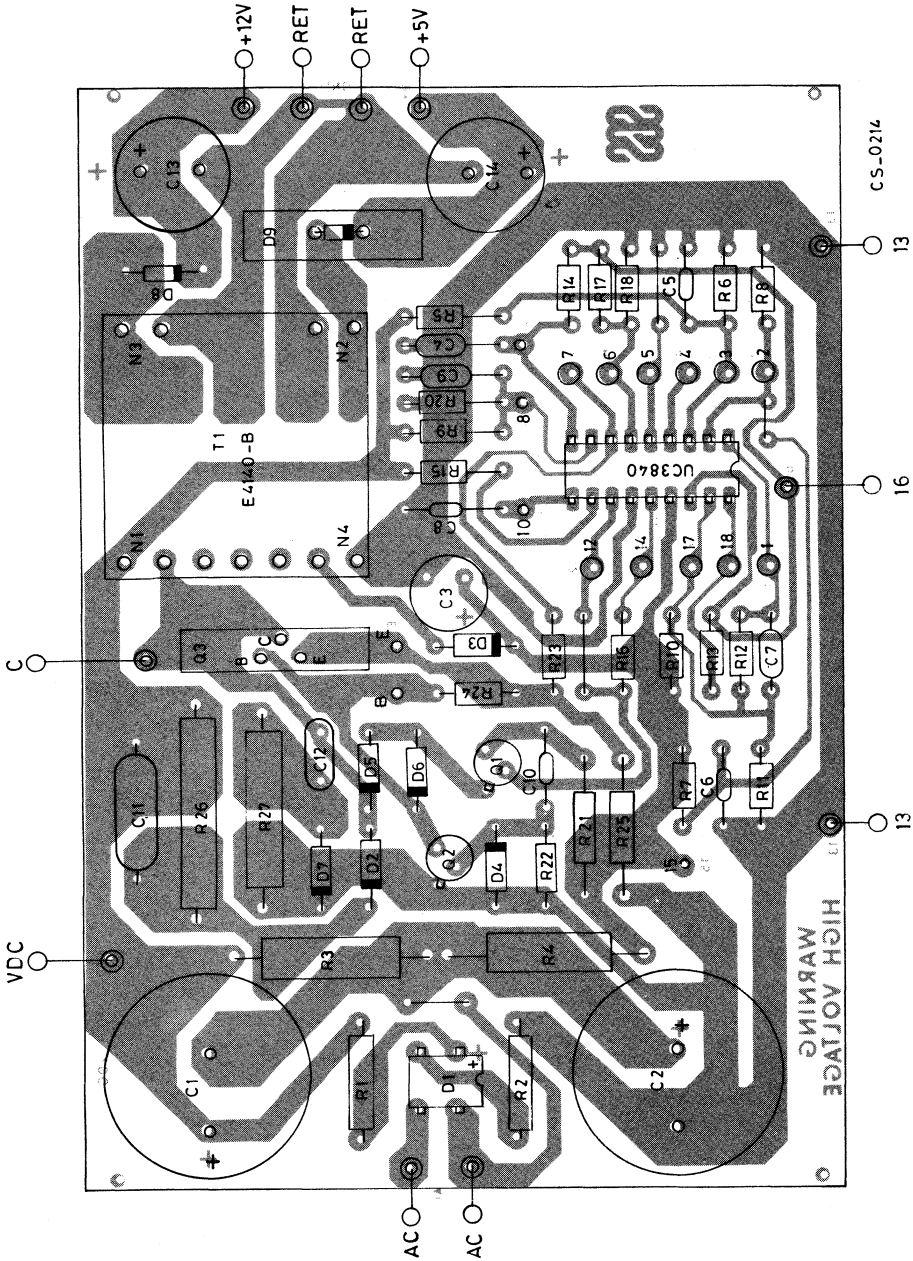


Fig. 5 — P.C. board components layout of the Fig. 4 (1 : 1 scale)



A SECOND-GENERATION IC SWITCH MODE CONTROLLER OPTIMIZED FOR HIGH FREQUENCY POWER MOS DRIVE

INTRODUCTION

Since the introduction of the SG1524 in 1976, integrated circuit controllers have played an important role in the rapid development and exploitation of high-efficiency switching power supply technology. The 1524 soon became an industry standard and was widely second-sourced. Although this device contained all the basic control elements required for switching regulator design, practical power supplies still required other functions which had to be implemented with additional external discrete circuitry.

An additional development within the semiconductor industry was the introduction of practical

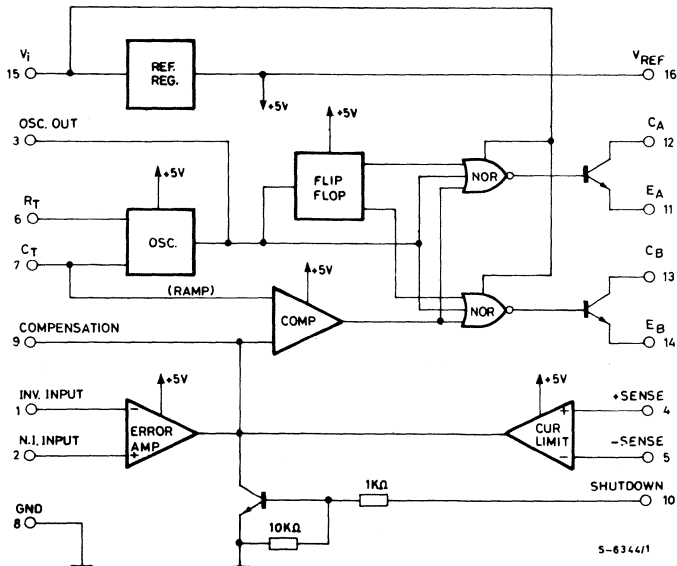
Power Mos which offered the potential of higher efficiencies at higher speeds with resultant lower overall system costs.

In order to be able to take full advantage of the speed capabilities of power MOS, it was necessary to provide high peak currents to the gate during turn-on and turn-off to quickly charge and discharge the gate capacitances of 800 to 2000pF present in higher current units.

The development of a second-generation regulating PWM IC, the SG1525A, and its complimentary output version, the SG1527A, was a direct result of the desire to add more power supply elements to the control IC, as well as to optimize the interfacing of high current power devices.

Fig. 1 — The SG1524 regulating PWM block diagram.

This design was the first complete I.C. control chip for switch mode power supplies.



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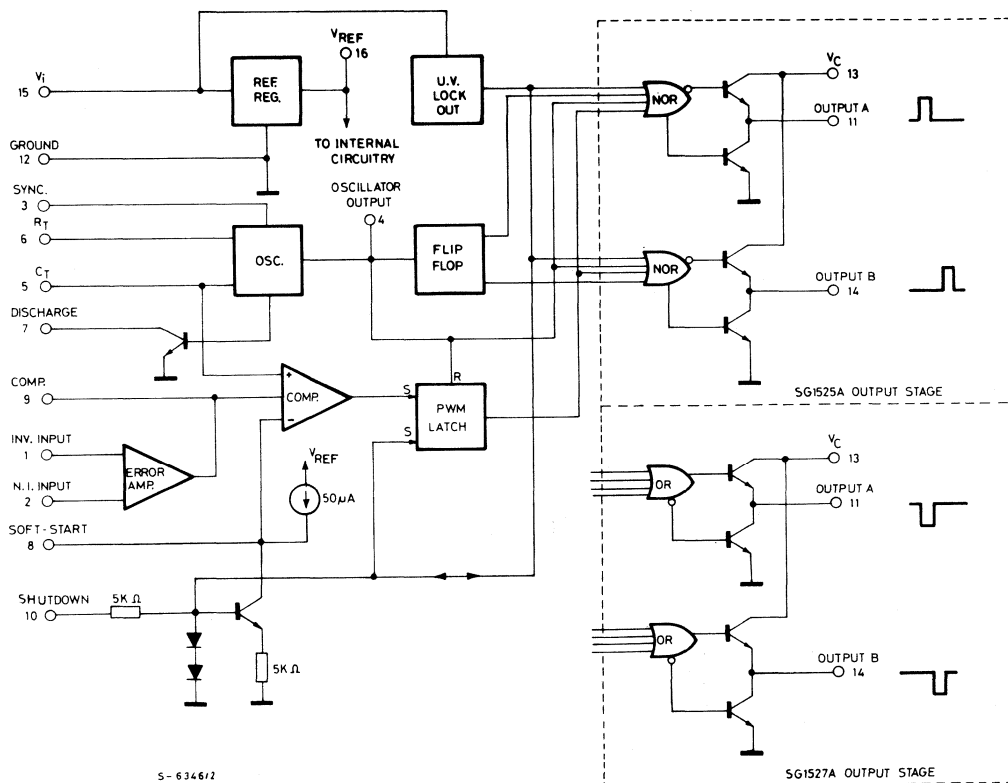
INTEGRATING MORE POWER SUPPLY FUNCTIONS

Having achieved the greatest level of acceptance among users of first generation control chips, the 1524 became the starting point for expanding IC controller capabilities. This early device, shown in Figure 1, contains a fixed-voltage reference source, an oscillator which generates both a clock signal and a linear ramp waveform, a PWM comparator, and a toggle flip-flop with output gating to switch the PWM signal alternately between the two outputs.

With this circuitry already defined, a two pronged development effort was initiated: 1) to add additional features required by most power supply designs and 2) to improve the utility of features already included within the 1524. The resultant block diagram for the SG1525A is shown in Figure 2. Two general comments should be made relative to the overall block diagram. First, in optimizing the output stage for bi-directional, low im-

pedance switching, commitments had to be made as to whether the output should be high or low during the active, or ON state. Since this is application defined there are needs for both output states, so both were developed with the SG1525A device defined by an output configuration which is high during the ON pulse, and the SG1527A configured to remain high during the OFF state. This difference is implemented by a mask option which eliminates inverter Q_4 (see Figure 3) for the SG1527A. In all other respects, the 1525A and 1527A are identical and any description of the 1525A characteristics apply equally to the 1527A. Second, a major difference between this new controller and the earlier 1524 is the deletion of the current limit amplifier. There are so many system considerations in providing current control that it is preferable to leave this as a user-defined external option and allocate the package pins to other, more universally requested functions. Current limiting possibilities are discussed further under shutdown options.

Fig. 2 — The SG1525A family represents a "second generation" of IC controllers.

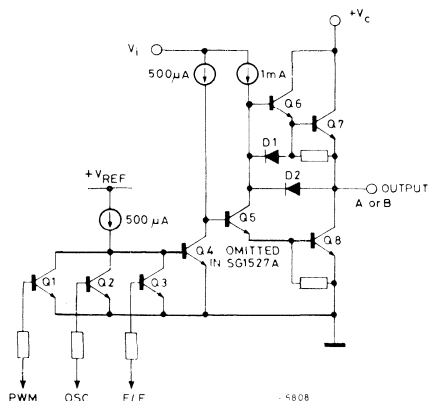


"TOTEM-POLE" OUTPUT STAGE

One of the most significant benefits in using the SG1525A is its output configuration. For the first time it has been recognized in an IC controller that it is more difficult to turn a power switch off than turn it on. With the SG1525A, a high-current, fast transition, low impedance drive is provided for both turn-on and turn-off of an external power transistor or Power MOS. The circuit schematic of one of the two output stages contained within the device is shown in Figure 3. This is a two-state output, either Q_8 is on, forming a low saturation voltage pull-down, or Q_7 is on, pulling the output up to V_C . Note that V_C is a separate terminal from the V_I supply to the rest of the device.

This offers the benefits of potentially operating the output drive from a lower supply than the rest of the circuit for power efficiencies, decoupling of drive transients from more sensitive circuits, and a third terminal for extracting a drive signal. Note that even though V_C can be set either higher or lower than V_I , the output cannot rise higher than approximately $1\frac{1}{2}$ volts below V_I .

Fig. 3 — One of two power output stages contained within the SG1525A which conduct alternately due to the internal flip-flop.



During the transition between states, there is a slight conduction overlap between source and sink which results in a pulse of current flowing from V_C to ground. However, due to the high-speed design configuration of this stage, this current spike lasts for only about 100 ns. A typical current waveform at V_C is shown in Figure 4. This transient will normally be decoupled from the rest of the control power by a $0.1\mu\text{F}$ capacitor from V_C to ground but it should not, otherwise, cause a problem unless very high frequency operation is contemplated where it will contribute to overall device power dissipation, by becoming a significant portion of the total duty cycle.

The output saturation characteristics of this stage are shown in Figure 5. The source transistor, Q_7 is

a straight forward Darlington and its saturation voltage remains between 1 and 2V out to 400 mA under the assumption that $V_I \geq V_{CC}$. The sink transistor, Q_8 , however, has a non-uniform characteristic which needs explanation. At low sink currents, the 1mA current source through Q_5 insures a very low saturation voltage at the output. As load current increases past 50 mA, Q_8 begins to come out of saturation for lack of base drive but only up to about 2V. Here diode D_2 becomes forward biased shunting a portion of the load current through Q_5 to boost the base current into Q_8 . With this circuit, the sink transistor can both support high peak discharge currents from a capacitive load, as well as insure the low static hold-off voltage required for bipolar transistors.

Fig. 4 — Current "spiking" on the V_C terminal caused by conduction overlap between source and sink is minimized by high-speed design techniques.

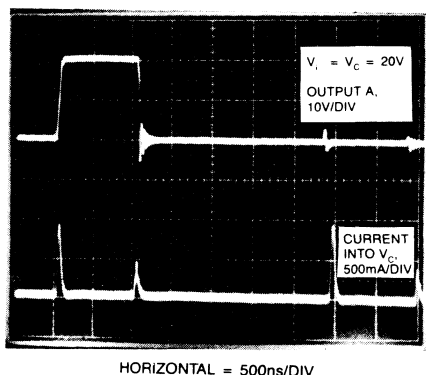
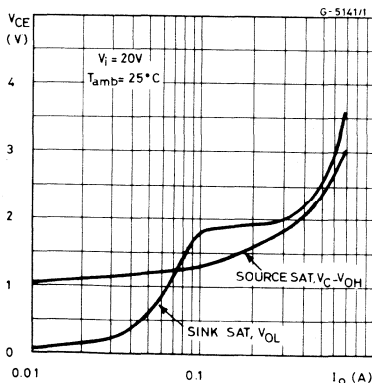


Fig. 5 — The output saturation characteristics of the SG1525A provide both high drive current and low hold-off voltage.



A typical output configuration for a push-pull bipolar transistor power stage is shown in Fig. 6. With a steady state base drive current from the SG1525A of 100mA, this stage should be able to switch 1 to 5A of transformer primary current, depending

upon the choice of transistors. The sum of R_1 and R_2 determine the maximum steady state output current of the SG1525A while their ratio defines the voltage across C_2 which, at turn off, becomes the reverse V_{BE} for Q_1 . With the values given, the output current and voltage waveforms are shown in Figure 7 for a one microsecond pulse. If power MOS are used for the output switches as shown in Figure 8, the interfacing circuitry can become even simpler with only a small series gate resistor potentially required to damp spurious oscillations within the power device.

Fig. 6 – A typical push-pull converter power stage using external bipolar power transistor switches.

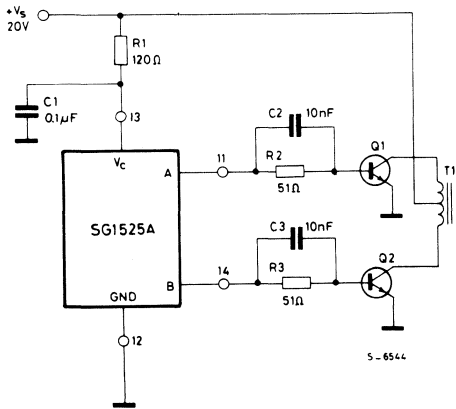
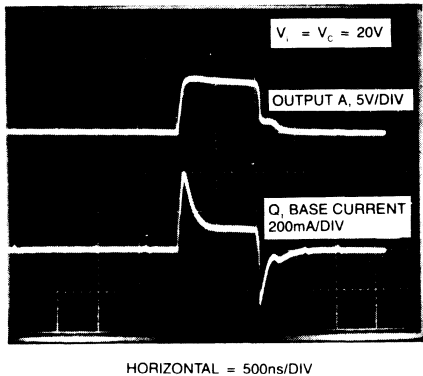


Fig. 7 – Base current waveforms (Figure 6 circuit) show the enhanced turn-on and turn-off current possible with the SG1525A.



Push-pull direct transformer drive is also particularly advantageous with SG1525A as shown in Figure 9. A version of this configuration is required for isolation when the control circuit is referenced

to the secondary side of an off-line power system, and to provide level shifting of drive signals for ½ bridge and full bridge switching. The configuration of Figure 9 has a couple of important advantages. First, by connecting the drive transformer primary directly between the outputs of the SG1525A, no center-tap is needed and the full primary is driven with opposite polarities. Secondly, between each output pulse, both outputs are pulled to ground which effectively shorts the two ends of the primary winding together coupling a low-impedance turn-off signal to the switching transistors.

A useful single-ended configuration, typical of buck regulators, is shown in Figure 10. Here the SG1525A outputs are grounded and the PWM signal is taken from the Vc terminal which switches close to ground during each clock period as the internal source transistors are alternately sequenced.

Fig. 8 – Replacing bipolar transistors with power MOS provides even greater simplicity due to the low driving impedances of the SG1525A in each transition.

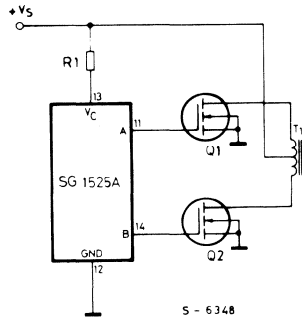
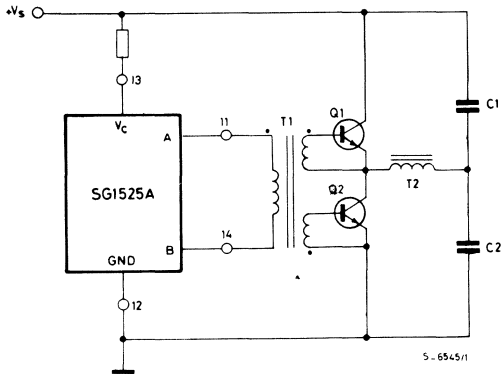
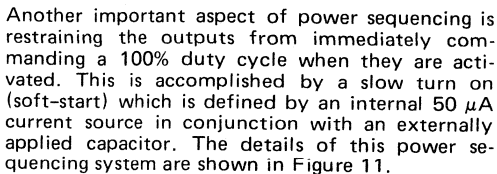


Fig. 9 – The SG1525A is ideally suited for driving a low-power base drive transformer and eliminates the need for a primary center-tap.



voltage which is less than the voltage required to turn the outputs on. This clamp is maintained until the supply reaches approximately 8V insuring that all the remaining SG1525A circuitry is fully operational prior to enabling the outputs. The clamp reactivates when the supply is lowered to approximately 7.5V. There is about 500mV of hysteresis built in to eliminate clamp oscillation at threshold.



Q₃ and Q₄ are the output gates normally driven by the oscillator through D₂ to provide output blanking between pulses. (One of these transistors is shown as Q₂ in Figure 3). At low supply voltages, Q₂ conducts with base drive from the 20μA current source. Q₂ provides three functions. First, current through R₄ activates the output gates with minimum voltage drop. Second, current through R₅ activates the shutdown transistor Q₅ holding the soft-start capacitor, C_{SS}, discharged. Third, R₂ provides a small bucking voltage across R₃ for hysteresis at the switch point.

When the input voltage becomes high enough to provide a little more than one volt at the base of Q_1 , that transistor turns on. This turns off Q_2 , activating the outputs and allowing C_{SS} to begin to charge from the internal $50\ \mu A$ current source. The time to reach approximately 50% duty cycle will be

$$t = \left(\frac{2 \text{ volts}}{50 \mu A} \right) C_{ss}$$

POWER SUPPLY SHUTDOWN

An important part of any PWM controller is the ability to shut it down at any time for a variety of reasons, including system sequencing requirements or fault protection. Several options are available to the user of the SG1525A, which require an understanding of the capability of the shutdown terminal, pin 10. Referring to Figure 11, the base of Q_5 is turned on by a signal which is clamped to approximately 1.4V by the action of D_1 and the V_{BE} of gates Q_3 and Q_4 . This holds the outputs off and keeps C_{SS} discharged by Q_5 which, with R_9 , becomes a 100 μ A net current sink.

If, during normal operation, pin 10 is pulled high, three things happen. First, the outputs are turned off within 200ns through D_1 . Second, the PWM latch is set by Q_6 so that even if the signal at pin 10 were to disappear, the outputs would stay off for the duration of that period, being reset by the next clock pulse. Third, Q_5 is activated commencing a 100 μ A discharge of C_{SS} . However, if the activation pulse on pin 10 has a duration shorter than $\frac{1}{3}$ of the clock period, the voltage on C_{SS} will remain high and soft-start will not be reactivated. Naturally, a fixed signal on pin 10 will eventually discharge C_{SS} , recycling soft-start.

Thus, the shutdown pin provides both sequencing capability as well as a convenient port for protective functions, including pulse-by-pulse current limiting.

REGULATING PWM PERFORMANCE IMPROVEMENTS

The SG1525A also offers significant performance and application improvements in almost all of the additional basic functions of a PWM over those obtainable with earlier devices. A general description of these features is outlined below:

Reference Regulator: The output voltage of this regulator is internally trimmed to $5.1V \pm 1\%$ during manufacture, eliminating the need for adjusting potentiometers in most applications.

Error Amplifier: SG1525A uses the same basic transconductance amplifier as the SG1524 with an important difference: it is powered by V_i rather than V_{REF} . Now the input common-mode range includes V_{REF} eliminating the need for a voltage divider with its attendant tolerances. An additional feature relative to the error amplifier is that the shutdown circuitry feeds into a separate input to the PWM comparator allowing pulse termination without affecting the output of the error amplifier which might have a slow recovery, depending upon the external compensation network selected. An important benefit of a transconductance amplifier is the ease with which its current mode output can be over-ridden by other external controlling signals.

PWM Comparator: The significant benefit of the SG1525A's PWM comparator is in its following latch. A common problem with earlier devices was that any noise or ringing on the output of the error amplifier would affect multiple crossings of the oscillator ramp signal resulting in multiple pulsing at the comparator's output. The SG1525A's latch terminates the output pulse with the first signal from the comparator, insuring that there can be only a single pulse per period, removing all jitter or threshold oscillation from the system. Another important advantage of this latch is the ability to easily implement digital or pulse-by-pulse current limiting by merely momentarily activating the shutdown circuitry within the SG1525A. This could be as simple as connecting pin 10 to a ground-referenced current sensing resistor. For greater accuracy, some added gain may be advantageous. Once a current signal causes shutdown, the output will remain terminated for the duration of the period, even though the current signal is now gone. An oscillator clock signal resets the latch to start each period anew.

Oscillator: The functions of the oscillator within the SG1525A have been broadened in two important aspects. One is the addition of a synchronization terminal, pin 3, allowing much easier interfacing to an external clock signal or to synchronize multiple SG1525A's together. The other is the separation of the oscillator's discharge network from its charging current source for deadtime control. Reference should be made to the schematic of Figure 12 for an understanding of the operation of this circuit. The heart of this oscillator is a double-threshold comparator, Q_7 and Q_8 , which allows the timing capacitor to charge to an upper threshold by means of the current source defined by R_T and mirrored by Q_1 and Q_2 . The comparator then switches to a lower threshold by turning on Q_{10} and discharges C_T through Q_3 and Q_4 with a rate defined by R_D . As long as C_T is discharging, the clock output is high, blanking the outputs.

Since the overall oscillator frequency is defined by the sum of the charge and discharge times, there are three elements now in the frequency equation which is approximately:

$$f \approx \frac{1}{C_T (.07 R_T + 3 R_D)}$$

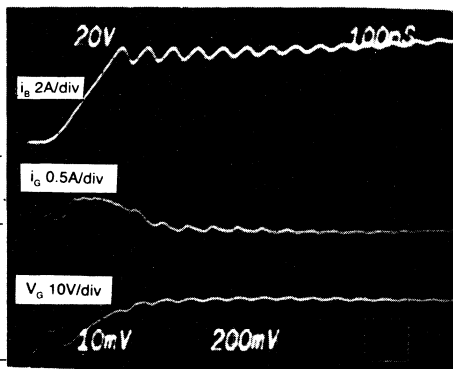
External synchronization can easily be accomplished with a 2.8V positive pulse at pin 3. This will turn on Q_9 , lowering the comparator threshold below wherever the voltage on C_T may happen to be. Two factors should be considered: First, the voltage on C_T determines the amplitude of the PWM ramp, and if the sync occurs too early, the loop gain will be higher and the resolution may be worse. Second, the sync circuit is regenerative within 200ns; and, while a wider pulse can be used, C_T will not begin to recharge as long as the sync pin is high. For synchronizing multiple SG1525A devices together, one need only to define a master with the correct $R_T C_T$ time constant, connect its output pin to the slave sync pins, and set each slave $R_T C_T$ for a time constant 10-20% longer than the master.

A 200 WATT, OFF-LINE, FORWARD CONVERTER

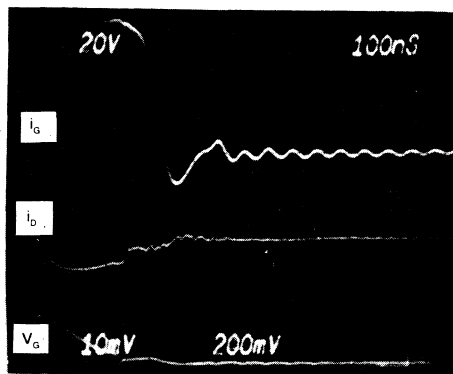
The ease of interfacing the SG1525A into a practical power supply system can be illustrated by the off-line, power converter shown in Figure 13. This 200W supply places the control circuitry on the primary side of the power transformer where direct coupling can be used to drive the power switch. While simplifying the drive electronics, this configuration usually requires an isolated voltage feedback signal which is most easily accomplished by an optocoupler driven by some type of voltage regulator IC such as a L123 or LM723. One other undefined block in Figure 13 is the auxiliary power supply which supplies the low voltage, low current bias supply for the SG1525A and the drive for Q_1 , the power switch. The choice of the SGSP479 power MOS for this switch keeps the total power requirements from the auxiliary supply at less than 1W; readily implemented with a small, line-driven transformer.

This converter is designed to operate at 150kHz which is accomplished by running the SG1525A at 300kHz and using only one of the outputs. This also automatically insures that the duty cycle can never be greater than 50%, a requirement of the power transformer in this configuration. The high operating frequency allows the output filter's roll-off to be set at 12kHz, greatly simplifying the overall loop stability considerations as adequate response can be achieved with only the single-pole compensation of the error amplifier provided by the 0.05 μ F capacitor on pin 9.

The totem-pole output of the SG1525A is used to advantage to drive Q_1 by providing a 400 mA peak current to charge and discharge the power MOS gate capacitance while keeping overall power dissipation low. Waveform photographs of this operation are shown in Figure 14.

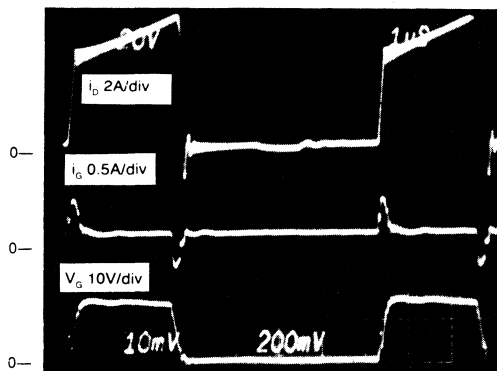


b) Risetime
 $\approx 90\text{ns}$



c) Falltime
 $\approx 30\text{ns}$

Fig. 14 — Current and voltage waveforms for the 200W off-line forward converter with a SG1525A direct driven power MOS switch (operating frequency is 150kHz with output current equal to 40A).



1 μ s/div
a) Waveforms of i_o , i_g , V_g

When operating at full load, the efficiency of this converter is 73% with by far the greatest power losses occurring in the output rectifiers—even though Schottky devices have been selected.

Switching losses have been minimized by the fast current transitions, primarily defined by the leakage inductance of the transformer. Although this switching time could probably be even further reduced, there could be problems with current spikes during rise time due to Schottky rectifier capacitance.

Current limiting for this converter is provided by measuring the current in SGSP479 with the 0.1 Ω resistor in series with the source and using this voltage to activate the shutdown circuitry within the SG1525A. While this will provide a fast-acting short circuit protection on a pulse-by-pulse basis, a comparator may need to be added for a more accurate current limit threshold.

500W, 100kHz, Off-Line, Half-Bridge Converter:

- | | | | |
|----|---|----|---|
| T1 | Core: Ferroxx 486T250-3C8
Pri: 14T #22AWG
Sec (2): 7T #22AWG | T3 | Core: Ferroxx 486T250-3C8
Pri: 1T
Sec: 20T, C.T. #22AWG |
| T2 | Core: Ferroxx EC52-3C8 (EE)
Pri: 14T, 2 layers, 2 #16AWG in parallel
Sec (2): each 2T, C.T., copper strap .01" x 0.8" | T4 | 117V/220V, 25V, 0.15A, 50-60 Hz |
| | | L1 | Core: Ferroxx IF30-3C8
4 turns. 5 #12AWG in parallel |

The circuit shown in Figure 15 uses a pair of SGSP479 power MOS in a half-bridge configuration with the SG1525A chip referenced to the secondary side of the power transformer.

The power MOS gates are driven directly from the control chip output through step down and isolation transformer T1. The SG1525A output terminals (pins 11 and 14) provide active pull-up and pull-down (dual source/sink) for the primary of T1. This provides the fast, high current turn-on and turn-off pulses needed for the power MOS gates. In addition, the two ends of the primary windings are shorted to ground during deadtime,

which prevents accidental turn-on by transients. Note that the current supplied by the SG1525A outputs drops to a small value when the gate capacitance has been charged or discharged to the desired gate voltage. Damping resistors with series blocking capacitors across the two secondaries of T1 minimize ringing due to the power MOS gate capacitance and the inductance of T1 and lead inductance, particularly during deadtime.

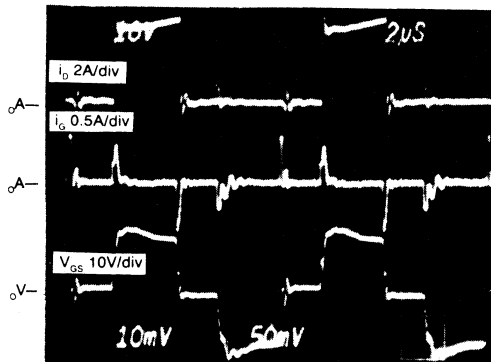
Deadtime for the SG1525A is set very simply by a single resistor between pins 5 and 7. Only a small amount of deadtime is needed since the power MOS have no storage time and a very short delay time.

Slow turn-on is accomplished by a single capacitor at pin 8.

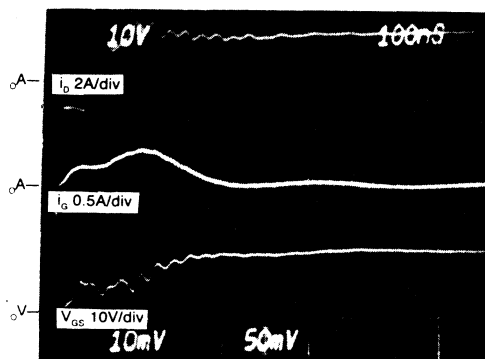
Current limiting is provided by current transformer T3 in series with the primary of the power transformer T2. The signal is rectified, threshold adjusted and sent to the shutdown terminal, pin 10, of the SG 1525A.

Waveforms of the converter are shown in the scope photos of Figure 16. Current rise and fall times are 20ns and 10ns.

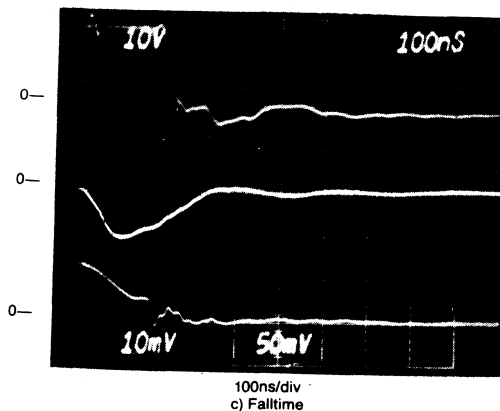
Fig. 16 — Performance waveforms for the half-bridge, 500W, 100kHz converter with output current of 80A.



2μs/div
a) Waveforms of i_o , i_g , V_g



100ns/div
b) Risetime



IMPROVED PERFORMANCE; LESS COMPLEXITY

Although power supply designers for some time now have had an ever widening inventory of IC components available to ease their design tasks, the final measure of improvement has to be in terms of system performance versus cost. With fewer interface components to the power stages, freedom from potentiometer adjustments, protected start-up and shut-down, a built in soft-start network and several additional system-level features, the SG1525A provides a significant contribution to both performance and costs while simultaneously making the designer's task easier. With these accomplishments, it is clear that this device truly does represent a step-function improvement, introducing a second-generation of power control components.

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A DESIGNER'S GUIDE TO THE L200 VOLTAGE REGULATOR

Delivering 2A at a voltage variable from 2.85V to 36V, the L200 voltage regulator is a versatile device that simplifies the design of linear supplies. This design guide describes the operation of the device and its applications.

The introduction of integrated regulator circuits has greatly simplified the work involved in designing supplies. Regulation and protection circuits required for the supply, previously realized using discrete components, are now integrated in a single chip. This has led to significant cost and space saving as well as increased reliability. Today the designer has a wide range of fixed and adjustable, positive and negative series regulators to choose from as well as an increasing number of switching regulators.

The L200 is a positive variable voltage regulator which includes a current limiter and supplies up to 2A at 2.85 to 36V.

The output voltage is fixed with two resistors or, if a continuously variable output voltage is required, with one fixed and one variable resistor.

The maximum output current is fixed with a low value resistor. The device has all the characteristics common to normal fixed regulators and these are described in the datasheet. The L200 is particularly suitable for applications requiring output voltage variation or when a voltage not provided by the standard regulators is required or when a special limit must be placed on the output current.

The L200 is available in two packages:

Pentawatt — Offers easy assembly and good reliability. The guaranteed thermal resistance ($R_{th j-case}$) is $3^{\circ}C/W$ (typically $2^{\circ}C/W$) while if the device is used without heatsink we can consider a guaranteed junction-ambient thermal resistance of $50^{\circ}C/W$.

TO-3 — For professional and military use or where good hermeticity is required.

The guaranteed junction-case thermal resistance is $4^{\circ}C/W$, while the junction-ambient thermal resistance is $35^{\circ}C/W$.

The junction-case thermal resistance of this package, which is greater than that of the Pentawatt, is partly compensated by the lower contact resistance with the heatsink, especially when an electrical insulator is used.

CIRCUIT OPERATION

As can be seen from the block diagram (fig. 1) the voltage regulation loop is almost identical to that of fixed regulators. The only difference is that the negative feedback network is external, so it can be varied (fig. 3). The output is linked to the reference by:

$$V_{out} = V_{ref} \left(1 + \frac{R_2}{R_1} \right) \quad (1)$$

Considering V_{out} as the output of an operational amplifier with gain equal to $G_v = 1 + R_2/R_1$ and input signal equal to V_{ref} , variability of the output voltage can be obtained by varying R_1 or R_2 (or both). It's best to vary R_1 because in this way the current in resistors R_1 and R_2 remains constant (this current is in fact given by V_{ref}/R_1).

(Equation (1) can also be found in another way which is more useful in order to understand the descriptions of the applications discussed.

$$V_{out} = R_1 i_1 + R_2 i_2$$

and since in practice $i_1 \gg i_4$ (i_4 has a typical value of $10 \mu A$) we can say that

$$V_{out} = R_1 i_1 + R_2 i_1 \quad \text{with} \quad i_1 = \frac{V_{ref}}{R_1}$$

Therefore

$$V_{out} = \frac{R_2}{R_1} V_{ref} + V_{ref} = V_{ref} \left(1 + \frac{R_2}{R_1} \right)$$

In other words R_1 fixes the value of the current circulating in R_2 so R_2 is determined.

Fig. 1 - Block diagram

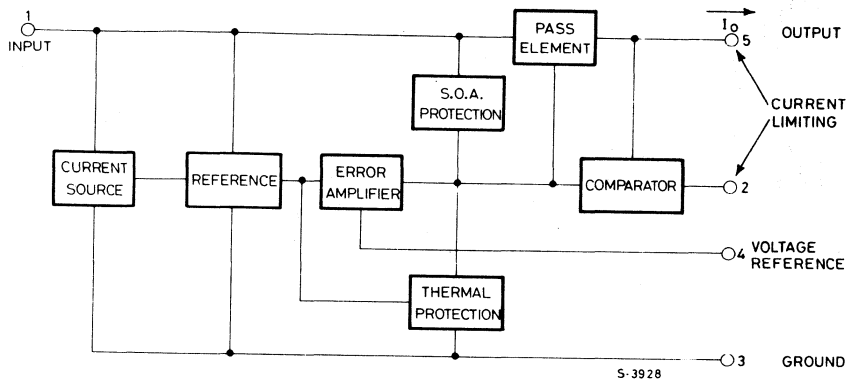


Fig. 2 - Schematic diagram

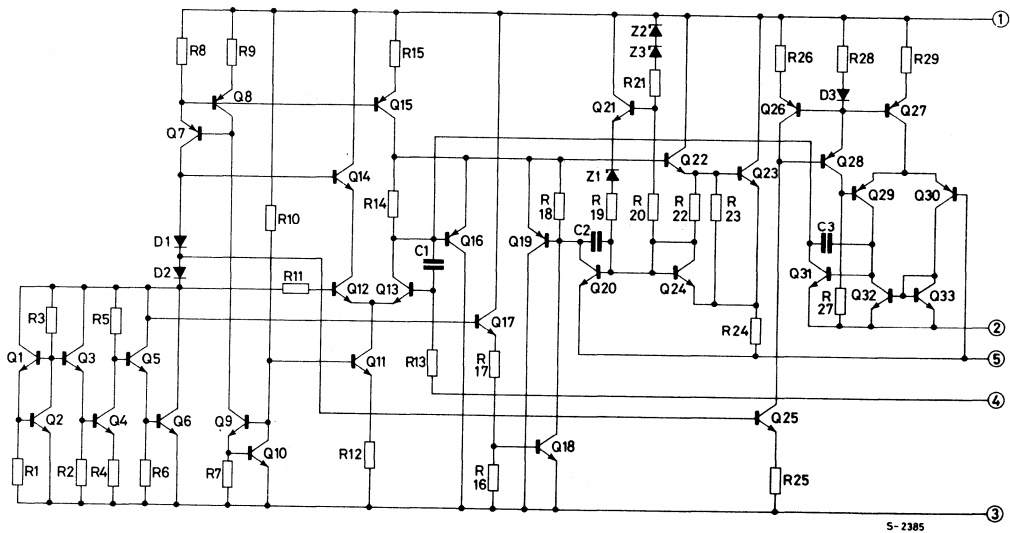
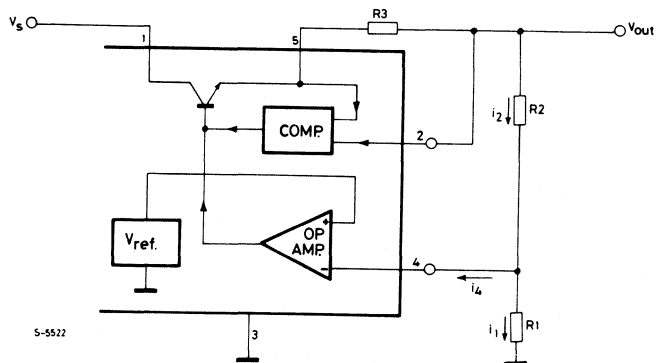


Fig. 3

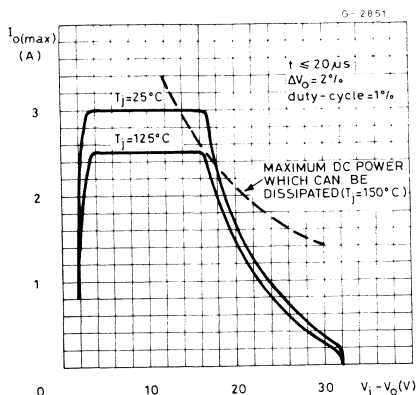


Overload protection

The device has an overload protection circuit which limits the current available.

Referring to fig. 2, R24 operates as a current sensor. When at the terminals of R24 there is a voltage drop sufficient to make Q20 conduct, Q19 begins to draw current from the base of the power transistor (darlington formed by Q22 and Q23) and the output current is limited. The limit depends on the current which Q21 injects into the base of Q20. This current depends on the drop-out and the temperature which explains the trend of the curves in fig. 4.

Fig. 4



Thermal protection

The junction temperature of the device may reach destructive levels during a short circuit at the output or due to an abnormal increase in the ambient temperature. To avoid having to use heatsinks which are costly and bulky, a thermal protection circuit has been introduced to limit the output current so that the dissipated power does not bring the junction temperature above the values allowed. The operation of this circuit can be summarized as follows.

In Q17 there is a constant current equal to:

$$\frac{V_{ref} - V_{BE17}}{R17 + R16} \quad (V_{ref} = 2.75V \text{ typ})$$

The base of Q18 is therefore biased at:

$$V_{BE18} = \frac{V_{ref} - V_{BE17}}{R16 + R17} \cdot R16 \approx 350 \text{ mV}$$

Therefore at $T_j = 25^\circ\text{C}$ Q18 is off (since 600 mV is needed for it to start conducting). Since the V_{BE} of a silicon transistor decreases by about 2 mV/ $^\circ\text{C}$, Q18 starts conducting at the junction temperature:

$$T_j = \frac{600 - 350}{2} + 25 = 150^\circ\text{C}$$

Current limitation

The innovative feature of this device is the possibility of acting on the current regulation loop, i.e. of limiting the maximum current that can be supplied to the desired value by using a simple resistor (R3 in fig. 2). Obviously if $R3 = 0$ the maximum output current is also the maximum current that the device can supply because of its internal limitation.

The current loop consists of a comparator circuit with fixed threshold whose value is V_{sc} . This comparator intervenes when $I_o \cdot R3 = V_{sc}$, hence

$$I_o = \frac{V_{sc}}{R3} \quad (V_{sc} \text{ is the voltage between pins 5 and 2 with typical value of } 0.45V).$$

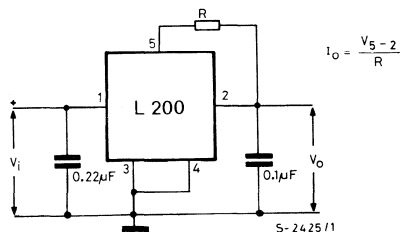
Special attention has been given to the comparator circuit in order to ensure that the device behaves as a current generator with high output impedance.

TYPICAL APPLICATIONS

Programmable current regulator

Fig. 5 shows the device used as current generator. In this case the error amplifier is disabled by short-circuiting pin 4 to ground.

Fig. 5



The output current I_o is fixed by means of R:

$$I_o = \frac{V_{5-2}}{R}$$

The output voltage can reach a maximum value $V_i - V_{drop} \approx V_i - 2V$ (V_{drop} depends on I_o).

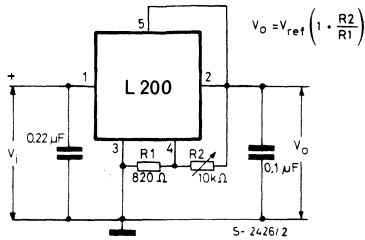
Programmable voltage regulator

Fig. 6 shows the device connected as a voltage regulator and the maximum output current is the maximum current that the device can supply. The output voltage V_o is fixed using potentiometer R2. The equation which gives the output voltage is as follows:

$$V_o = V_{ref} \left(1 + \frac{R2}{R1} \right)$$

By substituting the potentiometer with a fixed resistor and choosing suitable values for R1 and R2, it is possible to obtain a wide range of fixed output voltages.

Fig. 6



The following formulas and tables can be used to calculate some of the most common output voltages. Having fixed a certain V_O , using the previous formula, the maximum value is:

$V_{O \max} = V_{ref \max} (1 + \frac{R2_{\max}}{R1_{\min}})$ and the minimum value is:

$$V_{O \min} = V_{ref \min} (1 + \frac{R2_{\min}}{R1_{\max}})$$

The table below indicates resistor values for typical output voltages:

$V_O \pm 4\%$	$R1 \pm 1\%$	$R2 \pm 1\%$
5V	1.5 kΩ	1.2 kΩ
12V	1 kΩ	3.3 kΩ
15V	750 Ω	3.3 kΩ
18V	330 Ω	1.8 kΩ
24V	510 Ω	3.9 kΩ

Programmable current and voltage regulator

The typical configuration used by the device as a voltage regulator with external current limitation is shown in fig. 7. The fixed voltage of 2.77V at the terminals of R1 makes it possible to force a constant current across variable resistor R2. If R2 is varied, the voltage at pin 2 is varied and so is the output voltage.

The output voltage is given by:

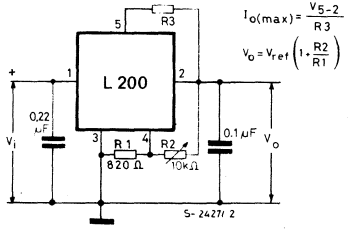
$$V_O = V_{ref} \cdot (1 + \frac{R2}{R1}), \text{ with } V_{ref} = 2.77V \text{ typ}$$

and the maximum output current is given by:

$$I_{O \max} = \frac{V_{5-2}}{R3} \text{ with } V_{5-2} = 0.45V \text{ typ.}$$

To maintain a sufficient current for good regulation the value of R1 should be kept low. When there is no load, the output current is $V_{ref}/R1$. Suitable values of R1 are between 500Ω and 1.5 kΩ. If the load is always present the maximum value for R1 is limited by the current value (10 μA) at the input of the error amplifier (pin 4).

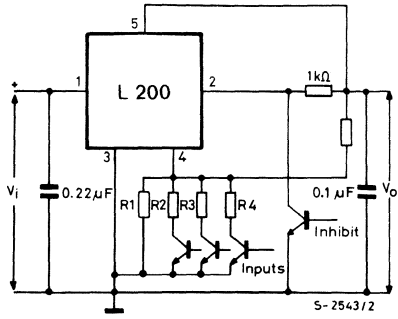
Fig. 7



Digitally selected regulator with inhibit

The output voltage of the device can be regulated digitally as shown in fig. 8. The output voltage depends on the divider formed by R5 and a combination of the divider formed by R1, R2, R3 and P2. The device can be switched off with a transistor. When the inhibit transistor is saturated, pin 2 is brought to ground potential and the output voltage does not exceed 0.45V.

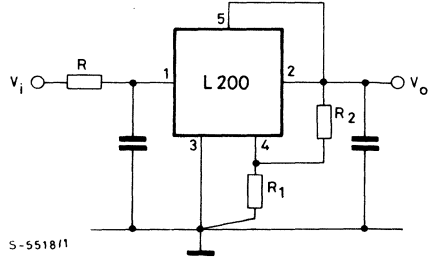
Fig. 8



Reducing power dissipation with dropping resistor

If may sometimes be advisable to reduce the power dissipated by the device. A simple and economic method of doing this is to use a resistor connected in series to the input as shown in fig. 9. The input-output differential voltage on the device is thus reduced.

Fig. 9



The formula for calculating R is as follows:

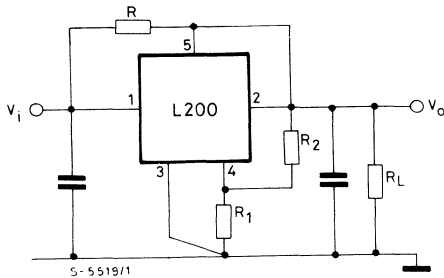
$$R = \frac{V_{i \min} - (V_o + V_{\text{drop}})}{I_o}$$

Where V_{drop} is the minimum differential voltage between the input and the output of the device at current I_o . $V_{i \min}$ is the minimum input voltage. V_o is the output voltage and I_o the output current.

With constant load, resistor R can be connected between pins 1 and 2 of the IC instead of in series with the input (fig. 10). In this way, part of the load current flows through the device and part through the resistor. This configuration can be used when the minimum current by the load is:

$$I_{o \min} = \frac{V_{\text{drop}}}{R} \quad (\text{instant by instant})$$

Fig. 10



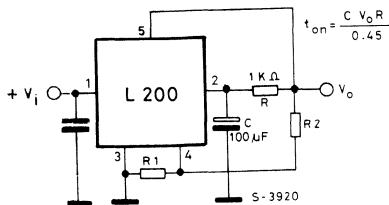
Soft start

When a slow rise time of the output voltage is required, the configuration in fig. 11 can be used. The rise time can be found using the following formula:

$$t_{on} = \frac{C V_o R}{0.45}$$

At switch on capacitor C is discharged and it keeps the voltage at pin 2 low; or rather, since a voltage of more than 0.45V cannot be generated between pins 5 and 2, the V_o follows the voltage at pin 2 at less than 0.45V.

Fig. 11



Capacitor C is charged by the constant current i_c .

$$i_c = \frac{V_{sc}}{R}$$

Therefore the output reaches its nominal value after the time t_{on} :

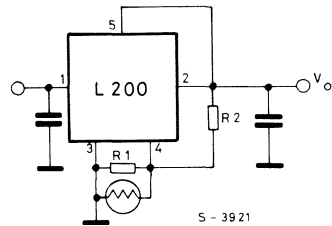
$$V_o - V_{sc} = \frac{i_c \cdot t_{on}}{C}$$

$$t_{on} = C \cdot \frac{(V_o - 0.45)}{0.45} \cdot R \cong \frac{C V_o R}{0.45}$$

Light controller

Fig. 12 shows a circuit in which the output voltage is controlled by the brightness of the surrounding environment. Regulation is by means of a photoresistor in parallel with R_1 . In this case, the output voltage increases as the brightness increases. The opposite effect, i.e. dimming the light as the ambient light increases, can be obtained by connecting the photoresistor in parallel with R_2 .

Fig. 12



Light dimmer for car display

Although digital displays in cars are often more aesthetically pleasing and frequently more easily read they do have a problem. Under varying ambient light conditions they are either lost in the background or alternatively appear so bright as to distract the driver. With the system proposed here, this problem is overcome by automatically adjusting the display brightness during daylight conditions and by giving the driver control over the brightness during dusk and darkness conditions.

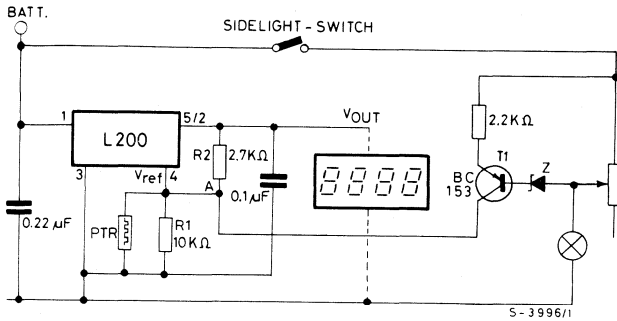
The circuit is shown in fig. 13. The primary supply is shown taken straight from the car battery however it is worth noting that in a car there is always the risk of dump voltages up to 120V and it is recommended that some form of protection is included against this.

Under daylight conditions i.e. with sidelights off and T1 not conducting the output of the device is determined by the values of R_1 , R_2 and the photoresistor (PTR). The output voltage is given by

$$V_{out} = V_{ref} \left(1 + \frac{R_2}{PTR/R_1} \right)$$

If the ambient light intensity is high, the resistance of the photoresistor will be low and therefore V_{out} will be high. As the light decreases, so V_{out} decreases dimming the display to a suitable level.

Fig. 13



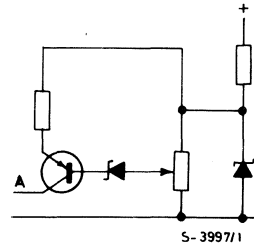
In dusk conditions, when the sidelights are switched on, T1 starts to conduct with its conduction set by the potentiometer. With the potentiometer wiper at its uppermost position the sidelights are at their brightest and current through T1 would be a minimum. With the wiper at its lowest position obviously the opposite conditions apply.

The current through T1 is felt at the summing node A along with the currents through R2 and the parallel network R1, PTR. Since V_{ref} is constant the current flowing through R1, PTR must also be constant. Therefore any change in the current through T1 causes an equal and opposite change in the current through R2. Therefore as I_{T1} increases, V_{out} decreases i.e. as the brightness of the sidelights is increased or decreased so is the brightness of the display.

The values of R2 and PTR should be selected to give the desired minimum and maximum brightness levels desired under both automatic and manual conditions although the minimum brightness under manual conditions can also be set by the maximum current flowing through T1 and, in any case, this should not exceed the maximum current through R2 under automatic operation.

The circuit shown with a small modification can also be used for dimmers other than in a car. Fig. 15 shows the modification needed. The zener diode should have a $V_F \geq 2.5V$ at $I = 10 \mu A$.

Fig. 15



Higher input or output voltages

Certain applications may require higher input or output voltages than the device can produce. The problem can be solved by bringing the regulator back into the normal operating units with the help of external components.

When there are high input voltages, the excess voltage must be absorbed with a transistor. Figs. 16 and 17 show the two circuits:

Fig. 16

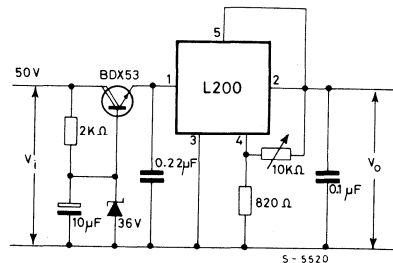


Fig. 17

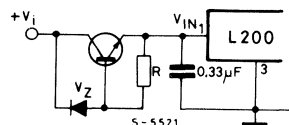
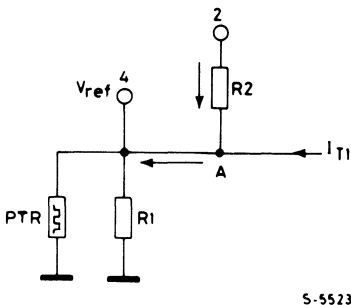


Fig. 14



The designer must take into account the dissipated power and the SOA of the preregulation transistor. For example, using the BDX53, the maximum input voltage can reach 56V (fig. 16). In these conditions we have 20V of V_{CE} on the transistor and with a load current of 2A the operation point remains inside the SOA. The preregulation used in fig. 16 reduces the ripple at the input of the device, making it possible to obtain an output voltage with negligible ripple.

If high output voltages are also required, a second zener, V_z , is used to refer the ground pin of an IC

Fig. 18

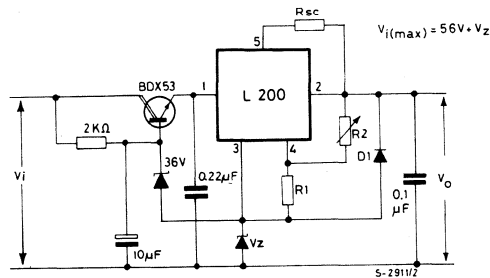
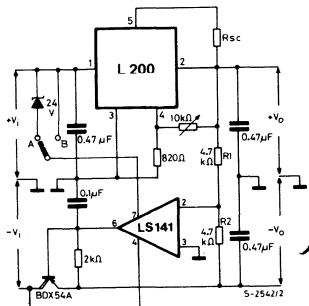
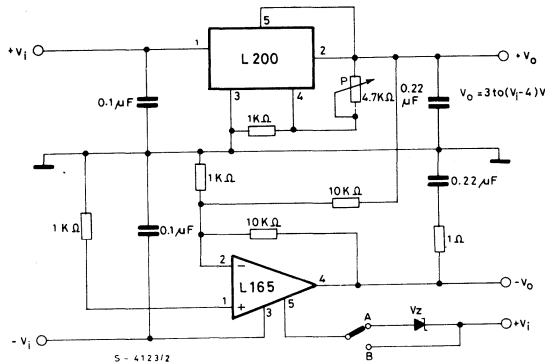


Fig. 19



- A: $V_i(\text{max}) \leq \pm 34\text{V}$ $3 < V_o < 30$
 B: $V_i(\text{max}) \leq \pm 22\text{V}$ $3 < V_o < 18$

Fig. 20



- A: for $\pm 18\text{V} \leq V_i \leq 32\text{V}$

Note: V_z must be chosen in order to verify $2 V_i - V_z = 36\text{V}$

- B: for $V_i \leq \pm 18\text{V}$

to a potential other than zero; diode D1 provides output shortcircuit protection (fig. 18).

Positive and negative voltage regulators

The circuit in fig. 19 provides positive and negative balanced, stabilized voltages simultaneously. The L200 regulator supplies the positive voltage while the negative is obtained using an operational amplifier connected as follower with output current booster.

Tracking of the positive voltage is achieved by putting the non-inverting input to ground and using the inverting input to measure the feedback voltage coming from divider R1-R2.

The system is balanced when the inputs of the operational amplifier are at the same voltage, or, since one input is at fixed ground potential, when the voltage of the intermediate point of the divider goes to 0 Volts. This is only possible if the negative voltage, on command of the op-amp, goes to a value which will make a current equal to that in R1 flows in R2. The ratio which expresses the negative output voltage is:

$$V^- = V^+ \cdot \frac{R2}{R1} \quad (\text{If } R2 = R1, \text{ we'll get } V^- = V^+)$$

Since the maximum supply voltage of the op amp used is $\pm 22\text{V}$, when pin 7 is connected to point B output voltages up to about 18V can be obtained. If on the other hand pin 7 is connected to point A, much higher output voltages, up to about 30V, be obtained since in this case the input voltage can rise to 34V.

Fig. 20 shows a diagram in which the L165 power op amp is used to produce the negative voltage. In this case (as in fig. 19) the output voltage is limited by the absolute maximum rating of the supply voltage of the L165 which is $\pm 18\text{V}$. Therefore to get a higher V_{out} we must use a zener to keep the device supply within the safety limits.

If we have a transformer with two separate secondaries, the diagram of fig. 21 can be used to obtain independent positive and negative voltages. The two output diodes, D1 and D2, protect the devices from shortcircuits between the positive and negative outputs.

Fig. 21

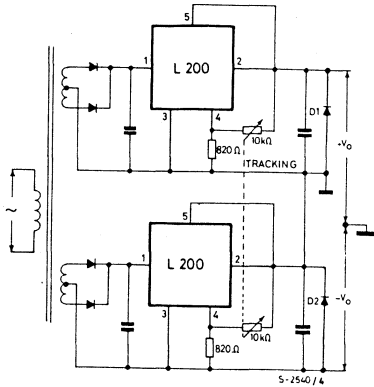
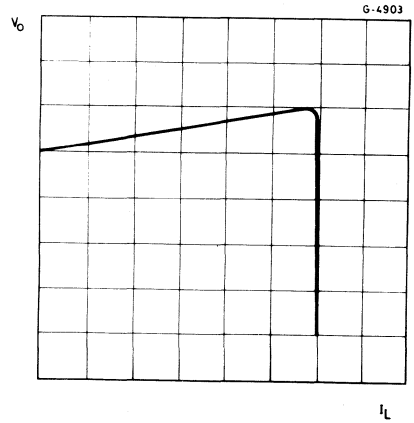


Fig. 23



Compensation of voltage drop along the wires

The diagram in fig. 22 is particularly suitable when a load situated far from the output of the regulator has to be supplied and when we want to avoid the use of two sensing wires. In fact, it is possible to compensate the voltage drop on the line caused by the load current (see the two curves in fig. 23 and 24). R_K transforms the load current I_L into a proportional voltage in series to the reference of the L200. $R_K I_L$ is then amplified by the factor

$$\frac{R_2 + R_1}{R_1}.$$

With the values of R_Z , R_2 and R_1 known, we get:

$$R_K = R_Z \frac{R_1}{R_1 + R_2}$$

R_Z , R_1 and R_2 are assumed to be constant.

If R_K is higher than 10Ω , the output voltage should be calculated as follows:

$$V_o = I_d R_K + V_{ref} \frac{R_2 + R_1}{R_1}$$

Fig. 24

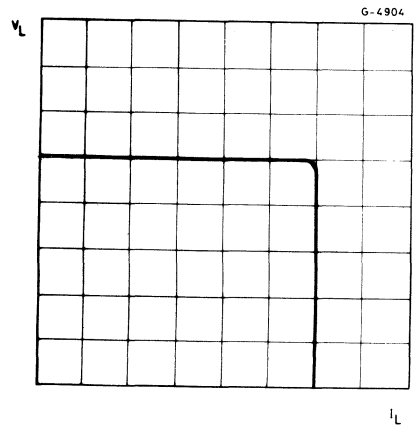
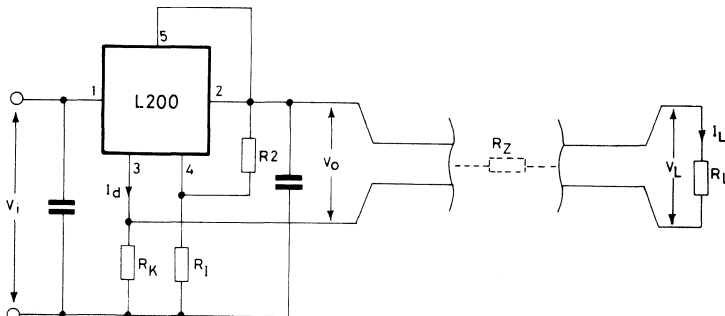


Fig. 22



Motor speed control

Fig. 25 shows how to use the device for the speed control of permanent magnet motors. The desired speed, proportional to the voltage at the terminal of the motor, is obtained by means of R1 and R2.

$$V_M = V_{ref} \left(1 + \frac{R2}{R1}\right)$$

To obtain better compensation of the internal motor resistance, which is essential for good regulation, the following equation is used:

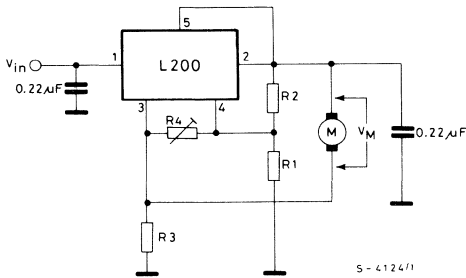
$$R3 \leq \frac{R1}{R2} \cdot R_M$$

This equation works with infinite R4. If R4 is finite, the motor speed can be increased without altering the ratio R2/R1 and R3. Since R4 has a constant voltage (V_{ref}) at its terminals, which does not vary as R4 varies, this voltage acts on R2 as a constant current source variable with R4. The voltage drop on R2 thus increases, and the increase is felt by the voltage at the terminals of the motor. The voltage increase at the motor terminals is:

$$V_M = \frac{V_{ref}}{R4 + R3} \cdot R2.$$

A circuit for a 30W motor with $R_M = 4\Omega$, $R1 = 1\text{ k}\Omega$, $R2 = 4.3\text{ k}\Omega$, $R4 = 22\text{ k}\Omega$ and $R3 = 0.82\Omega$ has been realized.

Fig. 25



Power amplitude modulator

In the configuration of fig. 26 the L200 is used to send a signal onto a supply line. Since the input signal V_i is DC decoupled, the V_o is defined by:

$$V_o = V_{ref} \left(1 + \frac{R2}{R1}\right)$$

The amplified signal V_i whose value is:

$$G_v = - \frac{R2}{R3}$$

is added to this component. By ignoring the current entering pin 4, we must impose $i_1 = i_2 + i_3$ (1) and since the voltage between pin 4 and ground remains fixed (V_{ref}) as long as the device is not in saturation, $i_1 = 0$ and equation (1) becomes:

$$i_2 = -i_3 \text{ with } i_3 = -\frac{V_i}{R3} \text{ (for } X_c \ll R3) \text{ -Therefore:}$$

$$v_o = R2 \cdot i_2 = - \frac{V_i}{R3} \cdot R2.$$

An application is shown in fig. 27. If the DC level is to be varied but not the AC gain, R1 should be replaced by a potentiometer.

Fig. 26

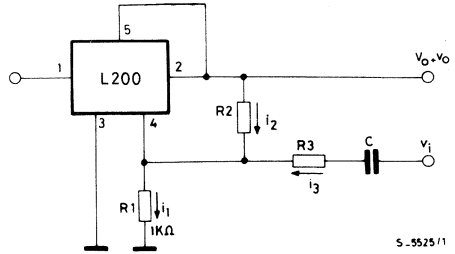
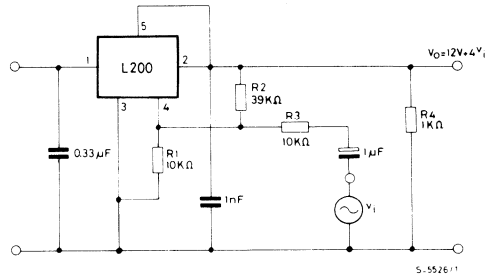


Fig. 27



HIGH CURRENT REGULATORS

To get a higher current than can be supplied by a single device one or more external power transistors must be introduced. The problem is then to extend all the device's protection circuits (short-circuit protection, limitation of T_j of external power devices and overload protection) to the external transistors. Constant current or foldback current limitation therefore becomes necessary.

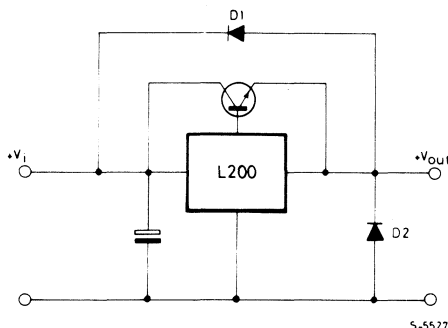
When the regulator is expected to withstand a permanent shortcircuit, constant current limitation becomes more and more difficult to guarantee as the nominal V_o increases. This is because of the increase in V_{CE} at the terminals of the transistor, which leads to an increase in the dissipated power. The heatsink has to be calculated in the heaviest working conditions, and therefore in shortcircuit. This increases weight, volume and cost of the heatsink and increase of the ambient temperature (because of high power dissipation). Besides heatsink, power transistors must be dimensioned for the short-circuit.

This type, of limitation is suited, for example, with highly capacitive loads. Efficiency is increased if preregulation is used on the input voltage to maintain a constant drop-out on the power element for all V_{out} , even in shortcircuit. Foldback limitation, on the other hand, allows lighter short-circuit operating conditions than the previous case. The type of load is important.

If the load is highly capacitive, it is not possible to have a high ratio between I_{max} and I_{sc} because at switch-on, with load inserted, the output may not reach its nominal value.

Other protection against input shortcircuit, mains failure, overvoltages and output reverse bias can be realized using two diodes, D1 and D2, inserted as indicated in fig. 28.

Fig. 28



Use of a PNP power transistor

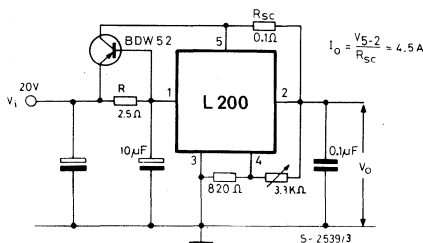
Fig. 29 shows the diagram of a high current supply using the current limitation of the L200. The output current is calculated using the following formula:

$$I_o = \frac{V_{sc}}{R_{sc}} \cong \frac{0.45V}{0.1\Omega} = 4.5A$$

Constant current limitation is used; so, in output shortcircuit conditions, the transistor dissipates a power equal to:

$$PD = V_i \cdot I_o = V_i \cdot \frac{V_{sc}}{R_{sc}}$$

Fig. 29



The operating point of the transistor should be kept well within the SOA; with $R_{sc} = 0.1\Omega$, V_i

must not exceed 20V. Part of the I_o crosses the transistor and part crosses the regulator.

The latter is given by: $I_{REG} = I_B + \frac{V_{BE}}{R}$.

where I_B is the base current of the transistor (-100 mA at $I_C = 4A$) and V_{BE} is the base-emitter voltage (-1V at $I_C = 4A$); with $R = 2.5\Omega$, $I_{REG} \cong 500$ mA.

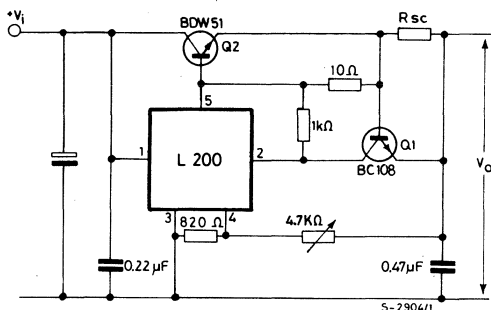
Use of an NPN power transistor

Fig. 30 shows the same application as described in figure 29, using an NPN power transistor instead of a PNP. In this case an external signal transistor must be used to limit the current. Therefore:

$$I_o = \frac{V_{BE Q1}}{R_{sc}}$$

As regards the output shortcircuit, see par. 1.5.

Fig. 30



12V 4A Power supply

The diagram in fig. 31 shows a supply using the L200 and the BD705. The 1 kΩ potentiometer, PT1, together with the 3.3 kΩ resistor are used for fine regulation of the output voltage.

Current limitation is of the type shown in fig. 32. Trimmer PT2 acts on stretch AB of characteristic. With the values indicated (PT2= 1 kΩ, PT3= 470Ω, R = 3 kΩ), currents from 3 to 4A can be limited. The field of variation can be increased by increasing the value of R_{sc} or by connecting one terminal of PT3 to the base of the power transistor, which, however, provides less stable limitation. If section AB is moved, section BC will also be moved.

The slope of BC can be varied using PT3. The voltage level at point B is fixed by the voltage of the zener diode. The capacitor in parallel to the zener ensures correct switch-on with full load. The BD705 should always be used well within its safe operating area. If this is not possible two or more BD705s should be used, connected in parallel (fig. 33).

Further protection for the external power transistor can be provided as shown in fig. 34. The PTC resistor, whose temperature intervention point must prevent the T_j of the power transistor from reaching its maximum value, should be fixed to the dissipator near the power transistor. Dimensioning of R_A and R_B depends on the PTC used.

Fig. 31

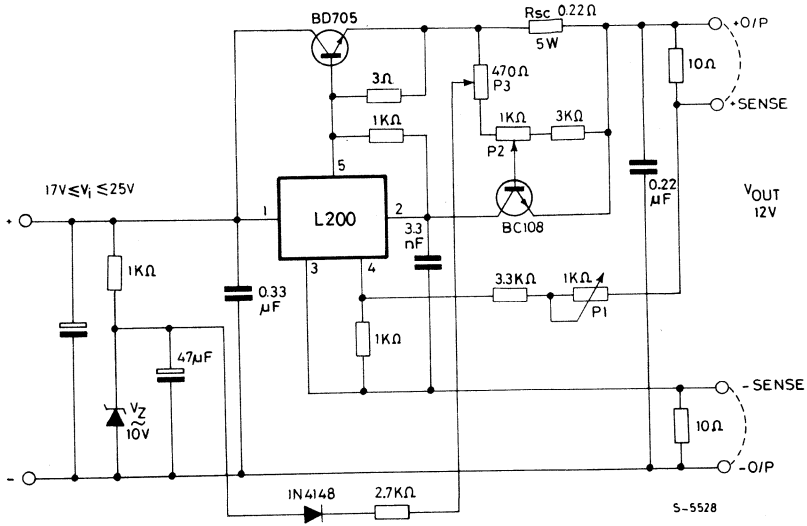


Fig. 32

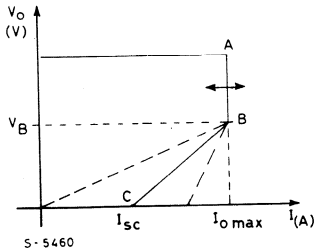


Fig. 34

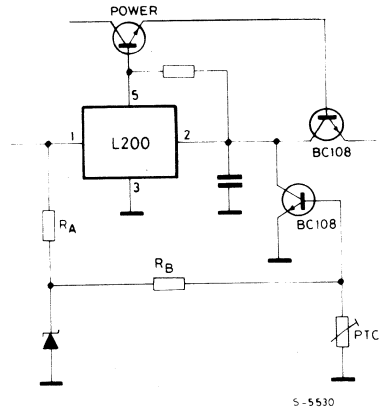
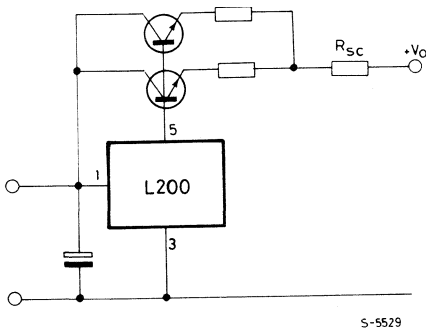


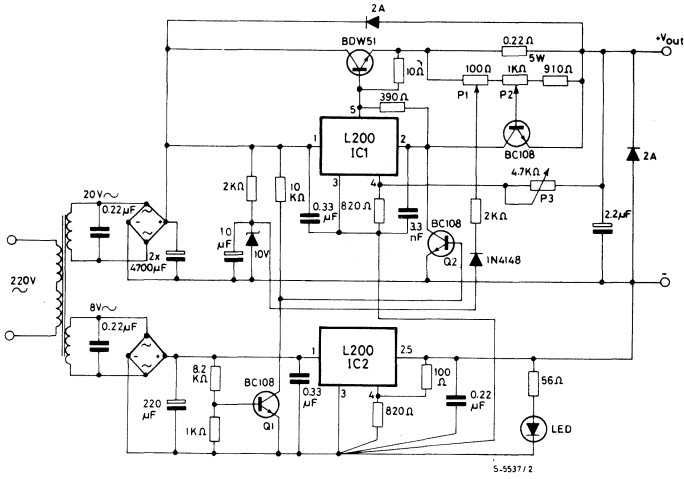
Fig. 33



Voltage regulator from 0V to 16V - 4.5A

Fig. 35 shows an application for a high current supply with output voltage adjustable from 0V to 16V, realized with two L200 regulators and an external power transistor. With the values indicated, the current can be regulated from 2A to 4.5A by potentiometer PT2. PT1, on the other hand, is used for constant current or foldback current limitation. The integrated circuit IC2, which does not require a heatsink and has excellent temperature stability, is used to obtain the 0V output. It is connected so as to lower pin 3 of IC1 until pin 4 reaches 0V. Q1 and Q2 ensure correct operation of the supply at switch-on and switch-off.

Fig. 35



Power supply with $V_o = 2.8$ to $18V$, $I_o = 0$ to $2.5A$

The diagram in fig. 36 shows a supply with output voltage variable from $2.8V$ to $18V$ and constant current limitation from $0A$ to $2.5A$. The output current can be regulated over a wide range by means of the op. amp. and signal transistor TR_2 . The op. amp. and the transistor are connected in the voltage-current converter configuration. The voltage is taken at the terminals of R_3 and converted into current by PT_2 .

I_o is fixed as follows:

$$\frac{R_4 I_o}{PT_2} = I_1 (*) \quad (**) I_{sc} = \frac{V_{sc}}{R_2}$$

When $I_1 = I_{sc}$, the regulator starts to operate as a

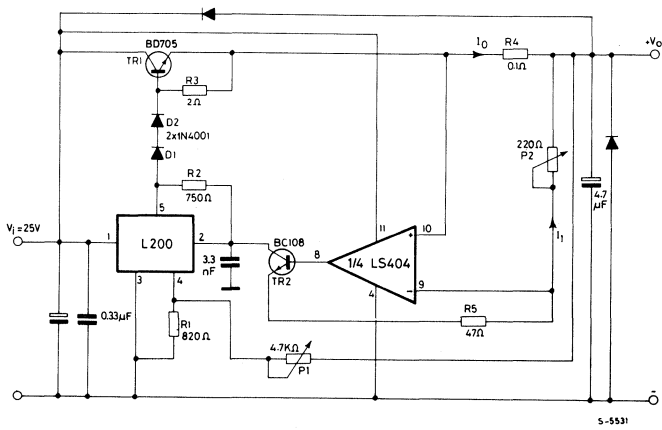
current generator. By making (*) equal to (**) we get:

$$\frac{R_4 I_o}{PT_2} = \frac{V_{sc}}{R_2}; \text{ therefore } I_o = \frac{V_{sc}}{R_2 \cdot R_4} \cdot PT_2$$

Diodes $D1$ and $D2$ keep transistor TR_2 in linear condition in the case of small output currents. If it is not necessary to limit the current to zero, one of the diodes can be eliminated: the second diode could also be eliminated if TR_1 were a darlington instead of a transistor.

The op. amp. must have inputs compatible with ground in order to guarantee current limitation even in shortcircuit. With a negative voltage available, even of only a few volts, current limitation is simplified.

Fig. 36



LAYOUT CONSIDERATIONS

The performance of a regulator depends to a great extent on the case with which the printed circuit is produced. There must be no impulsive currents (like the one in the electrolytic filter capacitor at the input of the regulator) between the ground pin of the device (pin 3) and the negative output terminal because these would increase the output ripple. Care must also be taken when inserting the resistor connected between pin 4 and pin 3 of the device.

The track connecting pin 3 to a terminal of this resistor should be very short and must not be

crossed by the load current (which, since it is generally variable, would give rise to a voltage drop on this stretch of track, altering the value of V_{ref} and therefore of V_O).

When the load is not in the immediate proximity of the regulator output “+ sense” and “- sense” terminals should be used (see fig. 37). By connecting the “+ sense” and “- sense” terminals directly at the charge terminals the voltage drop on the connection cable between supply and load are compensated. Fig. 37 shows how to connect supply and load using the sensing clamps terminals.

Fig. 37

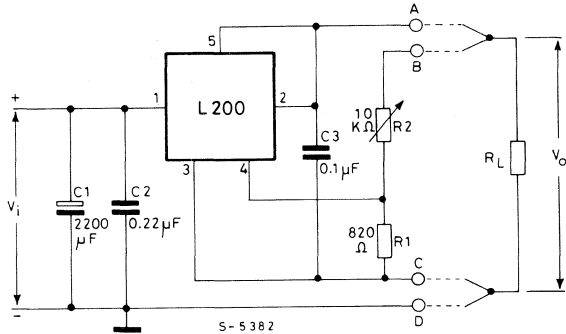
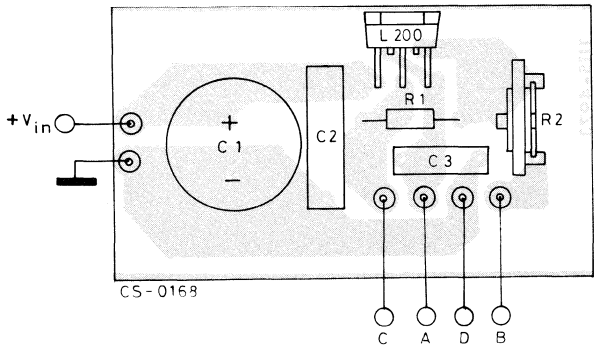


Fig. 38



HEATSINK DIMENSIONING

The heatsink dissipates the heat produced by the device to prevent the internal temperature from reaching values which could be dangerous for device operation and reliability.

Integrated circuits in plastic package must never exceed 150°C even in the worst conditions. This limit has been set because the encapsulating resin has problems of vitrification if subjected to temperatures of more than 150°C for long periods or of more than 170°C for short periods (24 h). In any case the temperature accelerates the ageing process and therefore influences the device life; an increase of 10°C can halve the device life. A well designed heatsink should keep the junction temperature between 90°C and 110°C. Fig. 39 shows

the structure of a power device. As demonstrated in thermodynamics, a thermal circuit can be considered to be an electrical circuit where $R_{1,2}$ represent the thermal resistance of the single elements (expressed in °C/W);

Fig. 39

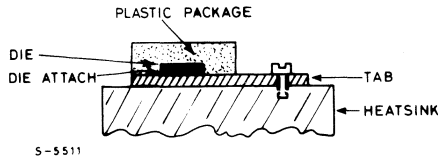
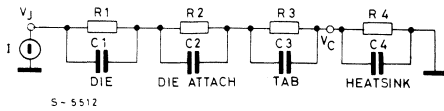


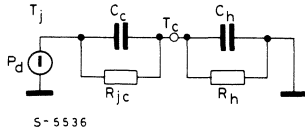
Fig. 40



C1, 2 the thermal capacitance (expressed in °C/W)
I the dissipated power
V the temperature difference with respect to the reference (ground).

This circuit can be simplified as follows:

Fig. 41



Where C_e is the thermal capacitance of the die plus that of the tab.

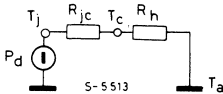
C_h is the thermal capacitance of the heatsink

R_{j-c} is the junction case thermal resistance

R_h is the heatsink thermal resistance.

But since the aim of this section is not that of studying the transistors, the circuit can be further reduced.

Fig. 42



If we now consider the ground potential as ambient temperature, we have:

$$T_j = T_a + (R_{jc} + R_h) P_D \quad (1)$$

$$R_h = \frac{T_j - T_a - R_{jc} \cdot P_D}{P_D} \quad (1a)$$

$$T_c = T_a + R_h \cdot P_D \quad (2)$$

For example, consider an application of the L200 with the following characteristics:

$V_{in\ typ} = 20V$
 $V_o = 14V$
 $I_o\ typ = 1A$
 $T_a = 40^\circ C$

typical conditions

$V_{in\ max} = 22V$
 $V_o = 14V$
 $I_o\ max = 1.2A$
 $T_a = 60^\circ C$

overload conditions

$$P_D\ typ = (V_{in} - V_o) \cdot I_o = (20-14) \cdot 1 = 6W$$

$$P_D\ max = (22-14) \cdot 1.2 = 9.6W$$

Imposing $T_j = 90^\circ C$ of (1a) we get (from L200

characteristics we get $R_{j-c} = 3^\circ C/W$)

$$R_h = \frac{90 - 40 - 3 \cdot 6}{6} = 5.3^\circ C/W$$

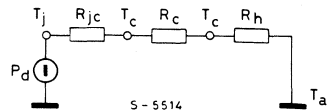
Using the value thus obtained in (1), we get that the junction temperature during the overload goes to the following value:

$$T_j = 60 + (3 + 5.3) \cdot 9.6 = 140^\circ C$$

If the overload occurs only rarely and for short periods, dimensioning can be considered to be correct. Obviously during the shortcircuit, the dissipated power reaches much higher values (about 40W for the case considered) but in this case the thermal protection intervenes to maintain the temperature below the maximum values allowed.

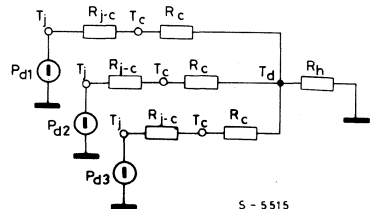
Note 1: If insulating materials are used between device and heatsink, the thermal contact resistance must be taken into account (0.5 to 1° C/W, depending on the type of insulant used) and the circuit in fig. 43 becomes:

Fig. 43



Note 2: In applications where one or more external transistors are used together with the L200, the dissipated power must be calculated for each component. The various junction temperatures can be calculated by solving the following circuit:

Fig. 44



This applies if the various dissipating elements are fairly near to one another with respect to the heat-sink dimensions, otherwise the heatsink can no longer be considered as a concentrated constant and the calculation becomes difficult.

This concept is better explained by the graph in fig. 45 which shows the case (and therefore junction) temperature variation as a function of the distance between two dissipating elements with the same type of dissipator and the same dissipated power. The graph in fig. 45 refers to the specific case of two elements dissipating the same power, fixed on a rectangular aluminium plate with a ratio

of 3 between the two sides. The temperature jump will depend on the dissipated power and one the device geometry but we want to show that there exists an optimal position between the two devices:

$$d = \frac{1}{2} \cdot \text{side of the plate}$$

Fig. 46 shows the trend of the temperature as a function of the distance between two dissipating elements whose dissipated power is fairly different (ratio 1 to 4).

Fig. 45

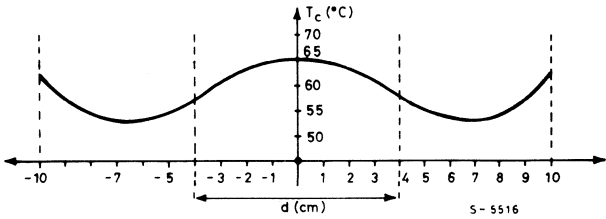
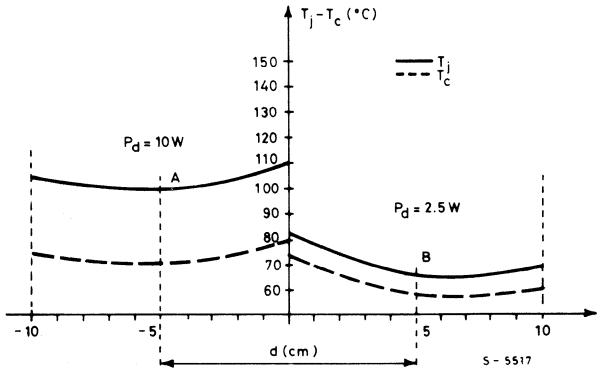


Fig. 46



- A : Position of the device with high power dissipation (10W)
- B : Position of the device with low power dissipation (2.5W)

This graph may be useful in applications with the L200 + external transistor (in which the transistor generally dissipates more than the L200) where the temperature of the L200 has to be kept as low as possible and especially where the thermal protection of the L200 is to be used to limit the transistor temperature in the case of an overload or abnormal increase in the ambient temperature. In other words the distance between the two elements can be selected so that the power transistor reaches the $T_j \text{ max}$ (200°C for a TO-3 transistor) when the L200 reaches the thermal protection intervention temperature.

CONTROL OF A DC MOTOR USING TRANSPACK

microprocessor based fully integrated solution

INTRODUCTION

This article covers the design of a controller for a DC permanent magnet motor. The design is preceded by a mathematical simulation of the controller. The controller design is complete with working drawings and a programme for the microprocessor. A comprehensive collection of diagrams and photos shows the operational performance of the design under normal and adverse working conditions.

Simulation of Motor Behaviour

The motor chosen for the design is a constant current type with a permanent magnet with a stator flux nearly constant and a good power to weight ratio compared with classic DC motors.

Simulation forecast: — Max. peak current, Ripple current at various chopper frequencies, Response speed of the system. Function in steady state.

The parameters are studied for extreme working conditions to optimise the choice of inverter components.

The Control Hardware

The hardware design is implemented with a microprocessor, D/A converter, switchmode driver and two power modules for the high current drive for a simple and integrated solution.

The bridge is constructed with two TO-240

TRANSPACK power modules of half bridge configuration, SGS30DB040D which permit fast acceleration of the motor and a compact structure.

The microprocessor allows simplicity and flexibility e.g. motor speed is controlled by a six bit word which accurately sets the speed between 0.5% and maximum.

Study of the System Behaviour

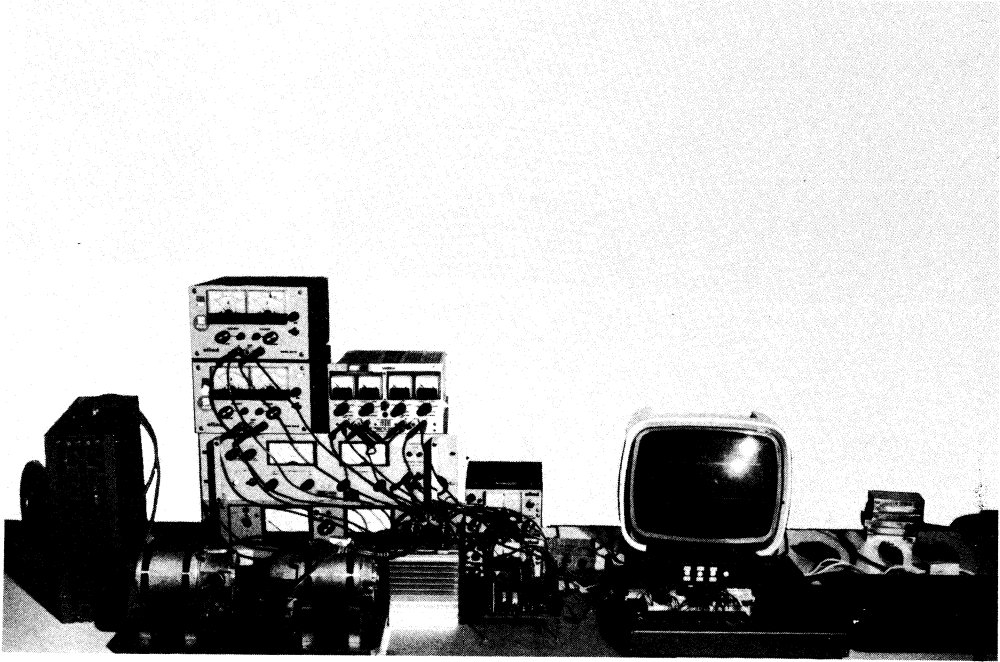
The system behaviour is studied to analyse the maximum stress conditions on the bridge corresponding to possible operating conditions, the algorithm of acceleration, braking, and inversion of the speed are demonstrated. The objective is to obtain the maximum performance possible with the transistors chosen for the bridge.

Balance of the Bridge

The evaluation of power absorbed by the various parts of the system demonstrates the efficiency of the design.

Detailed analysis of power absorbed in the motor and power dissipated in the bridge qualifies this design.

This study involves particularly heavy operating conditions for the power circuitry which verifies the excellent performance of the TRANSPACK devices above all in terms of switching speeds and low losses i.e. efficiency.



Motor Specification

Nominal Current	$I_A = 1.8A$
Nominal Supply Voltage	$V_A = 200-220V$
Peak Torque	$T = 6Nm$
Maximum Working Speed	$\Omega = 15000rpm$
Absolute Maximum Speed	$\Omega' = 20000rpm$
Rotor Inertia	$J = 0.6 \cdot 10^{-7} Kg.m^2$
Torque Constant	$K_T = 0.17Nm .A^{-1}$
Resistance	$R = 0.96\Omega$
Inductance	$L = 6.6mH$
Demagnetisation Current	$I_{dm} = 105A$
Nominal Power	$P = 200W$
Back EMF Constant	$K_v = 0.17 V.s$

Drive Specification

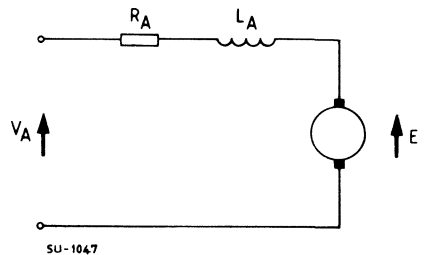
Maximum Motor Current	30A
Maximum Supply Voltage	400V
Minimum Speed Variation for each direction	1/32 maximum speed
Chopper Frequency	21.7KHz
4 Quadrant Control	

Simulation of Motor Behaviour

The motor is a (DC) constant current type with a

permanent magnet hence with a stator flux nearly constant and a good power to weight ratio compared with classic DC motors. The electrical circuit used for simulation is:

Fig. 1



For the mathematical model it was decided to neglect the variation of stator flux due to the inductive reaction, hence considering the flux generated by the permanent magnets to be constant.

This simplification has little effect on the representation of motor behaviour but it simplifies the calculations.

The equations which form the model are the

following:

-) $V_A = RA I_A + LA di_A/dt + E$
-) $C_M = J d\Omega/dt + D\Omega + Cr$
-) $E = K_V \phi \Omega$
-) $C_M = K_T \phi I_A$

Where:

- V_A = Armature Voltage (Volts)
- I_A = Armature Current (Ampere)
- R_A = Stator Resistance (Ω)
- L_A = Stator Inductance (H)
- E = Electro Motive Force (Volts)
- C_M = Torque (Nm)
- Cr = Friction (Nm)
- J = Inertial Moment ($Kg. m^2$)
- Ω = Angular Velocity (rad/sec)
- ϕ = Stator Magnetic Flux (Weber)
- D = Kinetic Friction (Nm)
- K_V = Back EMF Constant ($V.s$)
- K_T = Torque Constant ($Nm A^{-1}$)

From the balance of energy:

$C.\Omega = E.I_A$ where C equals the motor output (Watts)

$$= \frac{E}{K_V \phi} K_c \phi I_A \text{ from which } K_c = K_V$$

The differential equations were resolved by the Runge - Kutta method for solving non linear equations.

With the simulation it was proposed to forecast the following behaviour:

- Maximum Peak Current
- Ripple current at various chopper frequencies
- Response speed of the system
- Function in steady state

The phenomena were studied with the intention of seeing the maximum values of the observed parameters rather than instantaneous values in order to optimise the choice of inverter components. The simulation was made supposing a supply voltage of 200V.

N.B. — In Appendix A is the programme used for the simulation run on VAX.

Figures 2, 3 & 4 illustrate the simulated motor currents at chopper frequencies of 5, 10 & 20 KHz with the motor blocked and a 50% duty cycle ($A = 5$).

It can be seen that ripple current decreases in a practically linear relationship to the frequency, passing from 3A at 5KHz, to 0.9A at 20KHz.

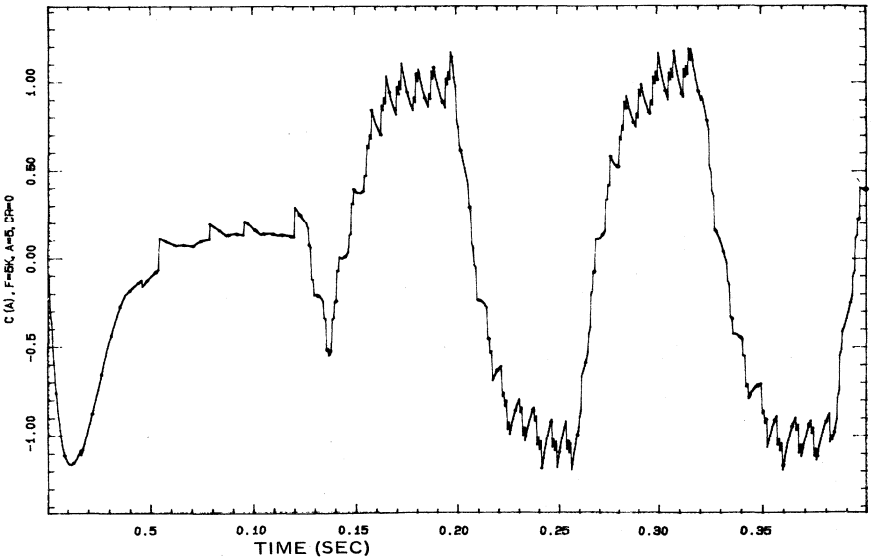
The average of the current is zero as is the torque. The absorbed power is however dissipated in the motor, becoming lower as the chopper frequency increases.

Figures 5 & 6 show the trend of velocity, at 10 & 20KHz, with a 70% duty cycle ($A = 7$) and load torque zero. Also the ripple on the speed is strongly influenced by the chopper frequency, going from 4.22% at 10KHz to 0.84% at 20KHz. Assuring a steady state speed of 237 rad/sec the ripple varies from 10 rad/sec at 10KHz to 2 rad/sec at 20KHz.

Under identical conditions (frequency and duty cycle) the motor current analysis shown in figures 7 & 8 was made.

The ripple current and hence the torque merit observations similar to those made for the speed. From the simulations it was decided to operate with a frequency close to 20KHz both in terms of reduced losses in the motor as well as the ripple effects on speed and torque.

Fig. 2



This choice is made possible by the availability of power transistors with very low switching losses. Also there is the advantage of much reduced interference on the supply.

From the performance reported in figures 5 & 6 the estimated acceleration time is around 80ms

for a steady state speed of 237 rad/sec.

The data supplied from the simulation has also enabled an estimate that with a duty cycle of 70% the peak current amounts to around 30A.

This data has led to the choice of the SGS30DB040D for the power bridge.

Fig. 2a

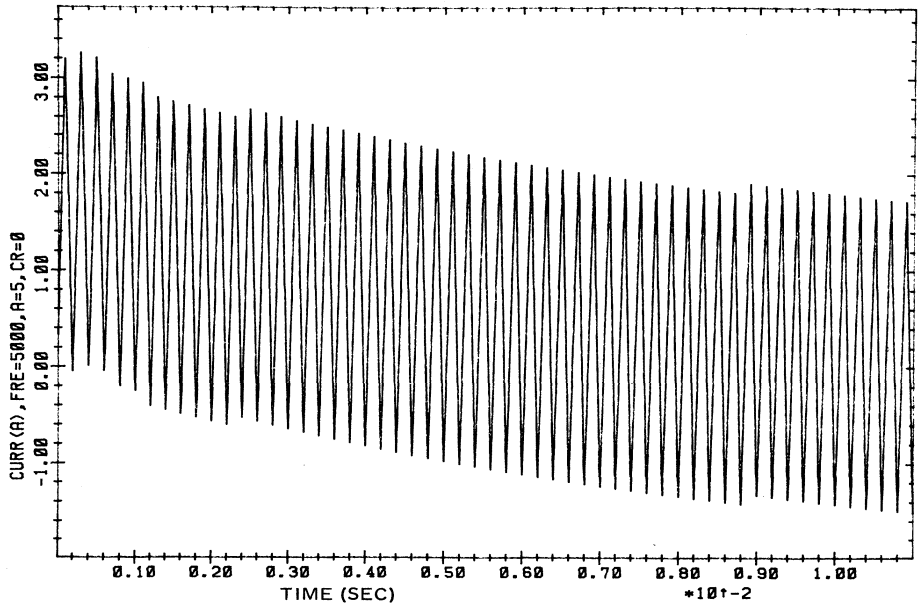


Fig. 3

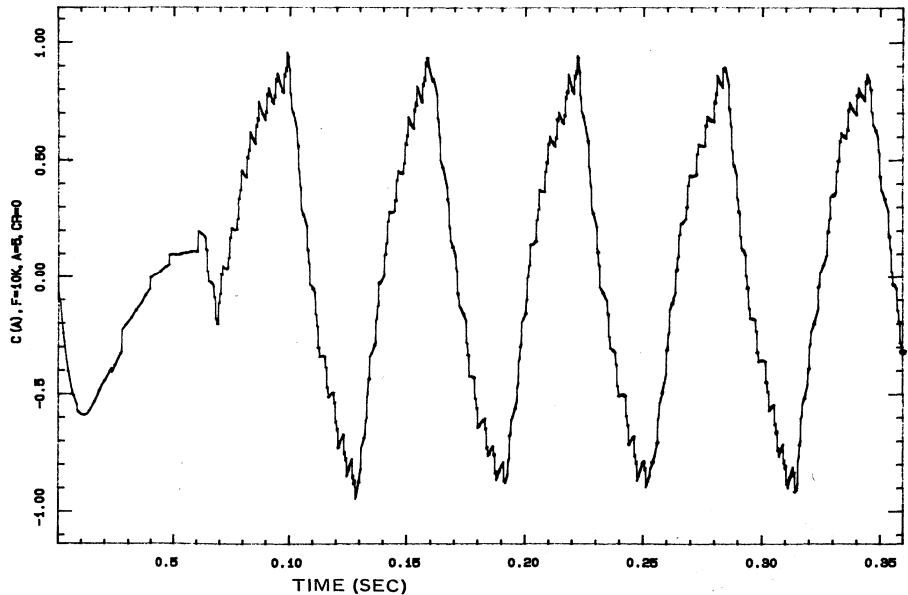


Fig. 4

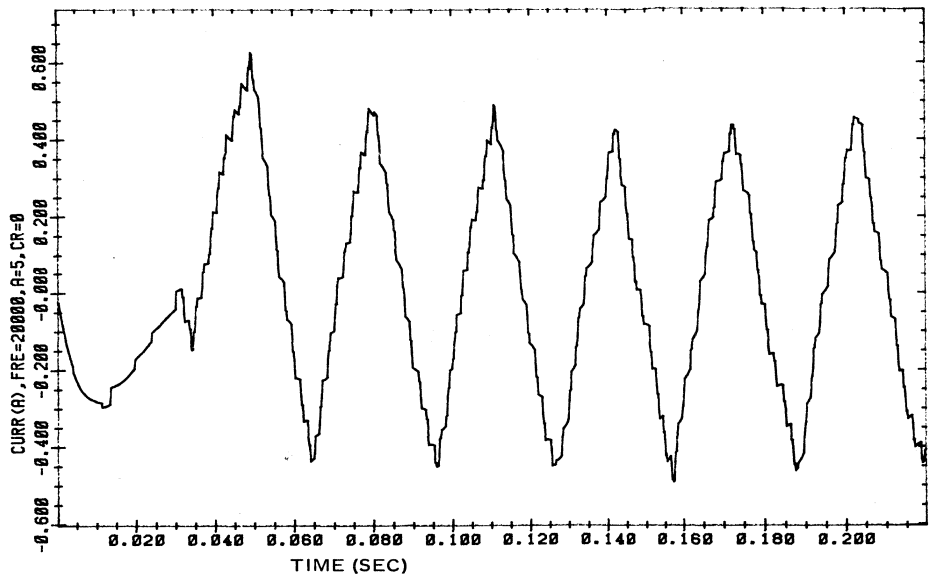


Fig. 5

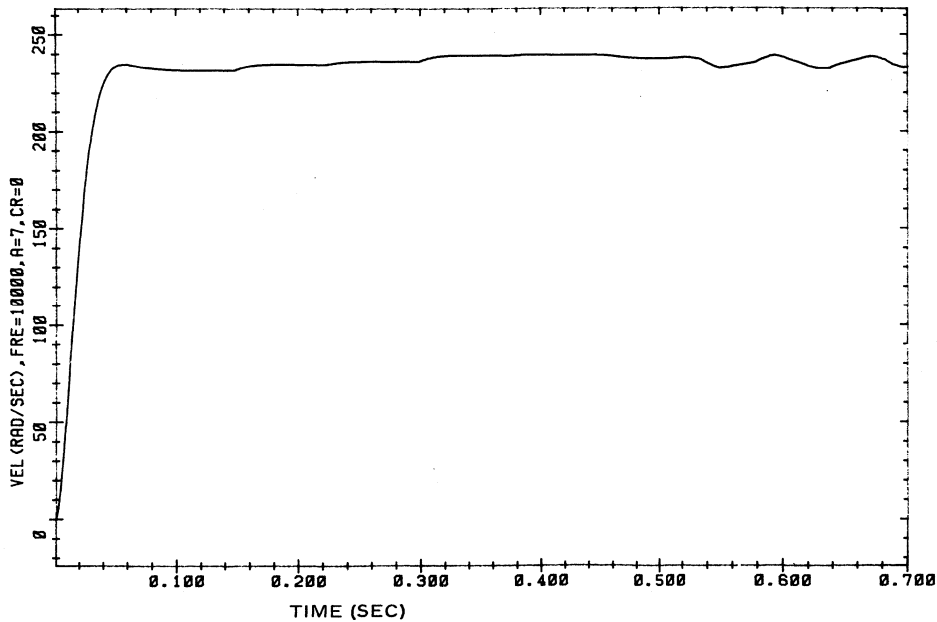


Fig. 6

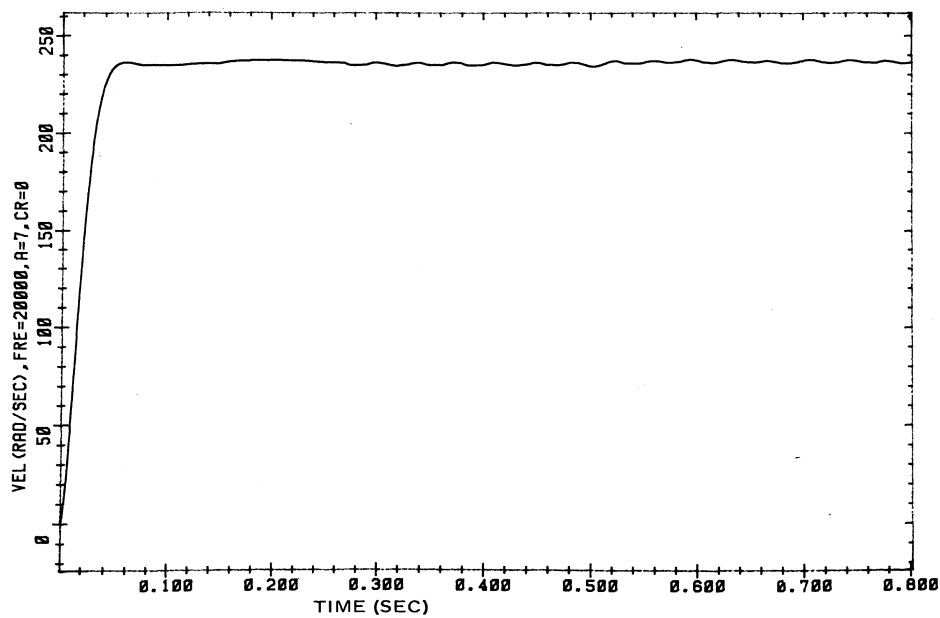


Fig. 7

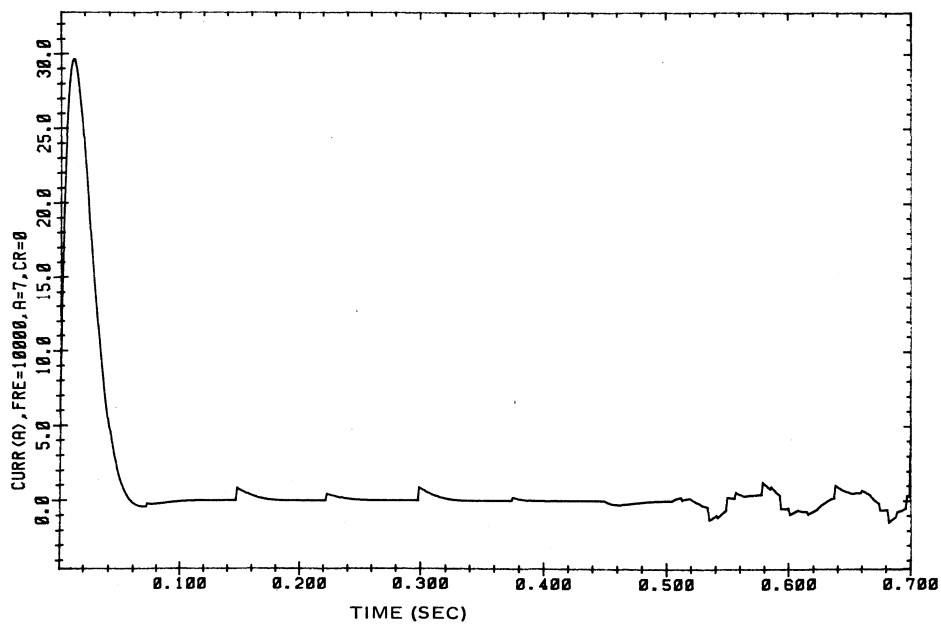


Fig. 8

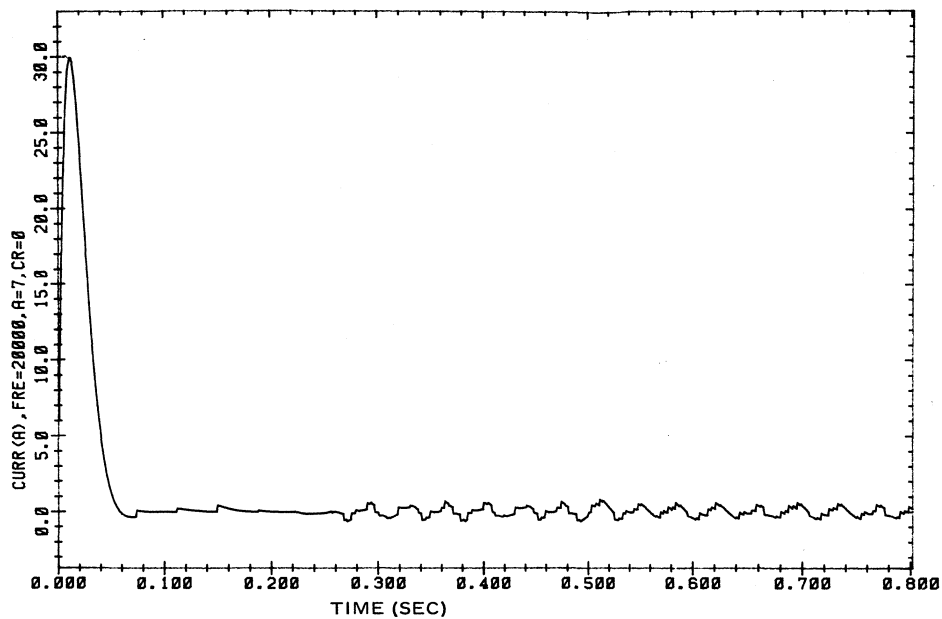
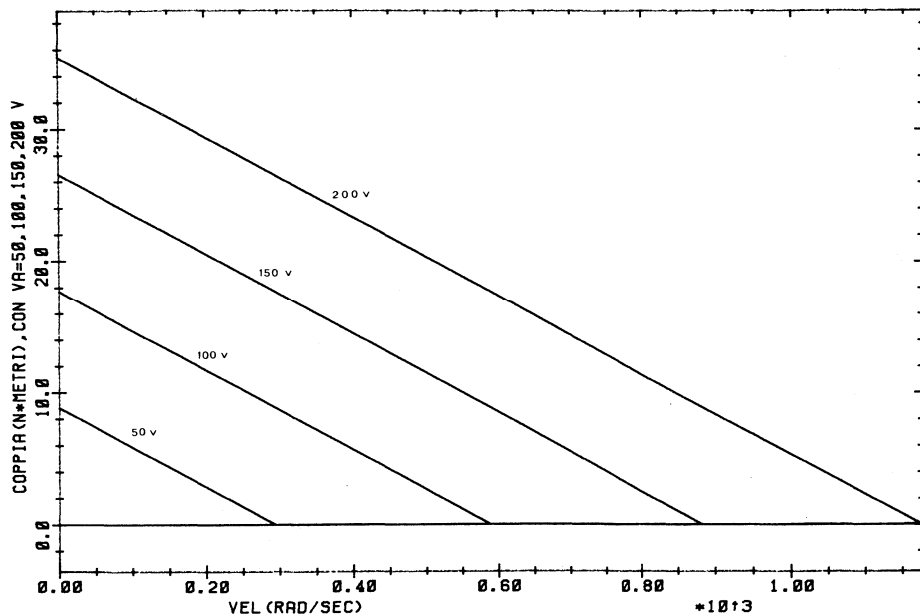


Fig. 9



The Controller Hardware

With the objective of analysing all the stresses on the components it was preferable to construct an open loop control which thanks to the lack of compensating feedback, permits an immediate study of the phenomena.

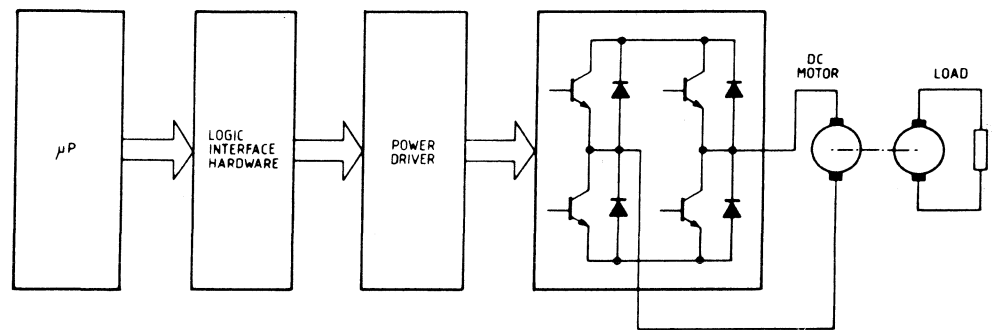
In order to operate with the maximum flexibility the system was designed to be microprocessor controlled using a NBZ80ASED "nanocomputer".

The digital to analogue conversion and drive waveform generation was realised with the SGS L291 and L292 for a simple and efficient integrated solution.

The bridge was constructed with two TO-240 TRANSPACK power modules of half bridge configuration, SGS30DB040D, which permit fast acceleration of the motor and a compact structure.

The block diagram is shown in figure 10.

Fig. 10 – Block diagram



SU-1048

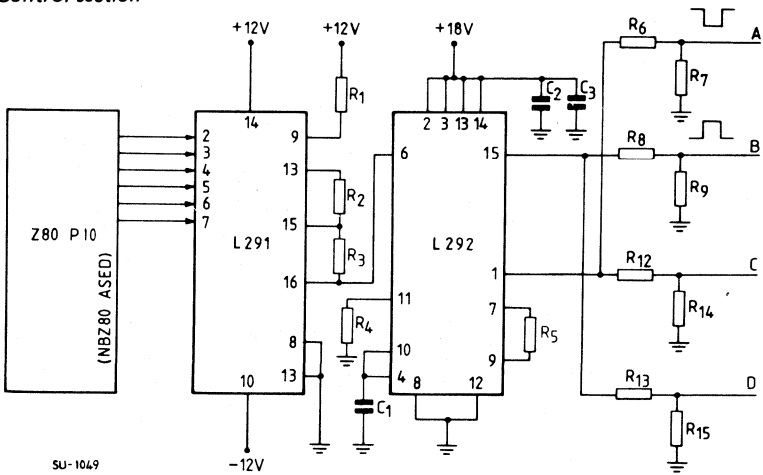
The Controller Schematic

The complete schematic of the controller is described as follows:

Fig 11 shows the control portion. A 6 bit word, generated by the microcomputer, representing the required speed of the motor, is converted into an

analogue current. This D/A conversion is carried out by the L291. The analogue signal is then used to drive the L292 which generates pulses of variable duty cycle. This device, normally used to drive low power motors, offers the advantage of outputs of two complementary signals of variable frequency between 1 and 30KHz.

Fig. 11 – Control section



SU-1049

Also it is possible to impose a delay between the end of one signal and the start of the complement, essential to avoid the short circuit condition on the bridge. The transfer of the signal from the controller to the high side of the bridge is via Q5 and Q6. These transistors are power devices working in the active zone with very low current and must sustain a voltage 5V greater than the voltage applied to the motor (fig. 11a).

This solution avoids the use of a transformer and is aimed towards the eventual integration of the power stage. The drive of the transistors in the bridge was realised with a simple integrated solu-

tion of the SGS L149, whose power for the high side is referred to the voltage at the motor terminals which follows the variations.

The power for the motor is provided by a full bridge circuit permitting operation in all 4 quadrants.

The two half bridge TRANSPACK, SGS30DB040D, are built using darlington transistors without integrated collector - emitter diodes which permits full use of the fast freewheel diodes incorporated in the power module and high frequency drive of the motor. The voltage waveforms on the motor are illustrated in photo 1.

Fig. 11a

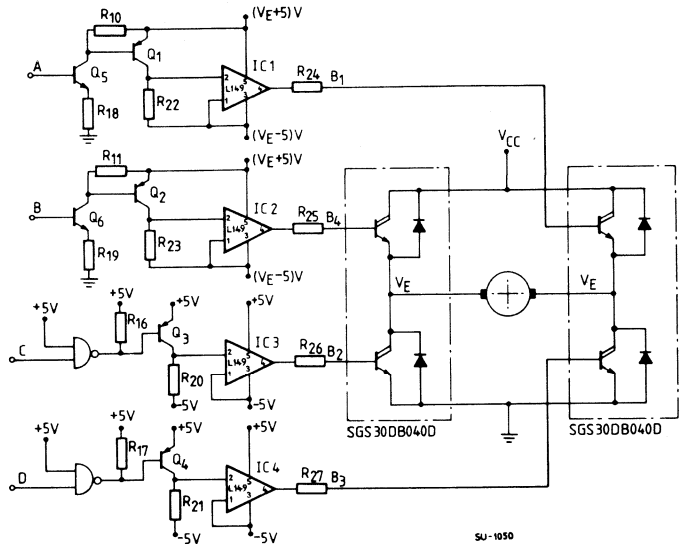
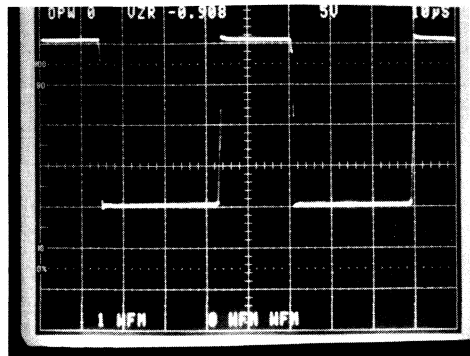
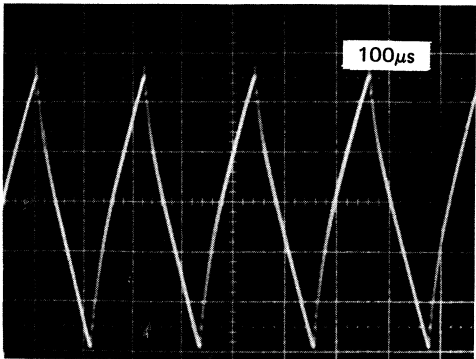


Photo 1 - Motor voltage



V = 50V/div
t = 10μs/div

Photo 2A - Ripple of 3A at 5KHz



I = 0.5A/div

The principle characteristics of the darlington are as follows:

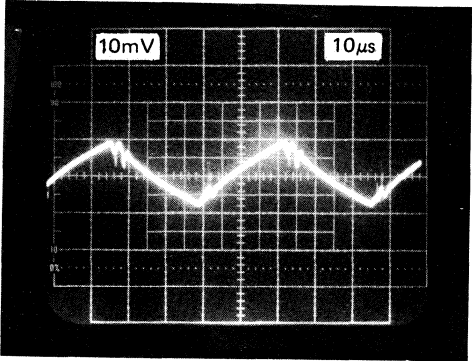
- $V_{CE0} = 400V$
- $I_C = 30A$
- $H_{FE} = (I_C = 30A) 50$
- $V_{CE(sat)} = (I_C = 30A, I_B = 2A) = 1.5V$
- t_s (storage time) = $1.2\mu s$
- t_f (fall time) = $0.2\mu s$

The main parameters of the diode are:

- $V_F = 1.2V$ ($I_F = 30A$)
- $t_{RR} < 0.2\mu s$ ($I_F = 30A, di/dt = 100A/\mu s$)
- $I_{RM} = 10A$
- $I_{FRM} = 250A$

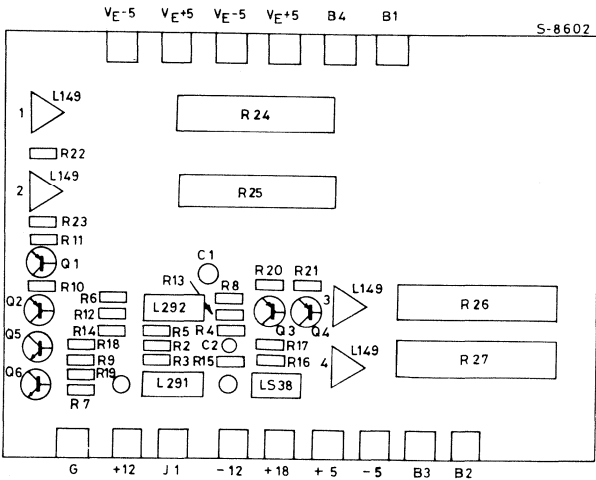
Photo 2 shows the behaviour of the motor, currents at chopper frequencies of 5KHz and 20KHz. It is possible to note in photo 2A (5KHz) a ripple of 3A in agreement with the simulated data, while in photo 2B one sees a ripple at 20KHz of around 0.9A.

Photo 2B - Ripple of 0.9A at 20KHz



$I = 0.5A/div$

Fig. 12 - Assembly of the circuit board



COMPONENTS LIST

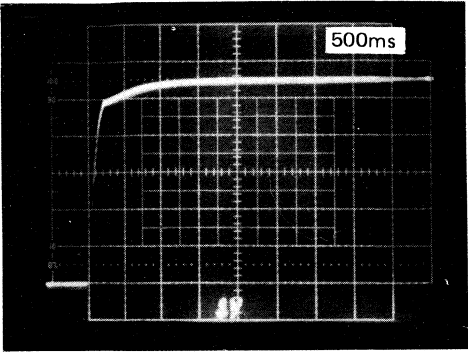
Components	Quantity	Value	Note	Components	Quantity	Value	Note
SGS30DB040D	2		TRANSPACK Driver d/a converter PWM generator	R16, R17	2	100Ω	2N4033 TIP50
L149	4			R18, R19	2	2.7KΩ	
L291	1			R20, R21	2	670Ω	
L292	1			R22, R23	2	10KΩ	
R1	1	4.9KΩ		R24, R25	2	5Ω	
R2	1	3.9KΩ		R26, R27	2	5Ω	
R3	1	22KΩ		C1	1	100nF	
R4	1	8.4KΩ		C2	1	1000μF	
R5	1	5KΩ		C3	1	22nF	
R6, R7	2	15KΩ		Q1, Q2, Q3, Q4	4		
R8, R9	2	3.8KΩ		Q5, Q6	2		
R10, R11	2	1KΩ		B1, B2	2		
R12, R13	2	1.5KΩ		B3, B4	2		
R14, R15	2	470Ω		I1			

Study of the system behaviour

To analyse the maximum stress condition on the bridge corresponding to possible operating conditions, the algorithm of acceleration, braking and inversion of the speed were performed. The objective was to obtain the maximum performance possible with the transistor s chosen for the bridge.

The strategy followed was to choose a speed of 3000rpm analysing the time needed to reach the speed.

Photo 5 - The trend of the velocity with four progressive steps of voltage at intervals of 25ms (560 rpm/div)



Acceleration Tests

Firstly the motor was accelerated with a duty cycle corresponding to the chosen speed (steady acceleration with a drive signal duty cycle of 70%). The result of this test is shown in photo 3 & 4.

Photo 3 - Trend of the speed with only voltage changing (560 rpm/div)

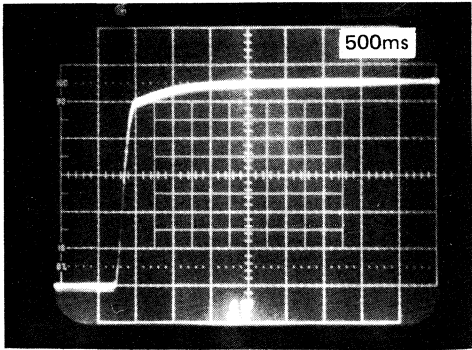


Photo 6 - The trend of the current under the conditions of photo 5 (5A/div)

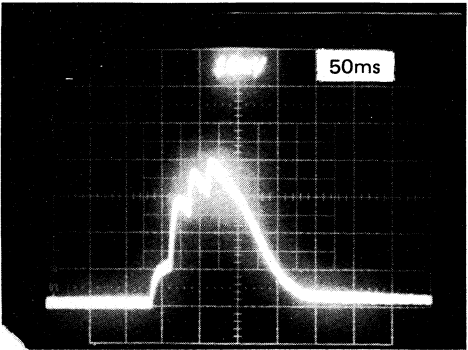
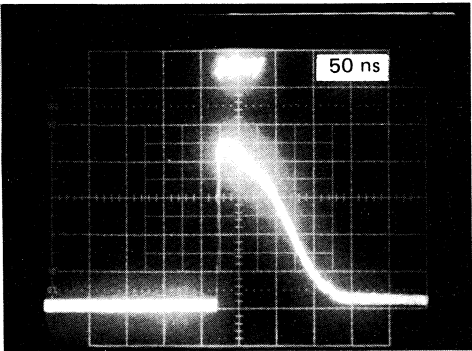


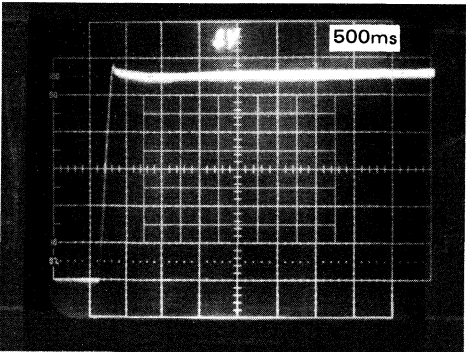
Photo 4 - Trend of the current under the same conditions as photo 3 (5A/div)



Also a ramp of acceleration was tested imposing 4 increases in duty cycle of 5% with a 25ms delay between each (photo 5 & 6).

In this way the maximum current during acceleration is reduced to 20A without any significant variation of the time to reach full speed.

Photo 7 - The trend of the speed with the drive of figure 13 (560 rpm/div)



In photo 4 it is seen that the current reaches a peak of 23A in a limited number of pulses and then goes to full speed much more slowly, with a current of 0.6A. Regarding the speed, the period of the transition may be estimated as around 1.2s.

Fig. 13

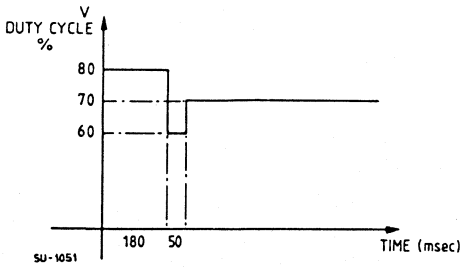


Photo 8 – Trend of the current with the drive of figure 13 (10A/div)

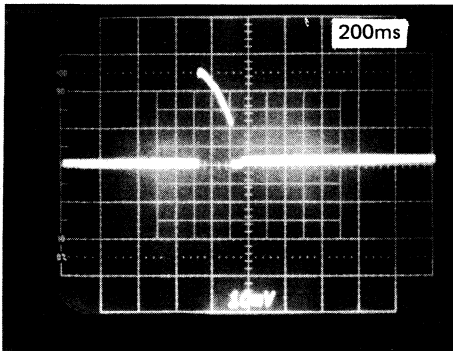


Photo 9 – Trend of velocity with an initial drive to produce 3750 rpm followed after 300ms by a drive to produce 3000 rpm (560 rpm/div)

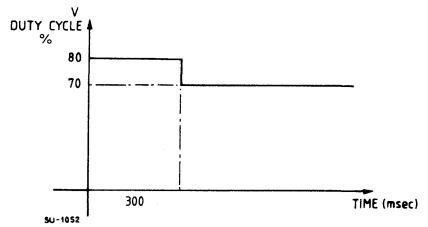
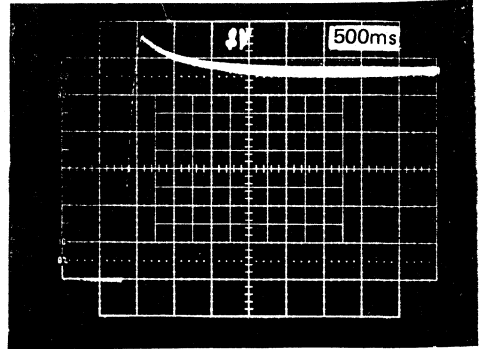
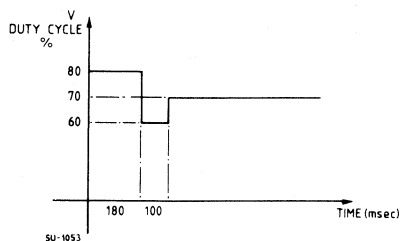
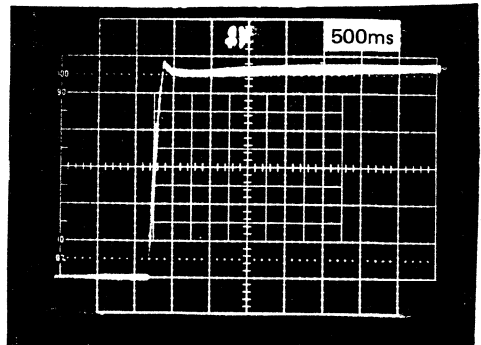


Photo 10 – Trend velocity with an initial drive to produce 3750 rpm followed after 180ms by a drive to produce 2250 rpm and finally after 100ms by a drive to produce 3000 rpm (560rpm/div)



Other test of acceleration are shown in photos 9, 10 & 11

A series of tests were performed attempting to obtain a determined speed in the minimum possible time, working with duty cycles above and below that of steady state with the appropriate delays.

The best result was obtained driving with the sequence of duty cycles illustrated in fig. 13 as shown in photo 7.

One notes that the duration of the transient may be estimated to be around 500ms, notably below the 1.2s in the case shown in photo 3, corresponding to an average acceleration of 628 rad/sec^2 and with an instantaneous acceleration of 7500 rad/sec^2 , corresponding to a maximum current of 26A shown in photo 8.

Photo 11 – Trend of velocity with a initial drive to produce 3750 rpm followed after 160ms by a drive to produce 2250 rpm and finally after 50ms by a drive to produce 3000 rpm

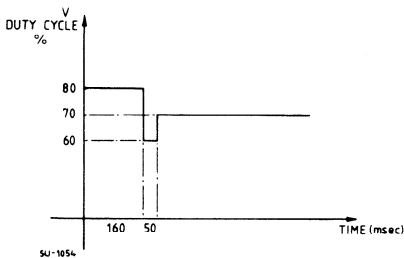
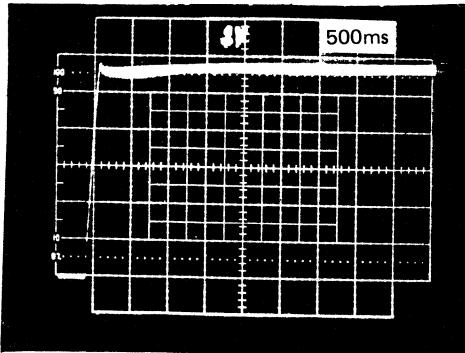
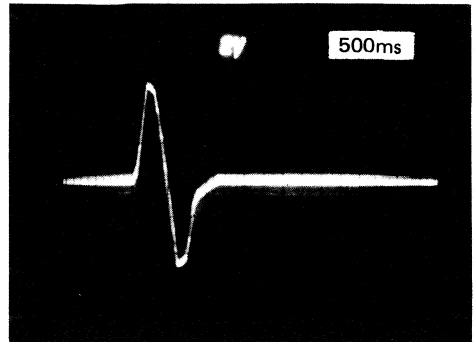
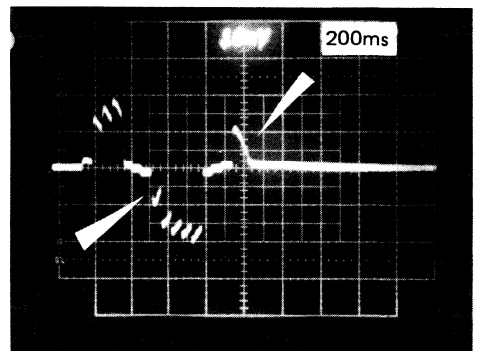


Photo 12 – Trend of velocity (1090 rads/sec/div)



The behaviour of the relevant currents are shown in photo 13 where points shown by the arrows are relative to the transformation of the motor into a generator.

Photo 13 – Current absorbed by the motor with the described speed inversion (10A/div)



Speed Reversal

Having reached the maximum, the objective was to achieve the maximum steady acceleration and to estimate the time needed to achieve an inversion of the speed passing from +3000rpm to -3000rpm having supposed that this is the most critical stress on the bridge.

There was first analysed the phenomena of braking and it was seen that braking too quickly may cause a change of function, making the motor a generator and creating excess emitter base voltage up to a situation intolerable for correct operation of the bridge components.

This phenomena was taken into account to achieve the most rapid braking possible without over-stressing the bridge components.

We succeeded in this way to obtain a time, from +3K to - 3Krpm, of about 500ms, as shown in photo no. 12 where the achievement of a steady state is not considered but only the transition from one speed to another.

Both the tests of acceleration and speed reversal were made with repetitive cycles, with appropriate programmes in the Nanocomputer[®], for periods of several hours without creating problems for the SGS30DB040D.

Balance of the Bridge

The evaluation of the power absorbed by the various parts of the system is analysed in the following paragraph.

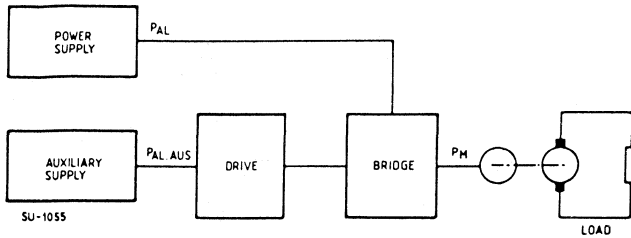
The estimates obtained give an indication of the efficiency of the control system in that it permits a ratio of the power absorbed to that of the motor.

The power was measured using the following system (fig. 14).

The chosen conditions were:

- Duty cycle of 76%
- Average motor current 1.25A

Fig. 14



The load was simulated by a generator connected to the motor and a rheostat of 200Ω.

In this situation the power taken from the supply was:

$$- P_{AL} = 200V \times 0.83A = 166W$$

The power absorbed by the drive circuit was:

$$- P_{AL \text{ Auxiliary}} = 7.86W$$

The power absorbed by the motor was:

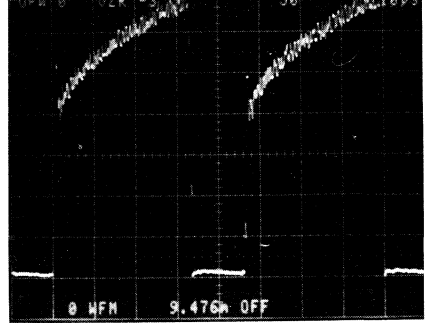
$$- P_M = V_{av} \times I_A = 123.2V \times 1.25A = 154W$$

Hence the power absorbed the bridge was:

$$- P_{BRIDGE} = 12W$$

Thus one has a dissipation of power in the bridge of 7.2%.

Photo 14



The power returned from the motor is shown in photo 15.

$$- E = 2.38mJ$$

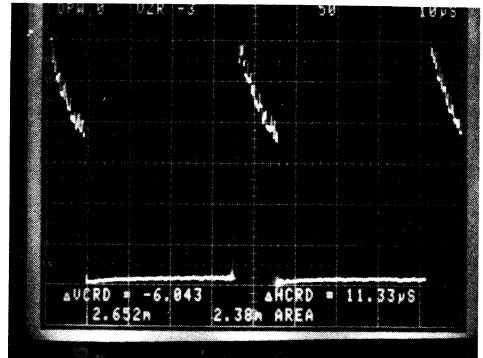
$$- F = 21700Hz$$

$$- P_{GEN.MOT.} = 51.6W$$

Thus the total power absorbed by the motor is:

$$P_{TOT.MOT.} = P_{ABS.MOT.} - P_{GEN.MOT.} = 205.6 - 51.6 = 154W$$

Photo 15



Power Absorbed by the Motor

Photo 13 shows the waveforms of current and voltage on one arm of the bridge. The power in the motor was computed as the difference of the power absorbed during the conducting phases of the bridge less that returned during the conduction of the free wheel diodes.

Photo 13

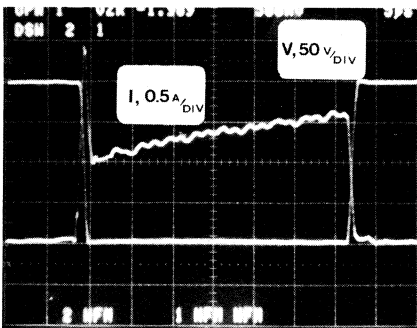


Photo 14 represents the power absorbed. The energy corresponds to the area under the curve in a period. Given that:

$$E = 9.47mJ, F = 21700Hz$$

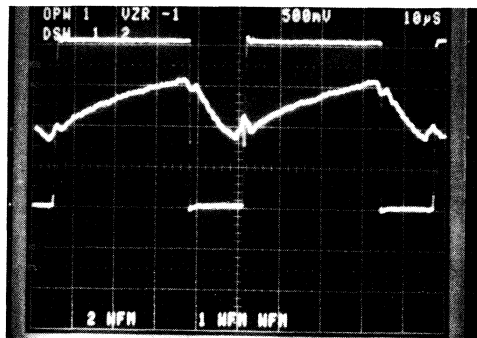
$$P_{ABS.MOT} = E \times F = 9.47 \times 10^{-3} \times 21.7 \times 10^3 = 205.6W$$

Power Dissipated in the Bridge

The power dissipated in the bridge was analysed in a more detailed manner by measuring the power dissipated in one transistor (high side) both in the turn-on and turn-off phases and estimating the dissipation during the on period.

The waveforms of voltage and current during an entire period can be seen in photo 16.

Photo 16



The power dissipated during the turn-on phase and the respective voltage and current waveforms are shown in photos 17 & 18.

Photo 17

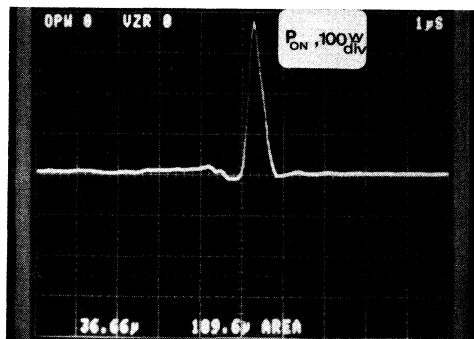
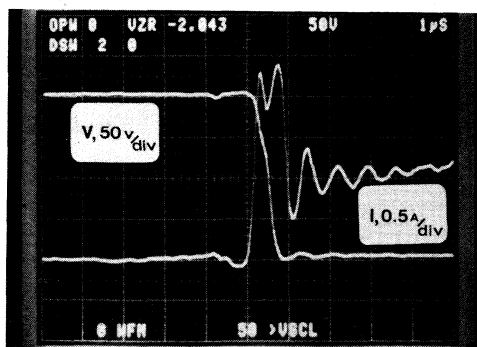


Photo 18



From the photo of the power it is possible also to measure the energy dissipated. This corresponds to an average power of:

$$P_{ON} = E \times F = 189.6 \mu J \times 21700 \text{ Hz} = 4.1 \text{ W}$$

The power dissipated during the turn-off phases and the respective waveforms are shown in photo 19 & 20.

The energy dissipated in this case is 118 μJ thus:

$$P_{OFF} = E \times F = 118.5 \times 21700 = 2.47 \text{ W}$$

Photo 19

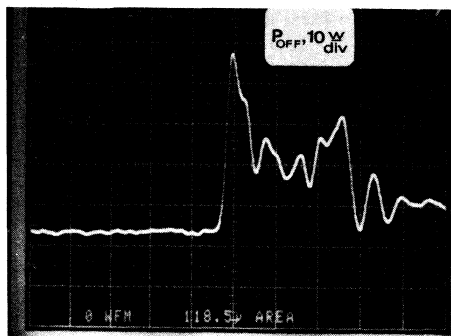
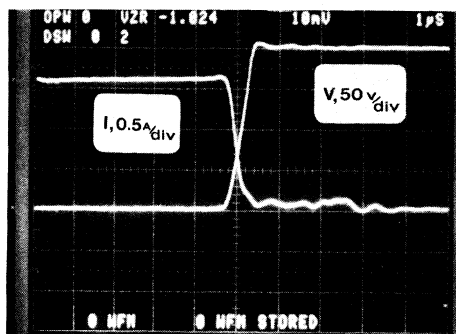


Photo 20



The dissipation of the conduction phase is not conveniently measured by the method used so it was preferred to make an estimate.

At the average current of 1.25 A from the characteristic curves a $V_{CE(sat)}$ of 0.8 V is found.

$$P_{COND.} = 1.25 \text{ A} \times 0.8 \text{ V} \times 0.76 = 0.76 \text{ W}$$

Taking into consideration that the conduction phase is 76% of the full period:

The power dissipated in a transistor of the bridge is thus:

$$P_{TOT} = P_{ON} + P_{OFF} + P_{COND} = (4.1 + 2.57 + 0.76) \text{ W} = 7.43 \text{ W}$$

CONCLUSION

During this work a study was made, both in theory and application, of the control of a DC motor. For this study, advantage was taken of the flexibility offered by using a microprocessor to make many tests. This allowed a comprehensive analysis of the behaviour of the SGS30DB045D TRANSPACK.

This involved the recreation of particularly heavy operating conditions for the power circuitry, which verified the excellent performance of the TRANSPACK devices, above all in terms of switching speed and low losses. Also studies were made of a number of drive circuits for the power transistors, useful for future projects.

APPENDIX A

```

# TY Motor For
  DIMENSION Y (20),YF (20)
  EXTERNAL FUNC
  REAL KC,KV
  OPEN (UNIT=7,FILE='MIKE,DAT',STATUS='NEW')
  OPEN (UNIT= 8,FILE='MIKE1,DAT',STATUS='NEW')
  OPEN (UNIT=9,FILE='MIKE2,DAT',STATUS='NEW')
  OPEN (UNIT=10,FILE='MIKE3,DAT',STATUS='NEW')
  OPEN (UNIT=11,FILE='MIKE4,DAT',STATUS='NEW')
  WRITE (*,30)
30  FORMAT (1X,'INTRODUCI H,NS,NT,CR,T,A')
  READ (*,*) H,NS,NT,CR,T,A
  TI=A*T/10
  T2=T-T1
  L=H*NS*NT/T
  WRITE(*,*)'VUOI I GRAFICI? (SI=1)'
  READ (*,*) AAA
  WRITE (*,*) 'LA MACCHINA E' QUELLA SOLITA? (SI=1)
  READ (*,*) Z
  IF (Z,NE,1) GO TO 40
  X=0.
  N=2
  Y (1)=0.
  Y (2)=0.
  RA=0.96
  XLA=0.006
  FL=1.
  RJ=.00056
  Kc=.17
  Kv=.17
  GO TO 50
40  WRITE (*,17)
17  FORMAT (1X,'INTRODUCI X,N,Y (I),RA,XLA,FL,RJ,Kc,Kv')
  READ (*,*) X,N,(Y(I),I=1,N),RA,XLA,FL,RJ,Kc,Kv
50  CONTINUE
  DO 2 J=1,NT
  DO 1 K=1,NS
  CALL RKUITA(N,X,Y,FUNC,H,XF,YF,CR,RA,XLA,FL,CM,E,RJ
#  Kc,Kv,L,T,T1,T2)
  X=XF
  DO 1 I=1,N
  Y(I)=YF(I)
1  CONTINUE
  CM=Kc*FL*Y (1)
  E=Kv*FL*Y (2)
  IF (AAA.EQ.1) GO TO 333
  WRITE (*,20)
20  FORMAT (1X,'TEMPO',7X,'IA',10X,'VEL',9X,'CM',10X,'E')
  WRITE (*,15) X,(Y(I),I=1,N),CM,E
15  FORMAT (5 E12.5)
  GO TO 2
333  WRITE (7,*) X,Y (2)
  WRITE (8,*) X,Y (1)
  WRITE (9,*) X,CM
  WRITE (10,*)X,E
  WRITE (11,*) Y (2),CM
2  CONTINUE
  CLOSE (UNIT=7)
  CLOSE (UNIT=8)
  CLOSE (UNIT=9)
  CLOSE (UNIT=10)

```

APPENDIX A (continued)

```

CLOSE (UNIT=11)
STOP
END

```

```

SUBROUTINE RKUTTA(N,X,Y,FUNC,H,XF,YF,CR,RA,XLA,FL,CM,E,RJ,
Kc,Kv,L,T,T1,T2)
DIMENSION Y (20),YI(20),YF(20),D(20),A(5)
REAL KC,KV
A (1) = H/2
A (2) = A (1)
A (3) = H
A (4) = H
A (5) = A (2)
XF=X
DO 10 K=1,N
YF (K) = Y (K)
10 YI (K) = Y (K)
DO 20 J=1,4
CALL FUNC (XF,YI,N,D,CR,RA,XLA,FL,CM,E,RJ,Kc,Kv,L,T,T1,T2)
XF=X+A (J)
DO 20 K=1,N
20 YI(K)=Y(K)+A(J)*D(K)
YF(K)=YF(K)+A(J+1)*D(K)/3
RETURN
END

```

```

SUBROUTINE FUNC (X,Y,N,D,CR,RA,XLA,FL,CM,E,RJ,Kc,Kv,L,T,T1,T2
DIMENSION Y (20),D (20)
REAL KC,KV
DO 16 M=0,(L-1)
IF(X-M*T).LE.T1) GO TO 11
IF((X-M*T).LE.(T1+T2)) GO TO 12
18 CONTINUE
11 VA=400.
GO TO 21
12 VA = - 400.
GO TO 21
21 CONTINUE
D (1) = (VA-E-RA*Y(1))/XLA
D (2) =(CM-CR)/RJ
RETURN
END

```

APPENDIX B (continued)

A>

A>type drive.lst

'dc motor control'

ln	addr	obj	code	t	e	i	line	source	statement
1							1	.title	"'dc motor control'"
2							2	init1	.equ 0d800h
3							3	piod	.equ 09h
4							4	pioc	.equ 0bh
5							5	ctc0	.equ 10h
6							6	.org	init1
7	D800	3E0F					7	ld	a,0fh
8	D802	D30B					8	out	(pioc),a
9	D804	3E07					9	ld	a,07h
10	D806	D30B				10	out	(pioc),a	
11	D808	3EC7				11	ld	a,0c7h	
12	D80A	D310				12	out	(ctc0),a	
13	D80C	3E01				13	ld	a,01h	
14	D80E	D310				14	out	(ctc0),a	
15	D810	16FF				15	ld	d,0ffh	
16	D812	1E1F				16	ld	e,1fh	
17	D814	0636				17	ld	b,36h	
18	D816	0E36				18	ld	c,36h	
19	D818	C31CD8				19	jp	main	
20	D81B	C9				20	ret		
21	D81C	78				21	main	ld a,b	
22	D81D	B7				22	or	a	
23	D81E	CA31D8				23	jp	z,ind2	
24	D821	78				24	ld	a,b	
25	D822	D61C				25	sub	1ch	
26	D824	FA2CD8				26	jp	m,ind1	
27	D827	05				27	dec	b	
28	D828	15				28	dec	d	
29	D829	C351D8				29	jp	out	
30	D82C	05				30	ind1	dec b	
31	D82D	14				31	inc	d	
32	D82E	C351D8				32	jp	out	
33	D831	79				33	ind2	ld a,c	
34	D832	B7				34	or	a	
35	D833	CA46D8				35	jp	z,ind4	
36	D836	79				36	ld	a,c	
37	D837	D61C				37	sub	1ch	
38	D839	FA41D8				38	jp	m,ind3	
39	D83C	0D				39	dec	c	
40	D83D	1D				40	dec	e	
41	D83E	C351D8				41	jp	out	
42	D841	0D				42	ind3	dec c	
43	D842	1C				43	inc	e	
44	D843	C351D8				44	jp	out	
45	D846	16FF				45	ind4	ld d,0ffh	
46	D848	1E1F				46	ld	e,1fh	
47	D84A	0636				47	ld	b,36h	
48	D84C	0E36				48	ld	c,36h	
49	D84E	C351D8				49	jp	out	
50	D851	78				50	out	ld a,b	
51	D852	B7				51	or	a	
52	D853	CA5CD8				52	jp	z,exit1	
53	D856	7A				53	ld	a,d	
54	D857	D309				54	out	(piod),a	
55	D859	C35FD8				55	jp	exit2	
56	D85C	7B				56	exit1	ld a,e	
57	D85D	D309				57	out	(piod),a	

APPENDIX B (continued)

'dc motor control'					
ln	addr	obj code	t e i	line	source statement
1	D85F	3E02		58	exit2 ld a,02h
2	D861	26FF		59	loop1 ld h,0ffh
3	D863	2EFF		60	loop2 ld l,0ffh
4	D865	2D		61	loop3 dec l
5	D866	C265D8		62	jp nz,loop3
6	D869	25		63	dec h
7	D86A	C263D8		64	jp nz,loop2
8	D86D	3D		65	dec a
9	D86E	C261D8		66	jp nz,loop1
10	D871	79		67	ld a,c
11	D872	87		68	or a
12	D873	C21CD8		69	jp nz,main
13	D876	16FF		70	init2 ld d,0ffh
14	D878	1E1F		71	ld e,1fh
15	D87A	0608		72	ld b,08h
16	D87C	0E08		73	ld c,08h
17	D87E	7A		74	ld a,d
18	D87F	D309		75	out (piod),a
19	D881	3E08		76	ld a,08h
20	D883	26FF		77	loop4 ld h,0ffh
21	D885	2EFF		78	loop5 ld l,0ffh
22	D887	2D		79	loop6 dec l
23	D888	C287D8		80	jp nz,loop6
24	D88B	25		81	dec h
25	D88C	C285D8		82	jp nz,loop5
26	D88F	3D		83	dec a
27	D890	C283D8		84	jp nz,loop4
28	D893	78		85	exit3 ld a,b
29	D894	87		86	or a
30	D895	CAACD8		87	jp z,ind6
31	D898	78		88	ld a,b
32	D899	D605		89	sub 05h
33	D89B	FAA5D8		90	jp m,ind5
34	D89E	05		91	dec b
35	D89F	15		92	dec d
36	D8A0	15		93	dec d
37	D8A1	15		94	dec d
38	D8A2	C3C5D8		95	jp out1
39	D8A5	05		96	ind5 dec b
40	D8A6	14		97	inc d
41	D8A7	14		98	inc d
42	D8A8	14		99	inc d
43	D8A9	C3C5D8		100	jp out1
44	D8AC	79		101	ind6 ld a,c
45	D8AD	87		102	or a
46	D8AE	CAC5D8		103	jp z,out1
47	D8B1	79		104	ld a,c
48	D8B2	D605		105	sub 05h
49	D8B4	FAEE08		106	jp m,ind7
50	D8B7	0D		107	dec c
51	D8B8	1D		108	dec e
52	D8B9	1D		109	dec e
53	D8BA	1D		110	dec e
54	D8BB	C3C5D8		111	jp out1
55	D8BE	0D		112	ind7 dec c
56	D8BF	1C		113	inc e
57	D8C0	1C		114	inc e

APPENDIX B (continued)

'dc motor control'						
ln	addr	obj code	t e i line	source statement		
1	D8C1	1C	115		inc e	
2	D8C2	C3C5D8	116		jp out1	
3	D8C5	78	117	out1	ld a,b	
4	D8C6	B7	118		or a	
5	D8C7	CAD0D8	119		jp z,exit4	
6	D8CA	7A	120		ld a,d	
7	D8CB	D309	121		out (piod),a	
8	D8CD	C303D8	122		jp exit5	
9	D8D0	-7B	123	exit4	ld a,e	
10	D8D1	D309	124		out (piod),a	
11	D8D3	3E01	125	exit5	ld a,01h	
12	D8D5	262F	126	loop7	ld h,2fh	
13	D8D7	2E5F	127	loop8	ld l,5fh	
14	D8D9	2D	128	loop9	dec l	
15	D8DA	C2D9D8	129		jp nz,loop9	
16	D8DD	25	130		dec h	
17	D8DE	C2D7D8	131		jp nz,loop8	
18	D8E1	3D	132		dec a	
19	D8E2	C2D5D8	133		jp nz,loop7	
20	D8E5	79	134		ld a,c	
21	D8E6	B7	135		or a	
22	D8E7	C293D8	136		jp nz,exit3	
23	D8EA	16FF	137	init3	ld d,0ffh	
24	D8EC	1E1F	138		ld e,1fh	
25	D8EE	0608	139		ld b,08h	
26	D8F0	0E08	140		ld c,08h	
27	D8F2	7A	141		ld a,d	
28	D8F3	D309	142		out (piod),a	
29	D8F5	3E08	143		ld a,08h	
30	D8F7	26FF	144	loop10	ld h,0ffh	
31	D8F9	2EFF	145	loop11	ld l,0ffh	
32	D8FB	2D	146	loop12	dec l	
33	D8FC	C2FB08	147		jp nz,loop12	
34	D8FF	25	148		dec h	
35	D900	C2F9D8	149		jp nz,loop11	
36	D903	3D	150		dec a	
37	D904	C2F7D8	151		jp nz,loop10	
38	D907	78	152	exit6	ld a,b	
39	D908	B7	153		or a	
40	D909	CA20D9	154		jp z,ind9	
41	D90C	78	155		ld a,b	
42	D90D	D605	156		sub 05h	
43	D90F	FA19D9	157		jp m,ind8	
44	D912	05	158		dec b	
45	D913	15	159		dec d	
46	D914	15	160		dec d	
47	D915	15	161		dec d	
48	D916	C339D9	162		jp out2	
49	D919	05	163	ind8	dec b	
50	D91A	14	164		inc d	
51	D91B	14	165		inc d	
52	D91C	14	166		inc d	
53	D91D	C339D9	167		jp out2	
54	D920	79	168	ind9	ld a,c	
55	D921	B7	169		or a	
56	D922	CA39D9	170		jp z,out2	
57	D925	79	171		ld a,c	

APPENDIX B (continued)

'dc motor control'

ln	addr	obj code	t e i	line	source	statement
1	D926	D605		172	sub	05h
2	D928	FA32D9		173	jp	m, ind10
3	D92B	0D		174	dec	c
4	D92C	1D		175	dec	e
5	D92D	1D		176	dec	e
6	D92E	1D		177	dec	e
7	D92F	C339D9		178	jp	out2
8	D932	0D		179	dec	c
9	D933	1C		180	inc	e
10	D934	1C		181	inc	e
11	D935	1C		182	inc	e
12	D936	C339D9		183	jp	out2
13	D939	78		184	ld	a, b
14	D93A	B7		185	or	a
15	D93B	CA44D9		186	jp	z, exit9
16	D93E	7A		187	ld	a, d
17	D93F	D309		188	out	(piod), a
18	D941	C347D9		189	jp	exit7
19	D944	78		190	ld	a, e
20	D945	D309		191	out	(piod), a
21	D947	3E01		192	ld	a, 01h
22	D949	265F		193	loop13	ld h, 5fh
23	D94B	2E5F		194	loop14	ld l, 5fh
24	D94D	2D		195	loop15	dec l
25	D94E	C24DD9		196	jp	nz, loop15
26	D951	25		197	dec	h
27	D952	C24BD9		198	jp	nz, loop14
28	D955	3D		199	dec	a
29	D956	C249D9		200	jp	nz, loop13
30	D959	79		201	ld	a, c
31	D95A	B7		202	or	a
32	D95B	C207D9		203	jp	nz, exit6
33	D95E	16FF		204	ld	d, 0ffh
34	D960	0604		205	ld	b, 04h
35	D962	7A		206	ld	a, d
36	D963	D309		207	out	(piod), a
37	D965	3E08		208	ld	a, 08h
38	D967	26FF		209	loop16	ld h, 0ffh
39	D969	2EFF		210	loop17	ld l, 0ffh
40	D96B	2D		211	loop18	dec l
41	D96C	C26BD9		212	jp	nz, loop18
42	D96F	25		213	dec	h
43	D970	C269D9		214	jp	nz, loop17
44	D973	3D		215	dec	a
45	D974	C267D9		216	jp	nz, loop16
46	D977	78		217	ld	a, b
47	D978	B7		218	or	a
48	D979	CA80D9		219	jp	z, ind11
49	D97C	05		220	dec	b
50	D97D	15		221	dec	d
51	D97E	15		222	dec	d
52	D97F	15		223	dec	d
53	D980	7A		224	ld	a, d
54	D981	D309		225	out	(piod), a
55	D983	3E01		226	ld	a, 01h
56	D985	265F		227	loop19	ld h, 5fh
57	D987	2E5F		228	loop20	ld l, 5fh

APPENDIX B (continued)

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'dc motor control'
ln  addr  obj code t e i line  source statement
 1  D989  2D                229  loop21  dec    l
 2  D98A  C289D9            230          jp    nz,loop21
 3  D98D  25                231          dec    h
 4  D98E  C287D9            232          jp    nz,loop20
 5  D991  3D                233          dec    a
 6  D992  C285D9            234          jp    nz,loop19
 7  D995  78                235          ld    a,b
 8  D996  B7                236          or    a
 9  D997  C277D9            237          jp    nz,exit8
10  D99A  3E2F             238          ld    a,02fh
11  D99C  26FF             239  loop22  ld    h,0ffh
12  D99E  2EFF             240  loop23  ld    l,0ffh
13  D9A0  2D                241  loop24  dec    l
14  D9A1  C2A0D9            242          jp    nz,loop24
15  D9A4  25                243          dec    h
16  D9A5  C29ED9            244          jp    nz,loop23
17  D9A8  3D                245          dec    a
18  D9A9  C29CD9            246          jp    nz,loop22
19  D9AC  060C             247          ld    b,0ch
20  D9AE  7A                248          ld    a,d
21  D9AF  D309            249          out   (piod),a
22  D9B1  78                250  exit10  ld    a,b
23  D9B2  B7                251          or    a
24  D9B3  CAB8D9            252          jp    z,ind12
25  D9B6  05                253          dec    b
26  D9B7  14                254          inc    d
27  D9B8  7A                255  ind12   ld    a,d
28  D9B9  D309            256          out   (piod),a
29  D9BB  3E01             257          ld    a,01h
30  D9BD  26FF             258  loop25  ld    h,0ffh
31  D9BF  2EFF             259  loop26  ld    l,0ffh
32  D9C1  2D                260  loop27  dec    l
33  D9C2  C2C1D9            261          jp    nz,loop27
34  D9C5  25                262          dec    h
35  D9C6  C2BFD9            263          jp    nz,loop26
36  D9C9  3D                264          dec    a
37  D9CA  C2BDD9            265          jp    nz,loop25
38  D9CD  78                266          ld    a,b
39  D9CE  B7                267          or    a
40  D9CF  C2B1D9            268          jp    nz,exit10
41  D9D2  C31CD8            269          jp    main
42                270  .end

0 error(s)

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TRANSISTOR OVERSTRESS IN BRIDGE CIRCUITS FOR MOTOR CONTROL APPLICATIONS

Interference by the anti-parallel diodes

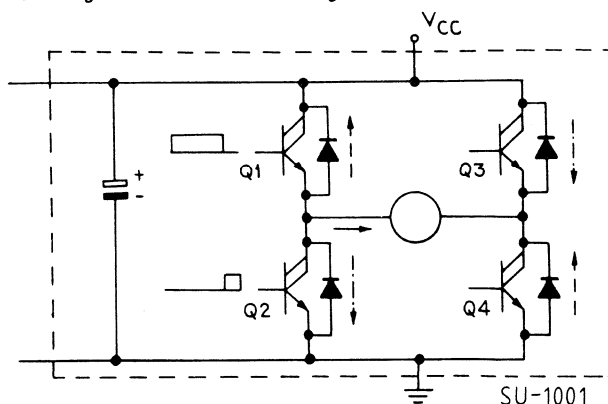
INTRODUCTION

Certain industrial drives used in robots, servos and avionics must be capable of exceptional performance to allow for very rapid speed variations. The phenomena involved, especially when braking, has been analysed to determine the stresses on the power devices in a bridge circuit driving a small dc permanent magnet motor. Although this investigation was carried out on a dc motor, the conclusions are of general validity for almost all motors. The purpose of the investigation was to locate the dangerous conditions created by the reciprocal influence of the power transistor (or darlington) and the associated fast recovery diode.

When braking the motor abruptly, the motor current reverses with respect to the previous phase, this is a consequence of the rotational energy stored in the motor which is converted into electrical energy and fed back to the filtering capacitor in parallel with the bridge.

Very high di/dt values are associated with these conditions due to both the switching of the bridge components and the fact that the supply generator faces a low impedance. These are highly critical conditions and the result can be very dangerous for the electronic components.

Fig. 1 - Current flows during normal drive and braking conditions



- Continuous line - current path during normal drive conditions
- - - Dashed line - current path during braking when $Q2$ and $Q3$ are off
- · - Dash-dot line - current path during the conduction of $Q2$ and $Q3$

PINPOINTING THE PROBLEMS

- A) Diode peak forward voltage -- during the conditions mentioned above the bridge components experience a transient voltage due to an overshoot of the forward voltage drop of the diodes at turn-on ($V_{Fdyn.}$), which is particularly high if the di/dt is large. This voltage is a transient high, negative V_{CE} value for the transistor in parallel with the diode.
- B) Positive steady state V_F -- The transistors are not in the normal bias condition for the entire period of conduction of their associated diodes (i.e. Q1 and Q4 in Fig. 1).
- C) Recovery of the CB junction -- By far the most serious phenomenon occurs when the diode turns-off and the transistor, although forward biased does not conduct. The recovery of the

diode takes place in parallel with the recovery of the base-collector junction of the transistor, this junction acts as a slow recovery diode.

FAILURE ANALYSIS

The failure mode of the device has been simulated on a curve tracer by forcing a reverse breakdown. The component put under the extreme conditions of failure in a real application was a SGS50DB045D TRANSPACK module in half bridge configuration implementing the left or right hand side of the circuit in Fig. 1. i.e. Q3, Q4 and the associated fast recovery diodes. Each transistor is made up of three fast darlington chips in parallel without parasitic c-e diodes and each diode is a single chip fast recovery epitaxial diode.

Darlington type SGSD310
Diode type SGS8R20

Photo 1 - Darlington chip inside a SGS50DB045D which failed under extreme working conditions

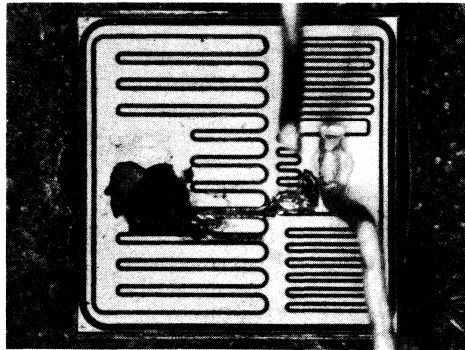


Photo 2 - A magnification of the damaged area

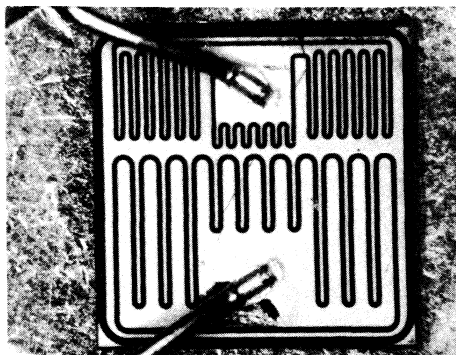


To make measurement easier a single chip darlington type SGSD310, analogous to the SGS50DB045D, was damaged intentionally on the curve tracer by a reverse collector to emitter breakdown (the SGSD310 chip can typically withstand up to

12 or 14V in this condition).

It is evident that the failure mechanism is the same in both cases and consequently, the operating conditions that can force the transistors into reverse conduction must be investigated.

Photo 3 - The SGSD310 chip which failed during simulated overstress conditions



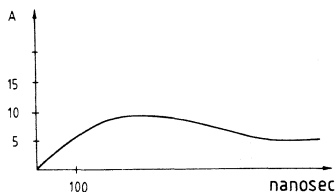
PEAK FORWARD VOLTAGE OF THE DIODE

The peak forward overvoltage (V_{FP}) on the bridge diodes is generated by very rapid current variations. In order to evaluate these variations a discrete bridge was constructed to make the diodes accessible for measurement. Each switch in the bridge was made up from three SGSD310 darlington transistors and one SGS8R20 diode, i.e. the configuration as one switch inside the TRANSPACK module.

The motor was accelerated abruptly bringing the duty cycle from 50% (zero speed) to 85% , and then braking to zero speed again in four subsequent steps. Values of di/dt as high as $50A/\mu s$ caused by the current generated during braking were observed on the diodes.

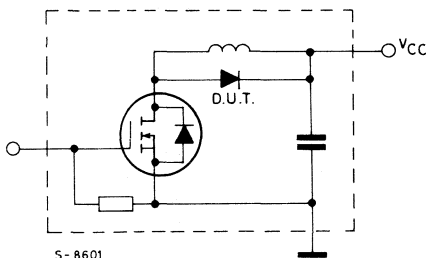
Taking into account that the discrete simulation implies stray inductances substantially larger than those inside the TRANSPACK module, the di/dt values inside the TRANSPACK are expected to be greater. In practice the connections inside a TRANSPACK are approximately 3cm long, while in the bridge constructed with discrete devices they are about 15cm long.

Fig. 2 - Waveform of the braking current through the diode



Following the above findings, some SGS8R20 diodes were tested with $di/dt = 50A/\mu s$ using the circuit shown in Fig. 3.

Fig. 3 - Basic schematic of the circuit used to measure V_F

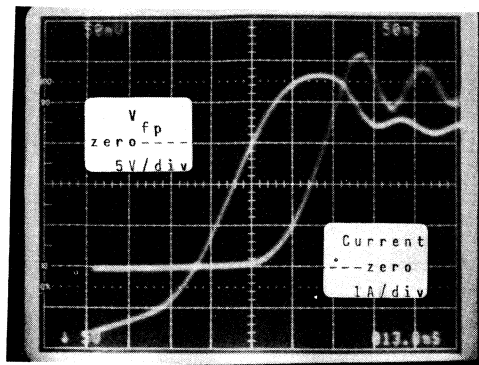


The peak voltages obtained under these conditions ($V_{F \text{ dyn.}}$) range from 7 to 9V.

A direct measurement of V_{FP} inside the TRANSPACK module was also carried out. A special configuration was used putting a $2.2K\Omega$ resistor in series with the diode chip where the forward voltage peak was measured. In this case peak voltages of about 18V were recorded, such a high value is due to both the V_{FP} of the diode as well as the stray inductance of internal connections. The oscilloscope photograph (Photo 5) shows the diode peak forward voltage inside the TRANSPACK module.

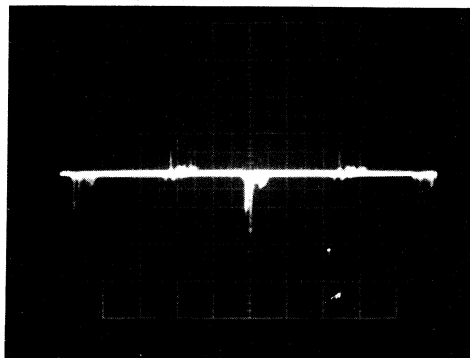
In the cases described the energy level is never high enough to imply transistor failure, due to the relatively low voltage and short length of time under stress.

Photo 4 – V_{FP} and current waveforms measured on the diode in fig. 3



V_{FP} at $di/dt = 50A/\mu s$:
 — Upper waveform V_F (5V/div)
 — Lower waveform I (1A/div)

Photo 5 – Peak forward voltage in the TRANSPACK diode: 10V/div, 10 μs /div



At diode turn-on, the transistor base is normally in the off-bias condition. There might be cases (in exceptional transitory conditions) of positive base bias at diode turn-on, mainly if the mechanical load accelerates the motor shaft instead of breaking it. However not even in this extreme case can the forward voltage peak cause transistor failure.

TRANSISTOR BEHAVIOUR

POSITIVE STEADY STATE V_F

During the braking phase another important phenomenon occurs:

Transistors Q1 and Q4 (see Fig. 1) are negatively biased (collector to emitter by the conduction of their anti-parallel diodes). Their base to emitter

junction is positively biased and consequently heavily saturated, with the emitter acting as a collector and vice-versa. In these conditions the turn-off time of the device is quite long, in the range of a few microseconds.

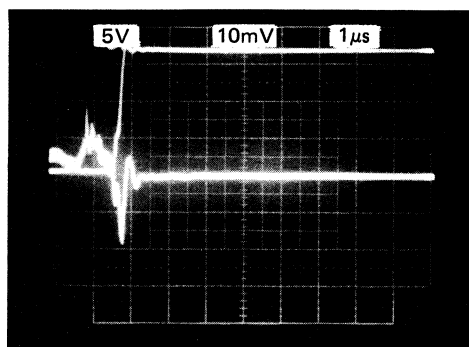
This inverse conduction of the transistor takes place during the conduction phase of the relevant anti-parallel diode. However, currents and voltages involved are small, and consequently during this "steady state" phase no overstressing of the transistor due to power dissipation occurs.

RECOVERY OF THE CB JUNCTION

There is a substantial power dissipation at diode turn-off when V_{CE} becomes high while a significant time elapses before the current through the collector disappears. This is mainly because the collector to base junction, forward biased during anti-parallel conduction, is slow in removing the stored charge when its biasing is reversed.

This situation is shown in Photo 6 (waveforms refer to Q4 in Fig. 1) where it can be noted that at a V_{CE} of 170V (the upper switch in the bridge has turned on), a current as much as 4A still remains in Q4, because the c-b junction has not yet depleted the stored charge from the previous phase of conduction.

Photo 6 – Current and voltage waveforms during inverse conduction



Upper waveform: V_{CE} (50V/div)
 Lower waveform: I_C (2A/div)

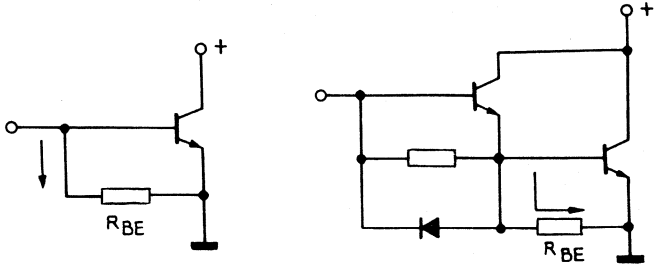
It is important to understand why a transistor that is supposed to receive a negative base bias, during conduction of the anti-parallel diode, conducts even though it is in reverse mode.

This actually happens when, instead of a negative bias, there is an unexpected positive base bias. In most cases an effective negative bias is applied to the base to turn off the transistor, and shortly after the turn-off phase a resistive path from emitter to base (R_{BE}) maintains the off-state.

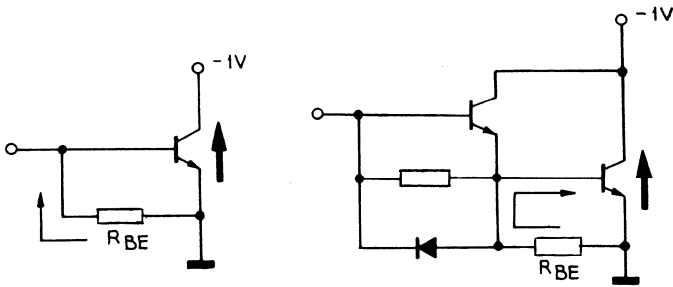
During the braking phase (when the anti-parallel diode conducts) the base to emitter resistance becomes a path for positive base current when the emitter is more positive than the collector. This is the origin of reverse conduction in a transistor

(or a darlington which has an integrated R_{BE} in the final transistor). The value of R_{BE} is of prime importance as the smaller it is, the larger the reverse conduction current.

Fig. 4 - The R_{BE} of the final transistor becomes a positive bias element if the collector is negative



4A) Positive collector: R_{BE} sinks the leakage current and ensures the off-state.



SU-1002

4B) Negative collector (V_F of the anti-parallel diode):

- The emitter acts as a collector and vice-versa;
- R_{BE} acts as a negative base current;
- I_B is multiplied by the gain (in reverse mode);
- A substantial charge is stored in the forward biased collector to base junction.
- It can take a few microseconds for this junction to recover to the off-state when the collector becomes positive again.

CONCLUSIONS

The analysis shows that the biasing of the collector-emitter junction of the bridge transistor by conduction of the free-wheeling diode, can over-stress it and even induce a failure. The origin of the failure is not only due to the peak overvoltage of the diode, since its duration is too short (about 100ns) but primarily to the reverse conduction of the transistor during turn-off of the bridge switch. The c-b junction therefore acts as a slow recovery

anti-parallel diode and if charge has been stored in this junction it causes the greatest stress on the device.

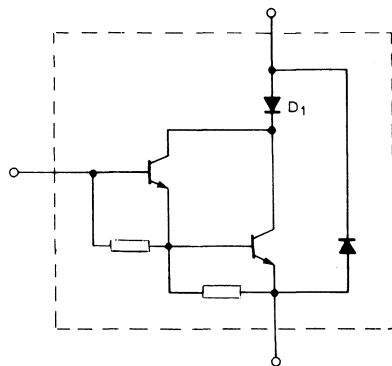
The transistor failure (disregarding the overstresses induced on purpose), is in practice triggered by more than the single switching phase described above, it is more a series of subsequent stresses at each switching cycle which leads the device into a critical state. It is also easy to appreciate that the failure concludes a phase of abnormal heating in a concentrated spot on the chip.

Whenever possible it is advisable to avoid alternate switching of the bridge diagonals, and only turn on one pair of the transistors when their conduction is required.

The overstress could be avoided by negatively biasing the base-emitter junction during the period of possible reverse conduction of the transistor. To maintain a negative V_{BE} is certainly a solution, but its implementation could be costly with an auxillary negative supply for each switch. On the other hand it is not possible to use a simple capacitor to store the charge for this purpose, as a motor drive circuit has a substantial duty cycle variation and a single value capacitor can only satisfy a fixed turn-off time.

Another more classical solution could be the introduction of a low voltage (both forward and reverse diode) diode in series with the collector, as shown in Fig. 5. The drawback in using this method is the additional power dissipation, while there is the advantage of simple implementation in open loop systems.

Fig. 5 - Circuit solution with a low voltage diode D1



SU-1009

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PARALLELING TRANSPACK MODULES

A practical example

INTRODUCTION

The requirement for a higher current rating than a single module can provide is not uncommon, but the circuit designer probably questions the practical feasibility of paralleling large transistor modules such as the SGS TRANSPACK.

Although these device are more complex than discrete transistors, in practice they can be paralleled quite easily, the main point to keep in mind is current sharing between the paralleled modules during turn-off when loaded inductively.

offer practically the same power switching capability. If a device is rated for a higher voltage, it will consequently be rated for a lower current.

As a result, it is clear that the most common case of paralleling occurs with high voltage parts.

The SGS30DA070D has been selected for this example as it represents the highest current rating in the high voltage range of TRANSPACK modules.

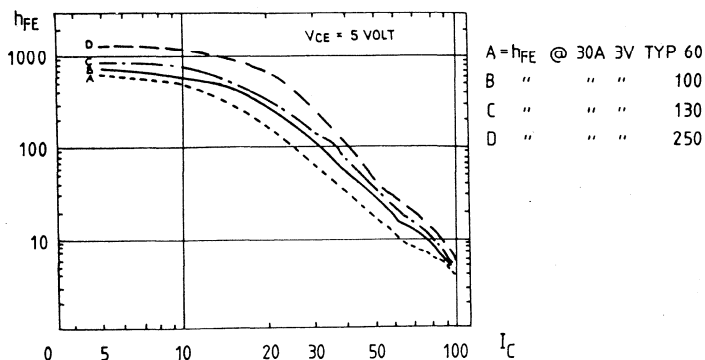
THE MOST COMMON CASE

Different kinds of SGS TRANSPACK modules

SGS30DA070D IN PARALLEL

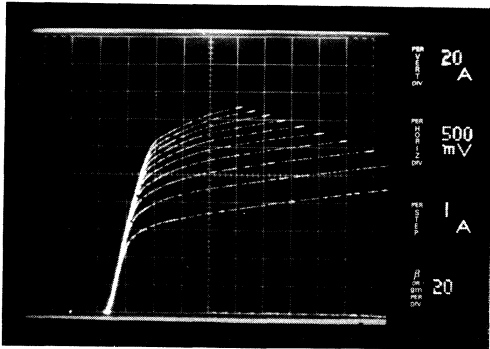
Four modules were used for the practical investigation and the relevant h_{FE} curves versus I_C can be seen in Fig. 1.

Fig. 1 - h_{FE} curves of four SGS30DA070D modules



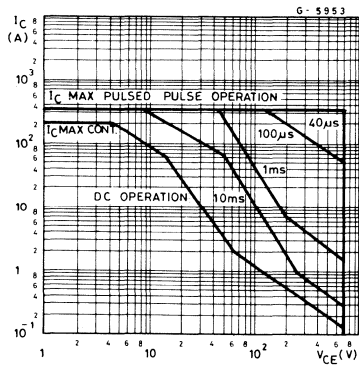
The h_{FE} variation between module A (h_{FE} typical 60) and module D (h_{FE} typical 250) represents a significant spread and by using one with high gain and two with low gain in parallel it has been possible to simulate extreme operating conditions.

Fig. 2 – Output characteristics of three paralleled modules



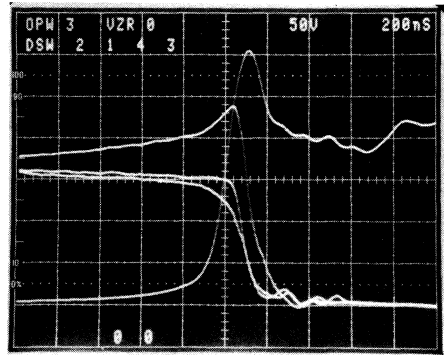
The curve tracer photograph Fig. 2 shows the output characteristics of the three SGS30DA070D TRANSPACK power modules in parallel and Fig. 3 shows the forward bias safe operating area for the same parallel circuit. It can be seen from these SOA characteristics that for normal pulsed operation, the paralleled modules can safely handle very high power levels.

Fig. 3 – Safe operating area (forward bias) of three SGS30DA070D in parallel



The most important point for consideration is the turn-off switching transition shown in Fig. 4, the three modules have a separate bias circuit which consists of two resistors (3.3k and 100Ω) and a single speed-up diode.

Fig. 4 – Turn-off transition of three SGS30DA070D modules in parallel



$t = 200\text{ns/div.}$
 $V_{CE} = 50\text{V/div.}$
 $I_{C1,2,3} = 5\text{A/div}$
 $V_{CC} = 200\text{V}$
 $V_{BE}(\text{extraction}) = -3\text{V}$
 $I_B(\text{extraction}) = 17\text{A}$
 $t_{stg}(\text{storage}) = 27\mu\text{s}$

In the oscilloscope photograph the three collector currents are shown separately, the device with the higher h_{FE} exhibits a current overshoot and as consequence an increased storage time.

Fig. 5 – RBSOA test driving circuit

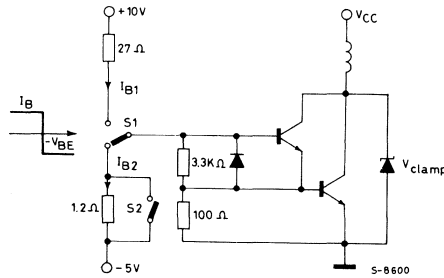
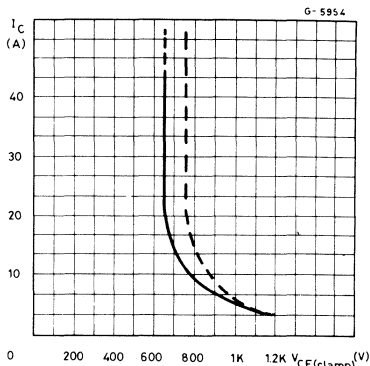
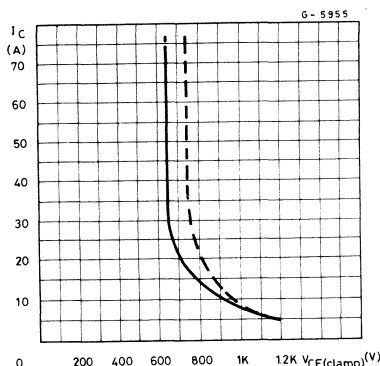


Fig. 6 – RBSOA of a single SGS30DA070D



The reverse bias safe operating area was obtained using the test driving circuit shown in Fig. 5. The RBSOA characteristics for a single module (Fig. 6) and the three modules in parallel (Fig. 7) show that the high voltage boundary is the same for both arrangements.

Fig. 7 - RBSOA of the three devices in parallel



The addition of a 1.2Ω resistor in the test driving circuit to limit the negative base current improves the high voltage boundary of both RBSOA characteristic curves, the dotted line corresponds to the new boundary.

THE BEST CHOICE

This example demonstrates the performance of

devices which were not specifically selected for the test. A further improvement can be achieved if parts with very close h_{FE} values are paralleled together, ideally the three parts should remain within a $\pm 10\%$ h_{FE} range.

h_{FE} matching ensures that the paralleled parts have almost the same storage time and that none of them supports the entire load current, during the interval between turn-off of one module and turn-off of the other two.

The high switching speed of SGS devices helps to minimise any minor variations between matched modules.

CONCLUSIONS

Care must be taken to ensure that current is equally shared between paralleled modules and layout is optimised to reduce stray inductance in the interconnection leads.

The easiest way to ensure a fair sharing of the current is by adding a separate speed up diode and bias resistor network to each module. However, this will not prevent the possibility of current overshoot in one module during turn-off (as shown in Fig. 4) so for optimum results it is best to ensure current matching during turn-off.

The most practical way is to use parts with h_{FE} values within a $\pm 10\%$ band for paralleled operation. SGS TRANSPACK power modules can be supplied in gain groups to suit customer applications.

ROBUSTNESS OF HIGH VOLTAGE POWER TRANSISTORS

INTRODUCTION

Most semiconductor manufacturers publish safe operating area (SOA) curves of some form in their data-sheets. These published curves are intended to convey to the user, the electronic equipment designer, a measure of the device robustness. The forward bias safe operating area (FBSOA) indicates the collector emitter voltage and current capability with the base emitter junction forward biased. The reverse bias safe operating area (RBSOA), as the name implies, indicates the collector emitter voltage and current capability with the base emitter junction reverse biased. This curve is used to determine the locus of the transistor operating point during the transition from forward biased conduction to the cut-off state.

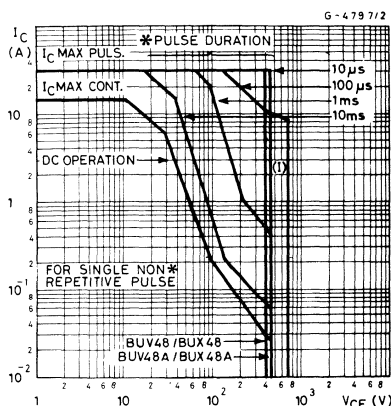
Generally speaking, safe operating area curves have been published for the transistor case temperature at 25°C. Derating is required, the amount being dependent on the transistor operating temperature and the temperature derating factor. Different derating factors are applied by some manufacturers to different parts of the SOA curve, depending on the failure mechanism which limits the transistor performance in that area. Thus, it is common to see both 'power derating' and ' $I_{s/p}$ (second breakdown) derating' factors published. Additions to the standard SOA curves are being made as the capabilities and the understanding of the process technology are improved. In particular, extensions above the V_{CEO} rating of the transistor are seen in both FBSOA and RBSOA curves to indicate the transistor capability during 'switch-on' and 'switch-off' transitions.

Non repetitive overload safe area curves are also appearing, and these will be found particularly useful in the motor control area. However, a degree of caution is necessary on the part of the design engineer in interpretation of this additional information. The semiconductor manufacturer will have defined the test conditions for which the overload safe area curve applies. Disparity between the application circuit and the semiconductor manufacturers test circuit, including any preconditioning, can cause significant differences in the ability of the transistor to withstand an overload.

FORWARD BIAS SAFE OPERATING AREA

The forward bias safe area for the SGS BUX48/SGS BUV48 transistor families is shown in figure 1. The curves apply for a case temperature of 25°C. The lower curve represents the continuous conduction case, with collector current, I_C , limited to 15 amps and collector emitter voltage, V_{CE} limited to 400V, or 450V for the 'A' part, 600V for the 'B' part or 700V for the 'C' part. Beyond the 15A 10V point on the curve, the current rating falls in conformance to the maximum power rating of the transistor. There are 2nd and 3rd break points (change of gradient) on the curve at 6A and 0.2A. In these areas the transistor is no longer limited by total power rating, but by second breakdown.

Fig. 1 - BUX48/BUV48 forward bias safe operating area



The outer set of curves represent the pulse current capability, as opposed to the DC capability of the transistor. The rating applies for a single pulse, so that the duty cycle effect and resulting temperature increase is discounted. All of these curves are terminated at the V_{CEO} rating (400V - 700V) of the transistor. A small additional area, marked

'I' has been added, and represents the permissible area of operation for 'turn-on' from a voltage in excess of V_{CE0} .

Figure 2. Illustrates the overload SOA for the BUX48 transistor. The SOA applies for a maximum case temperature of 125°C and for a single pulse of $20\mu\text{s}$ duration. The lower, hatched area of the curve is the normal FBSOA. Repetitive pulses are permitted in the hatched area, provided that the thermal limitations of the transistor are complied with.

Fig. 2 - BUX48 overload safe operating area

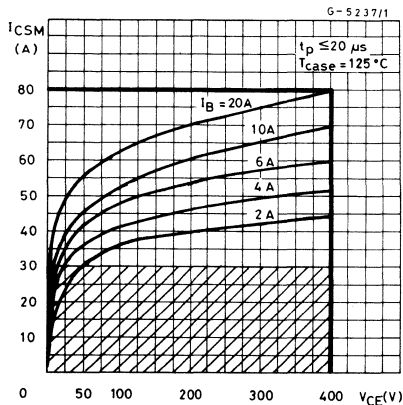
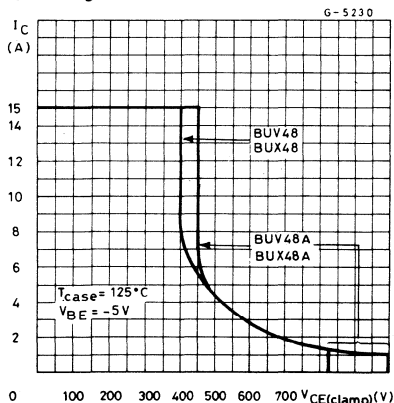


Fig. 3 - BUX48/BUV48 clamped reverse bias safe operating area



REVERSE BIAS SAFE OPERATING AREA

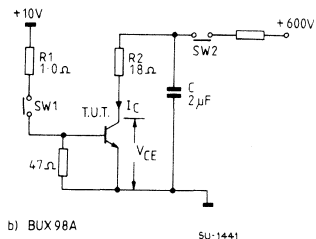
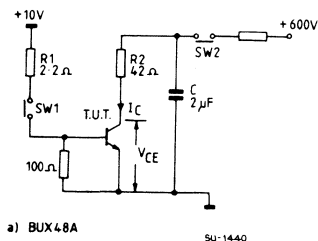
The clamped reverse bias safe operating area for the SGS BUX48/SGS BUV48 family of transistors is illustrated in figure 3. This curve should not be confused with the overload forward safe area previously mentioned. The conditions under which the tests were made in order to achieve the results

from which the curve has been derived are: Case temperature 125°C and base emitter reverse bias of 5V . The tests were performed with an inductive load, and with the collector emitter voltage appropriately clamped. The reverse bias SOA is, by it's nature, always a transient test condition. For this reason, time is not a control variable. The 'switch off' time of the transistor is determined by the test conditions.

SAFE AREA TEST CIRCUITS

The circuits shown in figures 4a and 4b illustrate a relatively simple way of measuring the FBSOA for the BUX48 and BUX98 transistor families respectively. Resistor R1 value is chosen to provide sufficient base current to saturate the transistor at the peak collector current which is, in turn, set by resistor R2. The resistor values shown are suitable for testing the transistor at rated DC collector current (15A and 30A respectively). The first step in the test cycle is to charge the high voltage capacitor, C to the appropriate voltage (V_{CE0} rating of the D.U.T.) with the base drive switch 'open'. The second step is to 'open' the capacitor charging switch, so disconnecting the high voltage supply from the test circuit, and to close the switch providing the forward base current. Closure of the switch turns on the T.U.T. which subsequently discharges the capacitor C through resistor R2.

Fig. 4 - Forward bias safe area test circuits



The operating point for the transistor follows the locus illustrated in figures 5 and 6. As the test is a 'one shot' measurement, temperature rise in the T.U.T. is negligible and the case temperature remains at 25°C .

Fig. 5 - Theoretical operating locus in FBSOA test

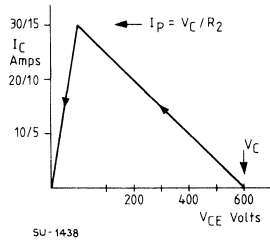
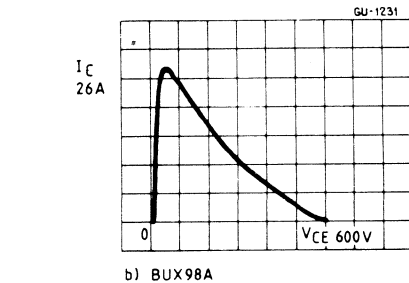
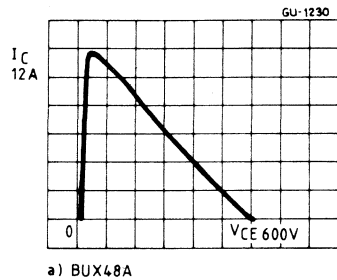


Fig. 6 - Oscilloscope display of operating locus in FBSOA test



The reverse bias SOA test is performed in 2 stages. This is to achieve a 'best fit' to the SOA curve. The first part of the test exercises the high current RBSOA extending up to the V_{CE0} for the transistor. The second part exercises the low current, high voltage area extending to V_{CER} . Figure 7. Illustrates the test circuit. Switch 1 closes to turn the T.U.T. 'on'. The condition time is controlled to limit the peak collector current.

As switch 1 opens, switch 2 closes reverse biasing the base emitter junction of the T.U.T. Following the storage time delay, during which time the excess charge in the collector base junction is extracted, the collector emitter voltage rises instantaneously to V_B when the rectifier, D1 conducts

returning the inductive energy stored in L to the supply, V_B . Resistor R3 connected in series with the rectifier D1 shapes the load line and so determines the locus of the operating point of the T.U.T. during 'turn off'. The peak voltage across the T.U.T. will be:

$$V_{CEpk} = V_B + I_{Cpk} \cdot R_3 + V_F D1$$

This simple equation neglects the effects of circuit wiring inductance and the forward recovery time of the rectifier, D1. Some adjustment in V_B or R3 value may be required to compensate for these effects. Figures 8 and 9 illustrate the locus of the operating point of the T.U.T. during 'turn off'.

Fig. 7 - Reverse bias safe area test circuit

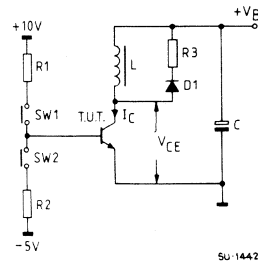


Fig. 8 - Theoretical operating loci in RBSOA tests

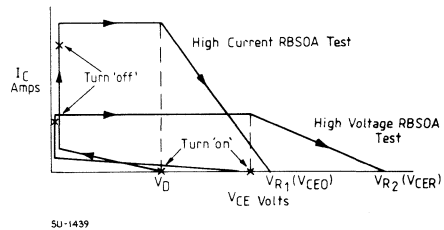


Fig. 9 - Oscilloscope display of operating loci in RBSOA test

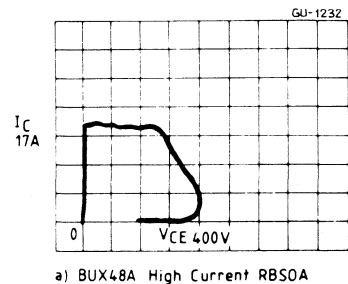
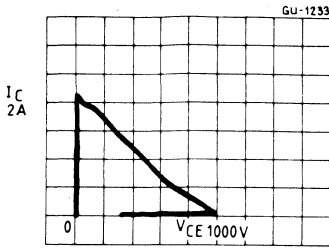
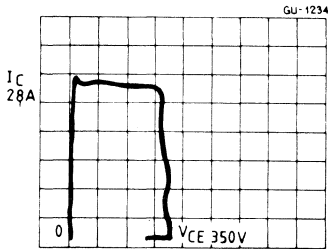


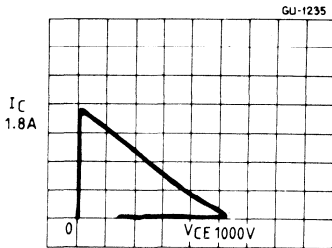
Fig. 9 (continued)



b) BUX48A High Voltage RBSOA



c) BUX98A High Current RBSOA



d) BUX98A High Voltage RBSOA

It is important when making measurement of RBSOA using an oscilloscope with X-Y display that the time delay in both X and Y amplifiers are

reasonably well matched. Otherwise, significant distortion of the operating locus display may occur.

POWER MOS TRANSISTORS

These are majority carrier devices which inherently do not exhibit the second breakdown phenomena that have plagued their bipolar counterparts. A glance at the FBSOA curve for a POWER MOS transistor will show that the device has a 'square loop' SOA capability, limited only by the power dissipation and maximum junction temperature of the semiconductor dice. The FBSOA extends all the way up to the BV_{DSS} , the drain source breakdown voltage rating. The inherent current sharing ability and the independence of its transconductance from I_D , the drain current, allow the POWER MOS transistor an increased surge current rating when compared with a bipolar transistor of equivalent DC current rating. There are no separate RBSOA curves for the power MOS device, the FBSOA can be used as the forward and reverse bias conditions are similar.

POWER MOS IN AVALANCHE BREAK-DOWN

SGS along with the majority of semiconductor manufacturers producing POWER MOS transistors, do not publish data, or recommend the use of the drain source avalanche capability of the device. There are several reasons for adopting this policy:

Avalanche energy capability is:

- not a function of dice size alone.
- drain current dependent.
- temp. dependent.
- dv/dt dependent.

A consensus of opinion on the failure mechanisms involved has not been seen.

Long term effects of operating in avalanche breakdown mode have not been evaluated.

In time, improvements in the understanding of the capabilities of POWER MOS transistors will emerge and the manufacturers will doubtless publish more definitive information.

TECHNOLOGY RELIABILITY AND APPLICATIONS OF SGS HIGH VOLTAGE NPN TRANSISTORS

Introduction

The basic technology chosen for high voltage ($V_{CE0} > 400V$ - $V_{CBO} > 600V$) transistors is fundamental to their in-circuit performance as well as their "built-in" reliability.

Also the technology effects the wafer size which may be used in production, as well as the yields. In some cases also packaging options may be restricted. These are important factors influencing the price and availability for any semiconductor device.

Subject

This note discusses the SGS Multiepitaxial Mesa process used for a wide variety of industry standard products as well as some innovative types.

This technology is illustrated in simplified form in figure 1, figure 2 shows an actual cross section of the edge of a die made up of several scanning electron microscope pictures.

Fig. 1a - Multiepitaxial Mesa wafer simplified cross section

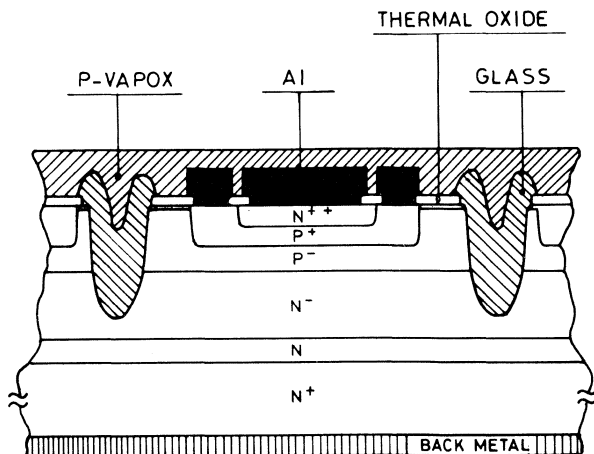


Fig. 1b - Multiepitaxial Mesa die in plan view

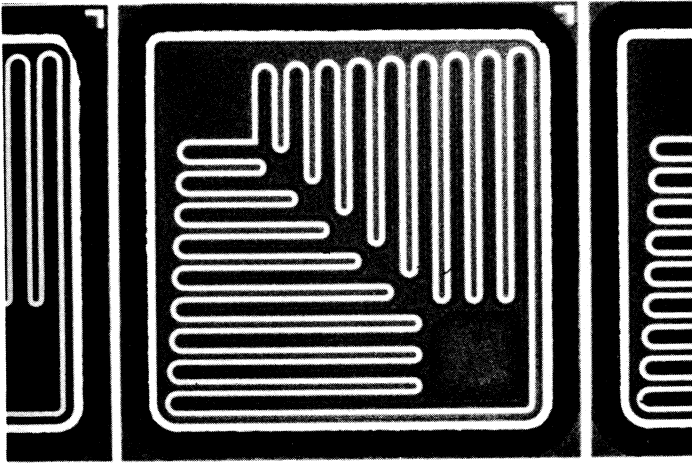
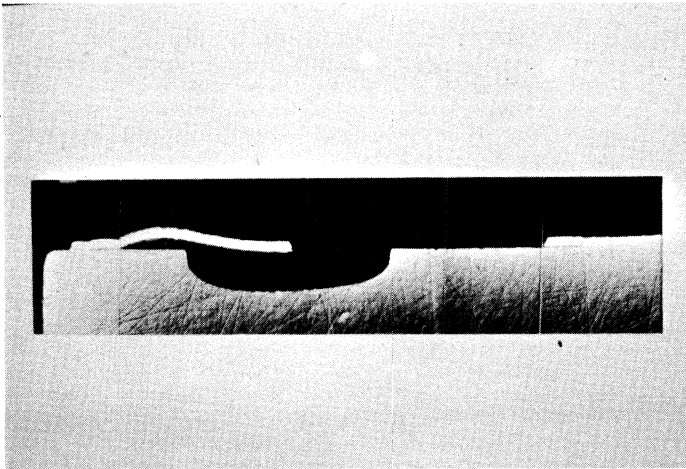


Fig. 2 - Actual section of Mesa edge termination



Features of the technology

Starting with an N^+ wafer, the N and N^- collector layers are grown in specially developed epitaxial reactors, to produce the layered structure of the collector for the H.V. transistors.

The thicknesses required are much higher than used in integrated circuit technologies.

The intermediate N layer was interposed for the main purpose of achieving a very high $E_{s/b}$ and RBSOA capability.

An additional P^- layer is then grown, to increase the voltage breakdown. For this first critical phase SGS is fully equipped to grow epitaxial layers entirely "in house" while other power transistor manufacturers are mostly dependent on outside suppliers.

The P^+ base is produced by diffusion of boron into the final P^- layer and the N^+ emitter is diffused into the base. It is important to note that during this processing a relatively thick wafer is being

handled allowing SGS to use 4" and 5" wafers with ease.

Following diffusion is the etching of the mesa which is filled with a very pure glass by an SGS patented selective deposition process which avoids any contaminants such as photoresist which may not be entirely evaporated during the fusion of the glass. The aluminium top metal is now deposited and the pattern defined. The entire top of the wafer is now protected by a thick deposited oxide in which windows are opened for bonding the base and emitter connecting wires.

Finally the wafer is reduced to the correct thickness, removing the excess N⁺ silicon by grinding the back of the wafer, after which the back is metallized.

Packaging

As the die must be separated from the wafer before

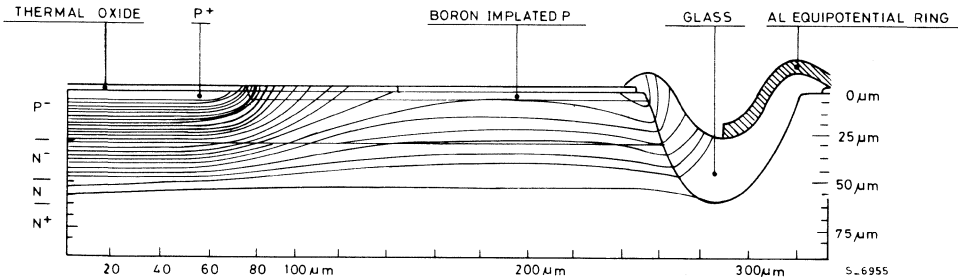
mounting in the package the fact that SGS cuts the silicon outside the mesa and its glass filling, eliminates the risk of mechanical damage to the passivation.

As the sawing creates a short circuit at the edge of the die from the collector to the field plate no "flashover" can occur in the package between the header which is at collector potential and the top of the die, which in alternative half mesa technologies will be at base potential. The surface is covered with a thick oxide as previously mentioned so no arcing occurs along the surface.

This process of passivation also ensures high reliability in plastic packages.

This technology also allows wafers to be 100% probe tested to high voltage specifications, an important point for users of high voltage transistors in chip form for hybrid assemblies.

Fig. 3 - Section of Mesa with simulated equipotential lines



Reliability

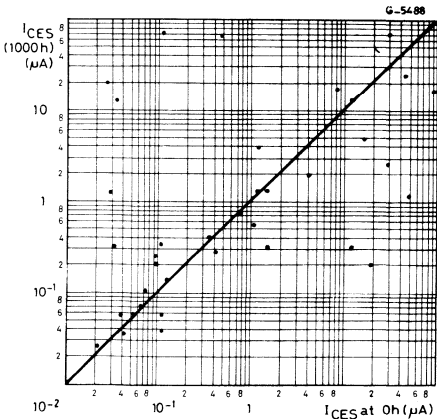
In the reliability of a high voltage transistor the voltage stress on the surface of the silicon in the region of the collector/base interface is very important. This region must be protected from contamination. By terminating the collector-base junction on the edge of the mesa, and using glass as the sealing against potential contaminants is assured. The use of the aluminium field plate ensures the glass is kept at a constant charge. The surface of the P-layer is treated with an ion implantation to ensure a very well controlled surface doping thus aiding close control of the electric field strength distribution and leakage currents. SGS has developed computer simulation programs which can predict the field strength enabling the design to be optimised for reliability. Figure 3 shows the equipotential lines superimposed on the actual device cross section demonstrating the low stress on the surface.

SGS continually monitors the reliability of the process by sampling production on a weekly basis. The high temperature reverse bias test (HTRB) is used to evaluate the stability and quality of the passivation.

Devices are subjected to T_{amb} = 125°C with the

base-emitter shorted, and 600V d.c. is applied to the collector. Figure 4 shows typical results of leakage currents measured at V_{ces} = 900V, a point on the line at 45 degrees indicates no drift in

Fig. 4 - Leakage current stability in HTRB life tests



leakage. It is important to note that the currents involved are much lower than the specified maximum allowed by the data sheet. The devices with significant drift are those with initial leakage below $1\mu\text{A}$ and they remain below $80\mu\text{A}$ following 1000 hours of extreme stress.

Application hints

The basic rules of application for fast switching high voltage devices apply equally to SGS devices as well as other manufactures who use different technologies however some points deserve particular mention.

The multiple epitaxial structure with its "energy layer" provides an exceptional RBSOA, figure 5 shows the RBSOA of the BUX48/BUV48 which can sustain up' to 2A at 700V or 15A at 400V during the device turn-off with an inductive load.

Figure 6 shows the accidental overload safe operating area. The safe limit, up to 80A at any voltage up to 400V, is independent of the transistor base current, the lines with different base current indicate the maximum current which can be expected when the load is short circuited for any supply voltage. The overload must be sensed within 20 microseconds and the base drive removed at which time the accidental overload reverse bias safe operating area, shown in figure 7, will apply.

This data shows that for occasional non-repetitive overloads the multi-epitaxial structure is exceptionally robust. As an indication devices have been stressed to 80A/400V for 40 microseconds during the on phase and then turned off at a P.R.F. of 100Hz for 4 hours without degradation - nearly 1.5 million pulses!

Attention should be paid to correct turn-on base drive. The BUX48/BUV48 data shows the dynamic $V_{CE(sat)}$ characteristics (figure 8) which are significantly improved by ensuring an overshoot of I_{B1} illustrated in figure 9.

Fig. 6 - Accidental overload SOA of BUX48/BUV48

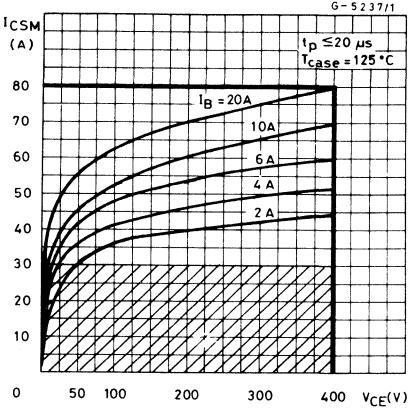


Fig. 7 - Accidental overload RBSOA of BUX48/BUV48

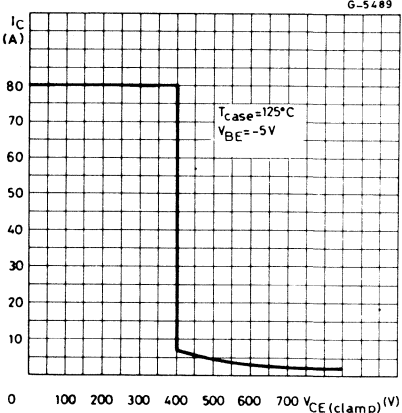


Fig. 5 - RBSOA of SGS BUX48/BUX48A (TO-3), BUV48/BUV48A (SOT-93)

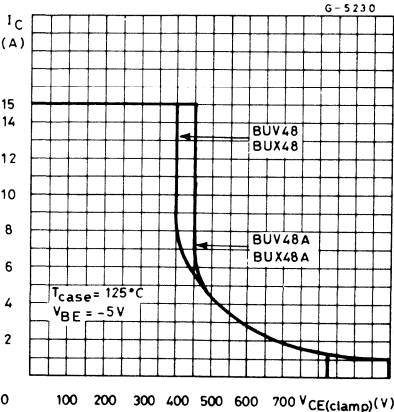


Fig. 8 - Dynamic $V_{CE(sat)}$ of BUX48/BUV48

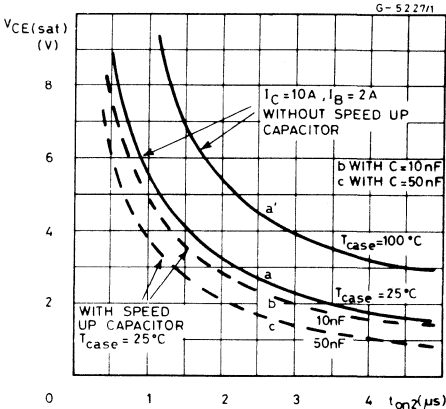
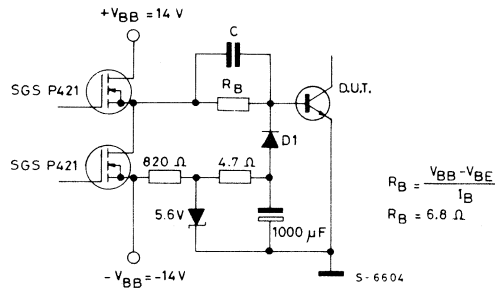
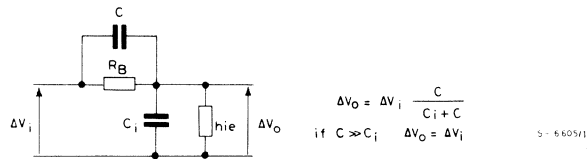


Fig. 9 - I_{B1} waveform for improved dynamic saturation

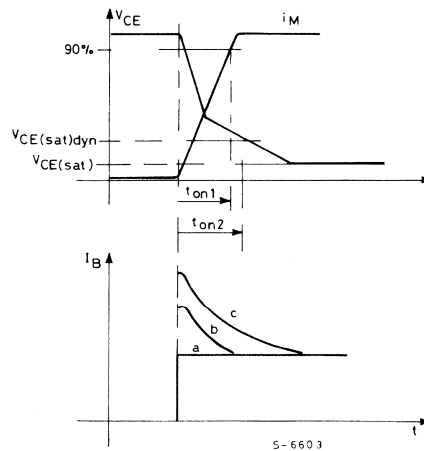
$V_{CE(sat)}$ dynamic test circuit



Equivalent input schematic circuit at turn-on



Remarks to $V_{CE(sat)}$ dyn. test circuit



The speed-up capacitor decreases the $V_{CE(sat)dyn}$ as shown in the diagram and modifies the shape of the base current with an overshoot.

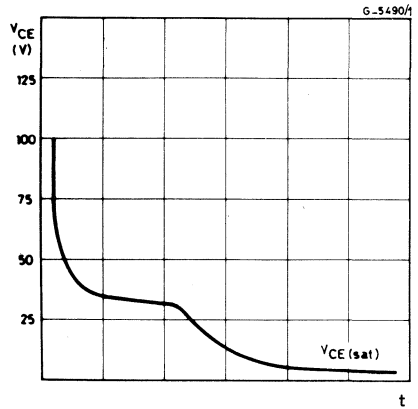
A slow rise time of I_{B1} can result in extremely high turn-on losses, as shown in figure 10 the multi-epitaxial device will have a V_{CE} of around 40V for some microseconds. This results in higher junction temperatures and in turn longer turn-off switching times, sometimes these longer turn-off times are misinterpreted as being a "cause" rather than an "effect". This can be cured by similar solutions as used to improve dynamic $V_{CE(sat)}$.

Conclusion

The Multiepitaxial Mesa process has been demonstrated to be a high volume, cost effective process yielding products with high intrinsic reliability and exceptional ruggedness to enhance field reliability.

The process is very flexible being readily "pilotable" to produce higher voltage or higher current "sub families" with good yield, thus avoiding the risks for both the user and the suppliers of selections from lower performance types.

Fig. 10 - High turn-on loss caused by too slow I_{B1} rise time



SECOND BREAKDOWN IN POWER TRANSISTORS

One of the basic failure mechanisms in power transistors is second breakdown.

Under this term, various physical phenomena which are completely different are included. They depend on the different use of transistors in the circuits and have in common the electrical and thermal instability inherent in transistors themselves.

The conduction behaviour of an emitter base junction and the current gain of a transistor depend significantly on the temperature and increase as a function of the temperature. Electrical and thermal instabilities may simultaneously act within the device, thereby giving rise to destructive second breakdown mechanism.

An understanding of this mechanism is of great importance for a safer and optimum application of a power transistor.

A distinction should be made between direct second breakdown ($I_{S/B}$ or more commonly SOA), which is distinguished by a normal direction of base current I_B (entering in an NPN transistor) and inverse second breakdown ($E_{S/B}$), when I_B is in the opposite direction (extracted from an NPN transistor). The limits to which a transistor may be used without entering into $E_{S/B}$ are defined by the reverse bias safe operating area (RBSOA).

DIRECT SECOND BREAKDOWN ($I_{S/B}$)

An important information for the power circuit designer is the locus of $I_C - V_{CE}$ points defining the boundary between stable and unstable operation of forward biased transistors. This locus defines the SOA (safe operating area) that is the area of the

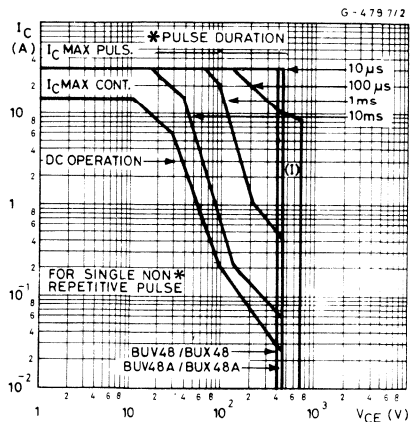
$\log I_C - \log V_{CE}$ plane which may be used without any risk in DC current conditions or with different width pulses at a known temperature. A typical SOA is shown in Fig. 1.

The limits of this area are the following:

- 1) The A-B section represents the upper limit of the collector current that may normally be used, generally limited by wire bonds. Operation at higher currents may cause damage to the wires of their bonding.
- 2) The B-C section is the -1 slope curve section (i.e. the section with constant dissipation) defined by:

$$V_{CE} \times I_C = P_{\max} = \frac{(T_{j\max} - T_o)}{R_{th}}$$

Fig. 1 - Safe operating areas



This section therefore indicates the maximum dissipable power of the device. T_{jmax} is the maximum temperature which the collector-base junction may reach, over which the device reliability may be compromised. In power transistors, T_{jmax} varies between 125 and 200 degrees C and generally depends on the metallurgy and the type of package.

R_{th} is the thermal resistance between the collector-base junction and the case, including all the silicon and package system. It may be observed that the increase of the maximum dissipable power when the pulse width decreases (Fig. 1) corresponds to the decrease of Z_{th} with respect to R_{th} .

- 3) The section C-D corresponds to the second breakdown phenomenon (or $I_{s/b}$) and limits the maximum power that the transistor can dissipate. This may occur even at relatively low V_{CE} voltages.
- 4) The section D-F is the limit due to the transistor's BV_{CEO} .

Second breakdown is generated by the electrical and thermal instability of the transistor. The main causes of this instability are;

- 1) The V_{BE} of a directly biased base-emitter junction, at constant current, decreases linearly with temperature, with a $\phi = 2$ to $2.5 mV/^{\circ}C$ slope. The base current of the transistor may therefore be expressed by:

$$I_B = I_0 \times e^{-q \frac{(V_{BE} - \phi T)}{KT}}$$

and, when V_{BE} is kept constant, it increases with temperature.

- 2) The h_{FE} at the relevant voltage values increases as a function of temperature according to the law:

$$h_{FE} = h_{FE0} \times e^{(\Delta E_g / KT)}$$

where ΔE_g is an activation energy which is a feature of the transistor.

- 3) The thermal conductivity of silicon decreases when temperature is increased, therefore worsening the thermal resistance of the transistor.

When these three phenomena are taken into con-

sideration, it may be seen that a pulse of power $P = V_{CE} \times I_C$ generates:

- a) an increase of the junction temperature, giving rise to an increase of I_B and h_{FE} , therefore to an increase of I_C , with a following increase of P and, therefore, a further temperature increase.
- b) a dissipation to the external environment, controlled by the thermal resistance $R_{th} = dT/dP$ which tends to stabilize the device.

The situation evolves towards stability when:

$$\frac{\Delta I_{C2}}{\Delta I_{C1}} = \frac{\partial I_C}{\partial T} \times V_{CE} \times R_{th} \text{ is smaller than } 1, \text{ or in-}$$

stability if > 1 .

In this way, a stability factor may be defined that will be a function of V_{CE} and I_C :

$$S = R_{th} \times V_{CE} \times \frac{\partial I_C}{\partial T}$$

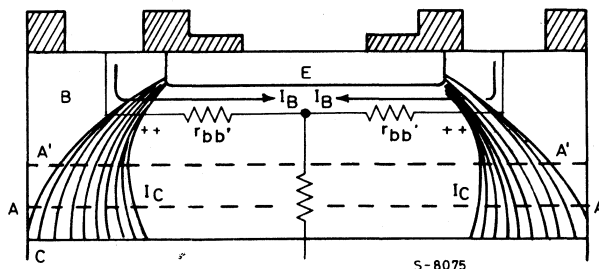
When $S > 1$ so called "thermal runaway" occurs and the junction temperature increases without any limit, therefore degrading and possibly damaging the transistor. The failure generally occurs when the surface temperature becomes greater than the eutectic temperature between silicon and the contact metal (front aluminium) with a consequent melting of the alloy.

Also, it may happen that a localized temperature increase damages the crystal, or that the inner temperature of the device reaches values high enough to melt the silicon.

For the understanding of $I_{s/b}$ phenomena giving rise to a reduction of the maximum power that the transistor can dissipate as V_{CE} increases (zone D - E) it is necessary to take into account that device operation isn't homogeneous on all the dice area. There are disuniformities in the emitter base current density, that may be due to junction disuniformities, crystal defects and, most of all, to the emitter edge concentration phenomenon.

The voltage drop due to the base current flowing through the cross resistance $r_{bb'}$ gives rise to a disuniformity of V_{BE} at the junction, therefore to the disuniformity of the current density J_E (see Fig. 2).

Fig. 2



A side drop of 26mV reduces by a $1/e$ factor the injected emitter current.

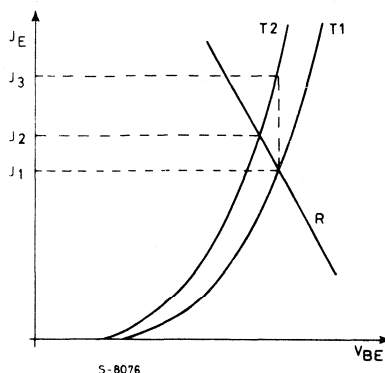
A concentration is therefore generated of the current at the emitter periphery, therefore the active silicon area is reduced and hot spots occur, leading to an effective increase of the thermal resistance. As a result, the maximum dissippable power is decreased.

When V_{CE} is increased the effect of the base - collector electric field is to increase the base current concentration.

Different techniques may be adopted to limit the I_S/b phenomenon. Fundamentally, they consist of minimising the mechanisms that trigger electrical and thermal instabilities in the transistor. The basic techniques are:

- 1) Minimization of crystal damages, metal impurities and of doping disuniformities.
- 2) Optimization of package and die attach techniques, to minimize the thermal resistance on which the stability factor S depends. Disuniformities of silicon die bondings to the case may give rise to adverse variations of R_{th} as a macroscopic parameter for the dice as a whole, but also to significant variations between different points, giving rise to premature second breakdown.
- 3) Increase of the base thickness to reduce the high current densities (due to emitter crowding) flowing through the collector base junction (where the electric field is localized), so that the density of the dissipated power is decreased. High base thicknesses, however, will result in lower cut off frequencies and slower switching times.
- 4) Optimization of the horizontal geometry.
- 5) Introduction of distributed ballast resistances connected in series with the base, the emitter or both, which tend to give a negative feedback to thermal runaway, therefore stabilizing the device. Fig. 3 shows the J_E/V_{BE} characteristic curves for two points in the junction, at different temperatures ($T_2 > T_1$).

Fig. 3



It may be seen that the introduction of a ballast resistance in series with the base or the emitter may reduce from J_3 to J_2 the current density in the hot spot.

The emitter ballast resistance is generally obtained by opening emitter contacts thinner than the emitter strip (Fig. 4).

In this way it is possible to limit the current density at the boundaries of the emitter. These resistances show the drawback of increasing the saturation voltage of the transistor by the amount $V_{CEsat} = R_E \times I_{Csat}$.

On the other hand, the base ballast resistance is obtained through a "N⁺ pocket" (in the case of NPN), around the emitter area (see Fig. 5). This N⁺ diffusion, being unbiased, can't be traversed by the base current, that is therefore forced to flow below the N⁺ through a small section and, in the case of a diffused base, encounters a higher resistance on the way to the edge of the emitter. In this way, it is possible to significantly improve I_S/b .

It should be noted that the SOA limits are temperature dependant and suitable derating must be applied.

Fig. 4

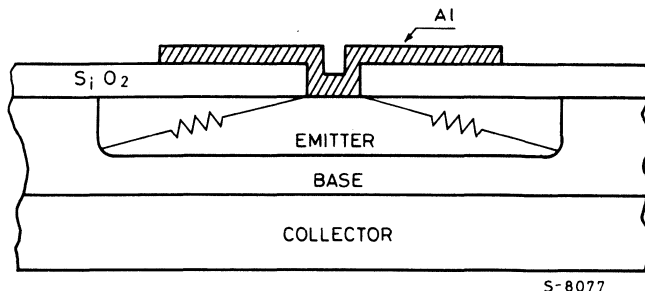
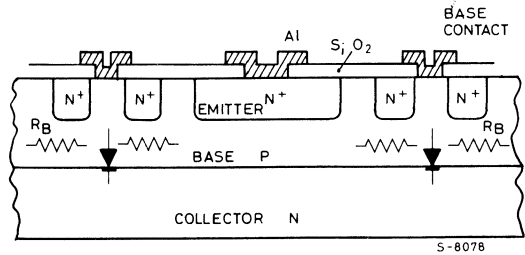


Fig. 5



REVERSE SECOND BREAKDOWN

The reverse breakdown phenomenon (E_s/b) is also due to thermal and electrical instability of the transistor. As already mentioned, it is distinguished from I_s/b by the presence of a reverse I_B (i.e. with a direction opposite to the normal direction of a transistor operating in the active zone) and by high V_{CE} values of the transistor. The device may be in these working conditions during turn off with an inductive load.

In the following figure (Fig. 6) the common emitter characteristic curves for a transistor are shown.

Fig. 8

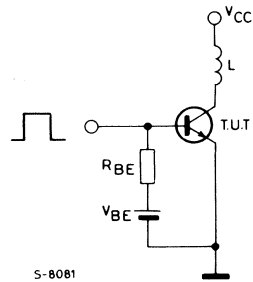


Fig. 6

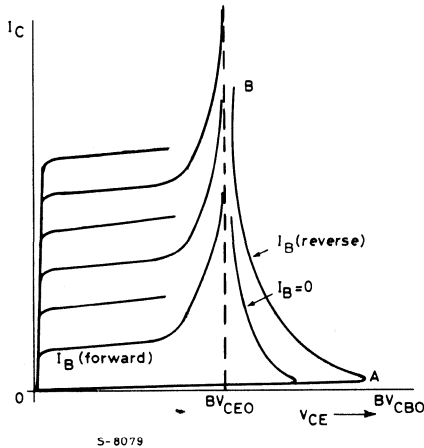
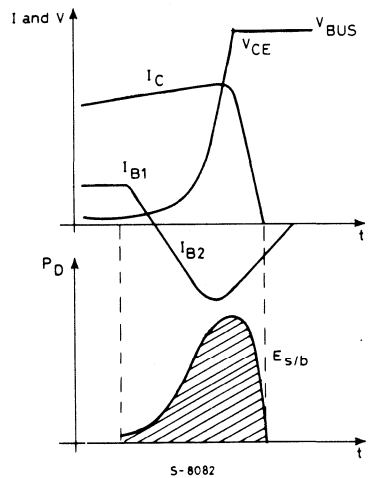
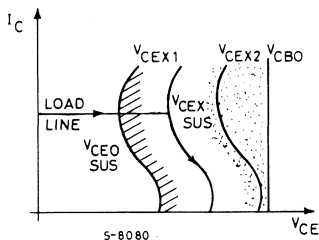


Fig. 7



It may be easy to understand the behaviour of these curves when the common emitter gain expression is considered:

$$h_{FE} = a_F / 1 - a_F \quad (1)$$

for high V_{CE} values, a_F is replaced with $M \times a_F$.

For low V_{CE} values, M is an insignificant factor, being very close to 1. M increases when V_{CE} is increased according to the following expression:

$$M = \frac{1}{1 - (V_{CE}/BV_{CBO})^n} \quad (2)$$

From expression (1) and (2) it is evident that h_{FE} depends on V_{CE} , becoming infinite when $M \times \alpha_F = 1$ (BV_{CEO}).

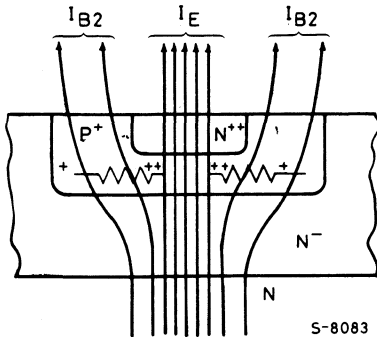
The negative slope section, which is a feature of the curves with $I_B < 0$ is due to the fact that α_F decreases at low values of the emitter current.

During turn off with an inductive load, the transistor has to operate with negative base current and a high value of I_C . It has often to reach a working area above V_{CEO} , remaining there all the time required for the inductance to be discharged (see Fig. 7). Fig. 8 shows the behaviours of I_C , V_{CE} , I_B and the power dissipated by the transistor during turn off.

The area of the dissipated power corresponds to the energy stored by the inductance $1/2 \times L \times I^2$, which is discharged into the transistor and this is called second breakdown energy ($E_{s/b}$).

Similarly to $I_{s/b}$, the voltage drop due to the reverse I_B flowing through the side resistance $r_{bb'}$ makes the centre of the emitter strip more biased than its periphery (Fig. 9). In this way, a current concentration occurs at the emitter centre.

Fig. 9



Let's analyse the case of an NPN transistor with diffused base and epitaxial collector, i.e. with constant concentration ND of donors doping particles.

Poisson's equation is recalled below:

$$\frac{\partial E}{\partial X} = - \frac{\partial^2 V}{\partial X^2} = \frac{\rho(x)}{\epsilon} \quad (3)$$

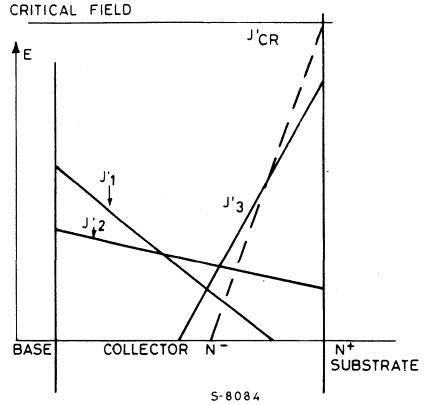
The X axis is normal to the silicon dice surface, $\rho(x)$ is the charge per unit volume, ϵ is the dielectric

constant of silicon. When the collector current is limited to low values, expression (3) becomes (q being the electron charge):

$$\frac{\partial E}{\partial X} = \frac{qN_0}{\epsilon} \quad (4)$$

and the electric field behaviour is similar to that shown in figure 10 for $J_C = J'_1$.

Fig. 10



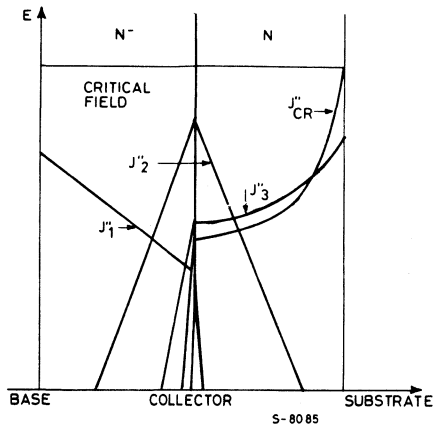
The voltage V_{CB} ($= V_{CE}$) is that given by the area of the E - X graph and is smaller than primary breakdown voltage, due to the reaching of critical field E_{cr} . In the presence of significant values of current density J_C , the expression (4) is modified due to the n concentration of electrons flowing at the speed V through the depletion layer.

$$\frac{\partial E}{\partial X} = \frac{q(ND - n)}{\epsilon} \quad \text{where } n = \frac{J_C}{qV} \quad (5)$$

At constant V_{CB} , the area limited by E has to remain constant. When J_C increases, the E - X slope varies (J'_2) until its sign is changed (J'_3) and E_{cr} is reached (J'_cr). At this point avalanche multiplication occurs locally of electron - hole pairs with an uncontrolled current increase and so a strip is formed with a very high temperature that gives rise to either crystal damage or silicon melting. Possible crystal defects, metal ions, junction disuniformities just further exaggerate this phenomenon. The avalanche multiplication is a very fast and very localized process, therefore the device remains externally cold. The $E_{s/b}$ behaviour isn't practically influenced by the die bonding quality. High $E_{s/b}$ values can be obtained with a proper design of geometry, to limit the current crowding and, most of all, by inserting a second epitaxial layer N of intermediate doping between the collector and the substrate.

The intermediate layer creates the condition shown in Fig. 11. When the current density increases (J'_2) the electric field at the interface N^-/N is in-

Fig. 11



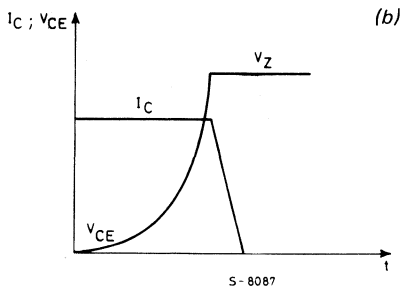
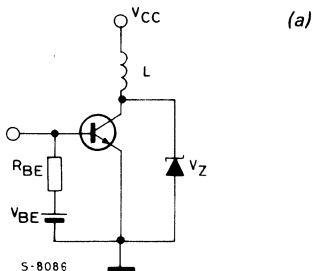
creased. Anyway, before the critical field E_{cr} is reached at this interface, the contribution of layer N becomes significant in sustaining the voltage. A further density increase (J'_3) reduces the electric field at the interface N^-/N and the breakdown isn't triggered until the critical field is reached at interface N/N^+ .

For a good power transistor with $V_{CE(sus)} = 450V$ the current density J'_{rc} corresponding to E_{cr} is in the order of $20A/mm^2$, greater by a factor 10 when compared to the average current density, given by the ratio between maximum saturation current and emitter area.

The $E_{s/b}$ behaviour is also influenced by the conditions outside the transistor, R_{BE} , V_{BE} , L .

The base conditions are especially important, as they regulate the crowding phenomenon.

Fig. 12



The most commonly used system by power designers to reduce the $E_{s/b}$ effect during turn off with inductive load is a clamping or 'snubber' circuit, that limits the voltage peak between collector and emitter.

The presence of the clamping circuit (in Fig. 12 for sake of simplicity it is schematized with a zener diode) allows only a minimal amount of the energy stored in the inductance to be absorbed by the transistor, and $E_{s/b}$ becomes independent of the value of L and practical RBSOA limits may be defined.

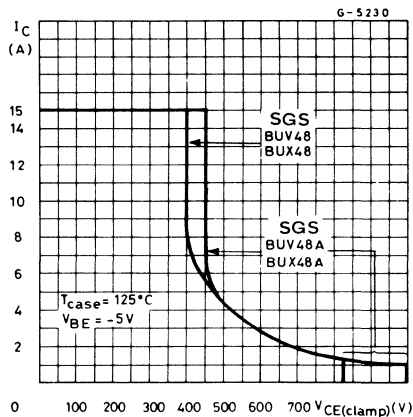
It must be noted anyway that the presence of high V_{CE} and negative I_B current may give rise at high current to the previously described $E_{s/b}$ phenomenon, even in the presence of the clamping circuit.

The multi-epitaxial transistors show a better behaviour even in the presence of a clamp.

The reverse bias safe operating area (Fig. 13) establishes the maximum switchable current with inductive load versus clamping voltage in very harsh base conditions that simulate the real base driving conditions in the circuits.

Note that the temperature is not a major factor in the $E_{s/b}$ and so the RBSOA rating can be considered to be independent of temperature.

Fig. 13



CONCLUSION

Second breakdown performance is a function of transistor technology and cannot always be improved without some trade-off in other parameters. The application conditions have a considerable effect on both $I_{s/b}$ and $E_{s/b}$ capability.

SGS HIGH VOLTAGE FAST RECOVERY DIODES AND THEIR SWITCHING PERFORMANCE

INTRODUCTION

SGS decided to introduce its line of power switching modules in the TO-240 TRANSPACK package.

To solve the problem of providing fast recovery rectifiers capable of matching the high voltage/high current of the transistor chips in the TO-240 package, SGS was able to exploit its technological leadership in power semiconductors. The rectifiers were fabricated by epitaxial growth with high voltage termination structures.

SGS was the first in the industry to introduce epitaxial growth for all its power transistors. Its epitaxy capability, fully in house, makes use of the fastest epitaxy reactors in the industry.

This note describes the switching behaviour of the fast recovery rectifiers used in SGS TRANSPACK power transistor modules and the SGS35R120 series of diodes.

The turn-off and turn-on behaviour is described and the characterization is oriented to the conditions of practical use.

The TRANSPACK product range and the internal diodes

This report deals with the first three diode chips developed, table 1 gives their main characteristics.

TABLE 1

Type	I _F (A)	V _{RRM} (V)
SGS35R80	35	800
SGS35R120	35	1200
SGS60R40	60	400

The second table below shows the TRANSPACK product range and the relevant fast recovery rectifier used in each device.

TABLE 2

Type C/E diode = D	Quart /Half	Trans /Darl	V _{CEO} (V)	V _{CES} (V)	I _C (sat) (A)	V _C at sat I _b	t _{off} (μs) typ. induct.	Diode type
SGS80DA020D	Q	D	200	300	80	2.0 1	1.9	SGS60R40
SGS40TA045	Q	T	450	850	40	2.0 8	2.2	none
SGS40TA045D	Q	T	450	850	40	2.0 8	2.2	SGS35R120
SGS50DA045D	Q	D	450	850	50	2.5 2	2.0	SGS35R120
SGS25DB070D	H	D	700	1000	25	3.0 2.5	2.4	SGS35R120
SGS25DB080D	H	D	800	1200	25	3.0 2.5	2.4	SGS45R80
SGS30DB040D	H	D	400	500	30	3.0 2	2.0	SGS45R80
SGS30DB045D	H	D	450	600	30	3.0 2	2.0	SGS45R80
SGS30DA060D	Q	D	600	1000	30	2.5 1.5	3.0	SGS35R120
SGS30DA070D	Q	D	700	1200	30	2.5 1.5	3.0	SGS35R120
SGS50DB040D	H	D	400	500	50	3.5 5.0	3.0	SGS45R80
SGS50DB045D	H	D	450	600	50	3.0 5.0	3.0	SGS45R80
SGS15DB070D	H	D	700	1000	15	3.0 1.5	2.5	SGS35R120
SGS15DB080D	H	D	800	1200	15	3.0 1.5	2.5	SGS35R120

Turn-off

- the recovery of a diode;
- t_{rr} definition;
- t_{rr} characterization;
- Q_r characterization;

The reverse recovery of a diode

When the voltage across a conducting diode is reversed, it takes a certain time for the diode to recover its reverse state. During this recovery phase current flows in the diode as follows:

- over a certain time, called reverse recovery time - t_{rr} ;
- with a negative current that reaches a peak maximum current - I_{RM} ;
- until the electric charge stored in the semiconductor junction, Q_r , is evacuated.

The physical mechanism involved is related to the

minority carriers (holes for the n-substrate diodes) that are present in the high resistivity side of the junction (the cathode in a n-substrate diode).

The off-state occurs when the minority carriers disappear:

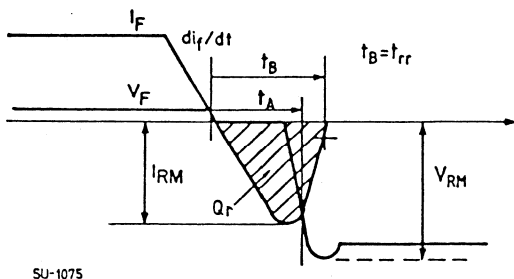
- when they recombine with majority carriers (a function of their lifetime);
- they are extracted by a reverse current.

When a diode is used in fast switching circuits the removal of these carriers by a reverse current is of prime importance. After this instant no more minority carriers are created by the direct current. The lifetime of minority carriers in fast diodes is also minimised by design.

Fig. 1 shows the relationship between voltage and current in a diode during the recovery phase. The elements of interest for its characterization are:

- di/dt , the rate of decrease of the forward current;
- Q_r , the stored charge (shaded area of Fig. 1).

Fig. 1 - Voltage and current across diode during recovery phase



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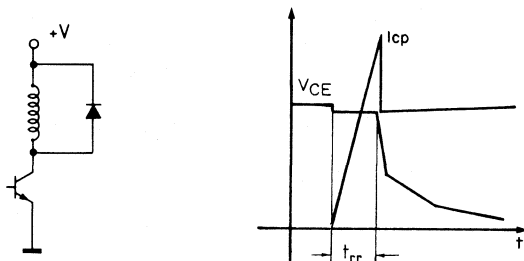
Fig. 2 represents a typical fast recovery rectifier application. Inductor current flows (free wheels) through the diode when the transistor is off, (back e.m.f). When the transistor is on, the full supply voltage is applied to the inductor, so that the energy is transferred from the power supply to the load.

For each cycle when the transistor is turned on,

the diode recovers its reverse state. During the change the diode acts as a short circuit between the transistor and the supply. The longer it takes for the diode to recover, the higher the stress on the transistor (I_{CP} is associated with a simultaneous high voltage condition).

This application is typical for fast recovery rectifiers.

Fig. 2 - Voltage and current across transistor at turn-on



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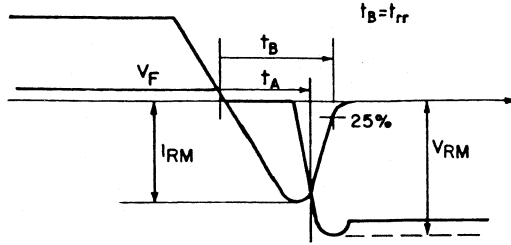
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T_{rr} definition

Figures 3 shows two possible definitions for the recovery time, t_A and t_B . In practice t_{rr} is defined as t_B in the figure.

In cases like that shown in Fig. 2, it is important to consider that only t_A is representative of the duration of the power pulse that the recovery of the diode induces in the transistor.

Fig. 3 - t_{rr} measurement methods



SU-1076

T_{rr} characterization

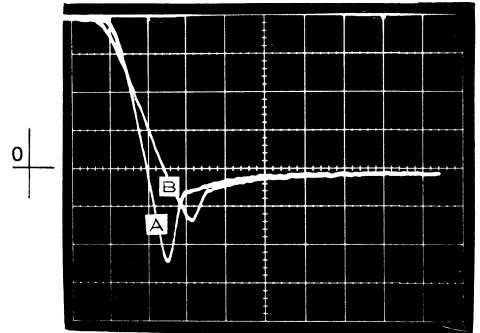
Photographs 1 and 2 show how different test conditions (I_F and di/dt) imply markedly different results for t_{rr} , for the same diode.

The blocking voltage V_{RM} can be disregarded as its influence on t_{rr} is not direct. di/dt is the significant factor and V_{RM} is of importance only to the extent where it modifies di/dt .

Photographs 3 to 5 show the behaviour of the SGS fast recovery rectifier diodes in conditions representing the real environment in which the devices are expected to work. For instance, t_A for SGS45R80 at 40A is 150ns. In a circuit like the one in figure 4, with 40A current in the inductor, the power pulse that the transistor must sustain (I_C peak $\times V_{CE}$) will last for 150ns.

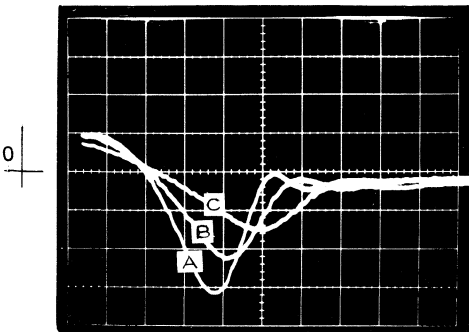
The capacity that SGS transistors have to safely absorb this energy is guaranteed in their FBSOA diagram.

Photo 2 - Recovery times vs. di/dt at 40A for SGS35R120



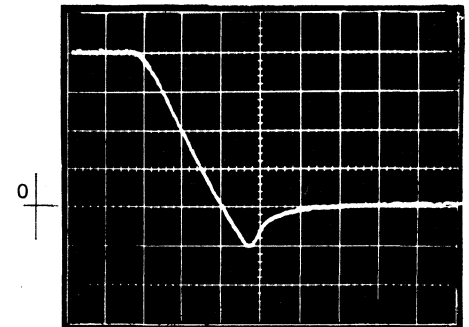
$I_F = 40A$; A : $di/dt = 250A/\mu s$;
B : $di/dt = 100A/\mu s$; $V_R = 30V$;
 $t = 200ns/div$; $\gamma = 10A/div$

Photo 1 - Recovery times vs. di/dt at 1A for SGS35R120



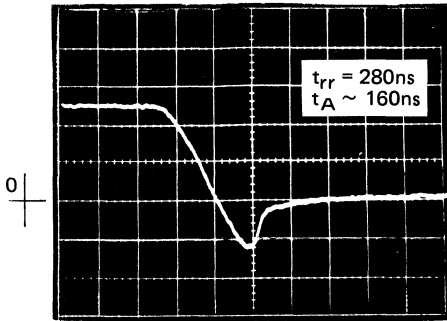
$I_F = 1A$; A : $di/dt = 100A/\mu s$;
B : $di/dt = 50A/\mu s$; C : $di/dt = 25A/\mu s$;
 $V_R = 30V$; $t = 20ns/div$; $\gamma = 1A/div$

Photo 3 - t_{rr} for SGS45R80



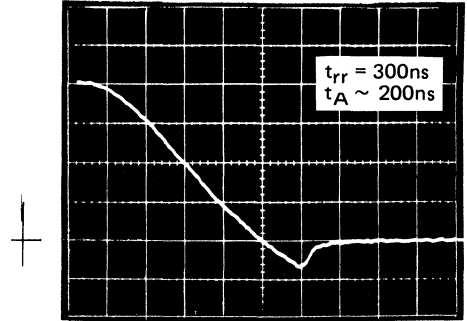
$I_F = 40A$; $di/dt = 100\mu s$; $V_R = 30V$;
 $t = 200ns/div$; $\gamma = 20A/div$

Photo 4 - t_{rr} for SGS35R120



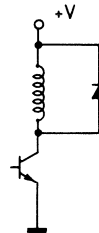
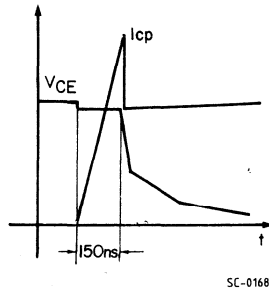
$I_F = 25A$; $di/dt = 100A/\mu s$; $V_R = 30V$;
 $t = 200ns/div$; $y = 10A/div$

Photo 5 - t_{rr} for SGS60R40



$I_F = 80A$; $di/dt = 10A/\mu s$; $V_R = 30V$;
 $t = 200ns/div$; $y = 20A/div$

Fig. 4 - Typical stress on transistor at turn-on



SC-0166

Turn-on

- the turn-on phase of a diode;
- V_{FP} and t_{FR} definitions;
- t_{FR} characterization;
- t_{FP} characterization;
- Q_r characterization.

The turn-on phase of a diode

In the circuit shown in Fig. 5 a fast diode is normally used. In general it is well understood that a fast diode is needed to avoid overstressing both the diode and the transistor during the diode recovery phase.

However the diode could also cause the transistor to be overstressed during its turn-on phase. Both circuits a) and b), if the transistor and its driving stage are fast, cause a very high di/dt on the diode when the transistor switches off.

In practice the forward voltage drop on the diode

will exhibit an overshoot before settling to its steady state value. This phenomenon is a consequence of the delay time needed by the minority carriers before flooding the epitaxial region (high resistivity).

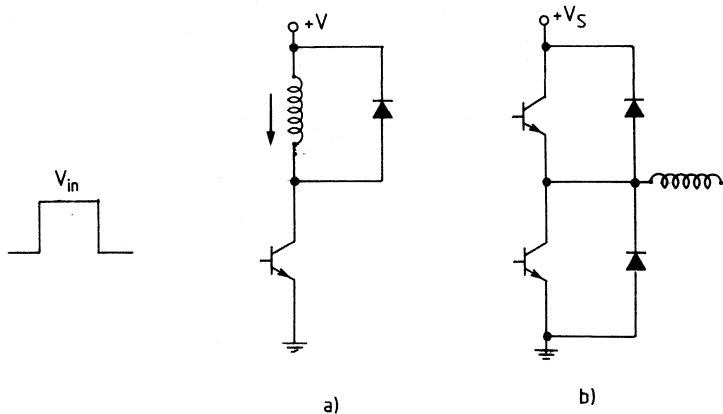
At first only the majority carriers are present, traversing the epitaxial layer, that exhibit its intrinsic resistivity. As soon as the minority carriers invade the epitaxial layer, its resistivity collapses (due to conductivity modulation) and the steady state is reached. Returning to Fig. 5, we can see that the stress on the transistor at its turn-on reaches an extreme point when:

- the collector current is still fully present;
- the collector voltage exhibits a transient peak up to V_S (the so called 'clamping voltage') plus V_F .

Other parasitic elements in the circuit may increase the overvoltage due to the diode.

Attention must be paid to the physical lay-out, and especially to the interconnections between the collector of the transistor and the diode.

Fig. 5 – Typical configurations for transistors switching



SC-0165

V_{FP} and t_{FR} definition

The turn-on phase of a diode in a practical situation is shown in Fig. 6.

V_{FP} is defined as the peak transient voltage.

For the same current, the turn-on overvoltage is higher for diodes that can withstand a higher reverse voltage. This can be seen in Fig. 7.

This is mainly related to the thicker epitaxial layer needed to implement a higher reverse voltage rating.

At the turn-on of a diode, a thicker epitaxial layer causes a higher resistance, before the conductivity modulation by the minority carriers takes place.

Fig. 7 – Direct overvoltage vs. di/dt

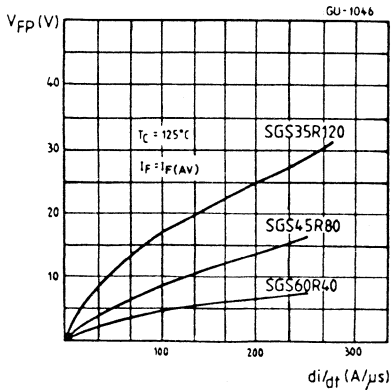
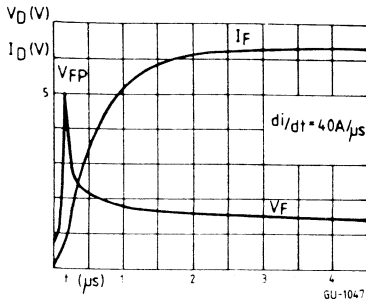


Fig. 6 – Turn-on transient of the diode



T_{FR} Characterization

In Fig. 8, the turn-on times, t_{fr} , for the SGS fast recovery rectifiers SGS45R80, SGS35R120 and SGS60R40 are shown as a function of di/dt .

t_{fr} is defined as the time from the instant V_F becomes positive till the time V_{FP} decreases to +2V.

V_{FP} Characterization

Figs. 9 to 11 characterize V_{FP} in all possible di/dt conditions of practical use for the diodes

Fig. 8 - Turn-on time vs. di/dt

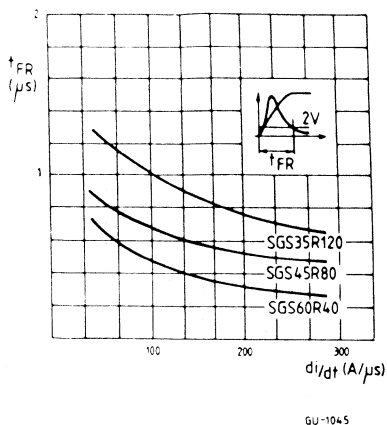
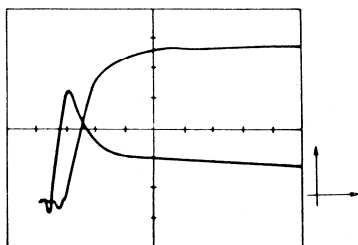
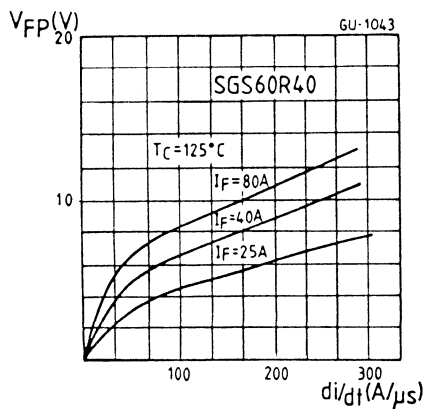
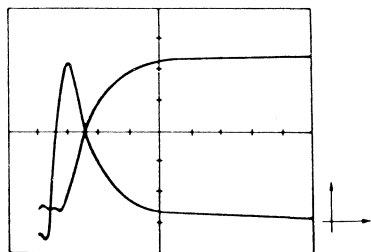
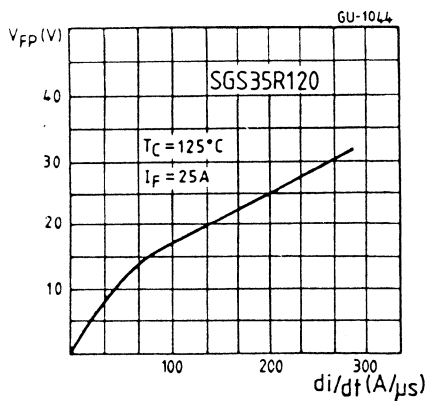


Fig. 9 - Direct overvoltage vs. di/dt



$t = 0.1 \mu s/div$; $V = 2V/div$; $I = 5A/div$

Fig. 10 - Direct overvoltage vs. di/dt



$V = 5V/div$; $I_F = 25A$; $di/dt = 200A/\mu s$;
 $t = 100ns/div$

under consideration. The values shown are typical. Maximum values are never more than 1.3 times the typical ones.

They are valid for a case temperature up to $125^\circ C$; V_{FP} will be moderately lower at a lower temperature.

Using an example it can be seen how V_{FP} may, in some cases, be the origin of some unexpected inconvenience.

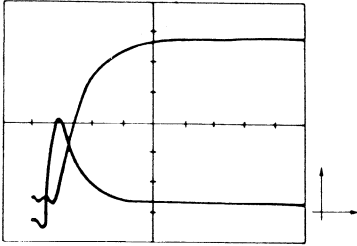
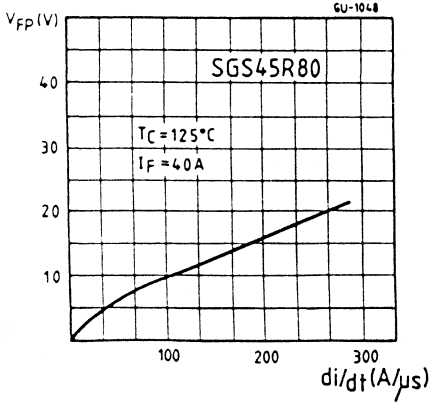
In Fig. 12, case (a) refers to an application where V_{FP} is of no concern (di/dt is very low).

In the case figure 12b, in contrast to figure 12a, di/dt may be high enough to create a significant V_{FP} overshoot.

Figure 12c emphasized V_{FP} for the diode D_2 , at the moment when the switches Q_1 and Q_3 are turned off.

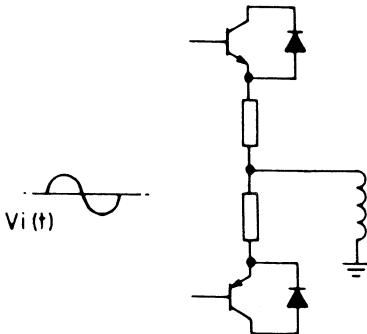
Immediately after turn-off when all the switches are off, the load current still flowing due to the inductive nature of the load, can only flow through D_2 and D_3 . V_{FP} across D_2 then acts as a negative bias on the collector (w.r.t. the emitter) of Q_2 .

Fig. 11 – Direct overvoltage vs. di/dt



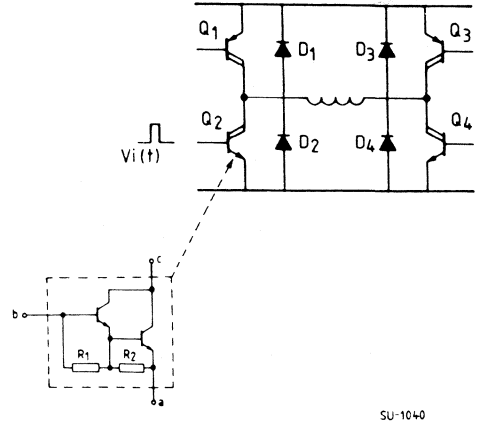
$V = 5\text{ V/div}$; $I_F = 25\text{ A}$; $di/dt = 200\text{ A}/\mu\text{s}$
 $t = 100\text{ ns/div}$

Fig. 12a – Final stage of power amplifier



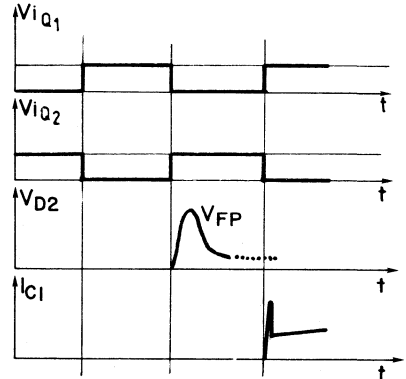
SU-1041

Fig. 12b – Bridge configuration for motor driving



SU-1040

Fig. 12c – Voltage and current waveforms with reference to Fig. 12b



SC-0164

If Q_2 is a darlington, this negative voltage may be enough to reverse bias (through the integrated resistances of the darlington) the final transistor and make it conduct a reverse current I_x .

The current I_x may be a significant proportion of the current that is expected to flow only through D_2 , and it can store a significant charge Q_r in the final darlington transistor.

The final darlington transistor base collector junction acts as a slow recovery diode.

As a result, when Q_1 is again turned on, it senses the behaviour of an 'equivalent D_2' ' with a much longer reverse recovery time. The peak current is higher than expected, creating reliability hazards or possibly the destruction of Q_1 .

SGS produces safe operating area diagrams (FBSOA) which specify the maximum V_C/I_C boundary for each device in the range so the

designer can select the most suitable device and ensure no repetitive overstress occurs.

Q_r Characterization

An electric charge Q_r, is stored in the diode during the direct conduction phase.

The amount of charge that is evacuated during the recovery phase is approximately:

$$Q_r = 1/2 I_{rm} \times I_r$$

Figures 13a, b and c plot Q_r as a function of di/dt, at room and at elevated case temperature (125°C), and with the currents of practical use for SGS45R80, SGS35R120 and SGS60R40.

Fig. 13a-b-c - Recovery charge vs. di/dt

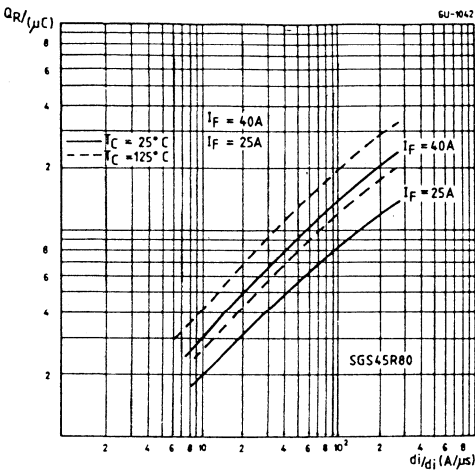


Fig. 13b

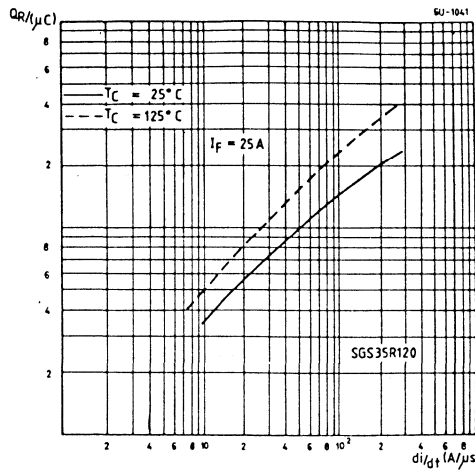
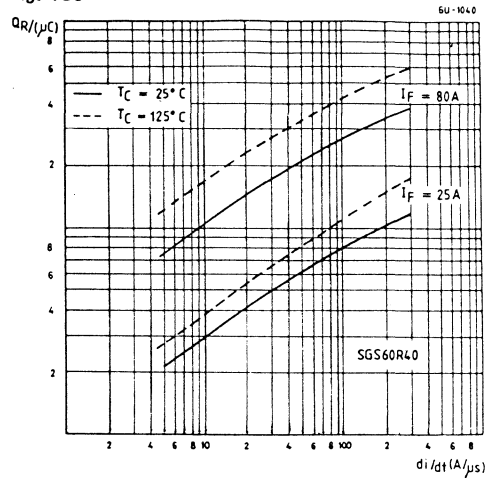


Fig. 13c



CONCLUSION

The devices described in this note can be classed in the high-speed range as far as turn-off is concerned, and in the medium-high range for turn-on.

In addition it can be noted that the reverse recovery of these devices is of the so called "soft" type, which makes them particularly suitable for applications where reduced radiated noise, ringing waveforms, etc. are of concern.

While nowadays it is relatively easy to find in the market high voltage/high current transistors for fast switching applications, the same is not true for the diodes needed in the same applications.

The fast recovery rectifier diodes SGS45R80, SGS35R120, and SGS60R40 represent part of a successful development that complement the SGS product range of power transistors in the high power area.

HANDLING AND MOUNTING ICs IN PLASTIC POWER PACKAGES

Integrated circuits mounted in plastic power packages can be damaged, or reliability compromised, by inappropriate handling and mounting techniques. Avoiding these problems is simple if you follow the suggestions in this section.

Advances in power package design have made it possible to replace metal packages with more economical plastic packages in many high power applications. Most of SGS' power driver circuits, for example, are mounted in the innovative MULTI-WATT® package, developed originally for high power audio amplifiers. Though the intrinsic reliability of these packages is now excellent the use of inappropriate techniques or unsuitable tools during mechanical handling can affect the long term reliability of the device, or even damage it. With a few simple precautions, careful designers and production engineers can eliminate these risks, saving both time and money.

BENDING AND CUTTING LEADS

The first danger area is bending and cutting the

leads. In these processes it is important to avoid straining the package and particularly the area where the leads enter the encapsulating resin. If the package/lead interface is strained the resistance to humidity and thermal stress are compromised, affecting reliability.

There are five basic rules to bear in mind:

- Clamp the leads firmly between the package and the bend/cut point (figure 1).
- Bend the leads at least 3 mm from the package (figure 2a).
- Never bend the leads more than 90° and never bend more than once (figure 2b).
- Never bend the leads laterally (figure 2c).
- Make sure that the bending/cutting tool does not damage the leads.

Fig. 1 - Clamp the leads between the package and bend/cut point.

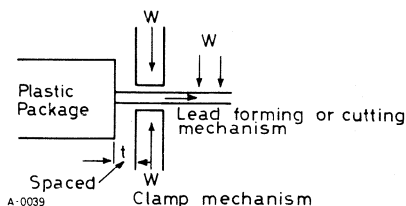
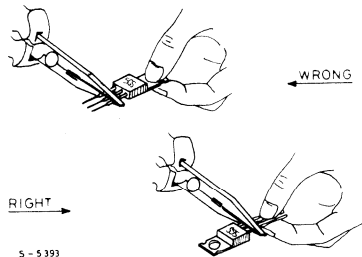
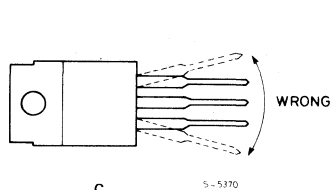
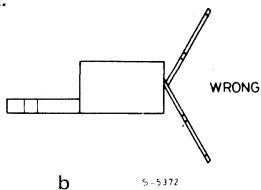
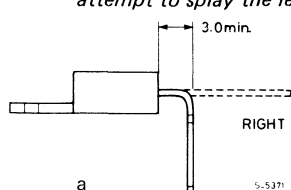


Fig. 2 - Bend the leads at least 3 mm. from the package, never bend leads more than 90° and never attempt to splay the leads out.



INSERTION

When mounting the IC on a printed circuit board the golden rule is, again, to avoid stress. In particular:

- Adhere to the specified pin spacing of the device; don't try to bend the leads to fit non-standard hole spacing.
- Leave a suitable space between the IC and the board. If necessary use a spacer.
- Take care to avoid straining the device after soldering. If a heatsink is used and it is mounted on the PC board it should be attached to the IC before soldering.

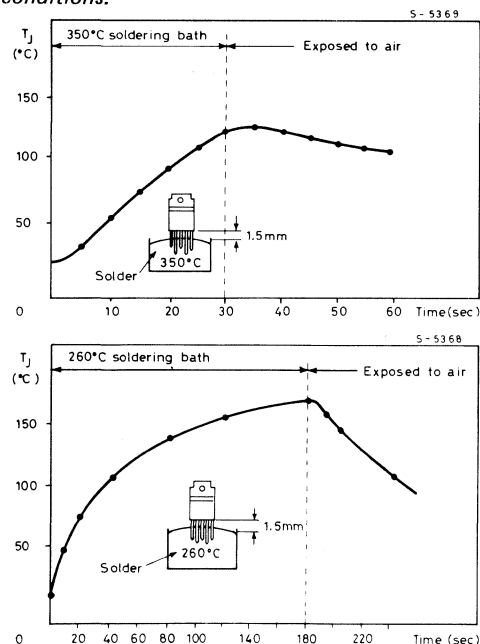
SOLDERING

The greater danger during soldering is overheating. If an IC is exposed to high temperature for an excessive period it may be damaged or reliability reduced.

Recommended soldering conditions are 260°C for ten seconds or 350°C for three seconds. Figure 3 shows the excess junction temperature of a PENTAWATT package for both methods.

It is also important to use suitable fluxes for the soldering baths to avoid deterioration of the leads or package resin. Residual flux between the leads or in contact with the resin must be removed to guarantee long term reliability. The solvent used to remove excess flux should be chosen with care. In particular, trichloroethylene ($\text{CHCl}_3 : \text{CCl}_2$) - based solvents should be avoided because the residue can corrode the encapsulant resin.

Fig. 3 - The excess junction temperature of a PENTAWATT package in the suggested soldering conditions.



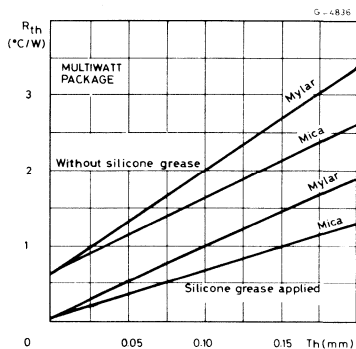
HEATSINK MOUNTING

To exploit the full capability of a power device a suitable heatsink must be used. The most important aspect from the point of view of reliability is that the heatsink is dimensioned to keep the junction temperature as low as possible. From a mechanical point of view, however, the heatsink must be designed so that it does not damage the IC. Care should also be taken in attaching the IC to the heatsink.

The contact thermal resistance between the device and the heatsink can be improved by adding a thin layer of silicon grease with sufficient fluidity to ensure uniform distribution. Figure 4 shows how the thermal resistance of a MULTIWATT package is improved by silicone grease.

An excessively thick layer or an excessively viscous silicon grease may have the opposite effect and could cause deformation of the tab.

Fig. 4 - The thermal resistance of a MULTIWATT package is improved by silicon grease. Here thermal resistance is plotted against grease thickness.



SGS plastic power packages - MULTIWATT, PENTAWATT and VERSAWATT - are attached to the heatsink with a single screw. A spring clip may also be used as shown in figure 5. The screw should be properly tightened to ensure that the package makes good contact with the heatsink. It should not be too tight or the tab may be deformed, breaking the die or separating the resin from the tab.

The appropriate tightening torque can be found by plotting thermal resistance against torque as shown in figure 6.

Suggested tightening torques for 3MA screws are 8 Kg/cm for VERSAWATT, PENTAWATT and MULTIWATT packages. If different screws, or spring clips, are used the force exerted by the tab must be equivalent to the force produced with these recommended torques.

Even if the screw is not overtightened the tab can be deformed, with disastrous results. If the surface of the heatsink is not sufficiently flat. The planarity of the contact surface between device and

Fig. 5 - MULTIWATT, PENTAWATT and VERSAWATT packages are attached to the heat-sink with a single screw or a spring clip.

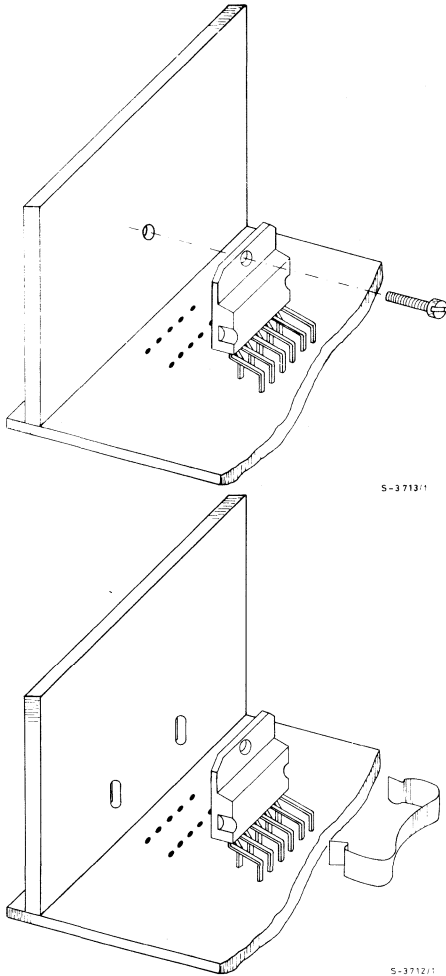
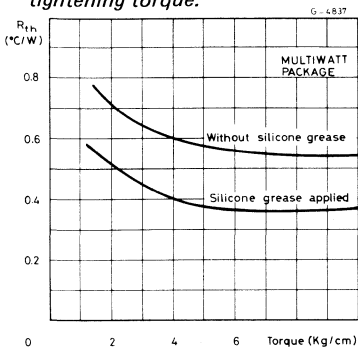
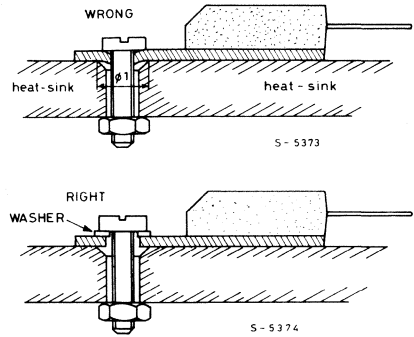


Fig. 6 - Contact thermal resistance depends on tightening torque.



heatsink must be better than 50 μ m for PENTAWATT and VERSAWATT packages and less than 40 μ m for MULTIWATT packages.

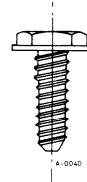
Fig. 7 - The heatsink tab may be deformed if a washer or a wide-headed screw is not used.



Similar problems may arise if the screwhead is too narrow compared to the hole in the heatsink (figure 7).

The solution here is to use a washer to distribute the pressure over a wider area. An alternative is to use screws of the type shown in figure 8 which have a wide flat head. When self-tapping screws are used it is also important to provide an outlet for the material deformed as the thread is formed. Poor contact will result if this is not done. Another possible hazard arises when the hole in the heatsink is formed with a punch: a circular depression may be formed around the hole, leading to deformation of the tab. This may be cured by using a washer or by modifying the punch.

Fig. 8 - The recommended screw type looks like this.



Serious reliability problems can be encountered if the heatsink and printed circuit board are not rigidly connected. Either the heatsink must be rigidly attached to the printed circuit board or both must be securely attached to the chassis. If this is not done the stresses and strains induced by vibration will be applied to the device and in particular to the lead/resin interface. This problem is more likely to arise when large boards and large heatsinks are used or whenever the equipment is subjected to heavy vibrations.

DEVELOPMENTS IN SURFACE MOUNTING PACKAGES FOR POWER INTEGRATED CIRCUITS

Thermal dissipation is recognized as a major problem in Surface Mount Technology. New packages are needed, having good thermal characteristics and meeting the SMT requirements: reduced size, automatic placement, compatibility with the SMT soldering systems.

In this paper, thermal data and measurement methods for the most popular SO and PLCC packages are reviewed; some new solutions for surface mountable medium power (up to 2W) and high power (more than 2W) devices are presented.

INTRODUCTION

A number of problems have been met in introducing the high density, high reliability mass production of SM systems. This can explain the experimental work and the complex characterization activity of both ICs suppliers and users.

As discussed elsewhere [1], the four main areas of such activity are: standardization, quality, reliability after soldering on PC boards and power dissipation.

Fast progress has been made and more confidence in the SM technology has been achieved in the first three areas. For example, it was demonstrated that the most common conditions used in double wave soldering and vapour phase reflow soldering do not affect the final reliability of SO packaged devices (Fig. 1).

On the contrary, referring to heat dissipation, progress is less fast, even if this point can strongly limit PERFORMANCE and COST of the system, thus losing the two main advantages of the SM technology, to a certain amount.

A development activity is needed, to cover the following points:

- 1) study of the relationship between thermal resistance of the package and board characteristics (density, lay-out, dissipated power). As it will be discussed later, this point cannot be ignored, even at dissipation levels (0.5W or less), typical of the "signal" packages like SO and PLCC packages;
- 2) study of the thermal properties in pulsed conditions, in order to avoid redundancy and cost increase;
- 3) development of new power packages with reduced thermal resistance and heat transfer features.

Moreover, a lack of standardized methodology exists when the thermal parameters have to be measured and compared.

In the present paper the above mentioned points are considered. The characterization activity running in SGS is presented, together with experimental data and details on development of new power packages.

Fig. 1 – SGS SO packages: reliability on FR4 board

	UNMOUNTED	SOLDERED ON PCB			
	% of rejects OPAMP family jan-june '86	Vapour phase 215° C/20s	Double wave		
			225° C/8s		250° C/8s
	SO-8, 14, 16	SO-14	SO-8	SO-14	SO-14
Pressure pot 98h 196h	 0.05 0.22	 0/32	 0/52	 0/52	 0/52
Operating life test 1000h	 0.66		 0/77	 0/77	 0/32
THB 85/85 T = 85° C RH = 85% 1000h 2000h	 0.5	 0/32 0/32		 1/105 (*)	 0/32 0/32
THB 130/85 T = 130° C RH= 85% (**) 200h		 0/60		 0/20	
Thermal cycles -65/+150° C 500 cycles	 0.0		 0/77	 0/154	

(*) Parametric failure between 500 and 1000h

(**) Acceleration factor to 85/85 can be assumed between 25 and 30 – Test is still running –.

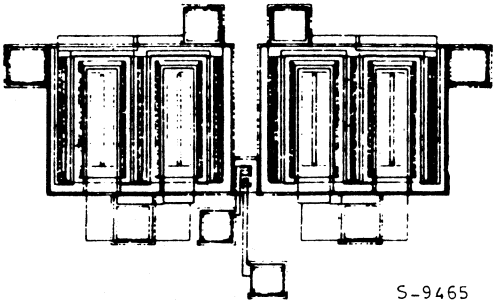
EXPERIMENTAL TECHNIQUE FOR
THE THERMAL CHARACTERIZA-
TION IN DC AND PULSED CONDI-
TIONS

THERMAL EVALUATION TEST PATTERN
P432

The expecially designed test pattern P432 is used
for thermal characterization (Fig. 2).

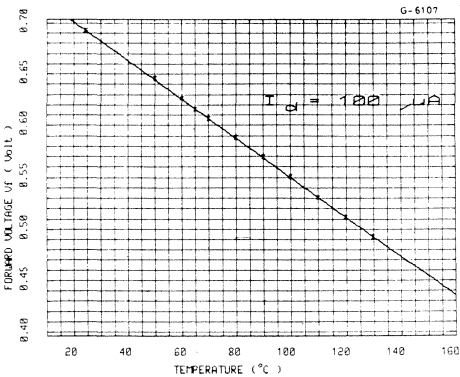
It is formed by two power NPN transistors, able to
dissipate 10W each. Their total area is about 1000
sq. mils. The junction temperature T_j of a sensing
diode, placed between the two transistors, is
recorded through the measurement of the diode
voltage V_f when forward biased at a current of
100 μ A. The relationship between V_f and T_j is
linear, as shown by the calibration curve of Fig. 3.

Fig. 2 – Thermal evaluation test Pattern P432



S-9465

Fig. 3 - Calibration curve for P432 sensing diode



The test pattern design ensures that the diode is positioned on the temperature plateau generated when the two transistors are biased in parallel; it

is than possible to know the transistor T_j , through the junction temperature of the diode.

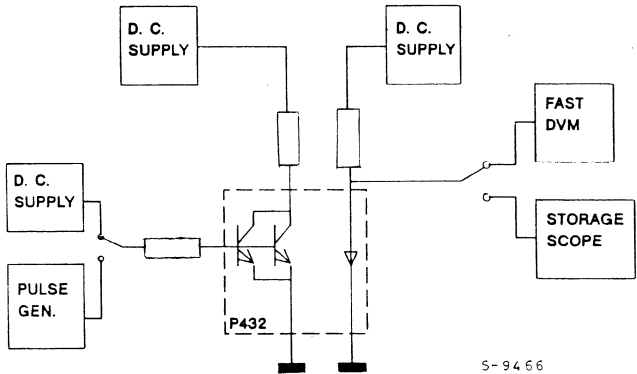
The evaluation die can be cut in different sizes, in order to quantify the effect of the die area on the thermal resistance.

MEASUREMENT TECHNIQUE

The measurement technique is simple [2] and does not need to switch the power element from the dissipation condition to the sensing condition, thus offering a better accuracy if short pulses are considered. Indeed, the same resolution cannot be achieved with other test patterns, in which the sensing diode is missing (as single power transistors or diode, ICs substrate diode, etc.).

The measurement circuit is shown in fig. 4. A DC power supply or a pulse generator biases the transistors in parallel; a fast voltmeter or a storage oscilloscope records the diode V_f . Resolution better than 50ns is obtained with this circuit.

Fig. 4 - Measurement circuit with P432



UNMOUNTED (FLOATING) SAMPLES

In order to simulate the thermal behaviour of the package in the worst condition (as in a high density, double sided card), samples are connected to 8 thin wires, needed for biasing the two transistors and the sensing diode. Measurement is performed on such devices, suspended horizontally in a one cubic foot plastic box, to prevent draft.

SAMPLES SOLDERED ON TEST SUBSTRATES

In order to characterize the thermal properties of parts mounted on a substrate, samples are reflow soldered on ceramic and epoxy glass substrates.

For the evaluation of SO packages, the size of the plastic FR4 test board is fixed while the copper pattern lay-out can be changed. Seven different

test boards are obtained from the basic configuration of Fig. 5, as summarized in Tab. 1.

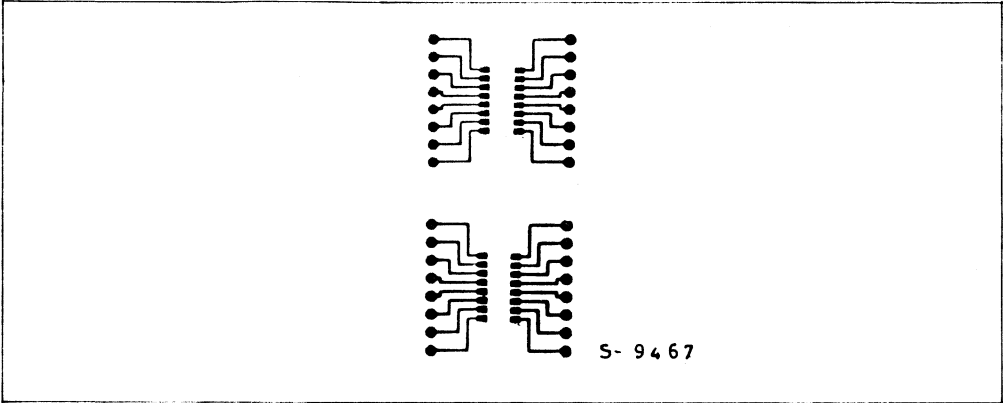
Table 1 - CHARACTERISTICS OF THE TEST BOARDS FOR SO PACKAGE EVALUATION

Type	Trace area (x 1000 sq. mils)	Heatsink
SM PCB 1 SGS	136	yes
1B	136	no
1A	21	no
1C	50	no
1D	71	no
1E	93	no
1F	102	no

substrate: FR4

size: 00.9" x 0.8" x 0.056"

Fig. 5 - Basic layout of thermal evaluation test board



Test board SM PCB1 SGS has a 0.2 sq. inch integral heatsink in the lower side obtained by a standard two layer PCB technology; in test board 1A the

traces are reduced to the solder pads, only. For 68 leads PLCC package only one PCB lay-out has been considered at present.

THERMAL RESISTANCE OF SO PACKAGES (STILL AIR)

Thermal properties of these packages are influenced by following factors:

- 1) thermal conductivity of the frame;
- 2) thermal conductivity of the molding compound;
- 3) frame design;
- 4) device area;
- 5) die pad area;
- 6) device power dissipation;
- 7) substrate type;
- 8) substrate area;
- 9) area of the connecting traces on the substrate.

Due to the significant number of parameters, some of them have been maintained constant, as package design, which meets the standard Jedec outline, the test board size and the thermal properties of the package materials, listed in Tab. 2:

Table 2 - PACKAGE THERMAL CONDUCTIVITIES

Molding Compound	2.67×10^{-3} W/cmC
Frame Alloy 42	0.105 W/cmC
Frame Copper	2.61 W/cmC

THERMAL RESISTANCE OF SO8, 14, 16 PACKAGES

Alloy 42 frame SO package have an intrinsic junction to ambient thermal resistance ranging between 250 and 430°C/W, depending on the power level: results for "floating" samples (die size: 4500sm) are summarized in Fig. 6.

The effect of the board is shown in Fig. 7: thermal resistance ranges now between 180 and 280°C/W, in the same conditions of die size and power dissipation.

Fig. 8 is related to copper frame SO-14 package, with different substrates: thermal performance of the heatsinked SM PCB1 SGS plastic board is noticeable, as it only slightly differs from a ceramic substrate.

For the same package, the relationship with the total area of the copper traces connected to the leads is shown in Fig. 9: actually, the traces behave as dissipating fins and this cannot be ignored when considering high density boards.

At last, Fig. 10 reports the dependance on die area: the different behaviour of copper and Alloy 42 can be explained taking into account that silicon thermal conductivity (1.3W/cmC) is higher than the alloy thermal conductivity by a factor of ten; silicon area is the dominating factor in this case.

Fig. 6 - R_{th} of "FLOATING" SO-8, 14, 16 (Alloy 42 frame)

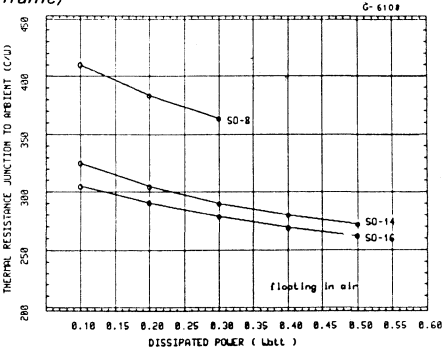


Fig. 7 - Alloy 42 SO-8, 14, 16 R_{th} on board

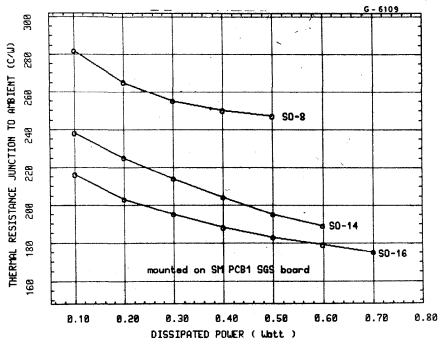


Fig. 8 - R_{th} of copper SO-14 with different substrates

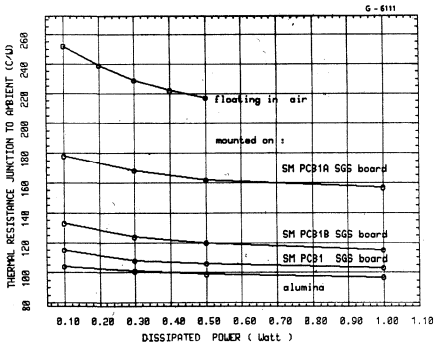


Fig. 9 - R_{th} of copper SO-14 vs. board trace area

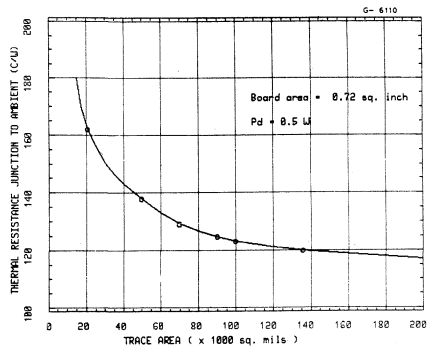
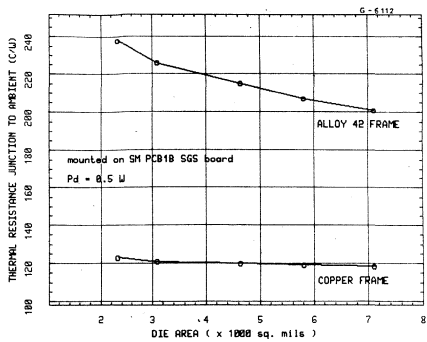


Fig. 10 - R_{th} of on board SO-14 packages vs. die area



THERMAL RESISTANCE OF 68 LEADS PLCC PACKAGE

Data concerning DC and pulsed conditions are obtained for this package /3/, which has Jedec outline and copper frame.

Fig. 11 - R_{th} of "FLOATING" 68 lead PLCC

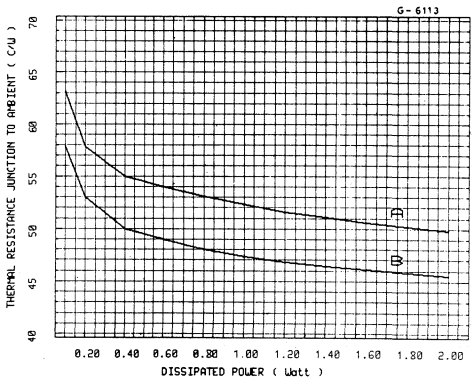
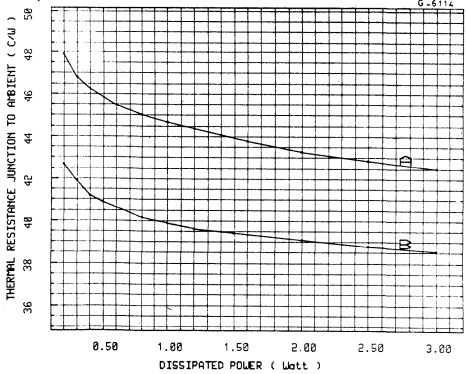


Fig. 12 - R_{th} of 68 lead PLCC mounted on board (Die pad area A = 300 $\times$ 300 sq. mils; B = 425 $\times$ 425 sq. mils)

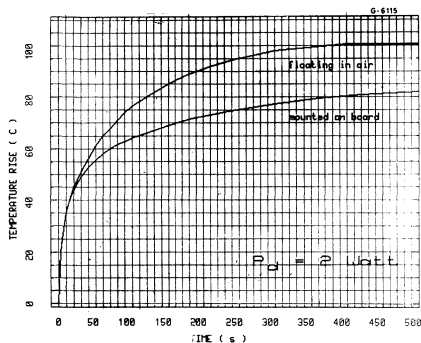


DC CONDITION

Fig. 11 and 12 show the thermal resistance for "floating" are assembled parts, respectively. Curves A and B refer to the minimum (300x300 sq. mils) and maximum (425x425 sq. mils die pad size, in both cases.

The package has a not negligible thermal capacitance, due to the thermal mass associated to the copper frame and to the molded body. From Fig. 13 a value of about 1-1.5J/s can be assumed for this parameter.

Fig. 13 - Temperature rise of 68 lead PLCC (DC)



PULSED CONDITIONS

Very interesting values are found for single pulses: power up to 10W can be delivered for about 1-2s (Fig. 14).

When the pulse is repeated with a certain duty cycle DC, junction temperature is oscillating about a mean value $T_J = T_{amb} + R_{th} P_d$ DC.

If the upper temperature values of the oscillation are considered, a peak transient thermal resistance can be defined, whose value is a function of pulse width and duty cycle. From the curves of Fig. 15 the thermal properties are obtained for different pulse conditions.

Fig. 14 - Transient R_{th} of 68 lead PLCC (Single pulse)

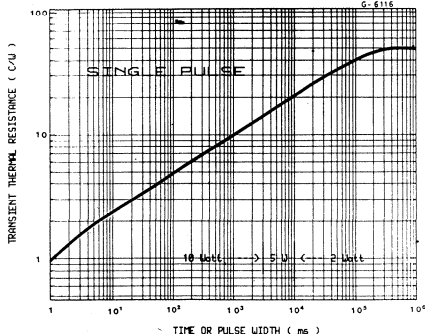
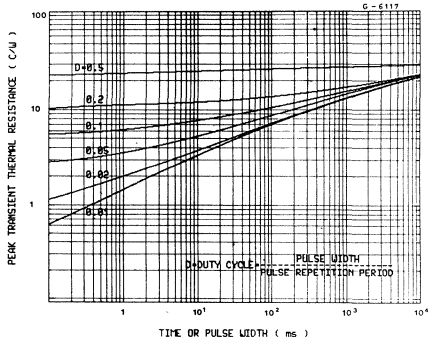


Fig. 15 - Peak transient R_{th} of 68 lead PLCC (AC)



DEVELOPMENT OF SMD POWER PACKAGE

The previous section has quantified the thermal performance limits for presently available SM standard packages.

Interesting values have been measured for 68 lead PLCC package: high pin count PLCCs are suitable to dissipate up to 1W in DC condition. No solution is standardized at present for higher power.

Two main development areas for power SM packages can be identified. The first is the medium power range (2W or less), where pin count up to 44 will be needed; the second is high power (more than 2W), where up to about 20 leads will be required /4/.

MEDIUM POWER SM PACKAGES

They can be derived very conveniently from existing SO and PLCC, by modifying the lead frame connecting a number of pins to the die pad, for heat removal.

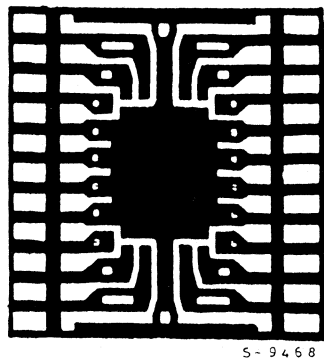
A thermal conductive path is obtained from the junction to an external heatsink, having a defined thermal resistance $R_{th}(j-sub)$. Cost effective heatsink is easily formed with a suitable copper area on the PCB, which the "grounded" pins are soldered to. Powers of 1-2W can be dissipated in this way.

This approach is particularly attractive because the external dimensions of the package are identical to the existing signal packages, allowing the use of standard tools for testing, shipping and assembly.

Example of modified SO20 package is given in Fig. 16.

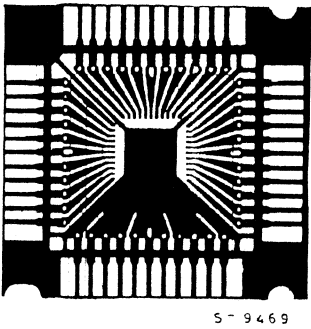
More interesting for future products is the application of modified leadframe techniques to PLCC. A PLCC 44 can be redesigned to obtain a A+B lead version (A+B = 44), which uses A signal pins and B leads connected to the die pad to reduce the junction to substrate thermal resistance. In Fig. 17, the frame of a new 33+11 power PLCC is shown, giving a junction to substrate thermal resistance better than 12°C/W. Such package is now entering in production is SGS. A typical application of this package for 2W dissipation is given in Fig. 18.

Fig. 16 - Medium power SO-20 frame



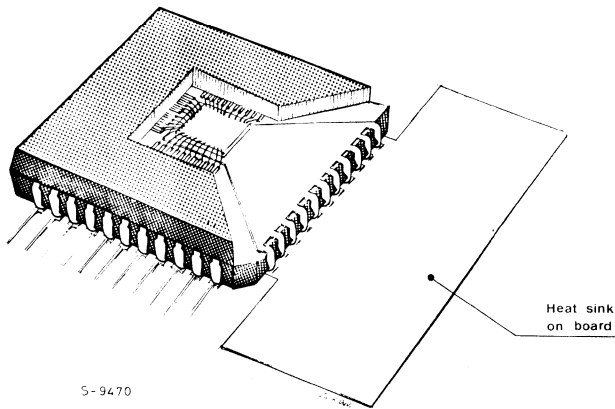
$R_{thj-amb}$	90°C/W
$R_{thj-sub}$	14°C/W
Max die size	125x205 mils

Fig. 17 - Medium power 33+11 lead PLCC frame



$R_{thj-amb}$	55°C/W
$R_{thj-sub}$	12°C/W
Max. die size	195 x 195 mils

Fig. 18 - Typical application (2W) of PLCC+11 with external heatsink integrated are the printed board



Additionally, the frame can be modified to incorporate dissipating 'fins' within the plastic body for a further reduction of the junction-to-ambient thermal resistance. In PLCC these fins are obtained easily at the corner of the package by sacrificing signal pins.

Due to availability of a high number of leads mils in PLCC, the reduction of useful pins is not a problem and junction to-ambient thermal resistances can be obtained in the range of 30-

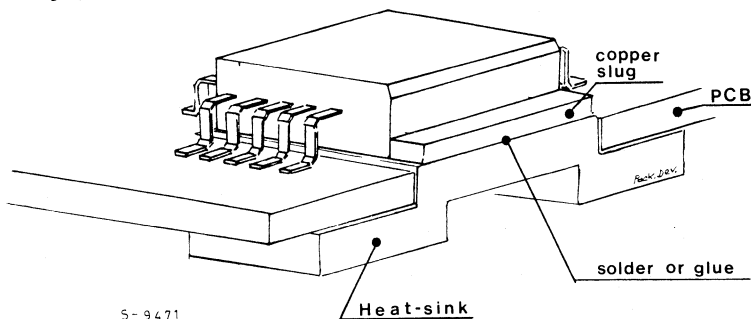
40°C/W, for the dissipation of 1.5-2W without any need of external heatsinks.

HIGH POWER SM PACKAGES

For IC's dissipating more than about 2W a different approach is needed.

One obvious solution is simply to form the leads of standard power packages so that they can be

Fig. 19 - High power module with external heatsink



surface mounted. SGS produces three terminal voltage regulators in a SM version of SOT-82 package arranged in this way.

In fact, development in this area is concentrated on a new generation of packages designed from the outset for surface mounting.

Recent trends in premolding techniques give additional possibility in defining the structure of the package.

A family of packages is now being studied with a junction-to-case thermal resistance of less than 5°C/W from 3 to 17 pins and a lead spacing of 50 mils. These packages will have a standard SO-width body and gull wing leads, allowing the use of SO packages handling equipments.

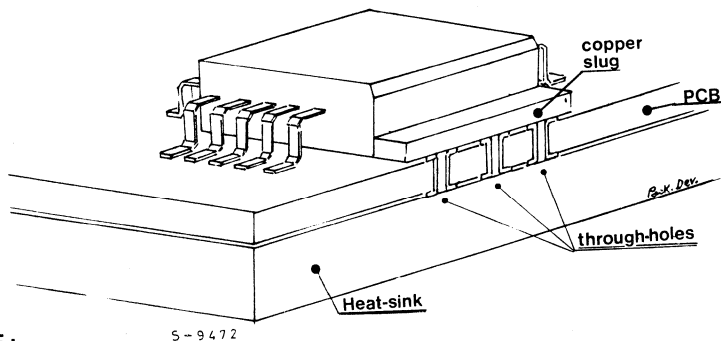
The low thermal resistance is obtained by a copper heatspreader on the lower surface of the package, upon which the die is attached. When the package

is soldered into place, the spreader is in contact with the substrate. Clearly the amount of power that can be dissipated depends on the conductivity of the substrate (Fig. 19).

In view of this trend there is now considerable interest in high conductivity substrates and the various alternatives, such as plastic boards bonded to aluminium or copper sheets. Plated through holes in the PCB under the chip's heat spreader may be used to improve the thermal resistance between the device and the metal (Fig. 20).

Another development area is the inclusion of a copper spreader on the under-side of pre-molded PLCC; the same substrate/heatsink possibilities apply to this package family too. This solution is obtained by moulding a plastic body having a cavity, into which the die is inserted later. It is more indicated for large area, high accuracy devices, for which some effects of the post epoxy molding process are very critical.

Fig. 20 - High power module with external heatsink and plated through holes



REFERENCE:

- /1/ C. Cognetti "Status of Active Surface Mounted Devices for Signal and Power Application" EIPC Conference Proc. p. 1.1.1 (Lugano, 1986)
- /2/ T. Hopkins, R. Tiziani, C. Cognetti "Improved Thermal Impedance Measurements by means of a simple Integrated Structure" Jemitherm Conf. Proc. Phoenix (USA) - Dicembre 86.
- /3/ SGS Technical Report MMD-86101
- /4/ C. Cognetti, R. Tiziani "Status of Power Packages and Evolution Towards Power SMD" Electronica - Munich - November 86.

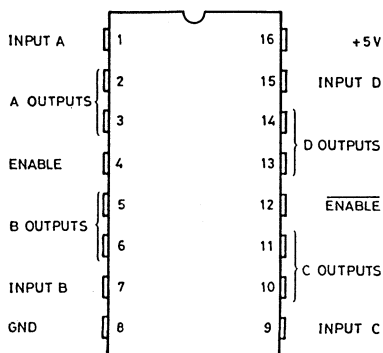
DATASHEETS



PRELIMINARY DATA

CONNECTION DIAGRAM

(Top view)

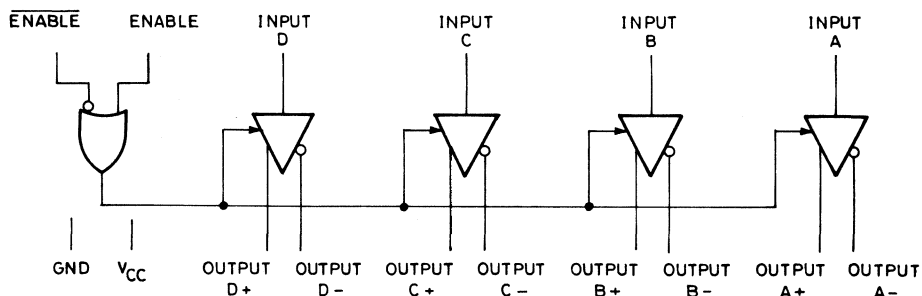


S-9166

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
DIP-16 Ceramic	-55 to 125°C	AM26LS31MJ
	0 to 70°C	AM26LS31CJ
DIP-16 Plastic	0 to 70°C	AM26LS31CN
SO-16J	0 to 70°C	AM26LS31D1

LOGIC DIAGRAM



S-9167

**THERMAL DATA**

			DIP-16 Ceramic	DIP-16 Plastic	SO-16
$R_{th\ j-amb}$	Thermal resistance junction-ambient	max.	150°C/W	200°C/W	165°C/W

ELECTRICAL CHARACTERISTICS (The following conditions apply unless otherwise specified:
 $T_{amb} = -55^{\circ}\text{C}$ to 125°C , $V_{CC} = 5\text{V} \pm 10\%$; $T_{amb} = 0$ to $+70^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$)

Parameter	Test Conditions	Min.	Typ. (Note 1)	Max.	Unit
V_{OH} Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -20\text{mA}$	2.5	3.2		V
V_{OL} Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 20\text{mA}$		0.32	0.5	V
V_{IH} Input HIGH Voltage	$V_{CC} = \text{Min.}$	2.0			V
V_{IL} Input LOW Voltage	$V_{CC} = \text{Max.}$			0.8	V
I_{IL} Input LOW Current	$V_{CC} = \text{Max.}, V_{IN} = 0.4\text{V}$		-0.20	-0.36	mA
I_{IH} Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = 2.7\text{V}$		0.5	20	μA
I_I Input Reverse Current	$V_{CC} = \text{Max.}, V_{IN} = 7.0\text{V}$		0.001	0.1	mA
I_O Off-State (High Impedance) Output Current	$V_{CC} = \text{Max.}$	$V_O = 2.5\text{V}$	0.5	20	μA
		$V_O = 0.5\text{V}$	0.5	-20	
V_I Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = 18\text{mA}$		-0.8	-1.5	V
I_{SC} Output Short Circuit Current	$V_{CC} = \text{Max.}$	-30	-60	-150	mA
I_{CC} Power Supply Current	$V_{CC} = \text{Max.},$ all outputs disabled		60	80	mA
t_{PLH} Input to Output	$V_{CC} = 5.0\text{V}, T_{amb} = 25^{\circ}\text{C}, \text{Load} = \text{Note 2}$		12	20	ns
t_{PHL} Input to Output	$V_{CC} = 5.0\text{V}, T_{amb} = 25^{\circ}\text{C}, \text{Load} = \text{Note 2}$		12	20	ns
SKEW Output to Output	$V_{CC} = 5.0\text{V}, T_{amb} = 25^{\circ}\text{C}, \text{Load} = \text{Note 2}$		2.0	6.0	ns
t_{LZ} Enable to Output	$V_{CC} = 5.0\text{V}, T_{amb} = 25^{\circ}\text{C}, C_L = 10\text{pF}$		23	35	ns
t_{HZ} Enable to Output	$V_{CC} = 5.0\text{V}, T_{amb} = 25^{\circ}\text{C}, C_L = 10\text{pF}$		17	30	ns
t_{ZL} Enable to Output	$V_{CC} = 5.0\text{V}, T_{amb} = 25^{\circ}\text{C}, \text{Load} = \text{Note 2}$		35	45	ns
t_{ZH} Enable to Output	$V_{CC} = 5.0\text{V}, T_{amb} = 25^{\circ}\text{C}, \text{Load} = \text{Note 2}$		30	40	ns

Notes: 1. A typical values are $V_{CC} = 5.0\text{V}$, $T_{amb} = 25^{\circ}\text{C}$

2. $C_L = 30\text{pF}$, $V_{IN} = 1.3\text{V}$ to $V_{OUT} = 1.3\text{V}$, $V_{PULSE} = 0\text{V}$ to $+3.0\text{V}$, See Below.



AM26LS31

Fig. 2 - Guaranteed V_{OH} and V_{OL} ($T_{amb} = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$)

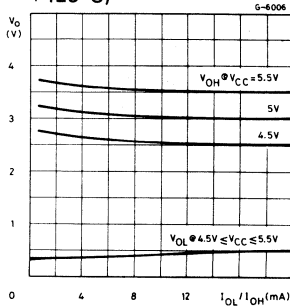


Fig. 3 - V_{OUT} vs. V_{CC}

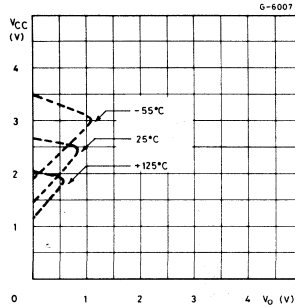


Fig. 4 - AC load test circuit for three-state outputs

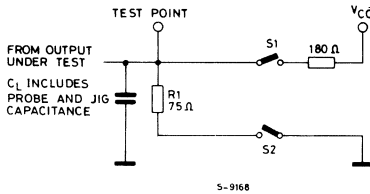


Fig. 5 - Propagation delay (Notes 1 and 3)

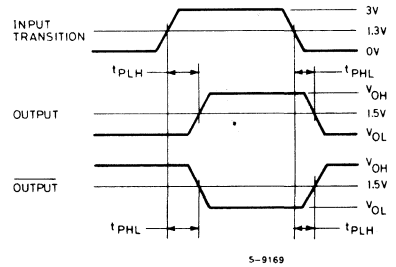
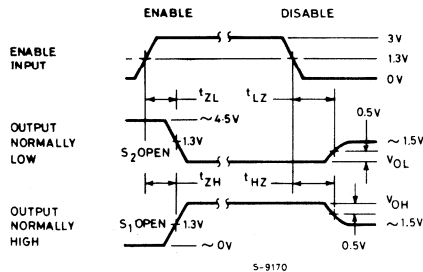


Fig. 6 - Enable and disable times (Notes 2 and 3)



- Notes:**
1. Diagram shown for Enable LOW.
 2. S1 and S2 of Load Circuit are closed except where shown.
 3. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_O = 50\Omega$; $t_r \leq 15\text{ns}$; $t_f \leq 6.0\text{ns}$.



AM26LS32 AM26LS33

PRELIMINARY DATA

RS422 AND RS423 QUAD DIFFERENTIAL LINE RECEIVERS

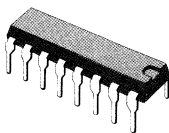
- THE AM26LS32 MEETS ALL THE REQUIREMENTS OF RS-422 AND RS-423
- 6K MINIMUM INPUT IMPEDANCE
- 30mV INPUT HYSTERESIS
- OPERATION FROM SINGLE +5V SUPPLY
- FAIL SAFE INPUT-OUTPUT RELATIONSHIP. OUTPUT ALWAYS HIGH WHEN INPUTS ARE OPEN
- THREE-STATE DRIVE, WITH CHOICE OF COMPLEMENTARY OUTPUT ENABLES, FOR RECEIVING DIRECTLY ONTO A DATA BUS
- PROPAGATION DELAY 17ns TYPICAL

The AM26LS32 is quad line receiver designed to meet the requirements of RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

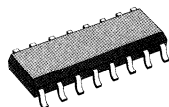
The AM26LS32 features an input sensitivity of 200mV over the input voltage range of $\pm 7V$.

The AM26LS33 features an input sensitivity of 500mV over the input voltage range of $\pm 15V$.

The AM26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-state outputs with 8mA sink capability and incorporate a fail safe input-output relationship which keeps the outputs high when the inputs are open.



DIP-16 Plastic (0.25)
and Ceramic



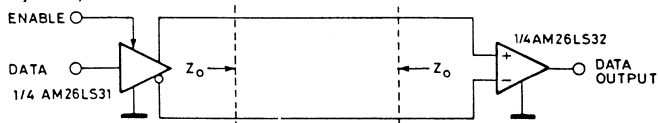
SO-16J

ABSOLUTE MAXIMUM RATINGS

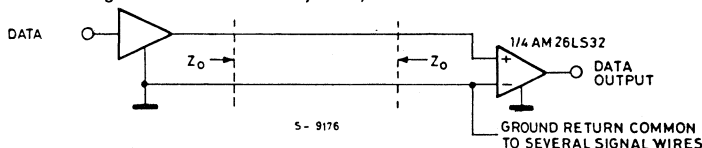
V_s	Supply voltage	7	V
CMR	Common mode range	± 25	V
V_i	Differential input voltage	± 25	V
V_E	Enable voltage	7	V
I_{os}	Output sink current	50	mA
T_{stg}	Storage temperature range	-65 to 150	$^{\circ}C$

Fig. 1 - Typical Applications

Two wire balanced system, RS-422



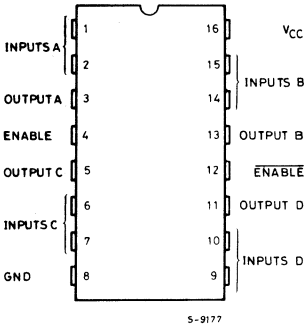
Single wire with common ground imbalanced system, RS-423



5 - 9176

CONNECTION DIAGRAM

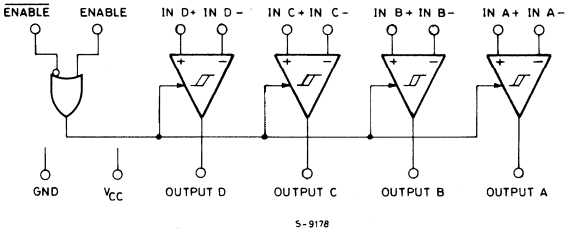
(Top view)



ORDERING INFORMATION

Package Type	Temperature Range	AM26LS32	AM26LS33
		Order Number	Order Number
Hermetic DIP	-55 to 125°C	AM26LS32MJ	AM26LS33MJ
Hermetic DIP	0 to 70°C	AM26LS32CJ	AM26LS33CJ
Molded DIP	0 to 70°C	AM26LS32CN	AM26LS33CN
SO-16J	0 to 70°C	AM26LS32D1	AM26LS33D1

LOGIC DIAGRAM



THERMAL DATA				DIP-16 Ceramic	DIP-16 Plastic	SO-16
$R_{th J-amb}$	Thermal resistance junction-ambient	max		150°C/W	200°C/W	165°C/W

ELECTRICAL CHARACTERISTICS (The following conditions apply unless otherwise specified: $T_{amb} = -55^{\circ}\text{C}$ to 125°C , $V_{CC} = 5\text{V} \pm 10\%$; $T_{amb} = 0$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$)

Parameter		Test Conditions	Min.	Typ. (1)	Max.	Unit
V_{TH}	Differential Input Voltage .	$V_{OUT} = V_{OL}$ or V_{OH}				V
		AM26LS32, $-7\text{V} \leq V_{CM} \leq +7\text{V}$	-0.2	± 0.06	+0.2	
		AM26LS33, $-15\text{V} \leq V_{CM} \leq +15\text{V}$	-0.5	± 0.12	+0.5	
R_{IN}	Input Resistance	$-15\text{V} \leq V_{CM} \leq +15\text{V}$ (One input AC ground)	6.0	9.8		$\text{K}\Omega$
I_{IN}	Input Current (Under Test)	$V_{IN} = +15\text{V}$, Other Input $-15\text{V} \leq V_{IN} \leq +15\text{V}$			2.3	mA
I_{IN}	Input Current (Under Test)	$V_{IN} = -15\text{V}$, Other input $-15\text{V} \leq V_{IN} \leq +15\text{V}$			-2.8	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$, $\Delta V_{IN} = +1.0\text{V}$	COM'L	2.7	3.4	V
		$V_{ENABLE} = 0.8\text{V}$, $I_{OH} = -440\mu\text{A}$	MIL	2.5	3.4	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$, $\Delta V_{IN} = -1.0\text{V}$	$I_{OL} = 4.0\text{mA}$		0.4	V
		$V_{ENABLE} = 0.8\text{V}$	$I_{OL} = 8.0\text{mA}$		0.45	
V_{IL}	Enable LOW Voltage				0.8	V
V_{IH}	Enable HIGH Voltage		2.0			V
V_I	Enable Clamp Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$			-1.5	V
I_O	Off-State (High Impedance) Output Current	$V_{CC} = \text{Max.}$	$V_O = 2.4\text{V}$		20	μA
			$V_O = 0.4\text{V}$		-20	
I_{IL}	Enable LOW Current	$V_{IN} = 0.4\text{V}$		-0.2	-0.36	mA
I_{IH}	Enable HIGH Current	$V_{IN} = 2.7\text{V}$		0.5	20	μA
I_I	Enable Input High Current	$V_{IN} = 5.5\text{V}$		1	100	μA
I_{SC}	Output Short Circuit Curr.	$V_O = 0\text{V}$, $V_{CC} = \text{Max.}$, $\Delta V_{IN} = +1.0\text{V}$	-15	-50	-85	mA
I_{CC}	Power Supply Current	$V_{CC} = \text{Max.}$, All $V_{IN} = \text{GND}$, Output Disabled		52	70	mA
V_{HYST}	Input Hysteresis	$T_{amb} = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{V}$, $V_{CM} = 0\text{V}$		30		mV
t_{PLH}	Input to Output	$T_{amb} = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{V}$, $C_L = 15\text{pF}$, see test cond. below		17	25	ns
t_{PHL}	Input to Output	$T_{amb} = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{V}$, $C_L = 15\text{pF}$, see test cond. below		17	25	ns
t_{LZ}	Enable to Output	$T_{amb} = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{V}$, $C_L = 5\text{pF}$, see test cond. below		20	30	ns
t_{HZ}	Enable to Output	$T_{amb} = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{V}$, $C_L = 5\text{pF}$, see test cond. below		15	22	ns
t_{ZL}	Enable to Output .	$T_{amb} = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{V}$, $C_L = 15\text{pF}$, see test cond. below		15	22	ns
t_{ZH}	Enable to Output	$T_{amb} = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{V}$, $C_L = 15\text{pF}$, see test cond. below		15	22	ns

(1) All typical values are $V_{CC} = 5.0\text{V}$, $T_{amb} = 25^{\circ}\text{C}$



AM26LS32 AM26LS33

Fig. 2 - Load test circuit for three-state outputs

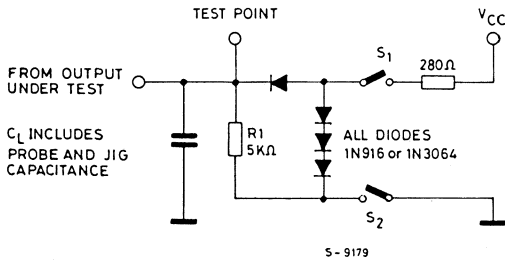


Fig. 3 - Propagation delay (notes 2 and 3)

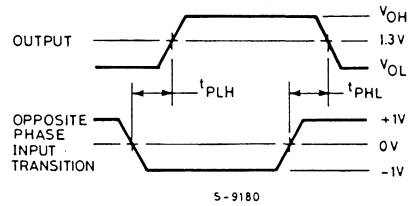
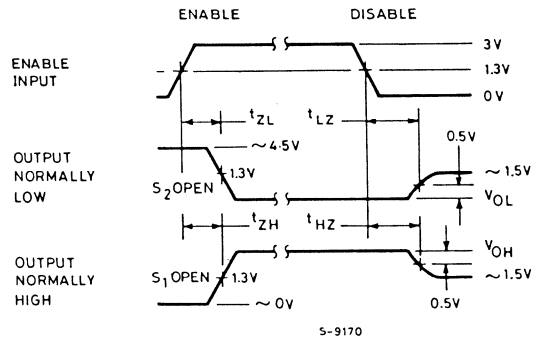


Fig. 4 - Enable and disable time (notes 2 and 3)



- Notes:**
1. Diagram shown for $\overline{\text{Enable}}$ LOW
 2. S1 and S2 of Load Circuit are closed except where shown.
 3. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_o = 50\Omega$; $t_r \leq 15\text{ns}$; $t_f \leq 6.0\text{ns}$



AM6012 AM6012A

PRELIMINARY DATA

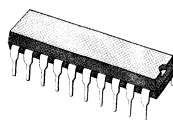
12-BIT HIGH SPEED MULTIPLYING D/A CONVERTERS

The AM6012 is an industry standard monolithic 12-bit digital-to analog converter. Complementary current output and high speed multiplying capability make the AM6012 useful in a wide range of applications such as video displays, process control circuitry and fast A/D converters. The 6012 is the first D/A to achieve 12-bit differential linearity without the use of thin film resistors or active trimming. The 6012's unique circuit design insures monotonicity without the precision trimming associated with most other 12-bit DAC architectures.

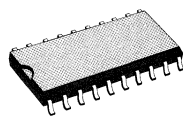
The AM6012 is packaged in a 20-pin plastic DIP and is SO-20L for surface mounting. Although tested and specified at $\pm 15V$, the AM6012 works well over a wide range of power supply voltages. Performance is essentially independent of supply voltage over the range of $+5$ volts, -12 volts to ± 18 volts. The AM6012 series guarantees full 12-bit monotonicity for all grades and differential nonlinearity as high as 0.012% (13 bits) for the A grades and 0.025% (12 bits) for the standard grades over the entire temperature range.

Guaranteed monotonicity and low cost make the AM6012 an ideal choice for high volume applications requiring fine local resolution. Typical applications include printer graphics and video displays. These applications need a minimum of 12 bits of resolution, although conformance to an ideal straight line from zero to full scale is less important.

- ALL GRADES 12-BIT MONOTONIC OVER TEMPERATURE
- DIFFERENTIAL NONLINEARITY TO $\pm 0.012\%$ (13 BITS) MAX OVER TEMPERATURE (A GRADES)
- 250ns TYPICAL SETTLING TIME
- FULL SCALE CURRENT 4mA
- HIGH SPEED MULTIPLYING CAPABILITY
- TTL/CMOS/ECL/HTL COMPATIBLE
- HIGH OUTPUT COMPLIANCE: $-5V$ TO $+10V$
- COMPLEMENTARY CURRENT OUTPUTS
- LOW POWER CONSUMPTION: 230mW

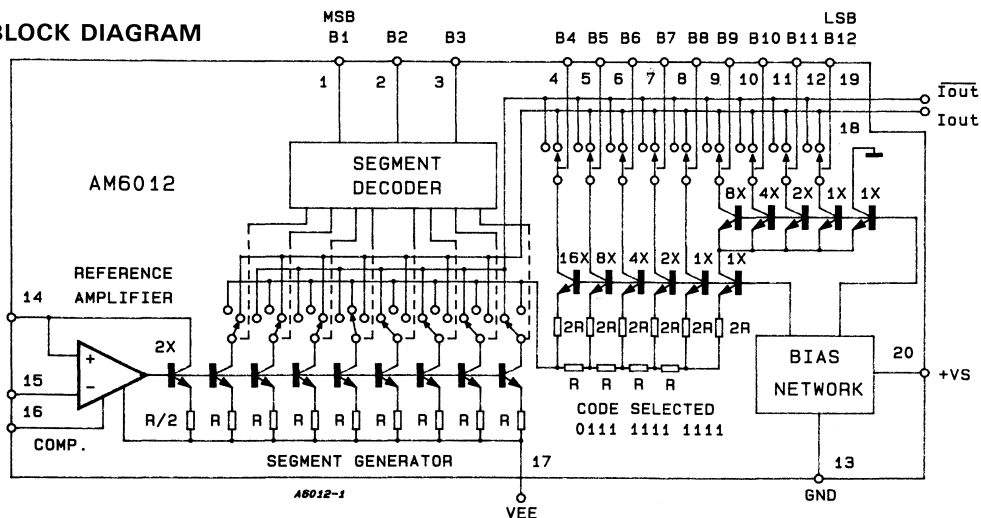


DIP-20 Plastic (X3P2)



SO-20L

BLOCK DIAGRAM



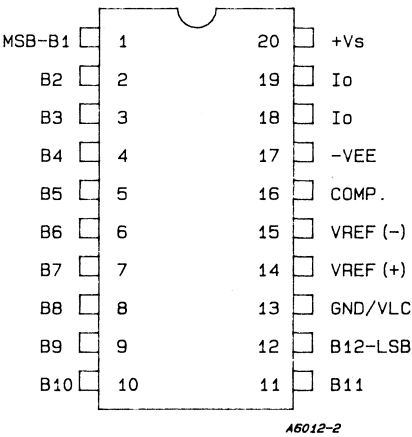
ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0 to 70	°C
Storage Temperature	− 65 to + 125	°C
Power Supply Voltage	± 18	V
Logic Inputs	− 5 to + 18	V
Voltage at Current Outputs Pins	− 8 to + 12	V
Reference Inputs	+ V _S to − V _{EE} ± 18V	V
Reference Input Current	max Differential 1.25	mA

CONNECTION DIAGRAM AND ORDERING INFORMATION

Type	Differential linearity (%)	Temperature Range (°C)	Package
AM6012PC	0.025	0 to 70	DIP.20
AM6012APC	0.012		
AM6012 D	0.025	0 to 70	SO.20L
AM6012 AD	0.012		

(TOP VIEW)



THERMAL DATA

R _{thj-amb}	Thermal resistance junction-ambient	max	100 °C/W
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ELECTRICAL CHARACTERISTICS

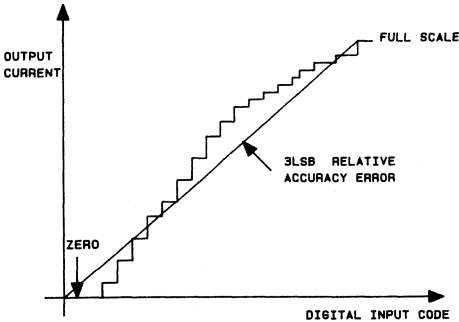
These specifications apply for $V_S = +15V$, $V_{EE} = -15V$, $I_{REF} = 1.0mA$, over the operating temperature range unless otherwise specified

Param.	Description	Test Conditions	AM6012A			AM6012			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
	Resolution		12	12	12	12	12	12	Bits
	Monotonicity		12	12	12	12	12	12	Bits
D.N.L.	Differential Nonlinearity	Deviation from ideal step size	—	—	$\pm .012$	—	—	$\pm .025$	%FS
			13	—	—	12	—	—	Bits
N.L.	Nonlinearity	Deviation from ideal straight line	—	—	$\pm .05$	—	—	± 0.05	%FS
I_{FS}	Full Scale Current	$V_{REF} = 10.000V$ $R_{14} = R_{15} = 10.000k\Omega$ $T_A = 25^\circ C$	3.967	3.999	4.031	3.935	3.999	4.063	mA
TCI_{FS}	Full Scale Temp.Co.		—	± 5	± 20	—	± 10	± 40	ppm $^\circ C$
			—	$\pm .0005$	$\pm .002$	—	$\pm .001$	$\pm .004$	%FS $^\circ C$
V_{OC}	Output Voltage Compliance	D.N.L. Specification guaranteed over compliance range $R_{OUT} > 10$ megohms typ.	-5	—	+10	-5	—	+10	V
I_{FSS}	Full Scale Symmetry	$I_{FS} - I_{FS}$	—	± 0.2	± 1.0	—	± 0.4	± 2.0	μA
I_{ZS}	Zero Scale Current		—	—	0.10	—	—	0.10	μA
I_S	Setting Time	To $\pm 1/2$ LSB, all bits ON or OFF, $T_A = 25^\circ C$	—	250	500	—	250	500	nSec
t_{PLH} t_{PHL}	Propagation Delay - all bits	50% to 50%	—	25	50	—	25	50	nSec
C_{OUT}	Output Capacitance		—	20	—	—	20	—	pF
V_{IL}	Logic Input Levels	Logic "0"	—	—	0.8	—	—	0.8	V
V_{IH}		Logic "1"	2.0	—	—	2.0	—	—	
I_{IN}	Logic Input Current	$V_{IN} = -5$ to $+18V$	—	—	40	—	—	40	μA
V_{IS}	Logic Input Swing	$V_{EE} = -15V$	-5	—	+18	-5	—	+18	V
I_{REF}	Reference Current Range		0.2	1.0	1.1	0.2	1.0	1.1	mA
I_{15}	Reference Bias Current		0	-0.5	-2.0	0	-0.5	-2.0	μA

ELECTRICAL CHARACTERISTICS (Continued)

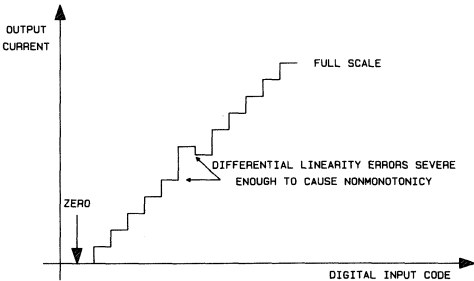
Param.	Description	Test Conditions	AM6012A			AM6012			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
di/dt	Reference Input Slew Rate	$R_{14(eq)} = 800\Omega$ $CC = 0pF$	4.0	8.0	—	4.0	8.0	—	$mA/\mu s$
$PSSI_{FS+}$	Power Supply Sensitivity	$V_S = (+13.5V \text{ to } +16.5V)$ $V_{EE} = -15V$	—	$\pm .00005$	$\pm .001$	—	± 0.0005	$\pm .001$	%FS/%
$PSSI_{FS-}$		$V_{EE} = -13.5V \text{ to } -16.5V$ $V_S = +15V$	—	$\pm .00025$	$\pm .001$	—	$\pm .00025$	$\pm .001$	
V_S	Power Supply Range	$V_{OUT} = 0V$	4.5	—	18	4.5	—	18	V
V_{EE}			-18	—	-10.8	-18	—	-10.8	
I+	Power Supply Current	$V_S = +5V, V_{EE} = -15V$	—	5.7	8.5	—	5.7	8.5	mA
I-			—	-13.7	-18.0	—	-13.7	-18.0	
I+		$V_S = +15V, V_{EE} = -15V$	—	5.7	8.5	—	5.7	8.5	
I-			—	-13.7	-18.0	—	-13.7	-18.0	
P_D	Power Dissipation	$V_S = +5V, V_{EE} = -15V$	—	234	312	—	234	312	mW
		$V_S = +15V, V_{EE} = -15V$	—	291	397	—	291	397	

Fig. 1 - Relative Accuracy Error



AM6012-10: : DIS

Fig. 2 - Example of Nonmonotonic Behavior



AM6012-10: : LIB

APPLICATION INFORMATION

FUNCTIONAL DESCRIPTION

The segmented design of the AM6012, shown in the block diagram, insures that there are no significant differential nonlinearities in the transfer characteristic. The eight major carries of the most significant bits are not subject to the gross differential nonlinearities that can occasionally occur in an R-2R type DAC. This advantage is due to the fundamentally different way that the current is handled in an AM6012. In a conventional R-2R type DAC, when the input code is incremented past a major carry, a current representing the new code is substituted for the sum of all the less significant bit currents that were previously on. To avoid any nonlinearities, the two total currents must be extremely well matched. In the case of the MSB major carry in a 12-bit DAC, the match must be better than one part in 2048 to maintain monotonicity. However, in the AM6012, a new current is never substituted for the sum of several smaller ones, but redirected through alternate channels and incremented one step at a time.

For example, consider the MSB carry in an AM6012. In the initial state of 011111111111 as shown in the block diagram, the switches in the segment generator are set in such a way that currents I_0 , I_1 and I_2 are steered directly into the noninverting output I_{OUT} . In addition, a portion of I_3 is directed through the 9-bit DAC that is controlled by the 9 least significant bits into I_{OUT} . With the 9LSBs set to "1", all of the I_3 current is directed to I_{OUT} except for the $1/512$ that goes to ground through the right-most transistor in the 9-bit DAC. After the input word is changed to 100000000000, the segment decoder switch for I_3 will be all the way to the right, the switch for I_4 will be in the middle, and all the switches in the 9-bit DAC will be to the left. I_{OUT} will be composed of I_0 , I_1 , I_2 and I_3 . None of I_4 will be directed into I_{OUT} until a higher code is reached. In other words, I_3 is now steered directly to I_{OUT} instead of being divided by a factor of $511/512$ in the 9-bit DAC. Since no major current substitution occurs, there is less chance of a large nonlinearity at this transition than in a comparable R-2R DAC.

RELATIVE ACCURACY VS. DIFFERENTIAL NONLINEARITY

SGS defines relative accuracy as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn between the lowest code output voltage and the highest code output voltage) for any bit combination. Relative

accuracy is often referred to as nonlinearity. The DAC transfer function shown in Figure 1 has a bow that results in a maximum relative accuracy error of 3LSB. This must be distinguished from a differential linearity error. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code.

For example, for a 4mA full scale output, a change of 1LSB in digital input code should result in a $0.98\mu A$ change in the analog output current ($1LSB = 4mA \times 1/4096 = 0.98\mu A$). If in actual use, however, a 1LSB change in the input code results in a change of only $0.24\mu A$ ($1/4LSB$) in output current, the differential linearity error would be $0.74\mu A$ or $3/4LSB$.

The AM6012 has very good differential linearity in spite of the poor relative accuracy. Conversely, the DAC of Figure 1 has very good relative accuracy but poor differential linearity. The anomaly in the middle of the transfer function is the result of a positive differential linearity error followed by a negative differential linearity error greater than 1LSB. A negative output step for an increase in digital input code is referred to as nonmonotonic behavior. In general, if a DAC has a differential linearity error specification greater than 1LSB, it may be nonmonotonic at one or more of the major carries. In most cases the worst differential linearity error will occur at the MSB transition point.

As noted in the functional description, the 6012's unique design minimizes differential linearity errors at the transition points of the 3MSBs. This results in a tight specification on maximum differential nonlinearity over temperature. Differential linearity is verified on all AM6012s with 100% final testing. In many converter applications, uniform step size (or minimum differential linearity error) is more important than conformance to an ideal straight line. Twelve-bit converters are usually needed for high resolution rather than high linearity as evidenced by the fact that few transducers are more linear than 0.1%. This is also true in video graphics, where the human eye has difficulty discerning nonlinearity of less than 5%. The AM6012 is especially well suited for these applications since it has inherently low differential linearity error.



APPLICATION INFORMATION (Continued)

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + I_{\bar{O}} = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 18 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 18 and turned on at pin 19. A decreasing logic count increase I_O as in a negative or inverter logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FR} ; do not leave an unused output pin one.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 25V above V_- and is independent of the positive supply. Negative compliance is +10V above V_- .

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The AM6012 operates over a wide range of power supply voltages from a total supply of 20V to 36V. When operating with V_- supplies of -10V or less, $I_{REF} \leq 1\text{mA}$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at -9V with $I_{REF} = 1\text{mA}$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the AM6012 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and mononicity specifications of the AM6012 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is flight, typically $\pm 10\text{ppm}/^\circ\text{C}$ with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full scale drift.

SETTLING TIME

The AM6012 is capable of extremely fast settling times, typically 250ns at $I_{REF} = 1.0\text{mA}$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 25ns for each of the 12 bits. Settling time to within 1/2 LSB of the LSB is therefore 25ns, with each progressively larger bit taking successively longer. The MSB settles in 250ns, thus determining the overall settling time of 250ns. Settling to 10-bit accuracy requires about 90 to 130ms. The output capacitance of the AM6012 including the package is approximately 20pF; therefore, the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 0.5mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve $\pm 2\mu\text{A}$, therefore a 2.5k Ω load is needed to provide adequate drive for most oscilloscopes. At I_{REF} values of less than 0.5mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 011111111111 to 100000000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within $\pm 0.1\%$ of the final value, and thus settling times may be observed at lower values of I_{REF} .

AM6012 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

APPLICATION INFORMATION (Continued)

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1 μ F capacitors at the supply pins provide full transient protection.

REFERENCE AMPLIFIER SETUP

The AM6012 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{RF} = \frac{4095}{4096} \times 4 \times (I_{REF}) = 3.999 I_{REF},$$

where $I_{REF} = I_{14}$

In positive reference applications, an external positive reference voltage forces current through R14 into the $V_{REF}(+)$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF}(-)$ at pin 15. Reference current flows from ground through R14 into $V_{REF}(+)$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors. (Figure 3).

Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: $V_{CM-} = V_-$ plus $(I_{REF} \times 3k\Omega)$ plus 1.8V. The positive common-mode range is V_+ less 1.23V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into two resistors with the junction bypassed to ground with a 0.1 μ F capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF} . If required, full scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14.

MULTIPLYING OPERATION

The AM6012 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1mA to 1 μ A. Monotonic operation is maintained over a typical range of I_{REF} from 100 μ A to 1.0mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V_- . The value of this capacitor depends on the impedance presented to pin 14. For R14 values of 1.0, 2.5 and 5 $0k\Omega$; minimum values of C_C are 5, 12 and 25 pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin (See Figure 4 and 5).

For fastest response to a pulse, low values of R14 enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall compensated which will decrease overall bandwidth and slew rate. For R14 = 1k Ω and C_C = 5pF, the reference amplifier slews at 4mA/ms enabling a transition from $I_{REF} = 0$ to $I_{REF} = 1$ mA in 250ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. Full scale transition (0 to 1mA) occurs in 62.5ns when the equivalent impedance at pin 14 is 800 Ω and $C_C = 0$. This yields a reference slew rate of 8mA/ μ s which is relatively independent of R_{IN} and V_{IN} values.

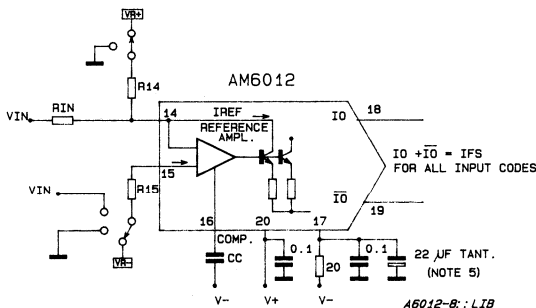
APPLICATION INFORMATION (Continued)

LOGIC INPUTS

The AM6012 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 40 μ A logic input current, and completely adjustable logic inputs may swing between -5 and $+10$ V. This enables direct interface with $+15$ V CMOS logic, even when the AM6012 is powered from a $+5$ V supply. Minimum input logic swing and minimum logic threshold may be ad-

justed over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 13, V_{LC}). For TTL interface, simply ground pin 13. When interfacing ECL, an $I_{REF} \leq 1$ mA is recommended. For interfacing other logic families, see block titled "Interfacing With Various Logic Families". For general setup of the logic control circuit, it should be noted that pin 13 will sink 1.1mA typical, external circuitry should be designed to accommodate this current (Figure 6).

Fig. 3 - Reference amplifier biasing



Reference Configuration	R_{14}	R_{15}	R_{IN}	C_C	I_{REF}
Positive Reference	V_{R+}	0V	N/C	.01 μ F	V_{R+} / R_{14}
Negative Reference	0V	V_{R-}	N/C	.01 μ F	$-V_{R-} / R_{14}$
Lo Impedance Bipolar Reference	V_{R+}	0V	V_{IN}	(Note 1)	$V_{R+} / R_{14} + (V_{IN} / R_{IN})$ (Note 2)
Hi Impedance Bipolar Reference	V_{R+}	V_{IN}	N/C	(Note 1)	$(V_{R+} - V_{IN}) / R_{14}$ (Note 3)
Pulsed Reference (Note 4)	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+} / R_{14}) + (V_{IN} / R_{IN})$

Notes:

1. The compensation capacitor a function of the impedance seen at the $+V_{REF}$ input and must be at least $5pF \times R_{14(eq)}$ in k Ω . For $R_{14} < 800\Omega$ no capacitor is necessary.
2. For negative values of V_{IN} , V_{R+} / R_{14} must be greater than $-V_{IN} \text{ Max} / R_{IN}$ so that the amplifier is not turned off.
3. For positive values of V_{IN} , V_{R+} must be greater than $V_{IN} \text{ Max}$ so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at pin 14 should be 800 Ω or less.
5. For optimum settling time, decouple V_- with 20 Ω and bypass with 22 μ F tantalum capacitor.
6. Reference current and reference resistor - there is a 1 to 4 scale factor between the reference current (I_{REF}) and the full scale output current (I_{FS}). If $V_{REF} = +10$ V and $I_{FS} = 4$ mA, the value of the R_{14} is:

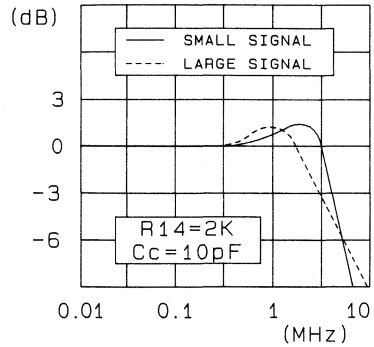
$$R_{14} = \frac{4 \times 10 \text{ Volt}}{4 \text{ mA}} = 10 \text{ k}\Omega \quad R_{14} = R_{15}$$

Fig. 4 - Minimum size compensation capacitor
($I_{FS}=4mA$, $I_{REF}=1.0mA$)

$R_{14}(EQ)(K\Omega)$	$C_C(pF)$
10	50
5	25
2	10
1	5
5	0

Note: A 0.01 μF capacitor is recommended for fixed reference operation.

Fig. 5 - Reference Amplifier Frequency response



A6012-11::DI

Fig. 6 - Interfacing Circuits

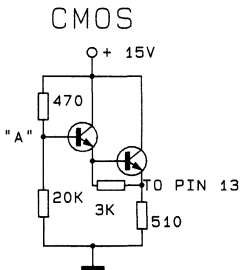
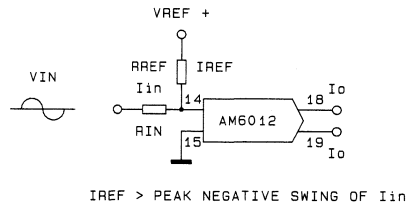
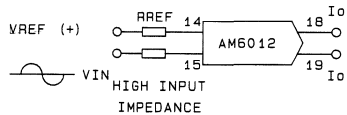
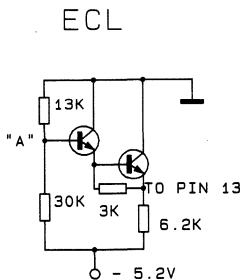


Fig. 7 - Accomodating Bipolar Reference

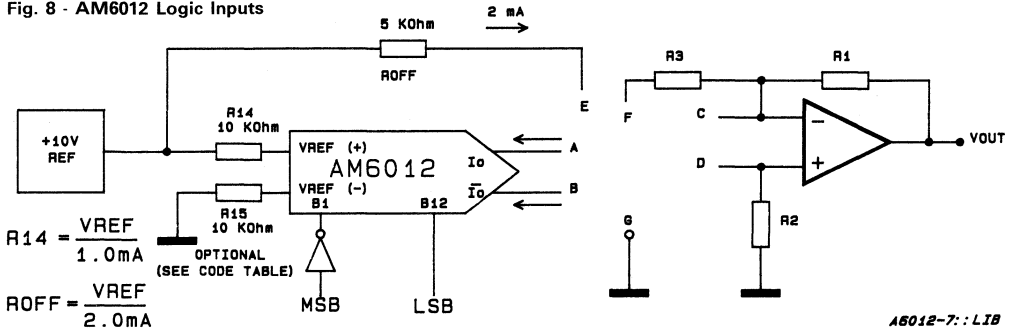


$I_{REF} > \text{PEAK NEGATIVE SWING OF } I_{in}$



$V_{REF} (+)$ MUST BE ABOVE PEAK POSITIVE SWING OF V_{IN}

Fig. 8 - AM6012 Logic Inputs



Code Format		Connec.	Output Scale	MSB	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	LSB	I ₀	I ₀	V _{OUT}
Unipolar	Straight binary one polarity with true input code, true zero output.	a-c b-g R ₁ = R ₂ = 2.5K	Positive full scale Positive full scale-LSB Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9978
				1	1	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9951
				0	0	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	.0000
	Complementary binary one polarity with complementary input code, true zero output.	a-g b-c R ₁ = R ₂ = 2.5K	Positive full scale Positive full scale-LSB Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	9.9976
				0	0	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	9.9951
				1	1	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	.0000
Symmetrical Offset	Straight offset binary; offset half scale, symmetrical about zero, no true zero output.	a-c b-d f-0 R ₁ = R ₃ = 2.5K R ₂ = 1.25K	Positive full scale Positive full scale-LSB (+) Zero scale (-) Zero scale Negative full scale-LSB Negative full scale	1	1	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
				1	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9927	
				1	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.0024	
				0	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-.0024	
				0	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	-9.9927	
				0	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	-9.9976	
	1's complement offset half scale symmetrical about zero, no true zero output MSB complemented (need inverter at B1).	a-c b-d f-g R ₁ = R ₃ = 2.5K R ₂ = 1.25K	Positive full scale Positive full scale-LSB (+) Zero scale (-) Zero scale Negative full scale-LSB Negative full scale	0	1	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
				0	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9927	
				0	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.0024	
				1	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-.0024	
				1	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	-9.9927	
				-1	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	-9.9976	
Offset with True Zero	Offset binary, offset half scale, true zero output.	e-a-c b-g R ₁ = R ₂ = 5K	Positive full scale Positive full scale-LSB +LSB Zero Scale -LSB Negative full scale +LSB Negative full scale	1	1	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9951
				1	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9902	
				1	0	0	0	0	0	0	0	0	0	0	0	0	2.001	1.998	.0049	
				1	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.000	
				0	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-.0049	
				0	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	-9.9951	
				0	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	-10.000	
	2's complement offset half scale true zero output MSB complemented (need inverter at B1)	e-a-c b-g R ₁ = R ₂ = 5K	Positive full scale Positive full scale-LSB +1 LSB Zero scale -1 LSB Negative full scale +LSB Negative full scale	0	1	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.006	9.9951
				0	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9902	
				0	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	.0049	
				0	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.000	
				1	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-.0049	
				1	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	-9.9951	
				1	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	-10.000	

ADDITIONAL CODE MODIFICATIONS

- Any of the offset binary codes may be complemented by reversing the output terminal pair.



AM6012
AM6012A

Fig. 9 - Basic Negative Reference Operation

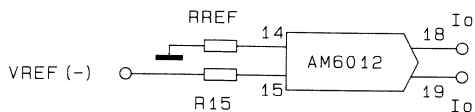


Fig. 10 - Recommended Full-scale Adjustment Circuit

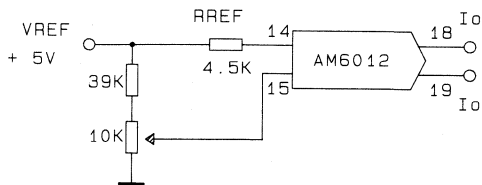


Fig. 11 - CRT Display Driver

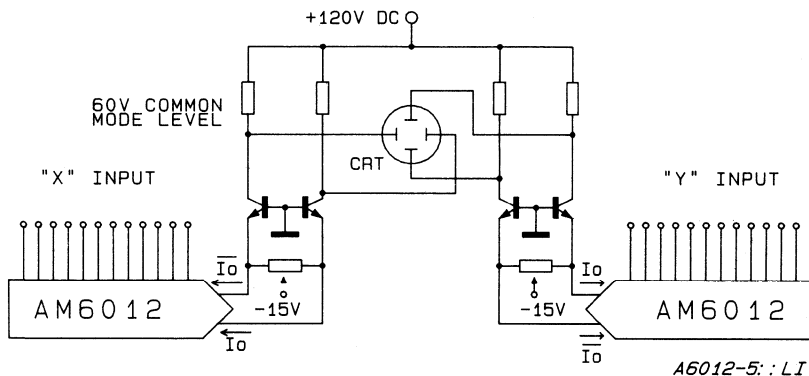
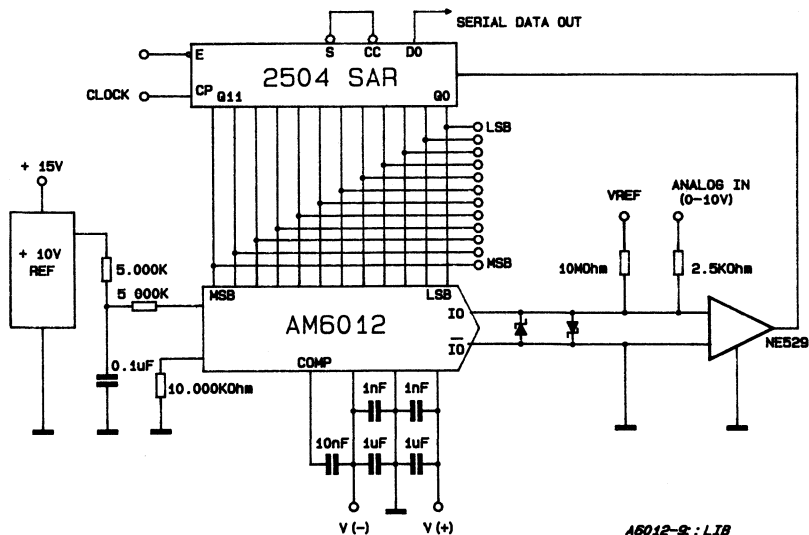


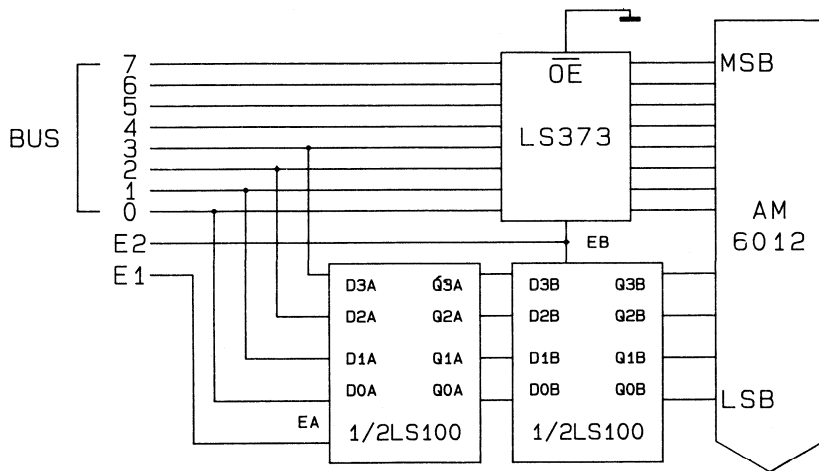
Fig. 12 - 12-BIT High-Speed A/D Converter





AM6012 AM6012A

Fig. 13 - Interface with 8-bit Microprocessor Bus



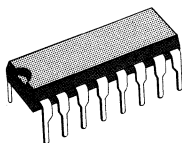
AM6012-4: L1B



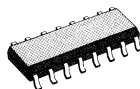
PRELIMINARY DATA

±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μ A provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, or CMOS logic levels, and is a direct replacement for the MC1508/MC1408.

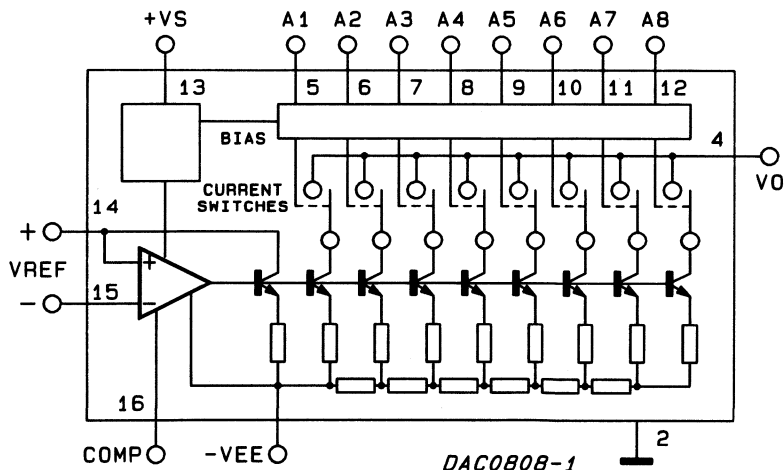


DIP-16 Plastic (0.25) and Ceramic



SO-16

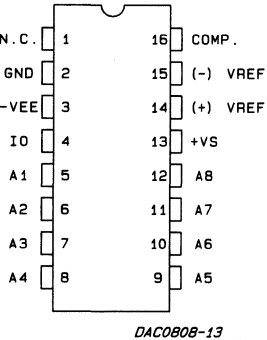
The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with $\pm 5V$ supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ± 1 LSB of $255 I_{REF}/256$. Relative accuracies of better than



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
Vs	+ 18 V
VEE	− 18 V
Digital Input Voltage V5 – V12	− 10 V to + 18 V
Reference Current, I14	5 mA
Reference Amplifier Inputs, V14, V15	VCC VEE
Operating Temperature Range	
DAC0808L	− 55°C ≤ TA ≤ + 125 °C
DAC0808LC/D	0 ≤ TA ≤ + 75 °C
Storage Temperature Range	− 65°C to + 150 °C

CONNECTION DIAGRAM AND ORDERING INFORMATION



Accuracy	Temperature range	Plastic DIP-16	Ceramic DIP-16	SO-16
8 bit	0 to 75°C	DAC0808LCN	DAC0808LCJ	DAC0808D
7 bit	0 to 75°C	DAC0807LCN	DAC0807LCJ	DAC0807D
6 bit	0 to 75°C	DAC0806LCN	DAC0806LCJ	DAC0806D
8 bit	− 55 to 125°C	—	DAC0808LJ	—

THERMAL DATA

	Ceramic DIP-16	SO-16	Plastic DIP-16
Rthj-amb Thermal resistance junction-ambient max	150°C/W	120°C/W	100°C/W

ELECTRICAL CHARACTERISTICS

($V_S = 5V$, $V_{EE} = -15V$, $V_{REF}/R_{14} = 2\text{ mA}$, $T_A = T_{MIN}$ to T_{MAX} and all digital inputs at high logic level unless otherwise noted.)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
E_r Relative Accuracy (Error Relative to Full Scale I_O) DAC0808L DAC0807LC/D1 (Note 1) DAC0806LC/D1 (Note 1) Settling Time to Within 1/2 LSB (Includes t_{PLH})	(Figure 10) $T_A = 25^\circ\text{C}$ (Note 2) (Figure 11)		150	± 0.19 ± 0.39 ± 0.78	% % % ns
t_{PLH} t_{PHL} Propagation Delay Time	$T_A = 25^\circ\text{C}$ (Figure 11)		30	100	ns
TC_{IO} Output Full Scale Current Drift			± 20		ppm/ $^\circ\text{C}$
MSB Digital Input Logic Levels V_{IH} High Level, Logic "1" V_{IL} Low Level, Logic "0"	(Figure 9)	2		0.8	V_{DC} V_{DC}
MSB Digital Input Current High Level Low Level	(Figure 9) $V_{IH} = 5V$ $V_{IL} = 0.8V$		0 -0.003	0.040 -0.8	mA mA
I_{15} Reference Input Bias Current Output Current Range	(Figure 3) (Figure 9) $V_{EE} = -5V$ $V_{EE} = -15V$, $T_A = 25^\circ\text{C}$	0 0	-1 2.0 2.0	-3 2.1 4.2	μA mA mA
I_O Output Current Output Current, All Bits Low Output Voltage Compliance $V_{EE} = -5V$ V_{EE} Below -10V	$V_{REF} = 2.000V$. $R_{14} = 1000\Omega$ (Figure 9) (Figure 9) $E_r \leq 0.19\%$, $T_A = 25^\circ\text{C}$	1.9	1.99 0	2.1 4 -0.55, +0.4 -5.0, +0.4	mA μA V V
$SR _{REF}$ Reference Current Slew Rate Output Current Power Supply Sensitivity	(Figure 14) -5V $\leq V_{EE} \leq -16.5V$	4	8 0.05	2.7	mA/ μs $\mu\text{A}/V$
Power Supply Current (All Bits Low) I_S I_{EE}	(Figure 9)		2.3 -4.3	22 -13	mA
Power Supply Voltage Range V_S V_{EE}	$T_A = 25^\circ\text{C}$ (Figure 9)	4.5 -4.5	5.0 -15	5.5 -16.5	V
Power Dissipation All Bits Low All Bits High	$V_S = 5V$, $V_{EE} = -5V$ $V_S = 5V$, $V_{EE} = -15V$ $V_S = 15V$, $V_{EE} = -5V$ $V_S = 15V$, $V_{EE} = -15V$		33 106 90 160	170 305	mW mW mW mW

Note 1: All current switches are tested to guarantee at least 50% of rated current.

Note 2: All bits switched.

Note 3: Range control is not required.

Fig. 1 - Supply Current vs Temperature

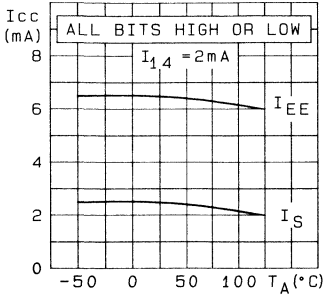


Fig. 2 - Supply Current vs Supply Voltage (V_{EE})

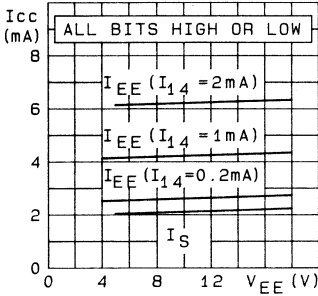


Fig. 3 - Supply Current vs Supply Voltage (V_S)

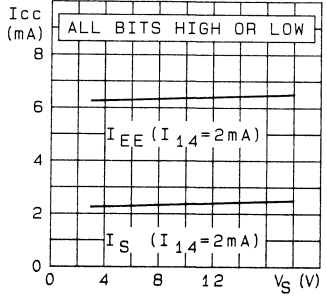


Fig. 4 - Logic Input Current vs Input Voltage

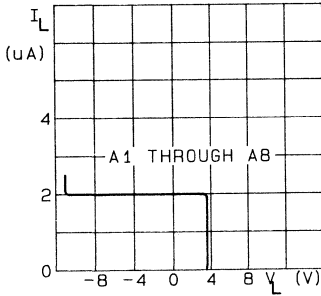


Fig. 5 - Bit Transfer Characteristics

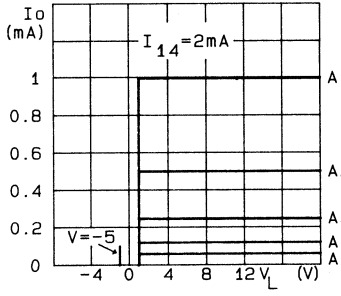


Fig. 6 - Output Voltage Compliance

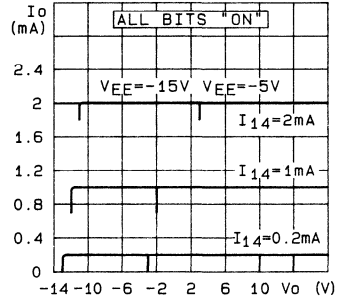


Fig. 7 - Output Voltage Compliance vs Temperature

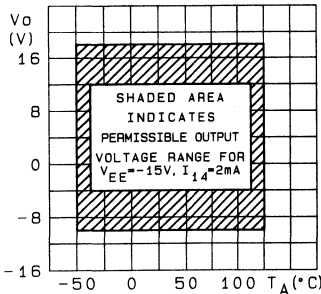
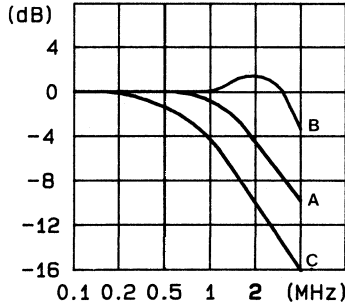


Fig. 8 - Frequency response



Unless otherwise specified: $R_{14} = R_{15} = 1 \text{ k}\Omega$, $C = 15 \text{ pF}$, pin 16 to V_{EE} ; $R_L = 50\Omega$, pin 4 to ground.

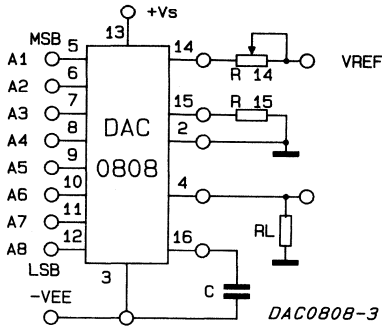
Curve A: Large Signal Bandwidth Method of Figure 7, $V_{REF} = 2 \text{ Vp-p}$ offset 1 V above ground

Curve B: Small Signal Bandwidth Method of Figure 7, $R_L = 250\Omega$, $V_{REF} = 50 \text{ mVp-p}$ offset 200 mV above ground.

Curve C: Large and Small Signal Bandwidth Method of Figure 9 (no op amp. $R_L = 50\Omega$, $R_S = 50\Omega$, $V_{REF} = 2\text{V}$, $V_S = 100 \text{ mVp-p}$ centered at 0V.

Test Circuits

FIGURE 9. Notation Definitions



The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K \left(\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right)$$

$$\text{where } K \equiv \frac{V_{REF}}{R_{14}}$$

and $A_N = "1"$ if A_N is at high level
 $A_N = "0"$ if A_N is at low level

FIGURE 10. Relative Accuracy

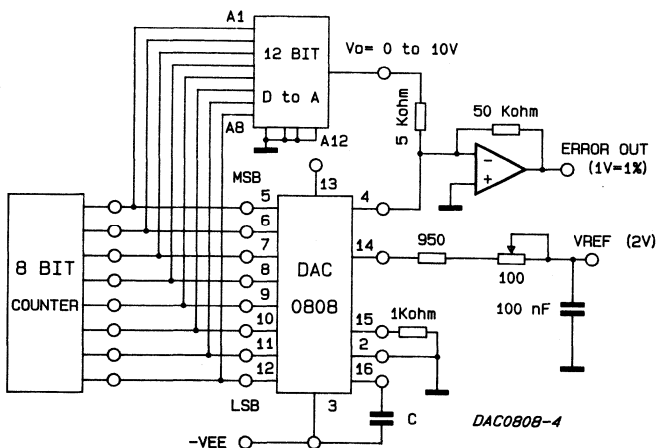


FIGURE 11. Transient Response and Settling Time

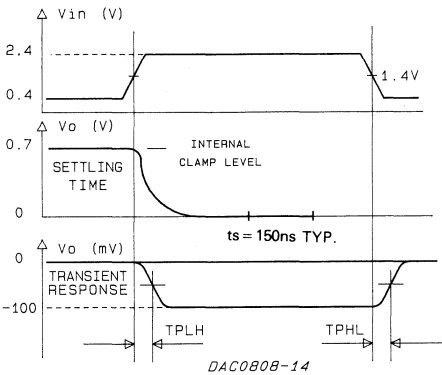
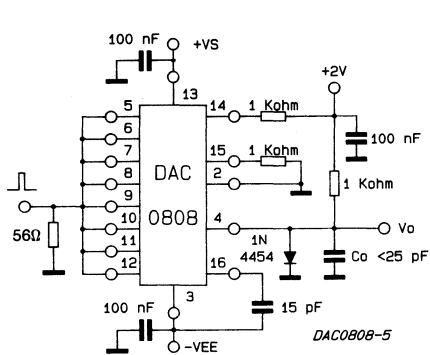


FIGURE 12. Positive V_{REF}

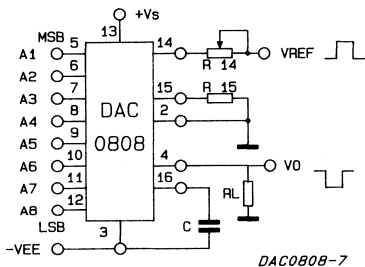


FIGURE 13. Negative V_{REF}

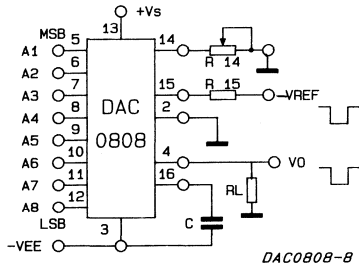
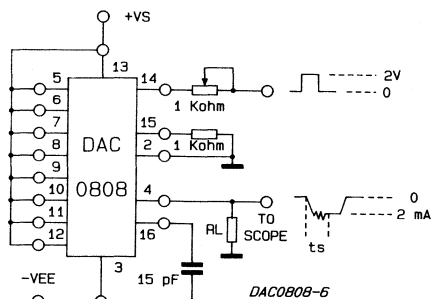


FIGURE 14. Reference Current Slew Rate Measurement



APPLICATION INFORMATION

CIRCUIT DESCRIPTION

The DAC0808 consists of a reference current amplifier, an R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added. The switches are noninverting in operation, therefore a high state on the input turns on the specified output current component. The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching and provides a low impedance termination of equal voltage for all legs of the ladder. The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Nota that there is always a remainder current which is equal to the last significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14} , must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

Connections for a positive voltage are shown in *Figure 12*. The reference voltage source supplies the full current I_{14} . For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 k Ω , minimum capacitor values are 15,37 and 75 pF. The capacitor may be tied to either VEE or ground, but using VEE increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in *Figure 13*. A high input impedance is the main advantage of this method. Compensation involves a capacitor to VEE on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3V above the VEE supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive by pass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1 μ F to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.



**DAC0808
DAC0807
DAC0806**

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of -0.6 to $0.5V$ when $V_{EE} = -5V$ due to the current switching methods employed in the DAC0808.

The negative output voltage compliance of the DAC0808 is extended to $-5V$ where the negative supply voltage is more negative than $-10V$. Using a full-scale current of 1.992 mA and load resistor of $2.5\text{ k}\Omega$ between pin 4 and ground will yield a voltage output of 256 levels between 0 and $-4.980V$. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance, but a $2.5\text{ k}\Omega$ load increases worst-case setting time to $1.2\text{ }\mu\text{s}$ (when all bits are switched ON). Refer to the subsequent text section on Settling Time for more details output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than $-7V$, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

The DAC0808 series is guaranteed accurate to within $\pm 1/2\text{ LSB}$ at a full-scale output current of 1.992 mA . This corresponds to a reference amplifier output current drive to the ladder network of 2 mA , with the loss of 1 LSB ($8\text{ }\mu\text{A}$) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA , allowing some mis-match in the NPN current source pair. The accuracy test circuit is shown in Figure 10. The 12-bit converter is calibrated for a full-scale output current of 1.992 mA . This is an optional step since the DAC0808 accuracy is essentially the same

between 1.5 and 2.5 mA . Then the DAC0808 circuits' full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of $\pm 1/2$ of one part in 65,536, or $\pm 0.00076\%$, which is much more accurate than the $\pm 0.019\%$ specification provided by the DAC0808.

MULTIPLYING ACCURACY

The DAC0808 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from $16\text{ }\mu\text{A}$ to 4 mA , the additional error contributions are less than $1.6\text{ }\mu\text{A}$. This is well within 8-bit accuracy when referred to full-scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC0808 is monotonic for all values of reference current above 0.5 mA . The recommended range for operation with a DC reference current is 0.5 to 4 mA .

SETTLING TIME

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a low-high transition for all bits. This time is typically 150 ns for settling to within $\pm 1/2\text{ LSB}$ for 8-bit accuracy and 100 ns to $1/2\text{ LSB}$ for 7 and 6-bit accuracy. The turn off is typically under 100 ns . These timers apply when $R_L \leq 500\text{ ohms}$ and $C_0 \leq 25\text{ pF}$.

The test circuit of Figure 11 requires a smaller voltage swing for the current switches due to internal voltage clamping in the DAC0808. A $1.0\text{-k}\Omega$ load resistor from pin 4 to ground gives a typical settling time of 200 ns . Thus, it is voltage swing and not the output RC time constant that determines setting time for most applications.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, $100\text{ }\mu\text{F}$ supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTENUATOR

When used in the multiplying mode can be applied as a digital attenuator. See Figure 15. One advantage of this technique is that if $R_S = 50$ ohms, no compensation capacitor is needed. The small and large signal band are now identical and are shown in Figure 8C.

The best frequency response is obtained by not allowing I_{14} to reach zero. However, the high impedance node, pin 16, is clamped to prevent saturation and insure fast recovery when the current through R_{14} goes to zero. R_S can be set for a ± 1.0 mA variation in relation to I_{14} . I_{14} can never be negative. The output current is always unipolar. The quiescent dc output current level changes with the digital word which makes accoupling necessary.

CURRENT TO VOLTAGE CONVERSION

Voltage output of a larger magnitude are obtainable with the circuit of fig. 16 which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the DAC0808 ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and setting time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases over compensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input. The LM301 can be used in a feedforward mode resulting in a full scale setting time on the order of $2.0 \mu s$.

COMBINED OUTPUT AMPLIFIER AND VOLTAGE REFERENCE

For many of its applications the DAC0808 requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular LM723 voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA output cur-

rent. See Figure 17. The reference voltage is developed with respect to the negative voltage and appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its amplifier as a classic current-to-voltage converter with the non-inverting input grounded.

Since $\pm 15V$ and $+5.0V$ are normally available in a combination digital-to-analog system, only the $-5.0V$ need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.

Full scale output may be increasing R_O and raising the $+15V$ supply voltage to $35V$ maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the LM723 C_O may be decreased to maintain the same $R_O C_O$ product if maximum speed is desired.

PROGRAMMABLE POWER SUPPLY

The circuit of figure 17 can be used as a digitally programmed power supply by the addition of thumb-wheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to $+25.5$ volts in 0.1 volt increments, ± 10 mV.

PANEL METER READOUT

The DAC0808 can be used to read out the status of BCD or binary registers or counters a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 20 mA full scale is used. Full scale calibration can be done by adjusting R_{14} or V_{ref} (see fig. 18).

CHARACTER GENERATOR

In a character generation system fig. 19 one DAC0808 circuit uses a fixed reference voltage and its digital input defines the starting point for a stroke. The second converter circuit has a ramp input for the reference and its digital input defines the slope of the stroke. Note that this approach does not result in a 16-bit D-to-A converter (see Accuracy Section).

TWO-DIGIT BCD CONVERSION

Two 8-bit, D-to-A converters can be used to build a two digit BCD D-to-A or A-to-D converter (fig. 21). If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten and thus an DAC0806 may be used for the least significant word.

FIGURE 16.

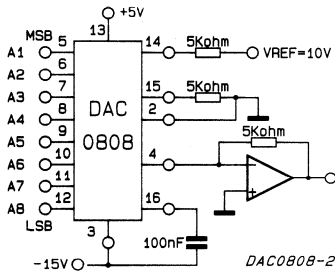
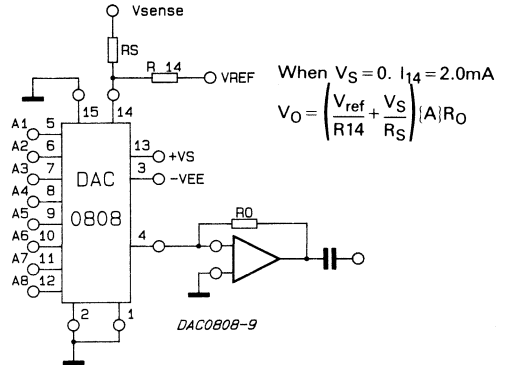


FIGURE 15. Programmable Gain Amplifier or Digital Attenuator Circuit



$$V_0 = 10V \left(\frac{A_1}{2} + \frac{A_2}{4} + \dots + \frac{A_8}{256} \right)$$

FIGURE 17. Combined output amplifier and voltage reference circuit

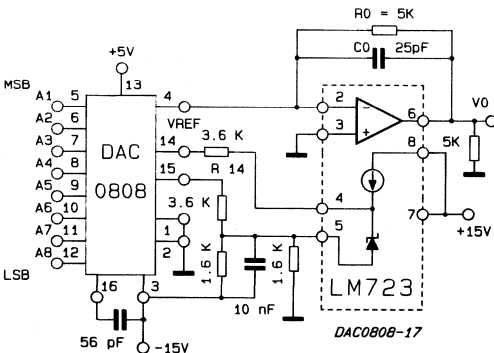


FIGURE 18. Panel meter readout circuit

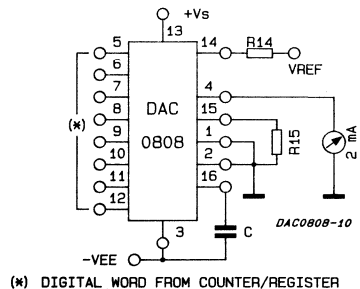
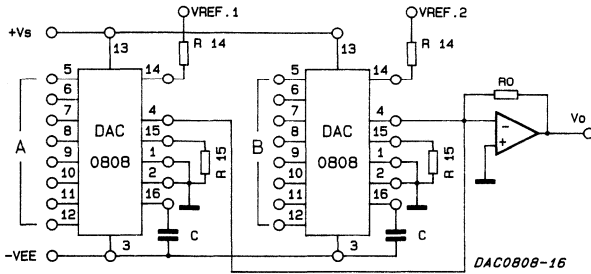


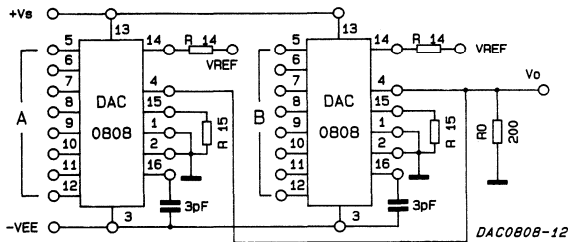
FIGURE 19. Digital summing and character generation



$$V_0 = (I_{O1} + I_{O2}) R_0$$

$$V_0 = \left[\frac{V_{ref1}}{R14_1} \{A\} + \frac{V_{ref2}}{R14_2} \{B\} \right] R_0$$

FIGURE 20. Analog product of two digital words (High Speed Operation)



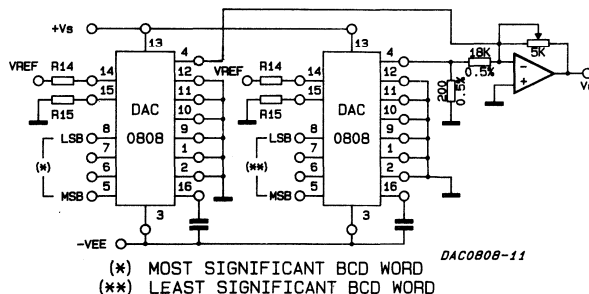
$$V_0 = -I_{O1} R_0 = \frac{V_{ref}}{R14_1} \{A\} R_0$$

$$I_{O2} = \frac{\{B\} |V_0|}{R14_2} = \frac{\{B\}}{R14_2} \left[R_0 \left(\frac{V_{ref}}{R14_1} \right) \{A\} \right]$$

$$\text{Since } R_0 = R14_2 \text{ and } K = \frac{V_{ref}}{R14_1}$$

$$I_{O2} = K \{A\} \{B\} \quad K \text{ can be an analog variable}$$

FIGURE 21. Two-digit BCD conversion



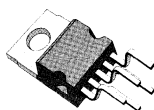
4A LINEAR DRIVER

- HIGH OUTPUT CURRENT (4A PEAK)
- HIGH CURRENT GAIN (10,000 TYP.)
- OPERATION UP TO $\pm 20V$
- THERMAL PROTECTION
- SHORT CIRCUIT PROTECTION
- OPERATION WITHIN SOA
- HIGH SLEW-RATE (30V/ μs)

The L149 is a general purpose power booster in Pentawatt[®] package consisting of a quasi-comp-

lementary darlington output stage with the associated biasing system and inhibit facility.

The device is particularly suited for use with an operational amplifier inside a closed loop configuration to increase output current.



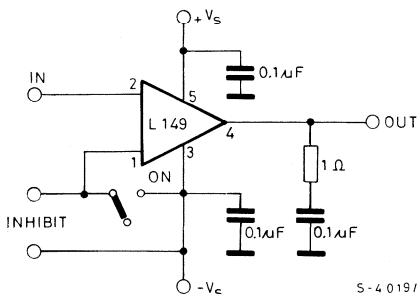
Pentawatt[®]

ORDERING NUMBER: L149V

ABSOLUTE MAXIMUM RATINGS

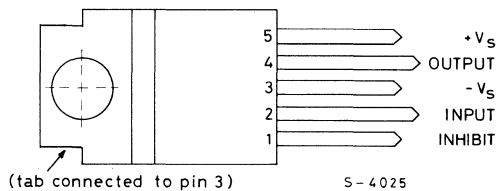
V_s	Supply voltage	± 20	V
V_i	Input voltage	V_s	
$V_5 - V_4$	Upper power transistor V_{CE}	40	V
$V_4 - V_3$	Lower power transistor V_{CE}	40	V
I_o	DC output current	3	A
I_o	Peak output current (internally limited)	4	A
V_{INH}	Input inhibit voltage	$-V_s + 5$	V
		$-V_s - 1.5$	V
P_{tot}	Power dissipation at $T_{case} = 75^\circ C$	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^\circ C$

TEST CIRCUIT

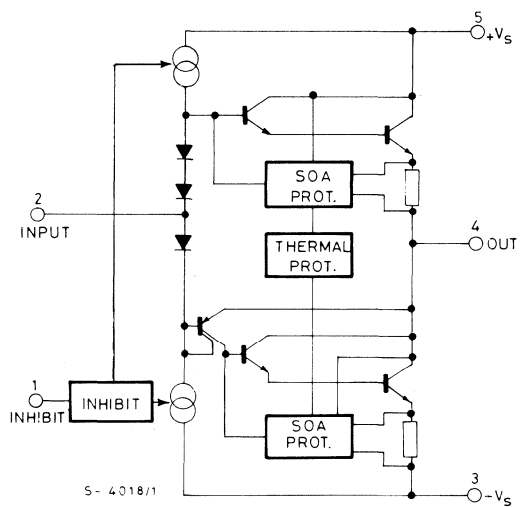


S-4 019/1

CONNECTION DIAGRAM (top view)



SCHEMATIC DIAGRAM



THERMAL DATA

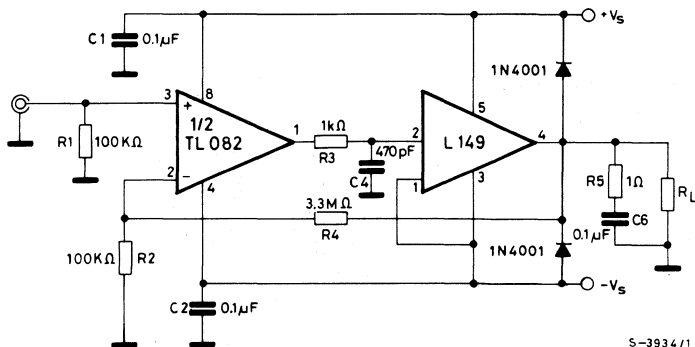
$R_{th \text{ j-case}}$	Thermal resistance junction-case	max	3	$^{\circ}\text{C/W}$
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ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}\text{C}$, $V_s = \pm 16\text{V}$)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s - Supply voltage				± 20	V
I_d Quiescent drain current	$V_s = \pm 16\text{V}$		30		mA
I_{in} Input current	$V_s = \pm 16\text{V}$ $V_i = 0\text{V}$		200	400	μA
h_{FE} DC current gain	$V_s = \pm 16\text{V}$ $I_o = 3\text{A}$	6000	10000		—
G_v Voltage gain	$V_s = \pm 16\text{V}$ $I_o = 1.5\text{A}$		1		—
V_{CEsat} Saturation voltage (for each transistor)	$I_o = 3\text{A}$			3.5	V
V_{os} Input offset voltage	$V_s = \pm 16\text{V}$			0.3	V
V_{INH} Inhibit input voltage (pins 1–3)	ON condition			± 0.3	V
	OFF condition	± 1.8			
R_{INH} Inhibit input resistance			2.0		$\text{K}\Omega$
SR Slew rate			30		$\text{V}/\mu\text{s}$
B Power bandwidth	$V_o = \pm 10\text{V}$, $d = 1\%$, $R_L = 8\Omega$		200		KHz

APPLICATION INFORMATION

Fig. 1 - High slew-rate power operational amplifier ($\text{SR} = 13\text{V}/\mu\text{s}$)



S-3934/1

Fig. 2 - Maximum saturation voltage vs. output current

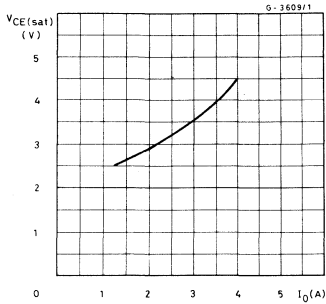


Fig. 3 - Current limiting characteristics

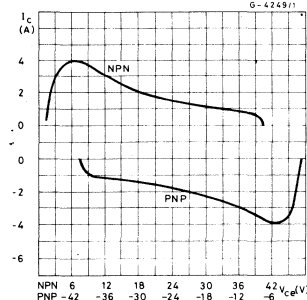


Fig. 4 - Supply voltage rejection vs. frequency

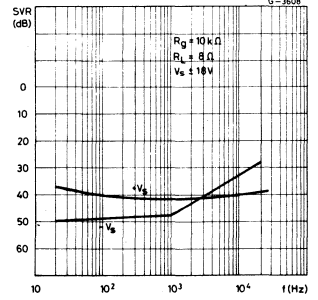


Fig. 5 - Distortion vs. output power (f = 1 KHz)

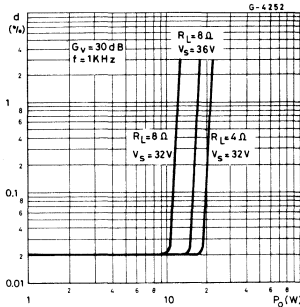


Fig. 6 - Distortion vs. output power (f = 10 KHz)

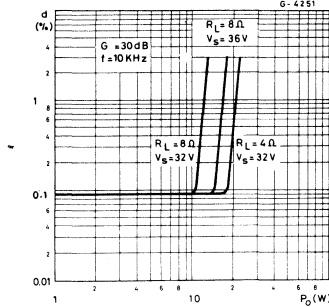


Fig. 7 - Output power vs. supply voltage

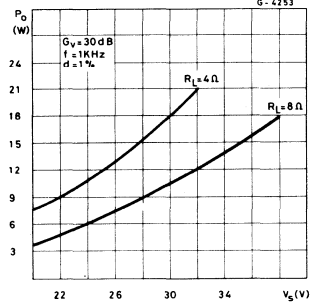
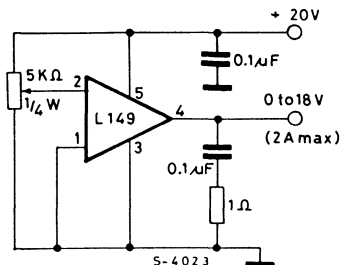


Fig. 8 - Electronic potentiometer (short-circuit protected)





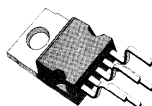
L165

3A POWER OPERATIONAL AMPLIFIER

- OUTPUT CURRENT UP TO 3A
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGES
- SOA PROTECTION
- THERMAL PROTECTION
- $\pm 18V$ SUPPLY

The L165 is a monolithic integrated circuit in Pentawatt[®] package, intended for use as power operational amplifier in a wide range of applications, including servo amplifiers and power sup-

plies. The high gain and high output power capability provide superior performance wherever an operational amplifier/power booster combination is required.



Pentawatt[®]

ORDERING NUMBER: L165V

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
$V_5 - V_4$	Upper power transistor V_{CE}	36	V
$V_4 - V_3$	Lower power transistor V_{CE}	36	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Peak output current (internally limited)	3.5	A
P_{tot}	Power dissipation at $T_{case} = 90^\circ C$	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^\circ C$

APPLICATION CIRCUITS

Fig. 1 - Gain > 10

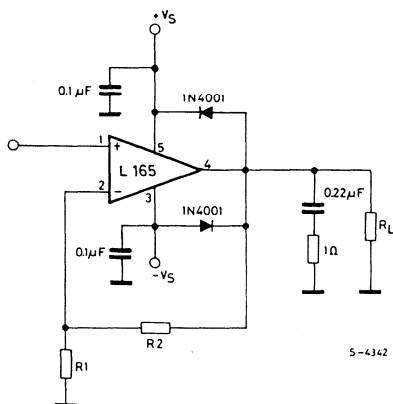
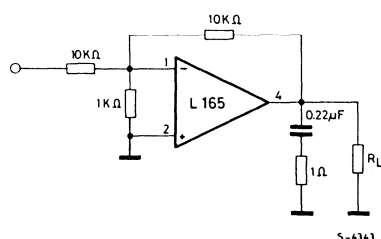
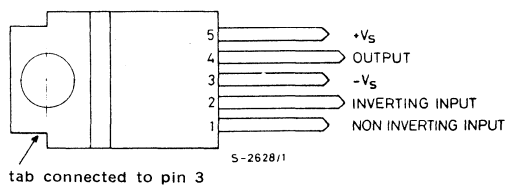


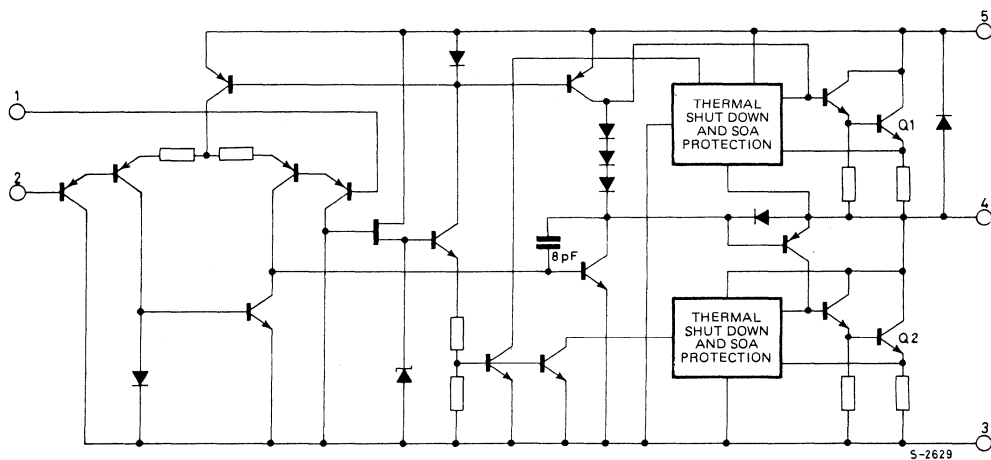
Fig. 2 - Unity gain configuration



CONNECTION DIAGRAM (top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th \text{ j-case}}$ Thermal resistance junction-case

max 3 °C/W

ELECTRICAL CHARACTERISTICS ($V_s = \pm 15V$, $T_j = 25^{\circ}C$ unless otherwise specified)

Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_s Supply voltage			± 6		± 18	V
I_d Quiescent drain current	$V_s = \pm 18V$			40	60	mA
I_b Input bias current				0.2	1	μA
V_{os} Input offset voltage				± 2	± 10	mV
I_{os} Input offset current				± 20	± 200	nA
SR Slew-Rate	$G_v = 10$			8		V/ μs
	$G_v = 1$ (°)			6		
V_o Output voltage swing	$f = 1$ kHz	$I_p = 0.3A$ $I_p = 3A$		27 24		V_{pp}
	$f = 10$ kHz	$I_p = 0.3A$ $I_p = 3A$		27 23		V_{pp}
R_i Input resistance (pin 1)	$f = 1$ KHz		100	500		K Ω
G_v Voltage gain (open loop)				80		dB
e_N Input noise voltage	$B = 10$ to 10 000 Hz			2		μV
i_N Input noise current				100		pA
CMR Common mode rejection	$R_g \leq 10$ K Ω $G_v = 30$ dB			70		dB
SVR Supply voltage rejection	$R_g = 22$ k Ω $V_{ripple} = 0.5 V_{rms}$ $f_{ripple} = 100$ Hz	$G_v = 10$		60		dB
		$G_v = 100$		40		dB
η Efficiency	$f = 1$ kHz $R_L = 4\Omega$	$I_p = 1.6A$; $P_o = 5W$		70		%
		$I_p = 3A$; $P_o = 18W$		60		%
T_{sd} Thermal shut-down case temperature	$P_{tot} = 12W$			110		$^{\circ}C$
	$P_{tot} = 6W$			130		

(°) Circuit of fig. 2

Fig. 3 - Open loop frequency response

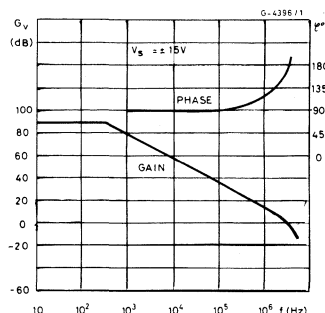


Fig. 4 - Closed-loop frequency response (circuit of fig. 2)

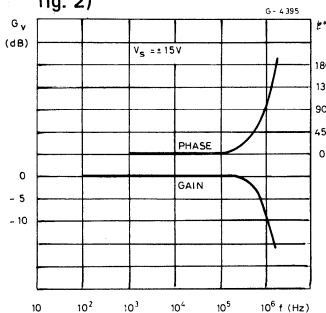


Fig. 5 - Large signal frequency response

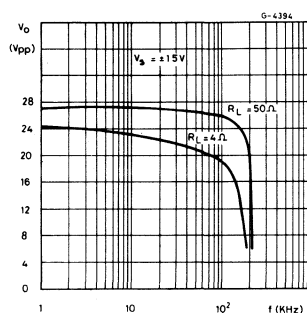


Fig. 6 - Maximum output current vs. voltage $[V_{CE}]$ across each output transistor

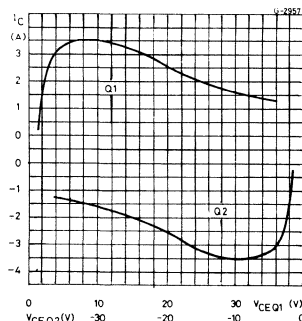


Fig. 7 - Safe operating area and collector characteristics of the protected power transistor

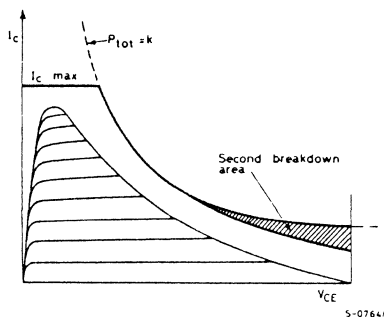


Fig. 8 - Maximum allowable power dissipation vs. ambient temperature

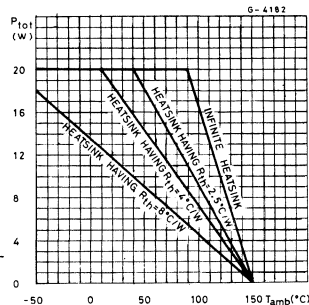
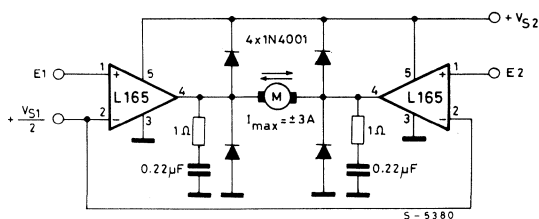


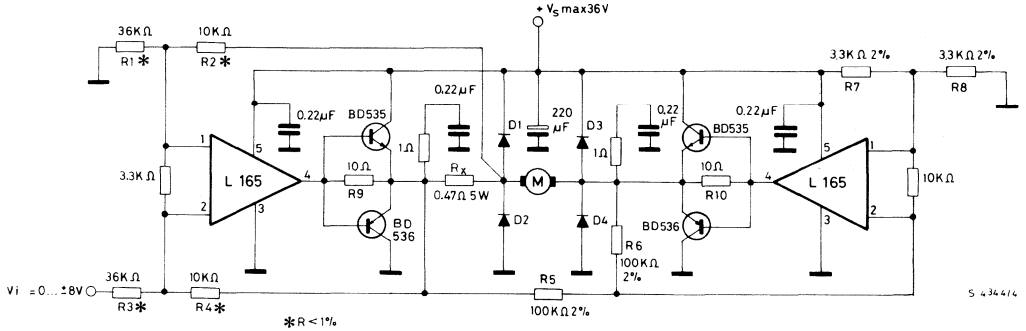
Fig. 9 - Bidirectional DC motor control with TTL/CMOS/ μP compatible inputs



Must be $V_{S2} \geq V_{S1}$

E1, E2 = logic inputs
 V_{S1} = logic supply voltage

Fig. 10 - Motor current control circuit with external power transistors ($I_{\text{motor}} > 3.5\text{A}$)

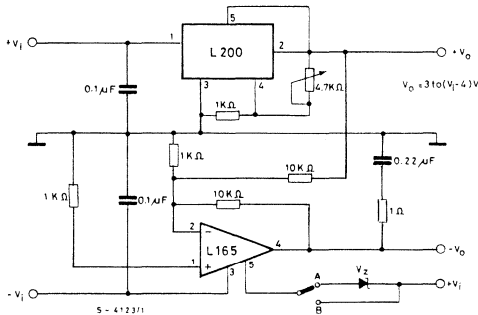


D1 to D4 : $\left\{ \begin{array}{l} V_F \leq 1.2\text{V} @ I = 4\text{A} \\ \text{trr} \leq 500 \text{ ns} \end{array} \right.$

Note: The input voltage level is compatible with L291 (5-BIT D/A converter).

$$\text{The transfer function is : } \frac{I_M}{V_i} = \frac{R_4}{R_x R_3}$$

Fig. 11 - High current tracking regulator

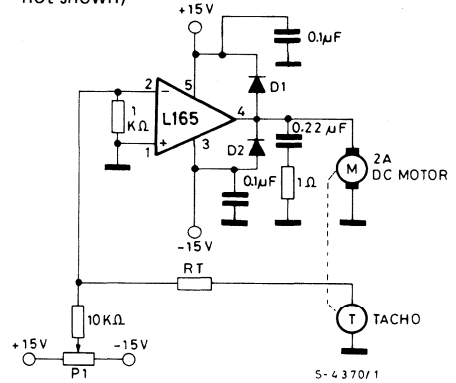


A: for $\pm 18 \leq V_i \leq \pm 32$

Note — V_z must be chosen in order to verify $2 V_i - V_z \leq 36\text{V}$

B: for $V_i \leq \pm 18\text{V}$

Fig. 12 - Bidirectional speed control of DC motor (Compensation networks not shown)



D1, D2 : $\left\{ \begin{array}{l} V_F \leq 1.2\text{V} @ I = 2\text{A} \\ \text{trr} \leq 500 \text{ ns} \end{array} \right.$

Fig. 13 - Split power supply

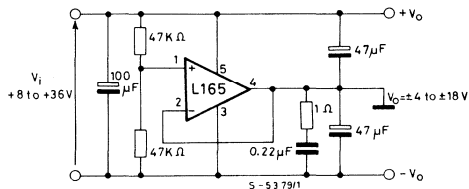
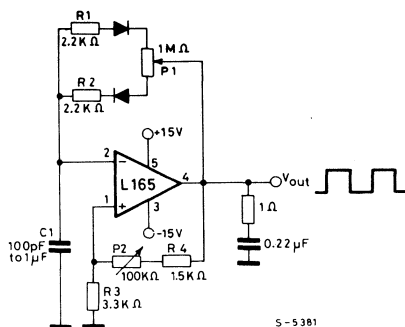


Fig. 14 - Power squarewave oscillator with independent adjustments for frequency and duty-cycle.

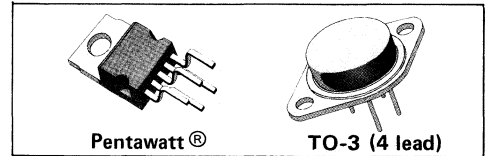


P1 : duty-cycle adjust
P2 : frequency adjust ($f = 700$ Hz with $C1 = 10$ nF, $P2 = 100$ KΩ, $f = 25$ Hz with $C1 = 10$ nF, $P2 = 0$)

ADJUSTABLE VOLTAGE AND CURRENT REGULATOR

- ADJUSTABLE OUTPUT CURRENT UP TO 2A (GUARANTEED UP TO $T_j = 150^\circ\text{C}$)
- ADJUSTABLE OUTPUT VOLTAGE DOWN TO 2.85V
- INPUT OVERVOLTAGE PROTECTION (UP TO 60V, 10ms)
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR S.O.A. PROTECTION
- THERMAL OVERLOAD PROTECTION
- LOW BIAS CURRENT ON REGULATION PIN
- LOW STANDBY CURRENT DRAIN

The L200 is a monolithic integrated circuit for voltage and current programmable regulation. It is available in Pentawatt® package or 4-lead TO-3 metal case. Current limiting, power limiting, thermal shutdown and input overvoltage protection (up to 60V) make the L200 virtually blow-out proof. The L200 can be used to replace fixed voltage regulators when high output voltage precision is required and eliminates the need to stock a range of fixed voltage regulators.



ABSOLUTE MAXIMUM RATINGS

V_i	DC input voltage	40	V
$V_{i\text{ peak}}$	Peak input voltage (10 ms)	60	V
ΔV_{i-o}	Dropout voltage	32	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$
T_{op}	Operating junction temperature for L200C for L200	-25 to 150	$^\circ\text{C}$
		-55 to 150	$^\circ\text{C}$

APPLICATION CIRCUITS

Fig. 1 - Programmable voltage regulator with current limiting

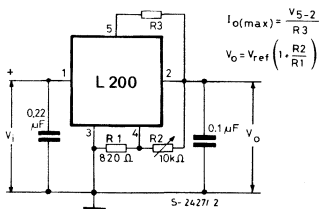
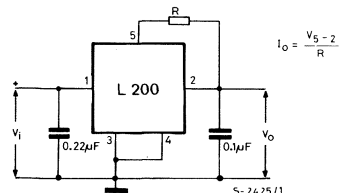


Fig. 2 - Programmable current regulator

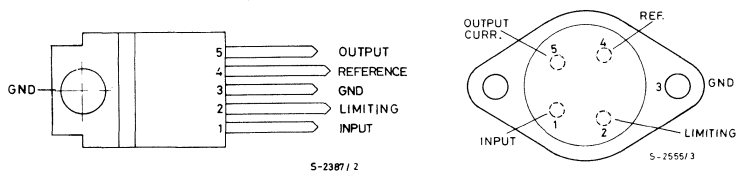




L200

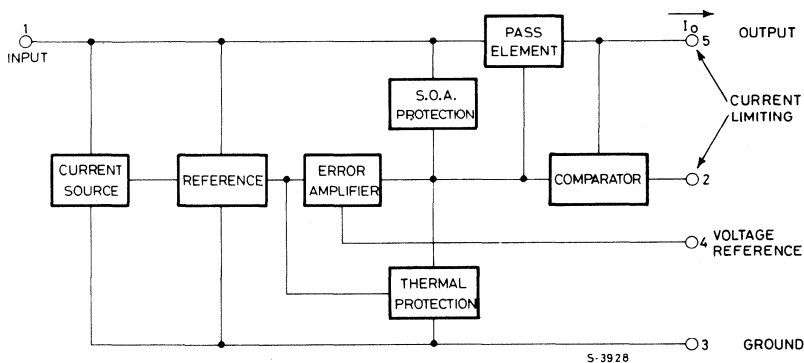
CONNECTION DIAGRAMS AND ORDERING NUMBERS

(top views)



Type	Pentawatt®	TO-3
L 200		L 200 T
L 200 C	L 200 CH L 200 CV	L 200 CT

BLOCK DIAGRAM



THERMAL DATA			TO-3	Pentawatt®
R _{th j-case}	Thermal resistance junction-case	max	4 °C/W	3 °C/W
R _{th j-amb}	Thermal resistance junction-ambient	max	35 °C/W	50 °C/W

Parameter	Test conditions	Min.	Typ.	Max.	Unit
-----------	-----------------	------	------	------	------

I_d	Quiescent drain current (pin 3)	$V_i = 20V$		4.2	9.2	mA
e_N	Output noise voltage	$V_o = V_{ref}$ $B = 1 \text{ MHz}$ $I_o = 10 \text{ mA}$		80		μV
V_o	Output voltage range	$I_o = 10 \text{ mA}$	2.85		36	V
$\frac{\Delta V_o}{V_o}$	Voltage load regulation (note 1)	$\Delta I_o = 2A$ $\Delta I_o = 1.5A$		0.15 0.1	1 0.9	% %
$\frac{\Delta V_i}{\Delta V_o}$	Line regulation	$V_o = 5V$ $V_i = 8 \text{ to } 18V$	48	60		dB
SVR	Supply voltage rejection	$V_o = 5V$ $\Delta V_i = 10 V_{pp}$ $f = 100 \text{ Hz}$ (note 2) $I_o = 500 \text{ mA}$	48	60		dB

**L200****ELECTRICAL CHARACTERISTICS** (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
ΔV_{i-o} Dropout voltage between pins 1 and 5	$I_o = 1.5A$ $\Delta V_o \leq 2\%$		2	2.5	V
V_{ref} Reference voltage (pin 4)	$V_i = 20V$ $I_o = 10\text{ mA}$	2.64	2.77	2.86	V
ΔV_{ref} Average temperature coefficient of reference voltage	$V_i = 20V$ $I_o = 10\text{ mA}$ for $T_j = -25$ to 125°C for $T_j = 125$ to 150°C		-0.25 -1.5		mV/ $^\circ\text{C}$ mV/ $^\circ\text{C}$
I_4 Bias current at pin 4			3	10	μA
$\frac{\Delta I_4}{\Delta T \cdot I_4}$ Average temperature coefficient (pin 4)			-0.5		%/ $^\circ\text{C}$
Z_o Output impedance	$V_i = 10V$ $V_o = V_{ref}$ $I_o = 0.5A$ $f = 100\text{ Hz}$		1.5		m Ω

CURRENT REGULATION LOOP

V_{sc} Current limit sense voltage between pins 5 and 2	$V_i = 10V$ $V_o = V_{ref}$ $I_5 = 100\text{ mA}$	0.38	0.45	0.52	V
$\frac{\Delta V_{sc}}{\Delta T \cdot V_{sc}}$ Average temperature coefficient of V_{sc}			0.03		%/ $^\circ\text{C}$
$\frac{\Delta I_o}{I_o}$ Current load regulation	$V_i = 10V$ $\Delta V_o = 3V$ $I_o = 0.5A$ $I_o = 1A$ $I_o = 1.5A$		1.4 1 0.9		% % %
I_{sc} Peak short circuit current	$V_i - V_o = 14V$ (pins 2 and 5 short circuited)			3.6	A

Note 1): A load step of 2A can be applied provided that input-output differential voltage is lower than 20V (see fig. 3).

Note 2): The same performance can be maintained at higher output levels if a bypassing capacitor is provided between pins 2 and 4.

Fig. 3 - Typical safe operating area protection

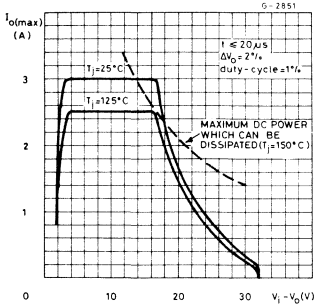


Fig. 4 - Quiescent current vs. supply voltage

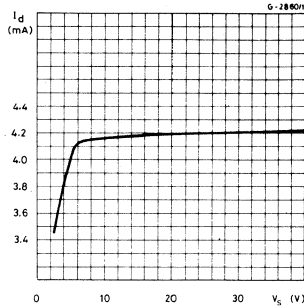


Fig. 5 - Quiescent current vs. junction temperature

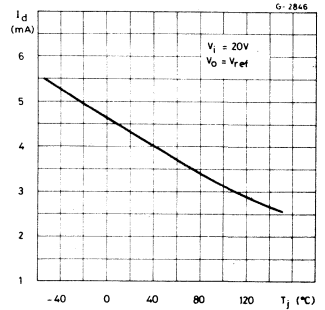


Fig. 6 - Quiescent current vs. output current

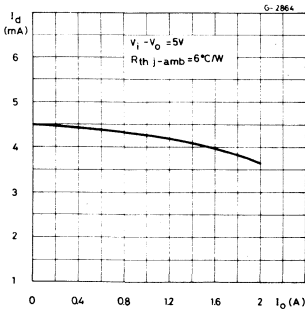


Fig. 7 - Output noise voltage vs. output voltage

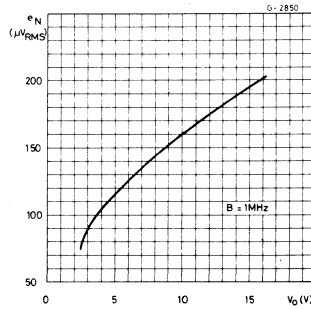


Fig. 8 - Output noise voltage vs. frequency

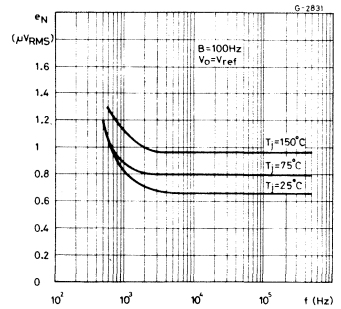


Fig. 9 - Reference voltage vs. junction temperature

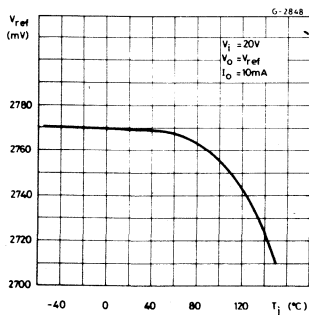


Fig. 10 - Voltage load regulation vs. junction temperature

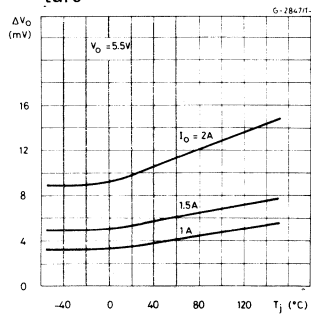


Fig. 11 - Supply voltage rejection vs. frequency

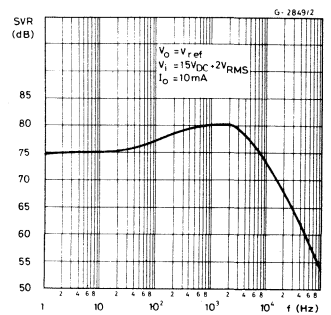


Fig. 12 - Dropout voltage vs. junction temperature

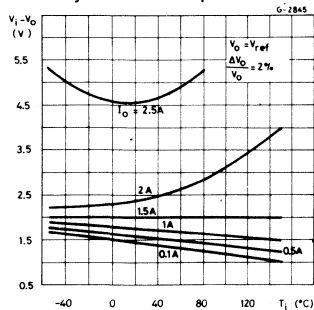


Fig. 13 - Output impedance vs. frequency

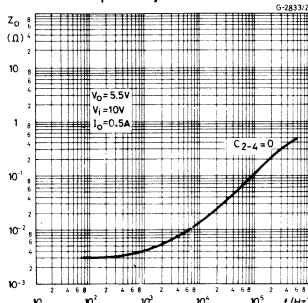


Fig. 14 - Output impedance vs. output current

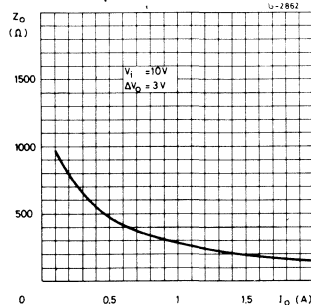


Fig. 15 - Voltage transient response

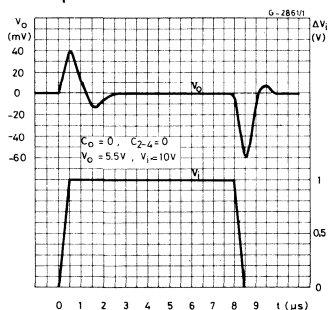


Fig. 16 - Load transient response

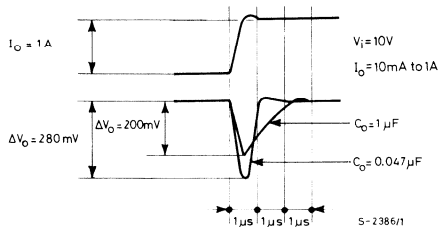


Fig. 17 - Load transient response

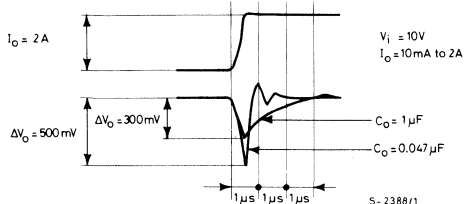
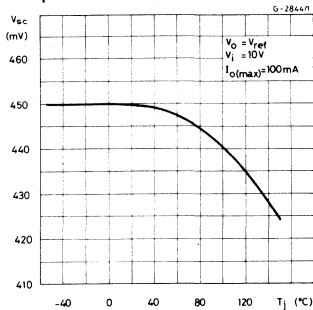


Fig. 18 - Current limit sense voltage vs. junction temperature



APPLICATION CIRCUITS

Fig. 19 - Programmable voltage regulator

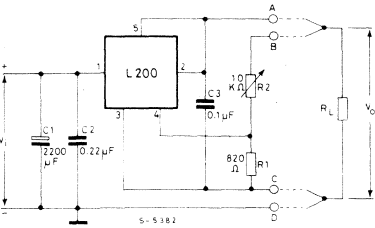


Fig. 20 - P.C. board and components layout of fig. 19. (1 : 1 scale)

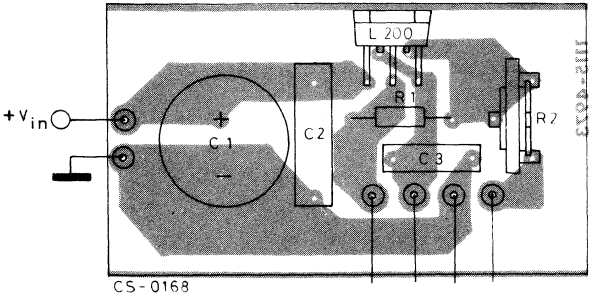


Fig. 21 - High current voltage regulator with short circuit protection

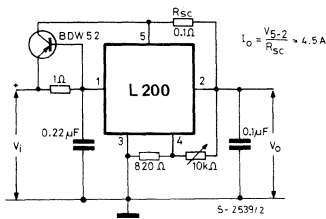


Fig. 22 - Digitally selected regulator with inhibit

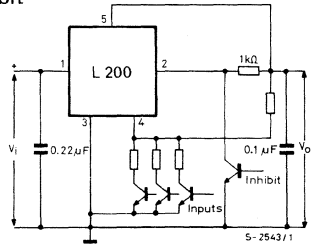
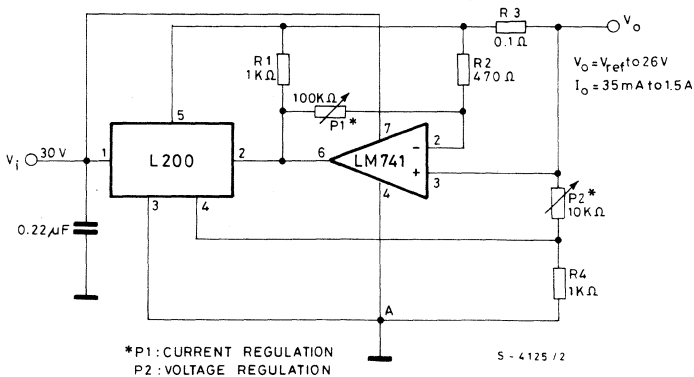


Fig. 23 - Programmable voltage and current regulator



Note: Connecting point A to a negative voltage (for example -3V/10 mA) it is possible to extend the output voltage range down to 0V and to obtain the current limiting down to this level (output short-circuit condition).

APPLICATION CIRCUITS

Fig. 24 - High current regulator with NPN pass transistor

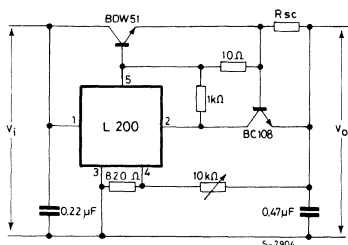
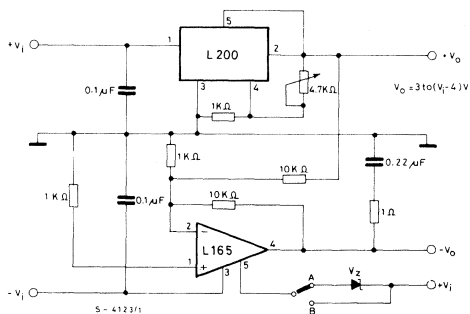


Fig. 25- High current tracking regulator



A: for $\pm 18 \leq V_i \leq \pm 32$

Note – V_z must be chosen in order to verify
 $2 V_i - V_z \leq 36V$

B: for $V_i \leq \pm 18V$

Fig. 26 – High input and output voltage

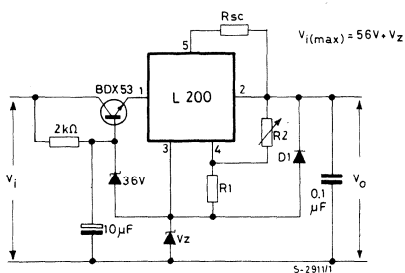
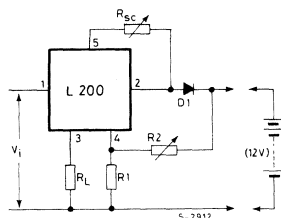


Fig. 27 – Constant current battery charger

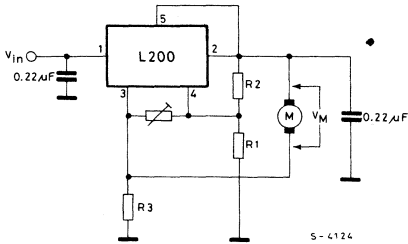


The resistors R_1 and R_2 determine the final charging voltage and R_{sc} the initial charging current. D_1 prevents discharge of the battery throught the regulator.

The resistor R_L limits the reverse currents through the regulator (which should be 100 mA max) when the battery is accidentally reverse connected. If R_L is in series with a bulb of 12V/50 mA rating this will indicate incorrect connection.

APPLICATION CIRCUITS (continued)

Fig. 28 - 30W Motor speed control



$$R_3 = \frac{R_1}{R_2} \cdot R_M$$

$$V_M = V_{ref} \cdot \left(1 + \frac{R_2}{R_1}\right)$$

Fig. 29 - Low turn on

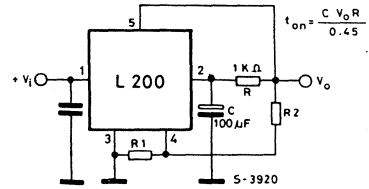
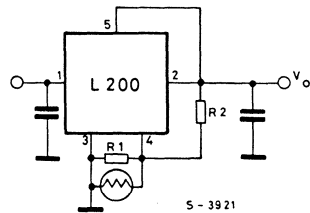


Fig. 30 - Light controller





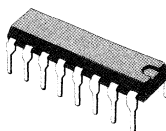
L272 L272M

PRELIMINARY DATA

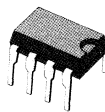
DUAL POWER OPERATIONAL AMPLIFIERS

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



Powerdip 8 + 8



Minidip Plastic

ORDERING NUMBERS:

L272

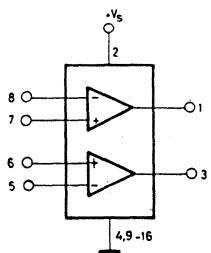
L272M

The L272 and L272M are monolithic integrated circuits in powerdip and minidip packages intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies, compact disc, VCR, etc.

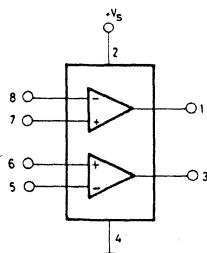
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at $T_{amb} = 80^\circ\text{C}$ (L272), $T_{amb} = 50^\circ\text{C}$ (L272M) $T_{case} = 75^\circ\text{C}$ (L272)	1	W
		5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

BLOCK DIAGRAM



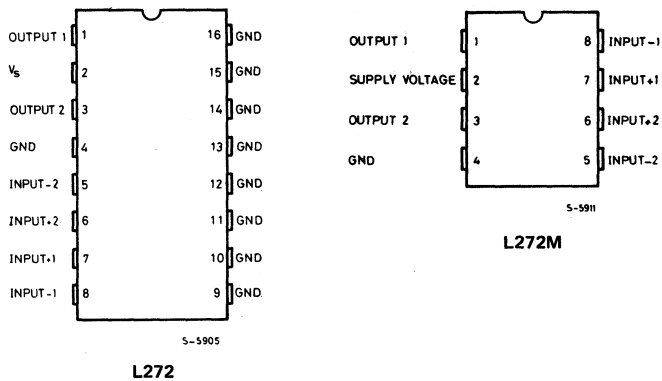
L272



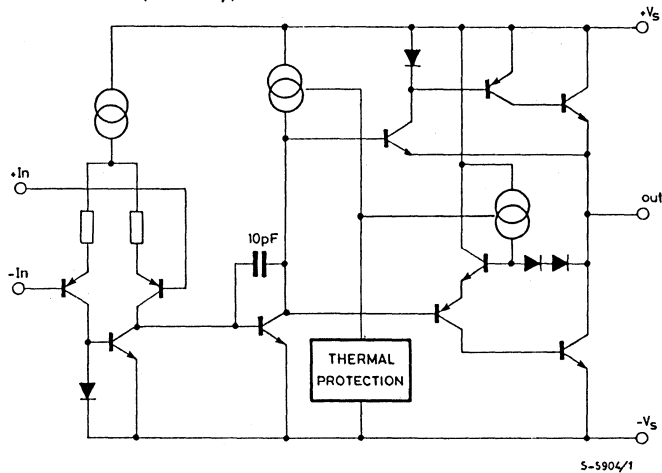
L272M

CONNECTION DIAGRAM

(Top view)



SCHEMATIC DIAGRAM (one only)



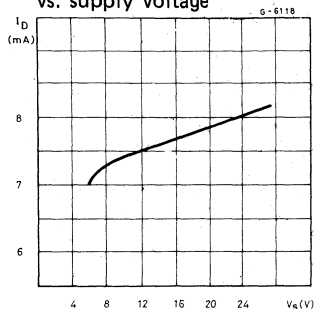
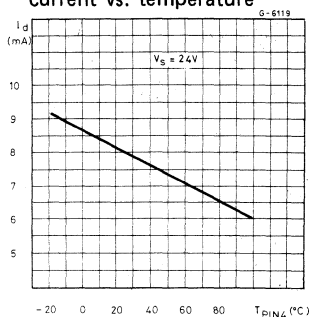
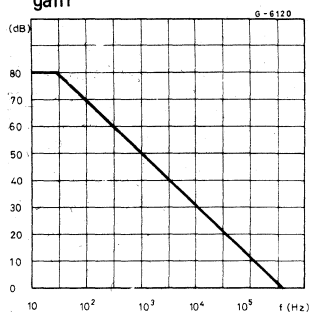
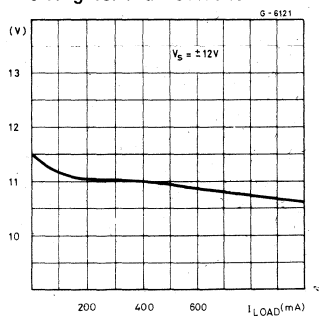
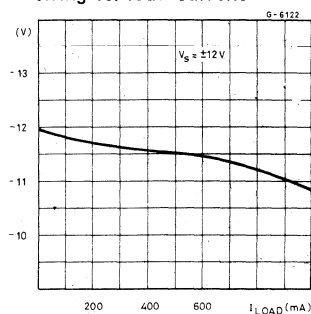
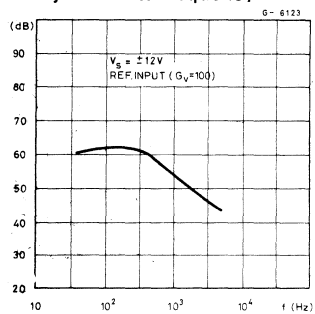
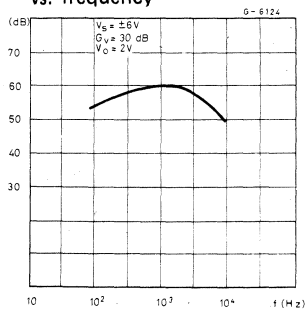
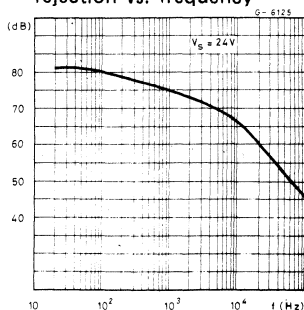
THERMAL DATA			Powerdip	Minidip
R _{th j-case}	Thermal resistance junction-pins	max	15°C/W	* 70°C/W
R _{th j-amb}	Thermal resistance junction-ambient	max	70°C/W	100°C/W
* Thermal resistance junction-pin 4				



L272
L272M

ELECTRICAL CHARACTERISTICS ($V_s = 24V$, $T_{amb} = 25^{\circ}C$ unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V _s	Supply voltage			4		28	V
I _s	Quiescent drain current	V _O = $\frac{V_s}{2}$	V _s = 24V		8	12	mA
			V _s = 12V		7.5	11	mA
I _b	Input bias current				0.3	2.5	μA
V _{OS}	Input offset voltage				15	60	mV
I _{OS}	Input offset current				50	250	mA
SR	Slew rate				1		V/μs
B	Gain-bandwidth product				350		KHz
R _I	Input resistance			500			KΩ
G _V	O.L. voltage gain	f = 100Hz		60	70		dB
		f = 1KHz			50		dB
e _N	Input noise voltage	B = 20KHz			10		μV
I _N	Input noise current	B = 20KHz			200		pA
CRR	Common Mode rejection	f = 1KHz		60	75		dB
SVR	Supply voltage rejection	f = 100Hz R _G = 10KΩ V _R = 0.5V	V _s = 24V V _s = ± 12V V _s = ± 6V	54	70 62 56		dB dB dB
V _O	Output voltage swing	I _p = 0.1A I _p = 0.5A		21	23 22.5		V V
C _s	Channel separation	f = 1KHz; R _L = 10Ω; G _V = 30dB V _s = 24V V _s = ± 6V			60 60		dB dB
d	Distortion	f = 1KHz V _s = 24V	G _V = 30dB R _L = ∞		0.5		%
T _{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

Fig. 2 - Quiescent drain current vs. temperature

Fig. 3 - Open loop voltage gain

Fig. 4 - Output voltage swing vs. load current

Fig. 5 - Output voltage swing vs. load current

Fig. 6 - Supply voltage rejection vs. frequency

Fig. 7 - Channel separation vs. frequency

Fig. 8 - Common mode rejection vs. frequency


APPLICATION SUGGESTION

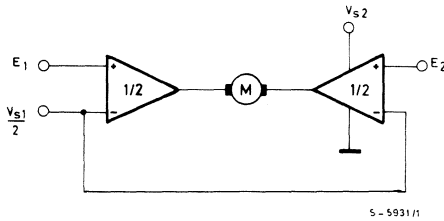
NOTE

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

— layout accuracy;

- A 100nF capacitor connected between supply pins and ground;
- boucherot cell (0.1 to 0.2 μ F + 1 Ω series) between outputs and ground or across the load.

Fig. 9 - Bidirectional DC motor control with μ P compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 10 - Servocontrol for compact-disc

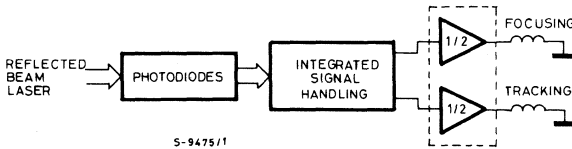


Fig. 11 - Compact-disc motor driver (1/2 section)

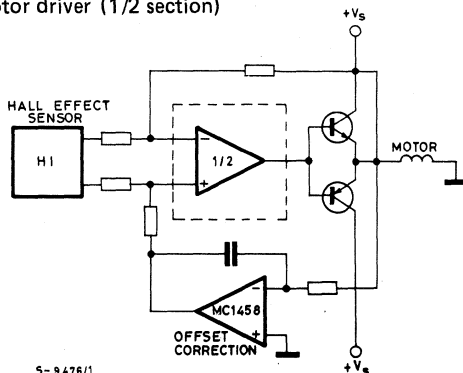


Fig. 12 – Capstan motor control in video recorders

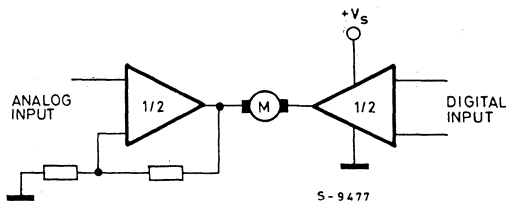
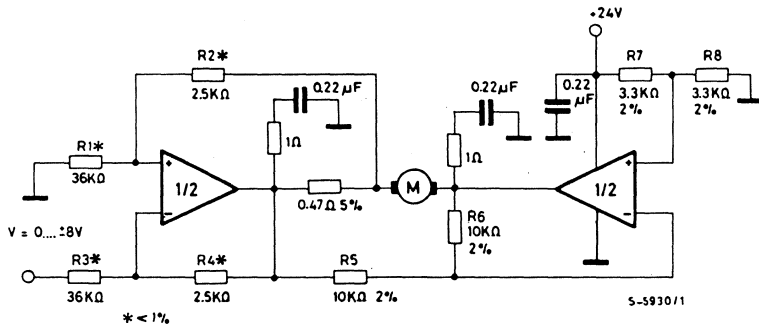


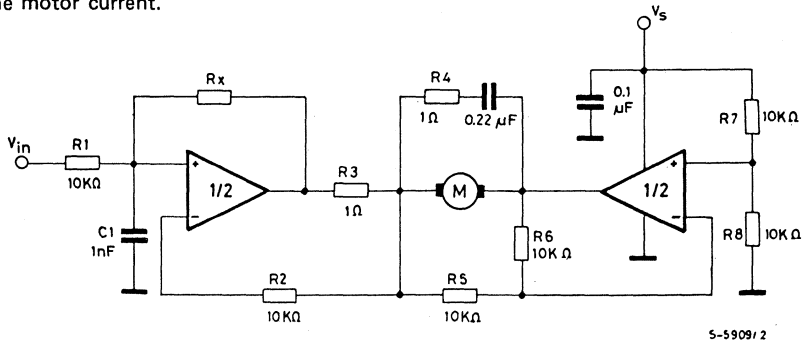
Fig. 13 – Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 14 – Bidirectional speed control of DC motors.

For circuit stability ensure that $R_x > \frac{2R_3 \cdot R_1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2 \left(V_1 - \frac{V_s}{2} \right) + |R_o| \cdot I_M$ where $|R_o| = \frac{2R \cdot R_1}{R_x}$ and I_M is the motor current.





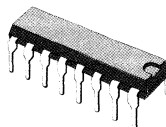
L290

TACHOMETER CONVERTER

The L290, a monolithic LSI circuit a 16-lead dual in-line plastic package, is intended for use with the L291 and L292 which together form a complete **3-chip DC motor positioning system** for applications such as carriage/daisy-wheel position control in typewriters.

The L290/1/2 system can be directly controlled by a microprocessor. The L290 integrates the following functions:

- tachometer generator (F/V converter)
- reference voltage generator
- position pulse generator



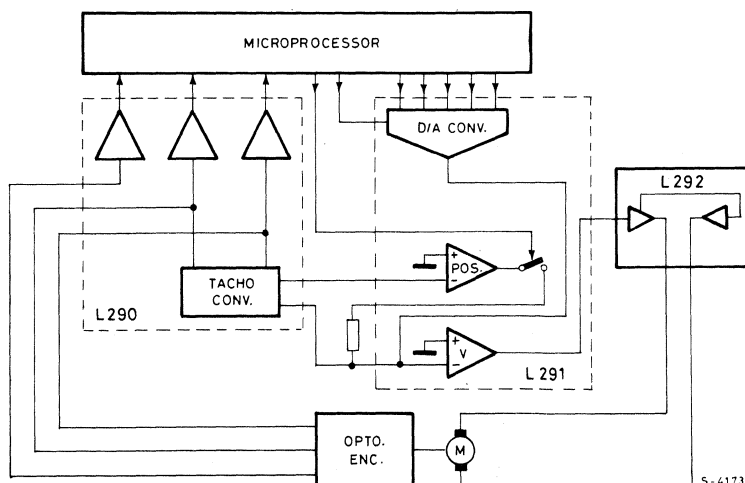
**DIP-16 Plastic
(0.4)**

ORDERING NUMBER: L290B

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 15	V
V_i (FTA, FTB, FTF)	Input signals	± 7	V
P_{tot}	Total power dissipation $T_{amb} = 70^\circ\text{C}$	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to +150	$^\circ\text{C}$

SYSTEM BLOCK DIAGRAM



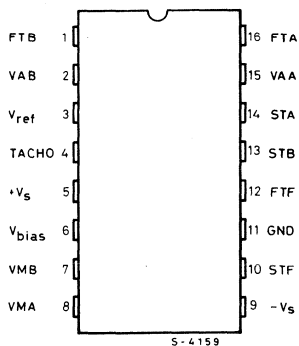
S-4173



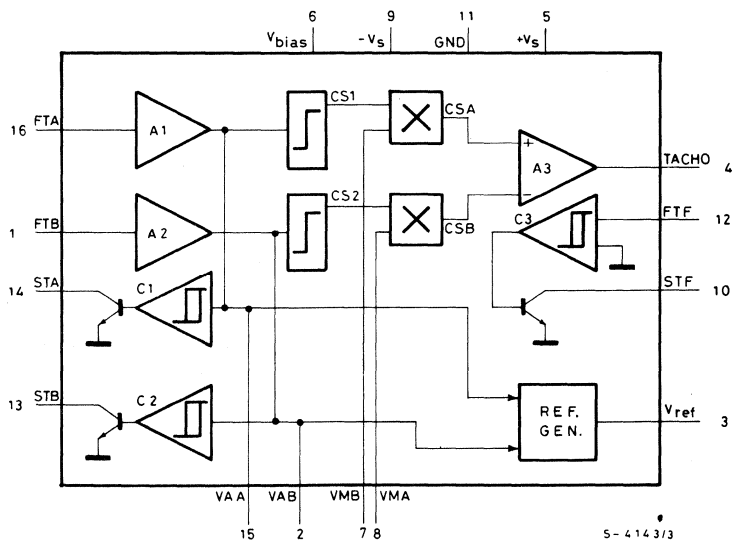
L290

CONNECTION DIAGRAM

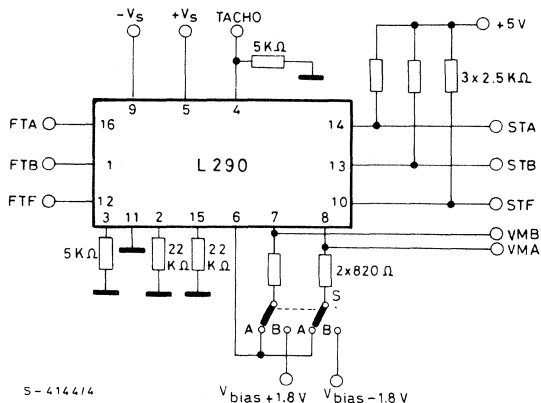
(top view)



BLOCK DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	80	°C/W
-----------------	-------------------------------------	-----	----	------

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, S in (A), $V_s = \pm 12V$, $T_{amb} = 25^\circ C$ unless otherwise specified)

Parameters		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 10		± 15	V
I_d	Quiescent drain current	$V_s = \pm 15V$		13	20	mA

INPUT AMPLIFIERS (A_1 and A_2)

FTA, FTB	Input signal from encoder (pin 1, 16)	$f_{\max} = 20 \text{ KHz}$	± 0.4		± 0.6	V_p
V_{os}	Output offset voltage (pin 2, 15)	FTA = FTB = 0V			± 55	mV
I_b	Input bias current (pin 1, 16)			0.15		μA
G_v	Voltage gain	$f = 10 \text{ KHz}$ FTA=FTB= $\pm 0.6V_p$	22	23	24	dB
V_o	Output voltage swing (pin 2, 15)	FTA= FTB= $\pm 1 V_p$	± 9.5			V

ELECTRICAL CHARACTERISTICS (continued)

Parameters	Test conditions	Min.	Typ.	Max.	Unit
------------	-----------------	------	------	------	------

COMPARATORS WITH HYSTERESIS (C_1 , C_2 and C_3)

$V_{THP}^{(o)}$	Positive Threshold voltage (pin 2, 12, 15)	C_1 and C_2	550		850	mV
		C_3	700		900	mV
$V_{THN}^{(oo)}$	Negative Threshold voltage (pin 2, 12, 15)	C_1 and C_2	55		175	mV
		C_3	570		830	mV
ΔFTF	Threshold Hysteresis	C_3	72		120	mV
V_L	Output voltage (low level) (pin 10, 13, 14)	$I_o = 2 \text{ mA}$ $FTA = FTB = FTF = 0V$		0.2	0.4	V
I_{leak}	(pins 10, 13, 14)	$FTA = FTB = 0.5V$ $V_{CE} = 5V$ $FTF = 1V$			1	μA

REFERENCE GENERATOR

V_{ref}	DC reference voltage (pin 3)	$FTA = FTB = \pm 0.5V_p(*)$ $I_{ref} = 1 \text{ mA}$	4.5	5	5.5	V
I_{ref}	Output current (pin 3)				1.4	mA

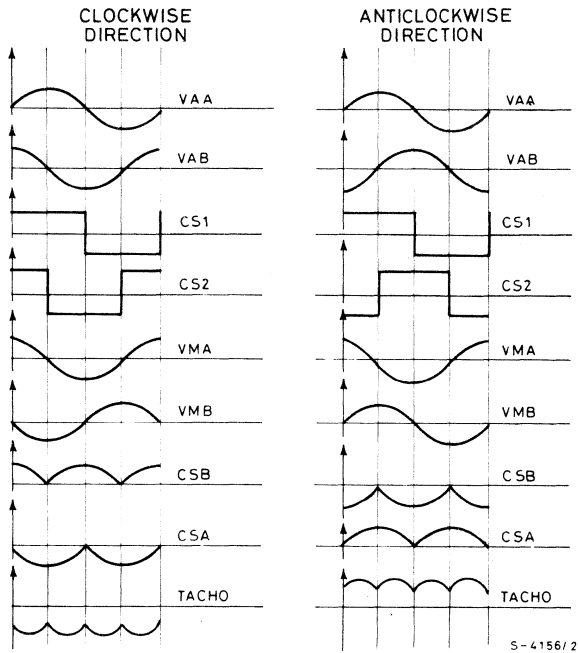
"TACHO" AMPLIFIER (A_3)

V _{os}	Output offset voltage (pin 4)	FTA = ± 15 mV FTB = 0.5V				± 80	mV
V _o	DC output voltage (pin 4)	FTA = FTB = ±0.5V _p	(**) V _{o1}	5.4	6	6.6	V
		V _{MA} = V _{MB} = ±1.25V _p	(***) V _{o2}	-5.4	-6	-6.6	
ΔV _o		V _{o1} + V _{o2}		-150		+150	mV
V _o	Output voltage swing (pin 4)		FTA = FTB = 0.5V	9			V
		S in (B)	FTA = FTB = -0.5V	-9			
V _{MA} V _{MB}	Multiplier input voltage (pin 7, 8)				± 1.25	± 1.7	V _p
V _{bias}	Bias voltage (pin 6)	FTA and FTB floating		-6.5		-8	V

$(^o)$: $FTA = FTB = FTF = 0 \int_0^{1V}$ $(^{oo})$: $FTA = FTB = FTF = 1V \int_0$

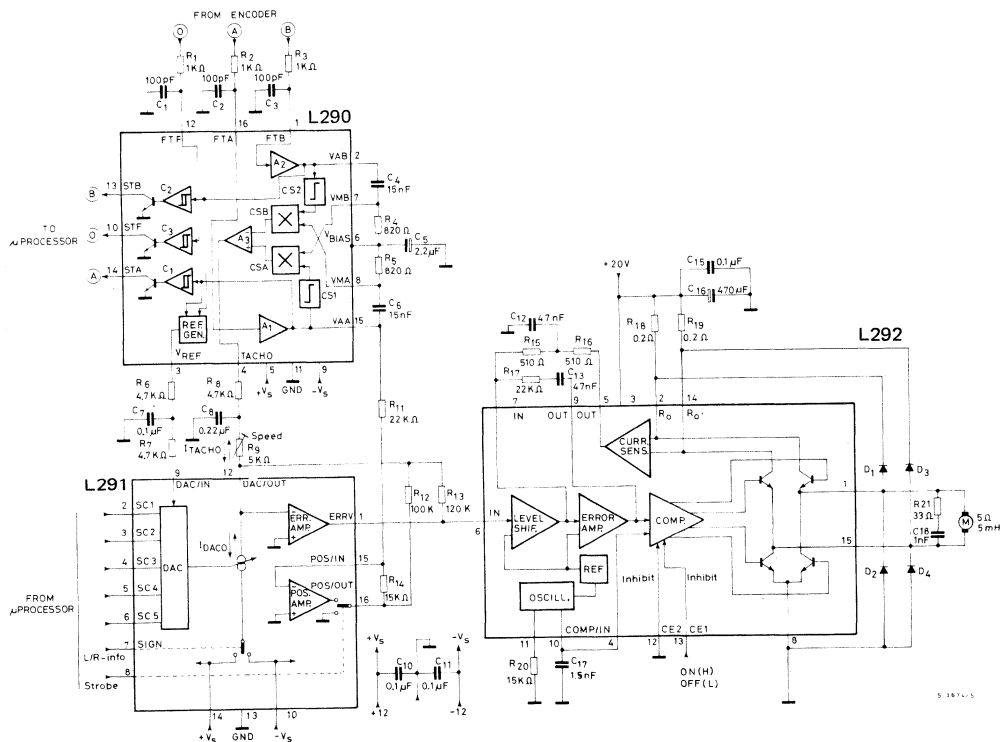
Note : Phase relationship between the signals:

* $FTA : 0^\circ$ $FTB : 90^\circ$
 ** $FTA : 0^\circ$ $FTB : -90^\circ$ $V_{MA} = 90^\circ$ $V_{MB} = 0^\circ$
 *** $FTA : 0^\circ$ $FTB : 90^\circ$ $V_{MA} = 90^\circ$ $V_{MB} = 180^\circ$

WAVEFORMS (Neglecting threshold voltage level of the comparators)


SYSTEM DESCRIPTION : refer to the L292 data sheet

Fig. 1 - Complete application circuit



D1 to D4 : $\left\{ \begin{array}{l} V_F \leq 1.2V @ I = 2A \\ trr \leq 200 ns \end{array} \right.$



L291

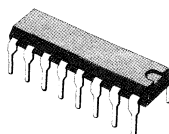
5 BIT - D/A CONVERTER AND POSITION AMPLIFIER

The L291, a monolithic LSI circuit in a 16-lead dual in-line plastic package, is intended for use with the L290 and L292 to form a complete **3 chip DC motor positioning system** for applications such as carriage/daisy-wheel position control in typewriters.

The L290/291/292 system can be directly controlled by a microprocessor.

The L291 integrates the following functions:

- 5 bit D/A converter ($\frac{1}{2}$ LSB max linearity error);
- error amplifier;
- position amplifier.



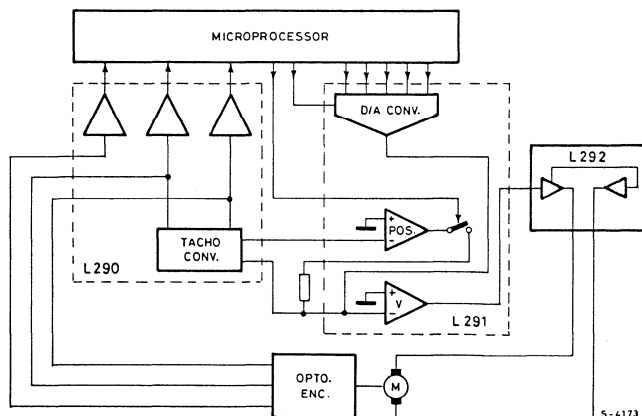
DIP-16 Plastic
(0.4)

ORDERING NUMBER: L291B

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 15	V
P_{tot}	Total power dissipation $T_{amb} = 70^\circ\text{C}$	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

SYSTEM BLOCK DIAGRAM

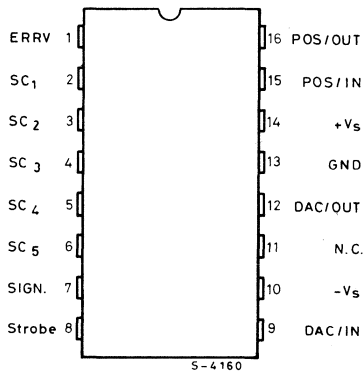




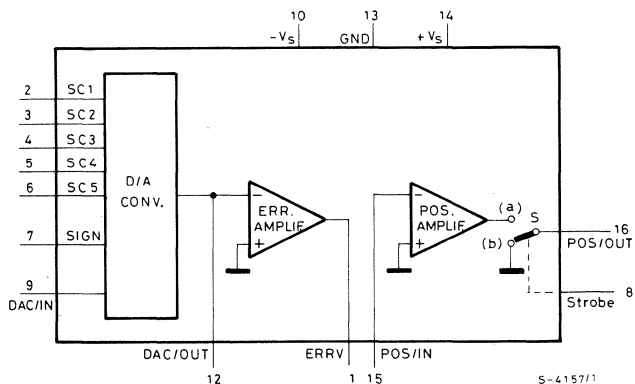
L291

CONNECTION DIAGRAM

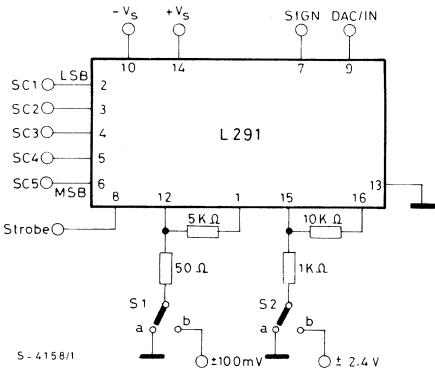
(top view)



BLOCK DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	80	°C/W
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ELECTRICAL CHARACTERISTICS (Refer to the circuit, S1 and S2 in (a), $V_s = \pm 12V$, $T_{amb} = 25^{\circ}C$, unless otherwise specified)

Parameters	Test conditions	Min.	Typ.	Max.	Unit
V_s Supply voltage		± 10		± 15	V
I_d Quiescent drain current			6.5	10	mA

POSITION AMPLIFIER

V_{strobe} Enable voltage level	V_L (S in (a)) *	0		0.8	V
	V_H (S in (b)) *	2.4		$+V_s$	V
V_{os} Output offset voltage (pin 16)	$V_{strobe} = V_L$; $G_v = 20\text{ dB}$			± 50	mV
I_b Input bias current (pin 15)	$V_{strobe} = V_L$			0.3	μA
V_o Output voltage swing (pin 16)	$V_{strobe} = V_L$; S2 in(b); $V_s = \pm 10.8V$	± 9			V
V_R Residual output voltage (pin 16)	$V_{strobe} = V_H$			± 20	mV

* See block diagram and the note for Position Amplifier. 379

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
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D/A CONVERTER

I _{ref}	Current reference input range (pin 9)		0.3		1.2	mA	
V _{os}	Current reference offset voltage (pin 9)	I _{ref} = 0.3 to 1.2 mA All inputs high			± 20	mV	
I _o	Output current range (pin 12)				1.4	mA	
I _o	Output current (pin 12)	I _{ref} = 0.722 mA SC1 to SC5 = L	SIGN = L (I _{o1}) SIGN = H (I _{o2})	-1.358 +1.358	-1.4 +1.4	-1.442 +1.442	mA
ΔI _o	Linearity error	I _{o1} + I _{o2}		-21		+21	μA
		I _{ref} = 0.722 mA				1.61	%FS
I _{os}	Pin 12 output offset current (including Error Amplifier bias current)	All inputs high			± 0.4	μA	
V _L	Low voltage level (digital inputs)	SC1 = LSB SC5 = MSB	0		0.8	V	
V _H	High voltage level (digital inputs)		2.4		+V _S	V	
I _L	Digital inputs current (low state)	V _L = 0.4V			-50	μA	
I _H	Digital inputs current (high state)	V _H = +V _s			1	μA	

ERROR AMPLIFIER

V_{os}	Output offset voltage (pin 1)	$I_{ref} = 0.5$ mA; All inputs high $G_v = 40$ dB			± 200	mV
I_o	Output current (pin 1)				± 5	mA
V_o	Output voltage swing (pin 1)	All inputs high S1 in (b); $R_L = 10$ K Ω	± 7.4		± 8.4	Vp

D/A Converter

The L291 contains a 5-bit D/A converter accepting a binary code and generating a bipolar output current, the polarity of which depends on the SIGN input. The amplitude of the output current is a multiple of a reference current I_{ref} .
The maximum output current is

$$I_{FS} = \pm \frac{31}{16} I_{ref}$$

The following table shows the value of I_o for different input codes. Note that the input bits are active low.

DIGITAL INPUT WORD						Output Current I_o
SIGN	SC5 MSB	SC4	SC3	SC2	SC1 LSB	
L	L	L	L	L	L	$-\frac{31}{16} I_{ref}$
L	H	H	H	H	L	$-\frac{1}{16} I_{ref}$
X	H	H	H	H	H	0
H	H	H	H	H	L	$+\frac{1}{16} I_{ref}$
H	L	L	L	L	L	$+\frac{31}{16} I_{ref}$

X = indifferent
L = low
H = high

This D/A converter has a maximum linearity error equal to $\pm 1/2$ LSB (or $\pm 1.61\%$ Full Scale); that guarantees its monotonicity.

Error Amplifier

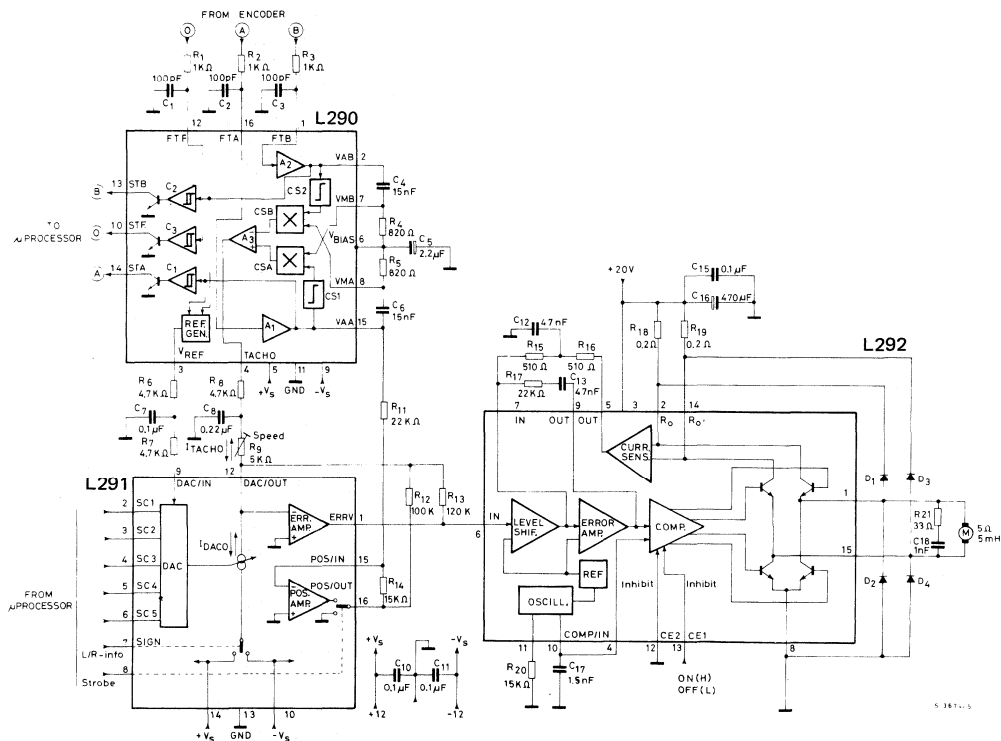
In order to have a good stability, the Error Amplifier must work with a closed loop gain greater or equal than 20 dB.

Position Amplifier

It is inserted by means of the strobe signal, TTL and microprocessor compatible. Its output is connected to pin 16 when $V_{strobe} = \text{Low}$; pin 16 is grounded for $V_{strobe} = \text{High}$.

SYSTEM DESCRIPTION: refer to the L292 data sheet.

Fig. 1 - Complete application circuit



D1 to D4 : $\begin{cases} V_F \leq 1.2V @ I = 2A \\ trr \leq 200 ns \end{cases}$



L292

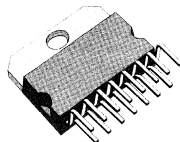
SWITCH-MODE DRIVER FOR DC MOTORS

The L292 is a monolithic LSI circuit in 15-lead Multiwatt[®] package. It is intended for use, together with L290 and L291, as a complete **3-chip motor positioning system** for applications such as carriage/daisy-wheel position control in typewrites.

The L290/1/2 system can be directly controlled by a microprocessor. The outstanding characteristics of the L292 are:

- Driving capability: 2A, 36V, 30KHz
- 2 Logic chip enable
- External loop gain adjustment

- Single power supply (18 to 36V)
- Input signal symmetric to ground
- Thermal protection



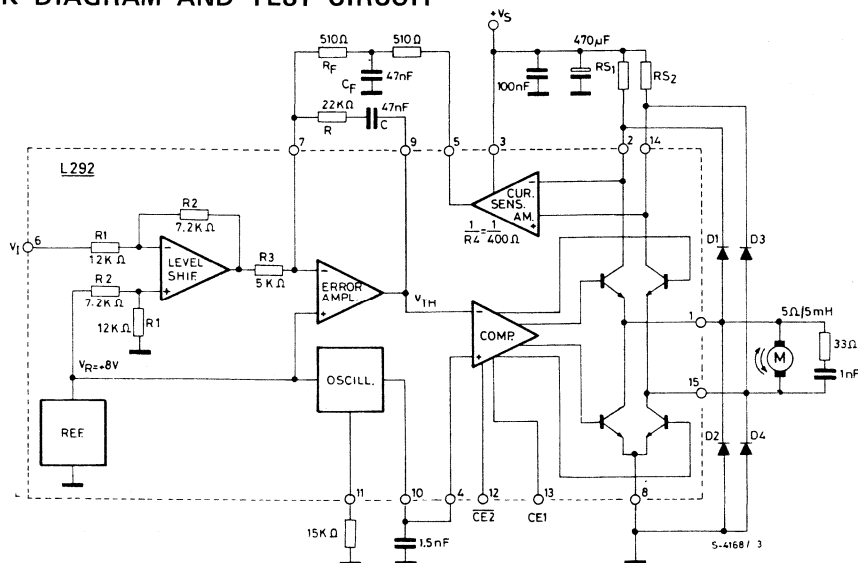
Multiwatt 15

ORDERING NUMBER: L292

ABSOLUTE MAXIMUM RATINGS

V_s	Power supply	36	V
V_i	Input voltage	-15 to $+V_s$	V
$V_{inhibit}$	Inhibit voltage	0 to V_s	V
I_o	Output current	2.5	A
P_{tot}	Total power dissipation ($T_{case} = 75^\circ\text{C}$)	25	W
T_{stg}	Storage and junction temperature	-40 to +150	$^\circ\text{C}$

BLOCK DIAGRAM AND TEST CIRCUIT



D1 · D2 · D3 · D4 = High speed diodes $\left\{ \begin{array}{l} V_F \leq 1.2\text{V @ } I = 2\text{A} \\ t_{rr} \leq 200\text{ ns} \end{array} \right.$

THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max	3	°C/W
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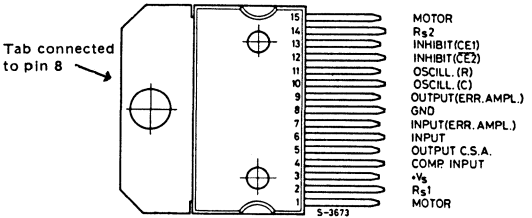
ELECTRICAL CHARACTERISTICS ($V_s = 36V$, $T_{amb} = 25^{\circ}C$, $f_{osc} = 20KHz$ unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		18		36	V
I_d	Quiescent drain current	$V_s = 20V$ (offset null)		30	50	mA
V_{os}	Input offset voltage (pin 6)	$I_o = 0$			±350	mV
$V_{inh.}$	Inhibit low level (pin 12, 13)				2	V
	Inhibit high level (pin 12, 13)		3.2			V
$I_{inh.}$	Low voltage condition	$V_{inh.} (L) = 0.4V$			-100	μA
	High voltage conditions	$V_{inh.} (H) = 3.2V$			10	μA
I_i	Input current (pin 6)	$V_i = -8.8V$ $V_i = +8.8V$			-1.8 0.5	mA mA
V_i	Input voltage (pin 6)	$R_{s1} = R_{s2} = 0.2\Omega$	$I_o = 2A$	9.1		V
			$I_o = -2A$	-9.1		V
I_o	Output current	$V_i = \pm 9.8V$ $R_{s1} = R_{s2} = 0.2\Omega$	± 2			A
$V_{D.}$	Total drop out voltage	(including sensing resistors)	$I_o = 2A$		5	V
			$I_o = 1A$		3,5	V
V_{RS}	Sensing resistor voltage drop	$T_j = 150^{\circ}C$ $I_o = 2A$			0.44	V
$\frac{I_o}{V_i}$	Transconductance	$R_{s1} = R_{s2} = 0.2\Omega$	205	220	235	mA/V
		$R_{s1} = R_{s2} = 0.4\Omega$		120		mA/V
f_{osc}	Frequency range (pin 10)		1		30	KHz

TRUTH TABLE

$V_{inhibit}$		Output stage condition
Pin 12	Pin 13	
L	L	Disabled
L	H	Normal operation
H	L	Disabled
H	H	Disabled

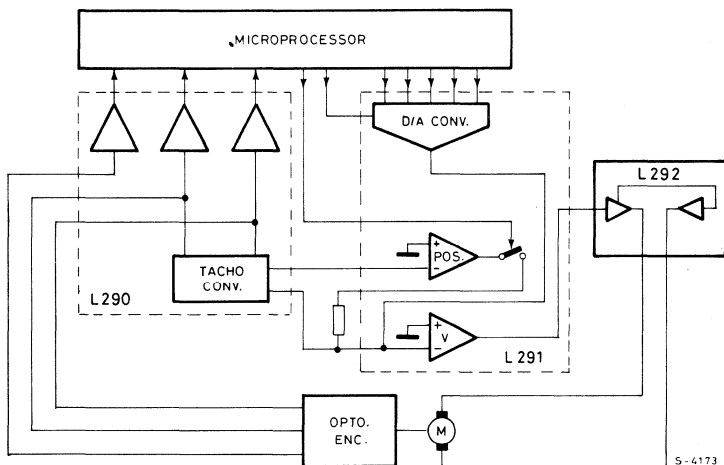
CONNECTION DIAGRAM (top view)



SYSTEM DESCRIPTION

The L290, L291 and L292 are intended to be used as a 3-chip microprocessor controlled positioning system. These devices may be used separately - particularly the L292 motor driver - but since they will usually be used together, a description of a typical L290/1/2 system follows.

Fig. 1 - System block diagram



The system operates in two modes to achieve high-speed, high-accuracy positioning.

Speed commands for the system originate in the microprocessor. It is continuously updated on the motor position by means of pulses from the L290 tachometer chip, which in turn gets its information from the optical encoder. From this basic input, the microprocessor computes a 5-bit control word that sets the system speed dependent on the distance to travel.

When the motor is stopped and the microprocessor orders it to a new position, the system operates initially in an open-loop configuration as there is no feedback from the tachometer generator. Therefore maximum current is fed to the motor. As maximum speed is reached, the tachometer chip output backs off the processor signal thus reducing accelerating torque.

The motor continues to run at top speed but under closed-loop control.

As the target position is approached, the microprocessor lowers the value of the speed-demand word; this reduces the voltage at the main summing point, in effect braking the motor. The braking is applied progressively until the motor is running at minimum speed.

At that time, the microprocessor orders a switch to the position mode, (strobe signal at pin 8 of L291) and within 3 to 4 ms the L292 drives the motor to a null position, where it is held by electronic "detenting".

SYSTEM DESCRIPTION (continued)

The mechanical/electrical interface consists of an optical encoder which generates two sinusoidal signals 90° out of phase (leading or lagging according to the motor direction) and proportional in frequency to the speed of rotation. The optical encoder also provides an output at one position on the disk which is used to set the initial position.

The opto encoder signals, FTA and FTB are filtered by the networks $R_2 C_2$ and $R_3 C_3$ (referring to Fig. 4) and are supplied to the FTA/FTB inputs on the L290.

The main function of the L290 is to implement the following expression:

$$\text{Output signal (TACHO)} = \frac{dV_{AB}}{dt} \cdot \frac{FTA}{|FTA|} - \frac{dV_{AA}}{dt} \cdot \frac{FTB}{|FTB|}$$

Thus the mean value of TACHO is proportional to the rotation speed and its polarity indicates the direction of rotation.

The above function is performed by amplifying the input signals in A_1 and A_2 to obtain V_{AA} and V_{AB} (typ. 7 V_p). From V_{AA} and V_{AB} the external differentiator RC networks $R_5 C_6$ and $R_4 C_4$ give the signals V_{MA} and V_{MB} which are fed to the multipliers.

The second input to each multiplier consists of the sign of the first input of the other multiplier before differentiation, these are obtained using the comparators C_{S1} and C_{S2} . The multiplier outputs, C_{SA} and C_{SB} , are summed by A_3 to give the final output signal TACHO. The peak-to-peak ripple signal of the TACHO can be found from the following expression:

$$V_{\text{ripple p-p}} = \frac{\pi}{4} (\sqrt{2} - 1) \cdot V_{\text{tachoc DC}}$$

The max value of TACHO is:

$$V_{\text{tachoc max}} = \frac{\pi}{4} \sqrt{2} \cdot V_{\text{tachoc DC}}$$

Using the comparators C_1 and C_2 another two signals from V_{AA} and V_{AB} are derived – the logic signals STA and STB.

These signals are used by the microprocessor to determine the position by counting the pulses.

The L290 internal reference voltage is also derived from V_{AA} and V_{AB} :

$$V_{\text{ref}} \equiv |V_{AA}| + |V_{AB}|$$

This reference is used by the D/A converter in the L291 to compensate for variations in input levels, temperature changes and ageing.

The "one pulse per rotation" opto encoder output is connected to pin 12 of the L290 (FTF) where it is squared to give the STF logic output for the microprocessor.

The TACHO signal and V_{ref} are sent to the L291 via filter networks $R_8 C_8 R_9$ and $R_6 C_7 R_7$ respectively. Pin 12 of this chip is the main summing point of the system where TACHO and the D/A converter output are compared.

The input to the D/A converter consists of 5 bit word plus a sign bit supplied by the microprocessor. The sign bit represents the direction of motor rotation. The (analogue) output of the D/A converter – DAC/OUT – is compared with the TACHO signal and the resulting error signal is amplified by the error amplifier, and subsequently appears on pin 1.

SYSTEM DESCRIPTION (continued)

The ERRV signal (from pin 1, L291) is fed to pin 6 of the final chip, the L292 H-bridge motor-driver. This input signal is bidirectional so it must be converted to a positive signal because the L292 uses a single supply voltage. This is accomplished by the first stage - the level shifter, which uses an internally generated 8V reference.

This same reference voltage supplies the triangle wave oscillator whose frequency is fixed by the external RC network (R_{20} , C_{17} - pins 11 and 10) where:

$$f_{osc} = \frac{1}{2RC} \quad (\text{with } R \geq 8.2 \text{ K}\Omega)$$

The oscillator determines the switching frequency of the output stage and should be in the range 1 to 30 KHz.

Motor current is regulated by an internal loop in the L292 which is performed by the resistors R_{18} , R_{19} and the differential current sense amplifier, the output of which is filtered by an external RC network and fed back to the error amplifier.

The choice of the external components in these RC network (pins 5, 7, 9) is determined by the motor type and the bandwidth requirements. The values shown in the diagram are for a 5 Ω , 5 mH motor. (See L292 Transfer Function Calculation in Application Information).

The error signal obtained by the addition of the input and the current feedback signals (pin 7) is used to pulse width modulate the oscillator signal by means of the comparator. The pulse width modulated signal controls the duty cycle of the H-bridge to give an output current corresponding to the L292 input signal.

The interval between one side of the bridge switching off and the other switching on, τ , is programmed by C_{17} in conjunction with an internal resistor R_{τ} .

This can be found from:

$$\tau = R_{\tau} \cdot C_{pin\ 10} \quad (C_{17} \text{ in the diagram})$$

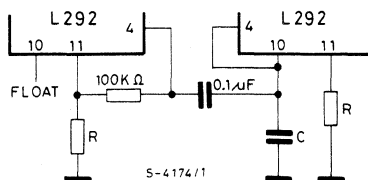
Since R_{τ} is approximately 1.5 K Ω and the recommended τ to avoid simultaneous conduction is 2.5 μ s $C_{pin\ 10}$ should be around 1.5 nF.

The current sense resistors R_{18} and R_{19} should be high precision types (maximum tolerance $\pm 2\%$) and the recommended value is given by:

$$R_{max} \cdot I_{o\ max} \leq 0.44V$$

It is possible to synchronize two L292's, if desired, using the network shown in fig. 2.

Fig. 2



Finally, two enable inputs are provided on the L292 (pins 12 and 13-active low and high respectively).

SYSTEM DESCRIPTION (continued)

Thus the output stage may be inhibited by taking pin 12 high or by taking pin 13 low. The output will also be inhibited if the supply voltage falls below 18V.

The enable inputs were implemented in this way because they are intended to be driven directly by a microprocessor. Currently available microprocessors may generate spikes as high as 1.5V during power-up. These inputs may be used for a variety of applications such as motor inhibit during reset of the logical system and power-on reset (see fig. 3).

Fig. 3

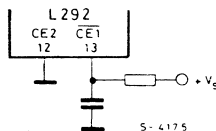
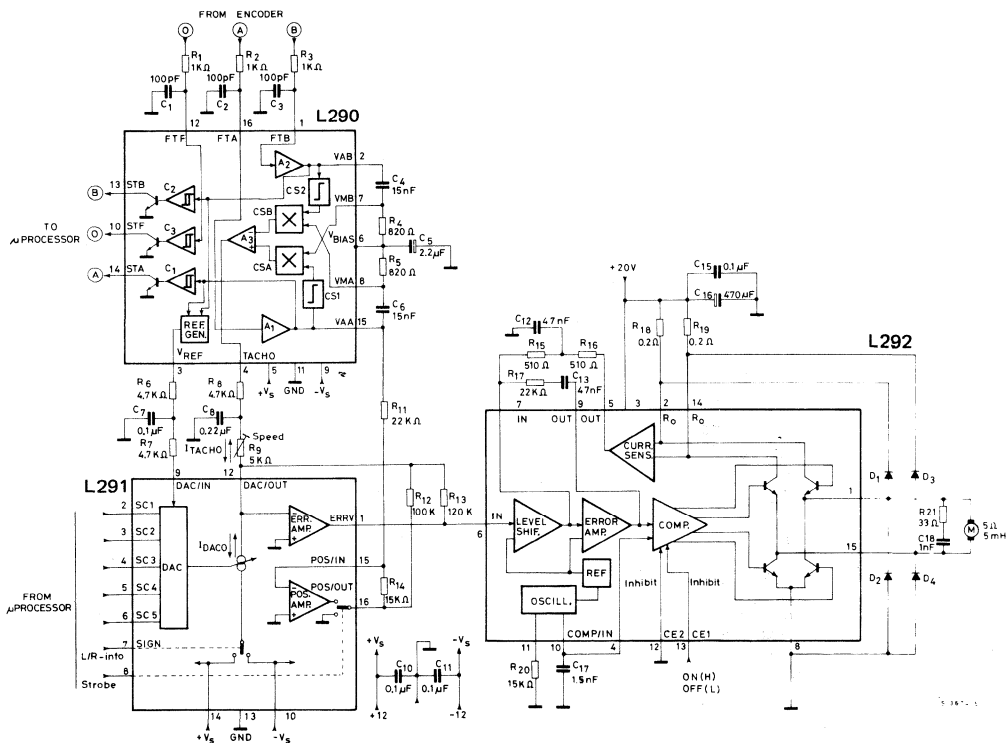


Fig. 4 - Application circuit

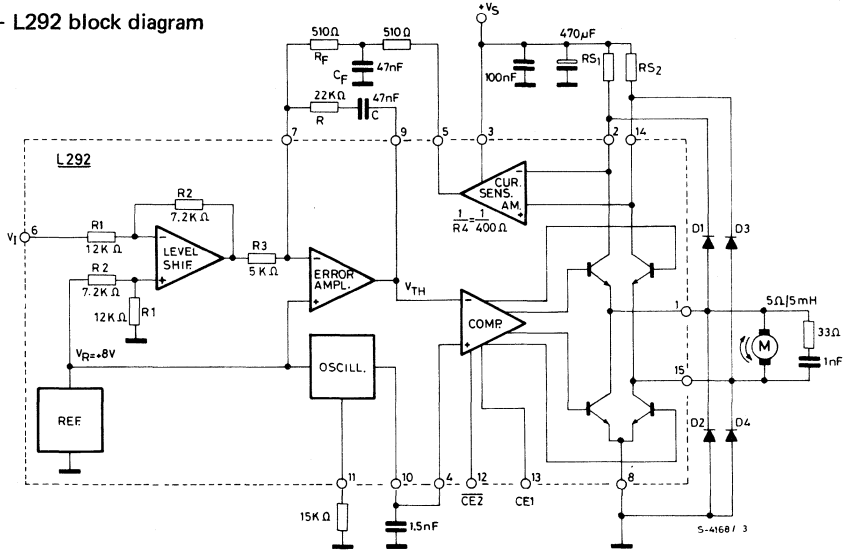


D1 to D4 : $\begin{cases} V_F \leq 1.2V @ I = 2A \\ t_{rr} \leq 200 ns \end{cases}$

APPLICATION INFORMATION

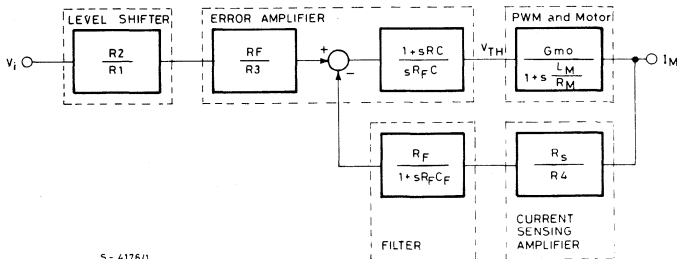
This section has been added in order to help the designer for the best choice of the values of external components.

Fig. 5 - L292 block diagram



The schematic diagram used for the Laplace analysis of the system is shown in fig. 6.

Fig. 6



$R_{S1} = R_{S2} = R_S$ (sensing resistors)

$\frac{1}{R_4} = 2.5 \cdot 10^{-3} \Omega$ (current sensing amplifier transconductance)

L_M = Motor inductance

R_M = Motor resistance

I_M = Motor current

$G_{mo} = \frac{I_M}{V_{TH}} \Big|_{s=0}$ (DC transfer function from the input of the comparator (V_{TH}) to the motor current (I_M)).

APPLICATION INFORMATION (continued)

Neglecting the V_{CEsat} of the bridge transistors and the V_{BE} of the diodes:

$$G_{mo} = \frac{1}{R_M} \frac{2 V_s}{V_R} \quad \text{where: } V_s = \text{supply voltage} \quad (1)$$

$$V_R = 8V \text{ (reference voltage)}$$

DC transfer function

In order to be sure that the current loop is stable the following condition is imposed:

$$1 + sRC = 1 + s \frac{L_M}{R_M} \quad (\text{pole cancellation}) \quad (2)$$

$$\text{from which } RC = \frac{L_M}{R_M} \quad (\text{Note that in practice } R \text{ must be greater than } 5.6 \text{ K}\Omega)$$

The transfer function is then,

$$\frac{I_M}{V_I}(s) = \frac{R_2 R_4}{R_1 R_3} G_{mo} \frac{1 + s R_F C_F}{G_{mo} R_s + s R_4 C + s^2 R_F C_F R_4 C} \quad (3)$$

In DC condition, this is reduced to

$$\frac{I_M}{V_I}(0) = \frac{R_2 R_4}{R_1 R_3} \cdot \frac{1}{R_s} = \frac{0.044}{R_s} \left[\frac{A}{V} \right] \quad (4)$$

Open-loop gain and stability criterion

For $RC = L_M/R_M$, the open loop gain is:

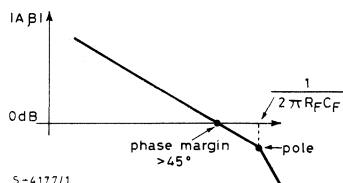
$$A\beta = \frac{1}{s R_F C} \cdot G_{mo} \frac{R_s}{R_4} \frac{R_F}{1 + s R_F C_F} = \frac{G_{mo} R_s}{R_4 C} \frac{1}{s (1 + s R_F C_F)} \quad (5)$$

In order to achieve good stability, the phase margin must be greater than 45° when $|A\beta| = 1$.

That means that, at $f_F = \frac{1}{2\pi R_F C_F}$, must be $|A\beta| < 1$ (see fig. 7), that is

$$|A\beta|_{f = \frac{1}{2\pi R_F C_F}} = \frac{G_{mo} R_s}{R_4 C} \frac{R_F C_F}{\sqrt{2}} < 1 \quad (6)$$

Fig. 7 - Open-loop frequency response



APPLICATION INFORMATION (continued)

Closed-loop system step response

a) Small-signals analysis.

The transfer function (3) can be written as follows:

$$\frac{I_M}{V_i}(s) = \frac{0.044}{R_s} \frac{1 + \frac{s}{2\xi\omega_o}}{1 + \frac{2\xi s}{\omega_o} + \frac{s^2}{\omega_o^2}} \quad (7)$$

where: $\omega_o = \sqrt{\frac{G_{mo} R_s}{R_4 C R_F C_F}}$ is the cutoff frequency

$\xi = \sqrt{\frac{R_4 C}{4 R_F C_F G_{mo} R_s}}$ is the dumping factor

By choosing the ξ value, it is possible to determine the system response to an input step signal. Examples:

1) $\xi = 1$ from which

$$I_M(t) = \frac{0.044}{R_s} \left[1 - e^{-\frac{t}{2R_F C_F}} \left(1 + \frac{t}{4R_F C_F} \right) \right] \cdot V_i$$

(where V_i is the amplitude of the input step).

2) $\xi = \frac{1}{\sqrt{2}}$ from which

$$I_M(t) = \frac{0.044}{R_s} \left(1 - \cos \frac{t}{2R_F C_F} e^{-\frac{t}{2R_F C_F}} \right) \cdot V_i$$

From fig. 9, it is possible to verify that the L292 works in "closed-loop" conditions during the entire motor current rise-time: the voltage at pin 7 (inverting input of the error amplifier) is locked to the reference voltage V_R , present at the non-inverting input of the same amplifier.

The previous linear analysis is correct for this example.

Decreasing the ξ value, the rise-time of the current decreases. But for a good stability, from relationship (6), the minimum value of ξ is:

$$\xi_{min} = \frac{1}{2\sqrt{2}}$$

(phase margin = 45°)

Fig. 8 - Small signal step response (normalized amplitude vs. $t/R_F C_F$)

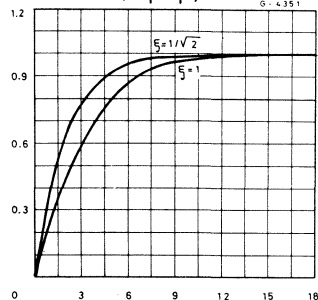
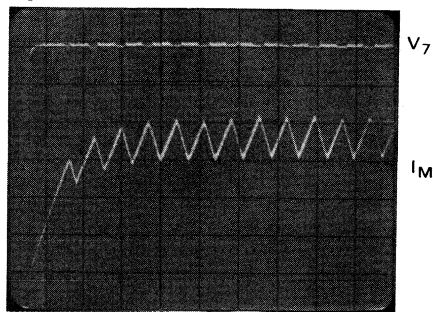


Fig. 9 - Motor current and pin 7 voltage waveforms (application of fig. 5). Small signal response



$V_7 = 200\text{mV/div.}$
 $I_M = 100\text{mA/div.}$
 $t = 100\mu\text{s/div.}$
 with $V_i = 1.5\text{Vp.}$

APPLICATION INFORMATION (continued)

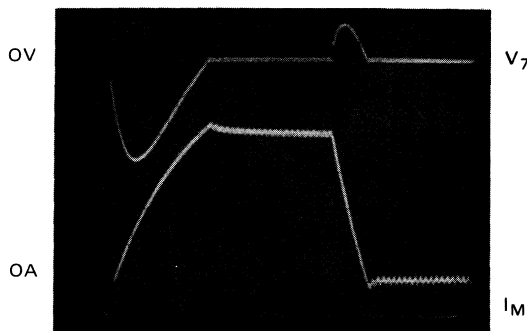
b) Large signal response

The large step signal response is limited by slew-rate and inductive load.

In this case, during the rise-time of the motor current, the L292 works in open-loop condition, as can be seen from the photograph of fig. 10.

Fig. 10 – Motor current and pin 7 voltage waveforms (application of fig. 5) Large signal response.

$V_7 = 1\text{V/div.}$
 $I_M = 0.5\text{A/div.}$
 $t = 500\mu\text{s/div.}$



The voltage at pin 7 (inverting input of the error amplifier) departs from the reference voltage V_R present at the non-inverting input and the feedback loop is open.

The feedback loop is on when the motor current reaches its steady-state value (2A).

Closed loop system bandwidth

A good choice for ξ is the value $1/\sqrt{2}$. In this case:

$$\frac{I_M}{V_I}(s) = \frac{0.044}{R_s} \frac{1 + s R_F C_F}{1 + 2s R_F C_F + 2s^2 R_F^2 C_F^2} \quad (8)$$

The module of the transfer function is:

$$\left| \frac{I_M}{V_I} \right| = \frac{0.044}{R_s} \frac{2 \sqrt{1 + \omega^2 R_F^2 C_F^2}}{\sqrt{[(1 + 2 \omega R_F C_F)^2 + 1] \cdot [(1 - 2 \omega R_F C_F)^2 + 1]}} \quad (9)$$

The cutoff frequency is derived by the expression (9) by putting $\left| \frac{I_M}{V_I} \right| = 0.707 \cdot \frac{0.044}{R_s}$ (-3 dB), from which:

$$\omega_T = \frac{0.9}{R_F C_F} \quad f_T = \frac{0.9}{2\pi R_F C_F}$$

APPLICATION INFORMATION (continued)

Example:

a) Data

- Motor characteristics : $L_M = 5 \text{ mH}$
 $R_M = 5 \Omega$
 $L_M/R_M = 1 \text{ msec}$
- Voltage and current characteristics:
 $V_s = 20V$ $I_M = 2A$ $V_I = 9.1V$
- Closed loop bandwidth: 3 kHz.

b) Calculation

- From relationship (4):

$$R_s = \frac{0.044}{I_M} \quad V_I = 0.2 \Omega$$

and from (1):

$$G_{mo} = \frac{2 V_s}{R_M V_R} = 1 \Omega^{-1}$$

- $RC = 1 \text{ msec}$ [from expression (2)].
- Assuming $\xi = 1/\sqrt{2}$; from (7) follows:

$$\xi^2 = \frac{1}{2} = \frac{400 C}{4 R_F C_F \cdot 0.2}$$

- The cutoff frequency is:

$$f_T = \frac{143 \cdot 10^{-3}}{R_F C_F} = 3 \text{ kHz}$$

c) Summarising

- $RC = 1 \cdot 10^{-3} \text{ sec}$
- $\frac{1000 C}{R_F C_F} = 1$
- $R_F C_F \cong 47 \mu s$

}

$$C = 47 \text{ nF}$$

$$R = 22 \text{ K}\Omega$$

$$\text{For } R_F = 510 \Omega \rightarrow C_F = 92 \text{ nF}$$



L293 L293E

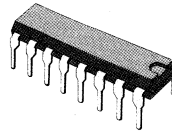
PUSH-PULL FOUR CHANNEL DRIVERS

- OUTPUT CURRENT 1A PER CHANNEL
- PEAK OUTPUT CURRENT 2A PER CHANNEL (NON REPETITIVE)
- INHIBIT FACILITY
- HIGH NOISE IMMUNITY
- SEPARATE LOGIC SUPPLY
- OVERTEMPERATURE PROTECTION

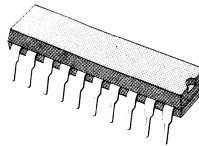
The L293 and L293E are quad push-pull drivers capable of delivering output currents to 1A per channel. Each channel is controlled by a TTL-compatible logic input and each pair of drivers (a full bridge) is equipped with an inhibit input which turns off all four transistors. A separate supply input is provided for the logic so that it may be run off a lower voltage to reduce dissipation.

Additionally, the L293E has external connection of sensing resistors, for switchmode control.

The L293 and L293E are packaged in 16 and 20-pin plastic DIPs respectively; both use the four center pins to conduct heat to the printed circuit board.



DIP-16 Plastic
(0.4)



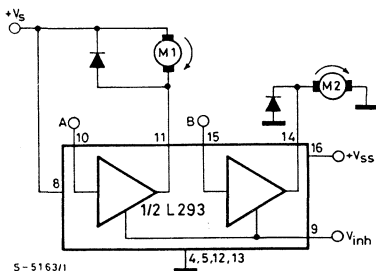
Powerdip
16 + 2 + 2

ORDERING NUMBERS: L293B (16 leads)
L293E (20 leads)

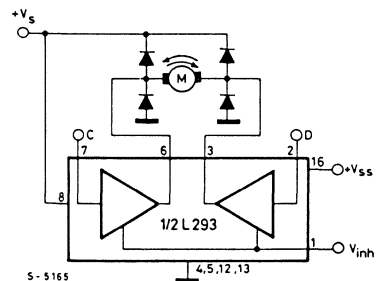
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	36	V
V_{ss}	Logic supply voltage	36	V
V_i	Input voltage	7	V
V_{inh}	Inhibit voltage	7	V
I_{out}	Peak output current (non-repetitive $t = 5ms$)	2	A
P_{tot}	Total power dissipation at $T_{ground-pins} = 80^\circ C$	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^\circ C$

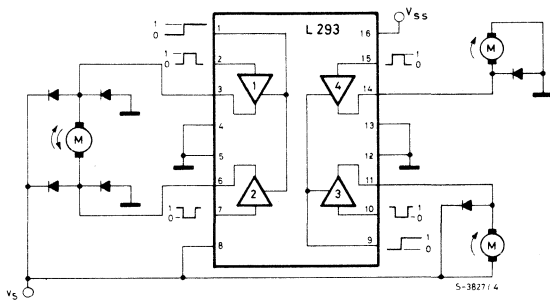
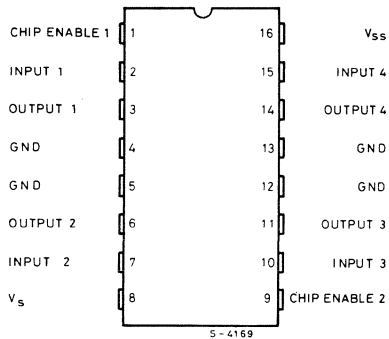
DC motor control



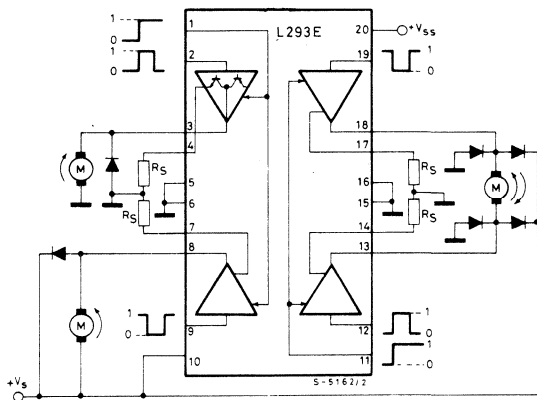
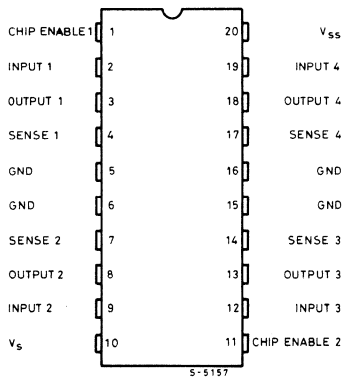
Bidirectional DC motor control



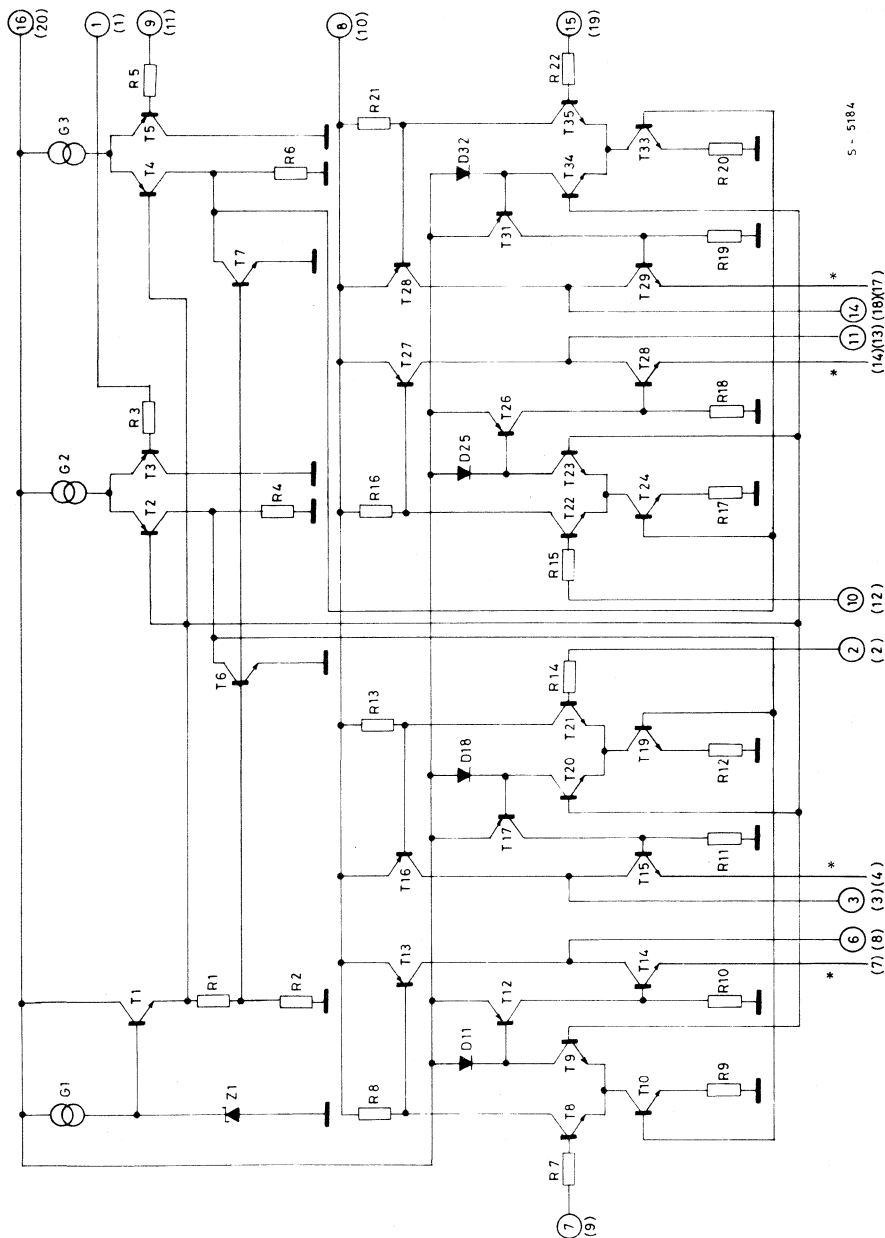
(top view)



(top view)



SCHEMATIC DIAGRAM



S - 5184

(*) In the L293 these points are not externally available. They are internally connected to the ground (substrate).

○ Pins of L293 () Pins of L293E

THERMAL DATA

$R_{th \text{ j-case}}$	Thermal resistance junction-case	max	14	°C/W
$R_{th \text{ j-amb}}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (For each channel, $V_S = 24V$, $V_{SS} = 5V$, $T_{amb} = 25^\circ C$, unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S Supply voltage		V_{SS}		36	V
V_{SS} Logic supply voltage		4.5		36	V
I_S Total quiescent supply current	$V_I = L \quad I_O = 0 \quad V_{inh} = H$		2	6	mA
	$V_I = H \quad I_O = 0 \quad V_{inh} = H$		16	24	
	$V_{inh} = L$			4	
I_{SS} Total quiescent logic supply current	$V_I = L \quad I_O = 0 \quad V_{inh} = H$		44	60	mA
	$V_I = H \quad I_O = 0 \quad V_{inh} = H$		16	22	
	$V_{inh} = L$		16	24	
V_{IL} Input low voltage		-0.3		1.5	V
V_{IH} Input high voltage	$V_{SS} \leq 7V$	2.3		V_{SS}	V
	$V_{SS} > 7V$	2.3		7	
I_{IL} Low voltage input current	$V_{IL} = 1.5V$			-10	μA
I_{IH} High voltage input current	$2.3V \leq V_{IH} \leq V_{SS} - 0.6V$		30	100	μA
V_{inhL} Inhibit low voltage		-0.3		1.5	V
V_{inhH} Inhibit high voltage	$V_{SS} \leq 7V$	2.3		V_{SS}	V
	$V_{SS} > 7V$	2.3		7	
I_{inhL} Low voltage inhibit current	$V_{inhL} = 1.5V$		-30	-100	μA
I_{inhH} High voltage inhibit current	$2.3V \leq V_{inhH} \leq V_{SS} - 0.6V$			± 10	μA
V_{CEsatH} Source output saturation voltage	$I_O = -1A$		1.4	1.8	V
V_{CEsatL} Sink output saturation voltage	$I_O = 1A$		1.2	1.8	V
V_{SENS} Sensing Voltage (pins 4, 7, 14, 17) (**)				2	V
t_r Rise time	0.1 to 0.9 V_O (*)		250		ns
t_f Fall time	0.9 to 0.1 V_O (*)		250		ns
t_{on} Turn-on delay	0.5 V_I to 0.5 V_O (*)		750		ns
t_{off} Turn-off delay	0.5 V_I to 0.5 V_O (*)		200		ns

(*) See fig. 1.

(**) Referred to L293E.

TRUTH TABLE

V_i (each channel)	V_o	$V_{inh.} (^{\circ})$
H	H	H
L	L	H
H	X ($^{\circ}$)	L
L	X ($^{\circ}$)	L

($^{\circ}$) High output impedance.

($^{\circ\circ}$) Relative to the considerate channel.

Fig. 1 - Switching times

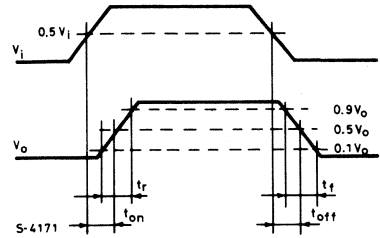


Fig. 2 - Saturation voltage vs. output current

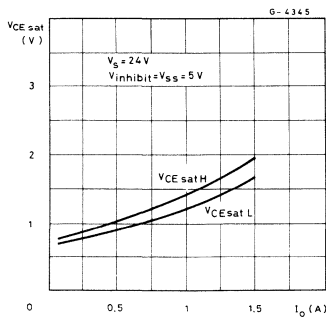


Fig. 3 - Source saturation voltage vs. ambient temperature

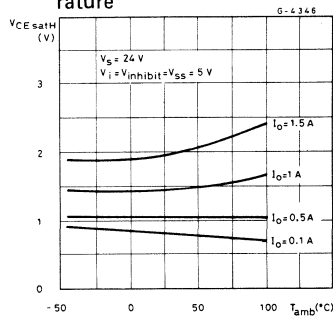


Fig. 4 - Sink saturation voltage vs. ambient temperature

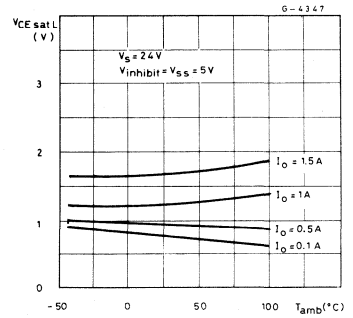


Fig. 5 - Quiescent logic supply current vs. logic supply voltage

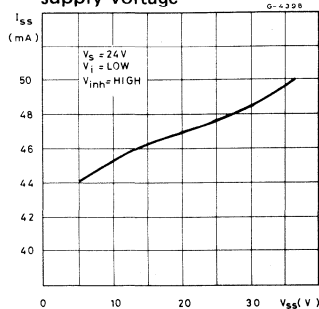


Fig. 6 - Output voltage vs. input voltage

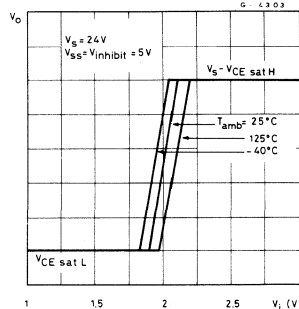
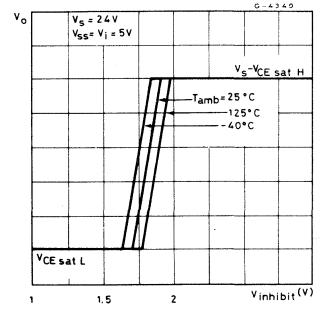
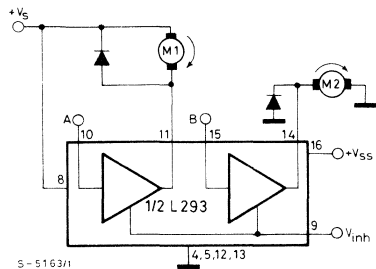


Fig. 7 - Output voltage vs. inhibit voltage



APPLICATION INFORMATION

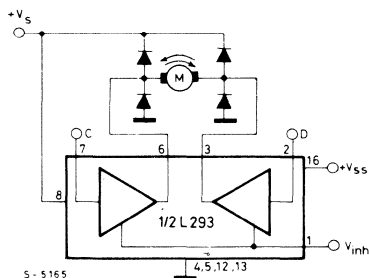
Fig. 8 – DC motor controls (with connection to ground and to the supply voltage)



V_{inh}	A	M1	B	M2
H	H	Fast motor stop	H	Run
H	L	Run	L	Fast motor stop
L	X	Free running motor stop	X	Free running motor stop

L = Low H = High X = Don't care

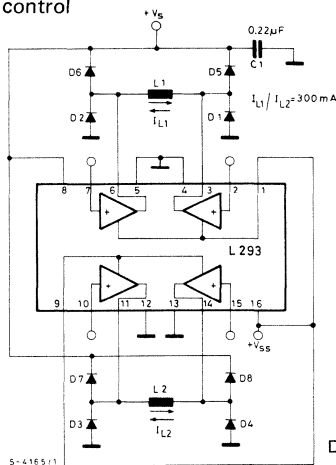
Fig. 9 – Bidirectional DC motor control



INPUTS		FUNCTION
$V_{inh} = H$	C = H; D = L	Turn right
	C = L; D = H	Turn left
	C = D	Fast motor stop
$V_{inh} = L$	C = X; D = X	Free running motor stop

L = Low H = High X = Don't care

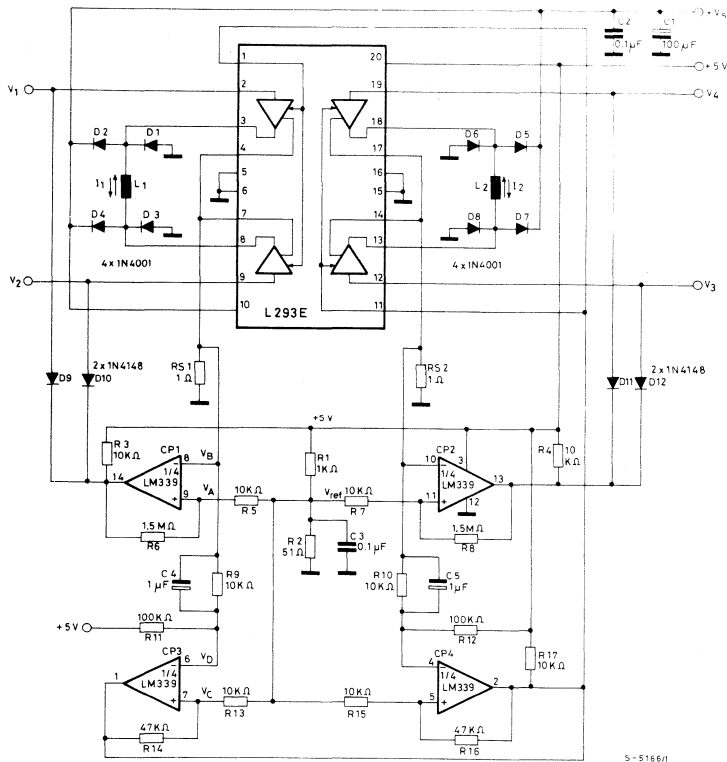
Fig. 10 – Bipolar stepping motor control



D1 - D8 = $\begin{cases} V_F \leq 1.2V @ I = 300 mA \\ t_{rr} \leq 500 ns \end{cases}$

APPLICATION INFORMATION (continued)

Fig. 11 – Stepping motor driver with phase current control and short circuit protection



D1 to D8 : $\begin{cases} V_F \leq 1.2V @ I = 300 \text{ mA} \\ t_{rr} \leq 200 \text{ ns} \end{cases}$

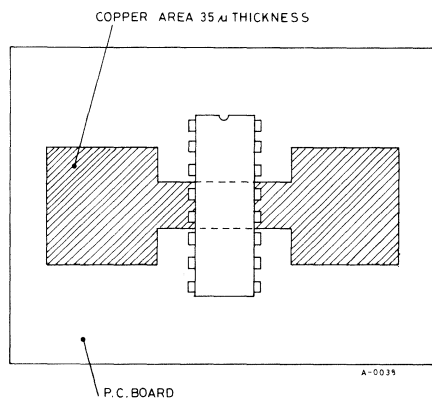


L293
L293E

MOUNTING INSTRUCTIONS

The $R_{th j-amb}$ of the L293 and the L293E can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board as shown in figure 12 or to an external heatsink (figure 13).

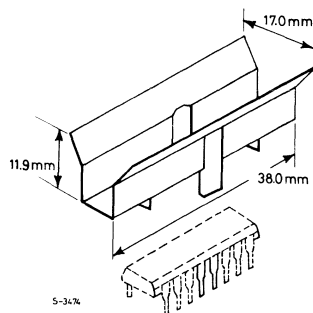
Fig. 12 - Example of P.C. board copper area which is used as heatsink



During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 13 - External heatsink mounting example ($R_{th} = 30\text{ }^{\circ}\text{C/W}$)





L293C

ADVANCE DATA

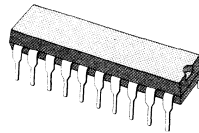
PUSH-PULL FOUR CHANNEL/DUAL H-BRIDGE DRIVER

- 600mA OUTPUT CURRENT CAPABILITY PER CHANNEL
- 1.2A PEAK OUTPUT CURRENT (NON REPETITIVE) PER CHANNEL
- ENABLE FACILITY
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5V (HIGH NOISE IMMUNITY)
- SEPARATE HIGH VOLTAGE POWER SUPPLY (UP TO 44V)

The L293C is a monolithic high voltage, high current integrated circuit four channel driver in a 20 pin DIP. It is designed to accept standard TTL or DTL input logic levels and drive inductive loads (such as relays, solenoids, DC and stepping motors) and switching power transistors.

The device may easily be used as a dual H-bridge driver: separate chip enable and high voltage power supply pins are provided for each H-bridge. In addition, a separate power supply is provided for the logic section of the device.

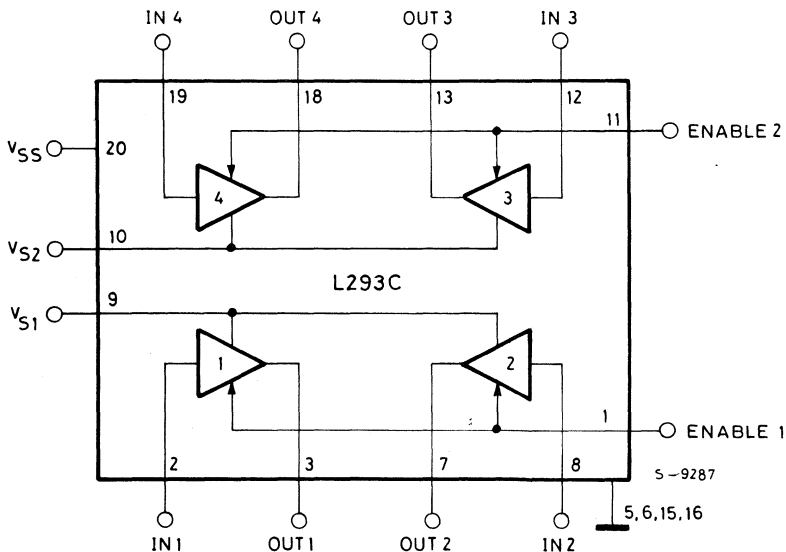
The L293C is assembled in a 20 lead plastic package which has 4 center pins connected together and used for heatsinking.



Powerdip
16+2+2

ORDER CODE: L293C

BLOCK DIAGRAM





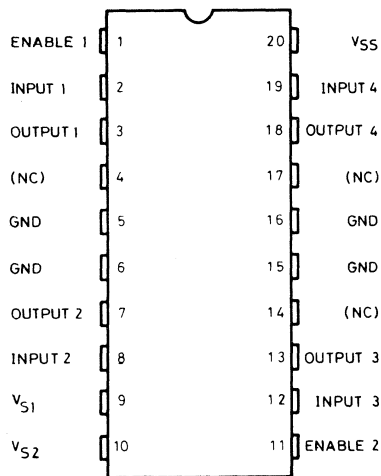
L293C

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	50	V
V_{ss}	Logic supply voltage	7	V
V_i	Input voltage	7	V
V_{EN}	Enable voltage	7	V
I_{out}	Peak output current (non-repetitive $t = 5ms$)	1.2	A
P_{tot}	Total power dissipation at $T_{ground-pins} = 80^{\circ}C$	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^{\circ}C$

CONNECTION DIAGRAM

(Top view)



S-9288

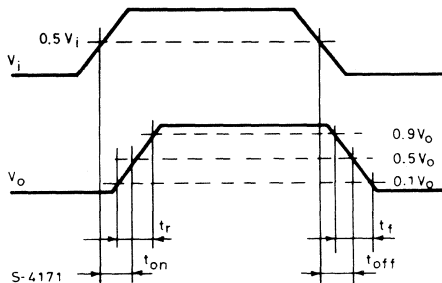
TRUTH TABLE

INPUT	ENABLE	OUTPUT
H	H	H
L	H	L
X	L	Z

Z = High output impedance

X = Don't care

SWITCHING TIMES



THERMAL DATA

$R_{th J-case}$	Thermal resistance junction-case	max	14	$^{\circ}C/W$
$R_{th J-amb}$	Thermal resistance junction-ambient	max	80	$^{\circ}C/W$

ELECTRICAL CHARACTERISTICS (For each channel, $V_S = 24V$, $V_{SS} = 5V$, $T_{amb} = 25^{\circ}C$, unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S Supply voltage (pin 9, 10)		V_{SS}		44	V
V_{SS} Logic supply voltage (pin 20)		4.5		7	V
I_S Total quiescent supply current (pin 9, 10)	$V_I = L; I_O = 0; V_{EN} = H$		2	6	mA
	$V_I = H; I_O = 0; V_{EN} = H$		16	24	
	$V_{EN} = L$			4	
I_{SS} Total quiescent logic supply current (pin 20)	$V_I = L; I_O = 0; V_{EN} = H$		44	60	mA
	$V_I = H; I_O = 0; V_{EN} = H$		16	22	
	$V_{EN} = L$		16	24	
V_{IL} Input low voltage (pin 2, 8, 12, 19)		-0.3		1.5	V
V_{IH} Input high voltage (pin 2, 8, 12, 19)		2.3		V_{SS}	V
I_{IL} Low voltage input current (pin 2, 8, 12, 19)	$V_I = 1.5V$			-10	μA
I_{IH} High voltage input current (pin 2, 8, 12, 19)	$2.3V \leq V_I \leq V_{SS} - 0.6V$		30	100	μA
V_{ENL} Enable low voltage (pin 1, 11)		-0.3		1.5	V
V_{ENH} Enable high voltage (pin 1, 11)		2.3		V_{SS}	V
I_{ENL} Low voltage enable current (pin 1, 11)	$V_{ENL} = 1.5V$		-30	-100	μA
I_{ENH} High voltage enable current (pin 1, 11)	$2.3V \leq V_{ENH} \leq V_{SS} - 0.6$			± 10	μA
$V_{CE(sat)H}$ Source output saturation voltage (pins 3, 7, 13, 18)	$I_O = -0.6A$		1.4	1.8	V
$V_{CE(sat)L}$ Sink output saturation voltage (pins 3, 7, 13, 18)	$I_O = +0.6A$		1.2	1.8	V
t_r Rise time (*)	0.1 to 0.9 V_O		250		ns
t_f Fall time (*)	0.9 to 0.1 V_O		250		ns
t_{on} Turn-on delay (*)	0.5 V_I to 0.5 V_O		750		ns
t_{off} Turn-off delay (*)	0.5 V_I to 0.5 V_O		200		ns

(*) See switching times diagram



L293D

PRELIMINARY DATA

PUSH-PULL FOUR CHANNEL DRIVER WITH DIODES

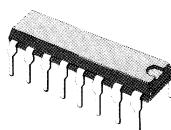
- 600mA OUTPUT CURRENT CAPABILITY PER CHANNEL
- 1.2A PEAK OUTPUT CURRENT (NON REPETITIVE) PER CHANNEL
- ENABLE FACILITY
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5V (HIGH NOISE IMMUNITY)
- INTERNAL CLAMP DIODES

The L293D is a monolithic integrated high voltage, high current four channel driver designed to accept standard DTL or TTL logic levels and drive inductive loads (such as relays solenoides, DC and stepping motors) and switching power transistors.

To simplify use as two bridges each pair of channels is equipped with an enable input. A separate supply input is provided for the logic, allowing operation at a lower voltage and internal clamp diodes are included.

This device is suitable for use in switching applications at frequencies up to 5 kHz.

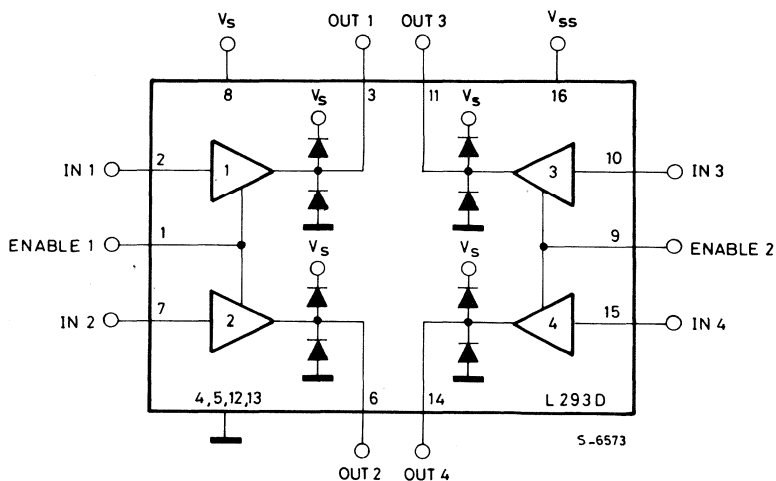
The L293D is assembled in a 16 lead plastic package which has 4 center pins connected together and used for heatsinking.



Powerdip
12 + 2 + 2

ORDERING NUMBER: L293D

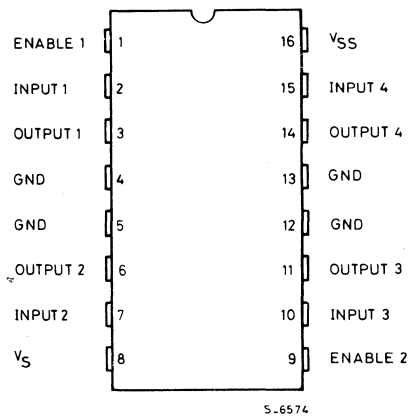
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	36	V
V_{SS}	Logic supply voltage	36	V
V_i	Input voltage	7	V
V_{en}	Enable voltage	7	V
I_o	Peak output current (100 μ s non repetitive)	1.2	A
P_{tot}	Total power dissipation at $T_{ground-pins} = 80^{\circ}C$	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^{\circ}C$

CONNECTION DIAGRAM



THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max	14	$^{\circ}C/W$
$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	80	$^{\circ}C/W$

ELECTRICAL CHARACTERISTICS (For each channel, $V_s = 24V$, $V_{ss} = 5V$, $T_{amb} = 25^\circ C$, unless otherwise specified)

Parameter	Test condition	Min.	Typ.	Max.	Unit
V_s Supply voltage (pin 8)		V_{ss}		36	V
V_{ss} Logic supply voltage (pin 16)		4.5		36	V
I_s Total quiescent supply current (pin 8)	$V_i = L \quad I_o = 0 \quad V_{en} = H$		2	6	mA
	$V_i = H \quad I_o = 0 \quad V_{en} = H$		16	24	
	$V_{en} = L$			4	
I_{ss} Total quiescent logic supply current (pin 16)	$V_i = L \quad I_o = 0 \quad V_{en} = H$		44	60	mA
	$V_i = H \quad I_o = 0 \quad V_{en} = H$		16	22	
	$V_{en} = L$		16	24	
V_{IL} Input low voltage (pin 2, 7, 10, 15)		-0.3		1.5	V
V_{IH} Input high voltage (pin 2, 7, 10, 15)	$V_{ss} \leq 7V$	2.3		V_{ss}	V
	$V_{ss} > 7V$	2.3		7	
I_{IL} Low voltage input current (pin 2, 7, 10, 15)	$V_{IL} = 1.5V$			-10	μA
I_{IH} High voltage input current (pin 2, 7, 10, 15)	$2.3V \leq V_{IH} \leq V_{ss} - 0.6V$		30	100	μA
V_{enL} Enable low voltage (pin 1, 9)		-0.3		1.5	V
V_{enH} Enable high voltage (pin 1, 9)	$V_{ss} \leq 7V$	2.3		V_{ss}	V
	$V_{ss} > 7V$	2.3		7	
I_{enL} Low voltage enable current (pin 1, 9)	$V_{enL} = 1.5V$		-30	-100	μA
I_{enH} High voltage enable current (pin 1, 9)	$2.3V \leq V_{enH} \leq V_{ss} - 0.6V$			± 10	μA
V_{CEsatH} Source output saturation voltage (pins 3, 6, 11, 14)	$I_o = -0.6A$		1.4	1.8	V
V_{CEsatL} Sink output saturation voltage (pins 3, 6, 11, 14)	$I_o = +0.6A$		1.2	1.8	V
V_F Clamp diode forward voltage	$I_o = 600 mA$		1.3		V
t_r Rise time (*)	0.1 to 0.9 V_o		250		ns
t_f Fall time (*)	0.9 to 0.1 V_o		250		ns
t_{on} Turn-on delay (*)	0.5 V_i to 0.5 V_o		750		ns
t_{off} Turn-off delay (*)	0.5 V_i to 0.5 V_o		200		ns

(*) See fig. 1

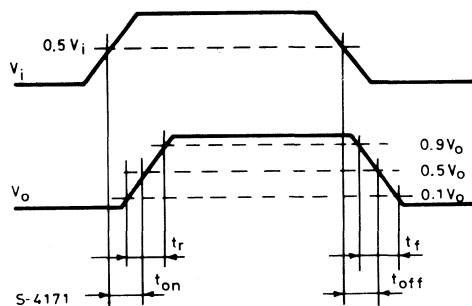
TRUTH TABLE (One channel)

INPUT	ENABLE (*)	OUTPUT
H	H	H
L	H	L
H	L	Z
L	L	Z

Z = High output impedance

(*) Relative to the considered channel

Fig. 1 – Switching Times



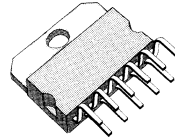
SWITCH-MODE SOLENOID DRIVER

- HIGH VOLTAGE OPERATION (UP TO 50V)
- HIGH OUTPUT CURRENT CAPABILITY (UP TO 4A)
- LOW SATURATION VOLTAGE
- TTL-COMPATIBLE INPUT
- OUTPUT SHORT CIRCUIT PROTECTION (TO GROUND, TO SUPPLY AND ACROSS THE LOAD)
- THERMAL SHUTDOWN
- OVERDRIVING PROTECTION
- LATCHED DIAGNOSTIC OUTPUT

The L294 is a monolithic switchmode solenoid driver designed for fast, high-current applications such as hammer and needle driving in printers

and electronic typewriters. Power dissipation is reduced by efficient switchmode operation. An extra feature of the L294 is a latched diagnostic output which indicates when the output is short circuited.

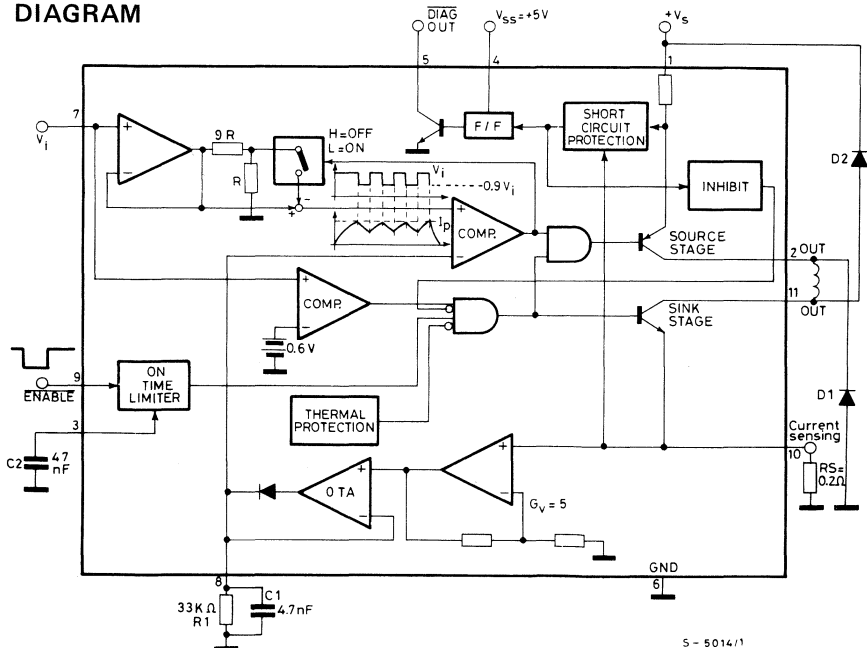
The L294 is supplied in a 11-lead Multiwatt[®] plastic power package.



Multiwatt 11

ORDER CODE : L294

BLOCK DIAGRAM



S-5014/1



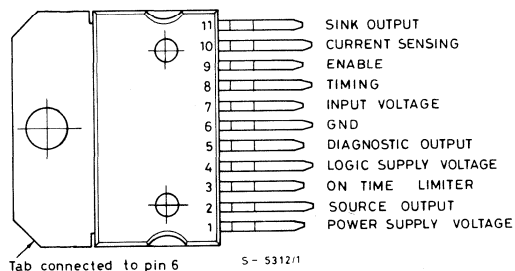
L294

ABSOLUTE MAXIMUM RATING

V_s	Power supply voltage	50	V
V_{ss}	Logic supply voltage	7	V
V_{EN}	Enable voltage	7	V
V_i	Input voltage	7	V
I_p	Peak output current (repetitive)	4.5	A
P_{tot}	Total power dissipation (at $T_{case} = 75^\circ\text{C}$)	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

CONNECTION DIAGRAM

(top view)



THERMAL DATA

$R_{th \text{ j-case}}$	Thermal resistance junction-case	max	3	$^\circ\text{C/W}$
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ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s = 40V$, $V_{ss} = 5V$, $T_{amb} = 25^\circ C$, unless otherwise specified).

Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s Power supply voltage (pin 1)	Operative condition	12		46	V
I_d Quiescent drain current (pin 1)	$V_{ENABLE} = H$		20	30	mA
	$V_i \geq 0.6V$; $V_{ENABLE} = L$		70		
V_{ss} Logic supply voltage (pin 4)		4.5		7	V
I_{ss} Quiescent logic supply current	$V_{DIAG} = L$		5	8	mA
	DIAG output at high impedance		10	100	
V_i Input voltage (pin 7)	Operating output	0.6			V
	Non-operative output			0.45	
I_i Input current (pin 7)	$V_i \geq 0.6V$		-1		μA
	$V_i \leq 0.45V$		-3		
V_{ENABLE} Enable input voltage (pin 9)	Low level	-0.3		0.8	V
	High level	2.4			
I_{ENABLE} Enable input current (pin 9)	$V_{ENABLE} = L$			-100	μA
	$V_{ENABLE} = H$			100	
I_{load}/V_i Transconductance	$R_s = 0.2 \Omega$ $V_i = 1V$	0.95	1	1.05	A/V
	$V_i = 4V$	0.97	1	1.03	
$V_{sat H}$ Source output saturation voltage	$I_p = 4A$		1.7		V
$V_{sat L}$ Sink output saturation voltage	$I_p = 4A$		2		V
$V_{sat H} + V_{sat L}$ Total saturation voltage	$I_p = 4A$			4.5	V
$I_{leakage}$ Output leakage current	$R_s = 0.2 \Omega$; $V_i \leq 0.45V$		1		mA
K On time limiter constant (°)	$V_{ENABLE} = L$		120		
V_{DIAG} Diagnostic output voltage (pin 5)	$I_{DIAG} = 10 mA$			0.4	V
I_{DIAG} Diagnostic leakage current (pin 5)	$V_{DIAG} = 40V$			10	μA
$V_{pin 8}$ OP AMP and OTA DC voltage gain (°°)	$V_{pin 10} = 100$ to $800 mV$		5		
$V_{pin 10}$					
V_{SENS} Sensing voltage (pin 10) (°°°)				0.9	V

(°) After a time interval $t_{max} = KC_2$, the output stages are disabled.

(°°) See the block diagram.

(°°°) Allowed range of V_{SENS} without the intervention of the short circuit protection.

CIRCUIT OPERATION

The L294 works as a transconductance amplifier: it can supply an output current directly proportional to an input voltage level (V_i). Furthermore, it allows complete switching control of the output current waveform (see fig. 1).

The following explanation refers to the Block Diagram, to fig. 1 and to the typical application circuit of fig. 2.

The t_{on} time is fixed by the width of the Enable input signal (TTL compatible): it is active low and enables the output stages "source" and "sink". At the end of t_{on} , the load current I_{load} recirculates through D1 and D2, allowing fast current turn-off.

The rise time t_r depends on the load characteristics, on V_i and on the supply voltage value (V_s , pin 1). During the t_{on} time, I_{load} is converted into a voltage signal by means of the external sensing resistance R_s connected to pin 10. This signal, amplified by the op amp and converted by the transconductance amplifier OTA, charges the external RC network at pin 8 ($R1$, $C1$). The voltage at this pin is sensed by the inverting input of a comparator. The voltage on the non-inverting input of this one is fixed by the external voltage V_i (pin 7).

After t_r , the comparator switches and the output stage "source" is switched off. The comparator output is confirmed by the voltage on the non-inverting input, which decreases of a constant fraction of V_i ($1/10$), allowing hysteresis operation. The current in the load now flows through D1.

Two cases are possible: the time constant of the recirculation phase is higher than $R1.C1$; the time constant is lower than $R1.C1$. In the first case, the voltage sensed on the non-inverting input of the comparator is just the value proportional to I_{load} . In the second case, when the current decreases too quickly, the comparator senses the voltage signal stored in the $R1.C1$ network.

In the first case t_1 depends on the load characteristics, while in the second case it depends only on the value of $R1.C1$.

In other words, $R1.C1$ fixes the minimum value of t_1 ($t_1 \geq 1/10 R1.C1$). Note that $C1$ should be chosen in the range 2.7 to 10 nF for stability reasons of the OTA).

After t_1 , the comparator switches again: the output is confirmed by the voltage on the non-inverting input, which reaches V_i again (hysteresis).

Now the cycle starts again: t_2 , t_4 and t_6 have the same characteristics as t_r , while t_3 and t_5 are similar to t_1 . The peak current I_p depends on V_i as shown in the typical transfer function of fig. 3.

It can be seen that for V_i lower than 450 mV the device is not operating.

For V_i greater than 600 mV, the L294 has a transconductance of 1A/V with $R_s = 0.2\Omega$. For V_i included between 450 and 600 mV, the operation is not guaranteed.

The other parts of the device have protection and diagnostic functions. At pin 3 is connected an external capacitor $C2$, charged at constant current when the Enable is low.

After a time interval equal to $K \cdot C2$ (K is defined in the table of Electrical Characteristics and has the dimensions of ohms) the output stages are switched off independently by the Input signal.

This avoids the load being driven in conduction for an excessive period of time (overdriving protection). The action of this protection is shown in fig. 1b. Note that the voltage ramp at pin 3 starts whenever the Enable signal becomes active (low state), regardless of the Input signal. To reset pin 3 and to restore the normal conditions, pin 9 must return high.

This protection can be disabled by grounding pin 3.

The thermal protection included in the L294 has a hysteresis.

It switches off the output stages whenever the junction temperature increases too much. After a fall of about 20°C, the circuit starts again.

Finally, the device is protected against any type of short circuit at the outputs: to ground, to supply and across the load.

When the source stage current is higher than 5A and/or when the pin 10 voltage is higher than 1V (i.e. for a sink current greater than $1V/R_s$) the output stages are switched off and the device is inhibited.

This condition is indicated at the open-collector output DIAG (pin 5); the internal flip-flop F/F changes and forces the output transistor into saturation. The F/F must be supplied independently through V_{ss} (pin 4). The DIAG signal is reset and the output stages are still operative by switching off the supply

CIRCUIT OPERATION (continued)

voltage at pin 1 and then by switching the device on again. After that, two cases are possible: the reason for the "bad operation" is still present and the protection acts again; the reason has been removed and the device starts to work properly.

Fig. 1 - Output current waveforms

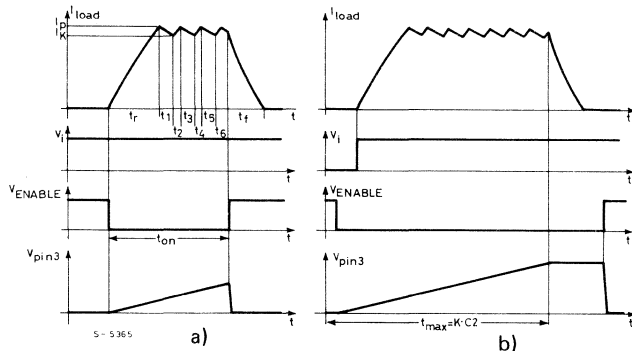
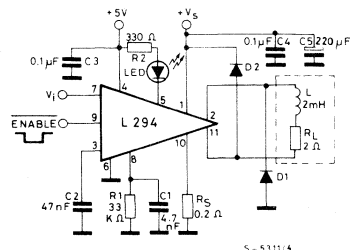


Fig. 2 - Test and typical application circuit



D1: 3A fast diode
D2: 1A fast diode } $t_{rr} \leq 200 \text{ ns}$

Fig. 3 - Peak output current vs. input voltage

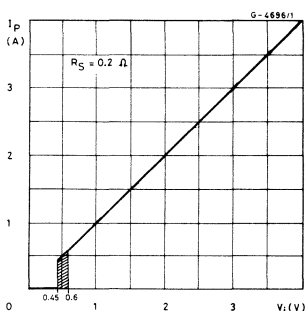


Fig. 4 - Output saturation voltages vs. peak output current

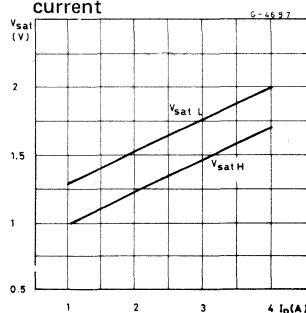


Fig. 5 - Safe operating areas

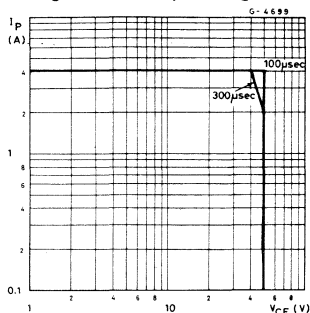
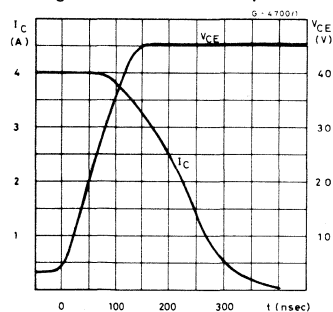


Fig. 6 - Turn-off phase



CALCULATION OF THE SWITCHING TIMES

Referring to the block diagram and to the waveforms of fig. 1, it is possible to calculate the switching times by means of the following relationships.

$$t_r = - \frac{L}{R_L} \ln \left(1 - \frac{R_L}{V_1} \cdot I_p \right)$$

$$\text{where: } V_1 = V_s - V_{\text{satL}} - V_{\text{satH}} - V_{R \text{ sens}}$$

$$t_f = - \frac{L}{R_L} \ln \frac{V_2}{V_2 + R_L \cdot I_o}$$

$$\text{where: } V_2 = V_s + V_{D1} + V_{D2}$$

$I_K \leq I_o \leq I_p$
 I_o is the value of the load current at the end of t_{on} .

$$t_1 = t_3 = t_5 = \dots = \begin{cases} \text{a) } - \frac{L}{R_L} \ln \frac{0.9 I_p \cdot R_L + V_3}{I_p R_L + V_3} & \text{where } V_3 = V_{\text{satL}} + V_{R \text{ sens}} + V_{D1} \\ \text{b) } - R_1 C_1 \ln 0.9 \cong \frac{1}{10} R_1 C_1 \end{cases}$$

$$t_2 = t_4 = t_6 = \dots = - \frac{L}{R_L} \ln \left(\frac{V_1 - I_p R_L}{V_1 - I_K R_L} \right)$$

Note that the time interval $t_1 = t_3 = t_5 = \dots$ takes the longer value between case a) and case b). The switching frequency is always:

$$f_{\text{switching}} = \frac{1}{t_1 + t_2}$$

In the case a) the main regulation loop is always closed and it forces:

$$I_K = (0.9 \pm S) I_p$$

$$\text{where: } S = 3\% \quad @ \quad V_i = 1V \\ S = 1.5\% \quad @ \quad V_i = 4V$$

In the case b), the same loop is open in the recirculation phase and I_K , which is always lower than $0.9 I_p$, is obtained by means of the following relationship.

$$I_K = I_p e^{-\frac{t_1 R_L}{L}} - \frac{V_3}{R_L} \left(1 - e^{-\frac{t_1 R_L}{L}} \right)$$

With the typical application circuit, in the conditions $V_s = 40V$, $I_p = 4A$, the following switching times result:

$$t_r = 255 \mu s$$

$$t_f = 174 \mu s \quad @ \quad I_o = I_p$$

$$t_1 = \begin{matrix} \text{a) } 70 \mu s \\ \text{b) } 16 \mu s \end{matrix}$$

$$t_2 = 29 \mu s$$

$$f = 10.2 \text{ KHz}$$



DUAL SWITCH-MODE SOLENOID DRIVER

- levels at the inputs and can drive 2 solenoids. The output current is completely controlled by means of a switching technique allowing very efficient operation. Furthermore, it includes an enable input and dual supplies (for interfacing with peripherals running at a higher voltage than the logic).

The L295 is particularly suitable for applications such as hammer driving in matrix printers, step motor driving and electromagnet controllers.



ORDERING NUMBER: L295

The L295 is a monolithic integrated circuit in a 15-lead Multiwatt[®] package; it incorporates all the functions for direct interfacing between digital circuitry and inductive loads. The L295 is designed to accept standard microprocessor logic

V_s	Supply voltage	50	V
V_{ss}	Logic supply voltage	12	V
V_{EN}, V_i	Enable and input voltage	7	V
V_{ref}	Reference voltage	7	V
I_o	Peak output current (each channel)		
	– non repetitive ($t = 100 \mu\text{sec}$)	3	A
	– repetitive (80% on -20% off; $t_{on} = 10 \text{ ms}$)	2.5	A
	– DC operation	2	A
P_{tot}	Total power dissipation (at $T_{case} = 75^\circ\text{C}$)	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

CIRCUIT

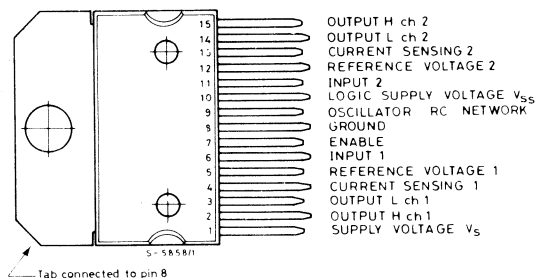
The diagram shows the L295 voltage detector IC with its 15 pins. The circuit includes various components connected to the pins:

- Pin 10:** Connected to $+V_{ss}$ through a $0.1\mu F$ capacitor C_1 .
- Pin 1:** Connected to $+V_s$.
- Pin 15:** Connected to a network of resistors R_2 , R_1 , and R_3 , and inductors L_2 and L_1 .
- Pin 14:** Connected to ground through a resistor R_{S2} .
- Pin 13:** Connected to ground.
- Pin 12:** Connected to V_{ref2} .
- Pin 11:** Connected to V_{in2} .
- Pin 7:** Connected to ground.
- Pin 6:** Connected to V_{ref1} .
- Pin 5:** Connected to ground.
- Pin 4:** Connected to ground through a resistor R_{S1} .
- Pin 3:** Connected to a network of resistors R_1 , R_3 , and R_2 , and inductors L_1 and L_2 .
- Pin 9:** Connected to ground through a $3.9nF$ capacitor C_3 .
- Pin 8:** Connected to ground through a 0.5Ω resistor.
- Pin 1:** Connected to a network of capacitors C_2 and C_4 , and a diode D_1 .
- Pin 2:** Connected to a network of capacitors C_2 and C_4 , and a diode D_2 .
- Pin 3:** Connected to a network of capacitors C_2 and C_4 , and a diode D_3 .
- Pin 4:** Connected to a network of capacitors C_2 and C_4 , and a diode D_4 .
- Pin 5:** Connected to a network of capacitors C_2 and C_4 , and a diode D_5 .
- Pin 6:** Connected to a network of capacitors C_2 and C_4 , and a diode D_6 .
- Pin 7:** Connected to a network of capacitors C_2 and C_4 , and a diode D_7 .
- Pin 8:** Connected to a network of capacitors C_2 and C_4 , and a diode D_8 .
- Pin 9:** Connected to a network of capacitors C_2 and C_4 , and a diode D_9 .
- Pin 10:** Connected to a network of capacitors C_2 and C_4 , and a diode D_{10} .
- Pin 11:** Connected to a network of capacitors C_2 and C_4 , and a diode D_{11} .
- Pin 12:** Connected to a network of capacitors C_2 and C_4 , and a diode D_{12} .
- Pin 13:** Connected to a network of capacitors C_2 and C_4 , and a diode D_{13} .
- Pin 14:** Connected to a network of capacitors C_2 and C_4 , and a diode D_{14} .
- Pin 15:** Connected to a network of capacitors C_2 and C_4 , and a diode D_{15} .

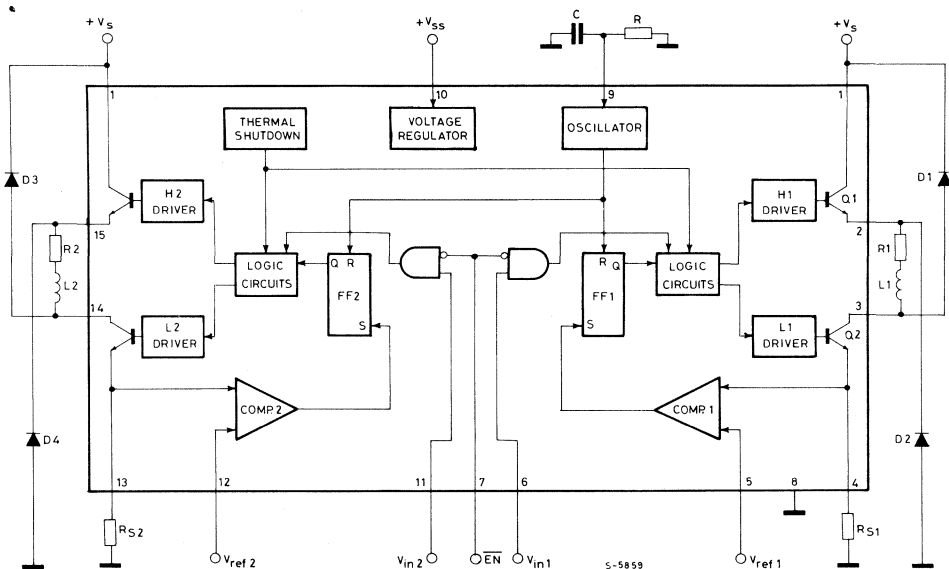
S-586011

CONNECTION DIAGRAM

(top view)



BLOCK DIAGRAM



THERMAL DATA

$R_{th \text{ j-case}}$	Thermal resistance junction-case	max	3	$^{\circ}\text{C/W}$
$R_{th \text{ j-amb}}$	Thermal resistance junction-ambient	max	35	$^{\circ}\text{C/W}$

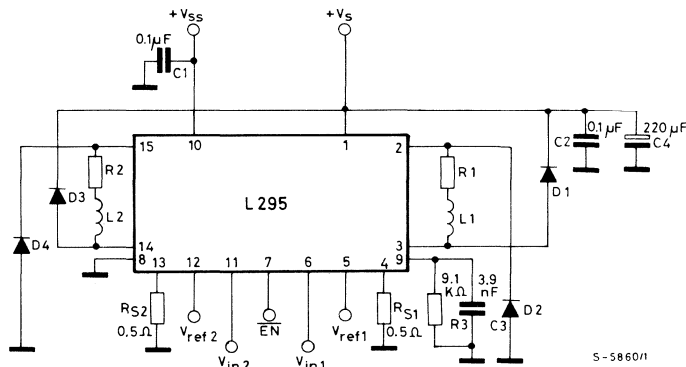


ELECTRICAL CHARACTERISTICS (Refer to the application circuit, $V_{SS}=5V$; $V_s=36V$; $T_j=25^\circ C$; L = low; H = high; unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s Supply Voltage		12		46	V
V_{SS} Logic Supply voltage		4.75		10	V
I_d Quiescent drain current (from V_s)	$V_s = 46V$; $V_{i1} = V_{i2} = V_{EN} = L$			4	mA
I_{ss} Quiescent drain current (from V_{ss})	$V_{ss} = 10V$			46	mA
V_{i1}, V_{i2} Input Voltage	Low	-0.3		0.8	V
	High	2.2		7	
V_{EN} Enable Input Voltage	Low	-0.3		0.8	V
	High	2.2		7	
I_{i1}, I_{i2} Input Current	$V_{i1} = V_{i2} = L$			-100	μA
	$V_{i1} = V_{i2} = H$			10	
I_{EN} Enable Input Current	$V_{EN} = L$			-100	μA
	$V_{EN} = H$			10	
V_{ref1}, V_{ref2} Input Reference Voltage		0.2		2	V
I_{ref1}, I_{ref2} Input Reference Current				-5	μA
f_{osc} Oscillation Frequency	$C = 3.9\text{ nF}$; $R = 9.1\text{ K}\Omega$		25		KHz
$\frac{I_p}{V_{ref}}$ Transconductance (each ch.)	$V_{ref} = 1V$ $R_s = 0.5\Omega$	1.9	2	2.1	A/V
V_{drop} Total output voltage drop (each channel) (*)	$I_o = 2A$		2.8	3.6	V
V_{sens1} V_{sens2} External sensing resistors voltage drop				2	V

(*) $V_{drop} = V_{CEsat\ Q1} + V_{CEsat\ Q2}$

APPLICATION CIRCUIT



S-5860/1

D2, D4 = 2A High speed diodes } $t_{rr} \leq 200 \text{ ns}$
D1, D3 = 1A High speed diodes

R1 = R2 = 2Ω
L1 = L2 = 5 mH

FUNCTIONAL DESCRIPTION

The L295 incorporates two independent driver channels with separate inputs and outputs, each capable of driving an inductive load (see block diagram).

The device is controlled by three microprocessor compatible digital inputs and two analog inputs. These inputs are:

- $\overline{\text{EN}}$ chip enable (digital input, active low), enables both channels when in the low state.
- V_{in1}, V_{in2} channel inputs (digital inputs, active high), enable each channel independently. A channel is activated when both $\overline{\text{EN}}$ and the appropriate channel input are active.
- V_{ref1}, V_{ref2} reference voltages (analog inputs), used to program the peak load currents. Peak load current is proportional to V_{ref} .

Since the two channels are identical, only channel one will be described.

The following description applies also to channel two, replacing FF2 for FF1, V_{ref2} for V_{ref1} etc. When the channel is activated by a low level on the $\overline{\text{EN}}$ input and a high level on the channel input, V_{in2} , the output transistors Q1 and Q2 switch on and current flows in the load according to the exponential law:

$$I = \frac{V}{R1} \left(1 - e^{-\frac{R1 t}{L1}} \right)$$

where: R1 and L1 are the resistance and inductance of the load and V is the voltage available on the load ($V_s - V_{drop} - V_{sense}$).

The current increases until the voltage on the external sensing resistor, R_{S1} , reaches the reference voltage, V_{ref1} . This peak current, I_{p1} , is given by:

$$I_{p1} = \frac{V_{ref1}}{R_{S1}}$$

At this point the comparator output, Comp1, sets the RS flip-flop, FF1, that turns off the output transistor, Q1. The load current flowing through D2, Q2, R_{S1} , decreases according to the law:

$$I = \left(\frac{V_A}{R1} + I_{p1} \right) e^{-\frac{R1 t}{L1}} - \frac{V_A}{R1}$$

where

$$V_A = V_{CEsat Q2} + V_{sense 1} + V_{D2}$$

If the oscillator pin (9) is connected to ground the load current falls to zero as shown in fig. 1.

At the time t_2 the channel 1 is disabled, by taking the inputs V_{in1} low and/or $\overline{EN}$ high, and the output transistor Q2 is turned off. The load current flows through D2 and D1 according to the law:

$$I = \left(\frac{V_B}{R1} + I_{T2} \right) e^{-\frac{R1 t}{L1}} - \frac{V_B}{R1}$$

where

$$V_B = V_s + V_{D1} + V_{D2}$$

I_{T2} = current value at the time t_2 .

Fig. 2 in shows the current waveform obtained with an RC network connected between pin 9 and ground. From to t_1 the current increases as in fig. 1. A difference exists at the time t_2 because the current starts to increase again. At this time a pulse is produced by the oscillator circuit that resets the flip flop, FF1, and switches on the output transistor, Q1. The current increases until the drop on the sensing resistor R_{S1} is equal to V_{ref1} (t_3) and the cycle repeats.

The switching frequency depends on the values of R and C, as shown in fig. 4 and must be chosen in the range 10 to 30 KHz.

It is possible with external hardware to change the reference voltage V_{ref} in order to obtain a high peak current I_p and a lower holding current I_h (see fig. 3).

The L295 is provided with a thermal protection that switches off all the output transistors when the junction temperature exceeds 150°C. The presence of a hysteresis circuit makes the IC work again after a fall of the junction temperature of about 20°C.

The analog input pins (V_{ref1} , V_{ref2}) can be left open or connected to V_{SS} ; in this case the circuit works with an internal reference voltage of about 2.5V and the peak current in the load is fixed only by the value of R_S :

$$I_p = \frac{2.5}{R_S}$$

Fig. 1 – Load current waveform with pin 9 connected to GND.



S - 5063



L296 L296P

ADVANCE DATA

HIGH CURRENT SWITCHING REGULATORS

- 4A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 100% DUTY CYCLE RANGE
- PRECISE ($\pm 2\%$) ON-CHIP REFERENCE
- SWITCHING FREQUENCY UP TO 200KHz
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- RESET OUTPUT
- EXTERNAL PROGRAMMABLE LIMITING CURRENT (L296P)
- CONTROL CIRCUIT FOR CROWBAR SCR
- INPUT FOR REMOTE INHIBIT AND SYNCHRONOUS PWM
- THERMAL SHUTDOWN.

The L296 and L296P are stepdown power switching regulators delivering 4A at a voltage variable from 5.1V to 40V.

Features of the devices include soft start, remote

inhibit, thermal protection, a reset output for microprocessors and a PWM comparator input for synchronization in multichip configurations.

The L296P includes external programmable limiting current.

The L296 and L296P are mounted in a 15-lead Multiwatt[®] plastic power package and requires very few external components.

Efficient operation at switching frequencies up to 200KHz allows a reduction in the size and cost of external filter components. A voltage sense input and SCR drive output are provided for optional crowbar overvoltage protection with an external SCR.

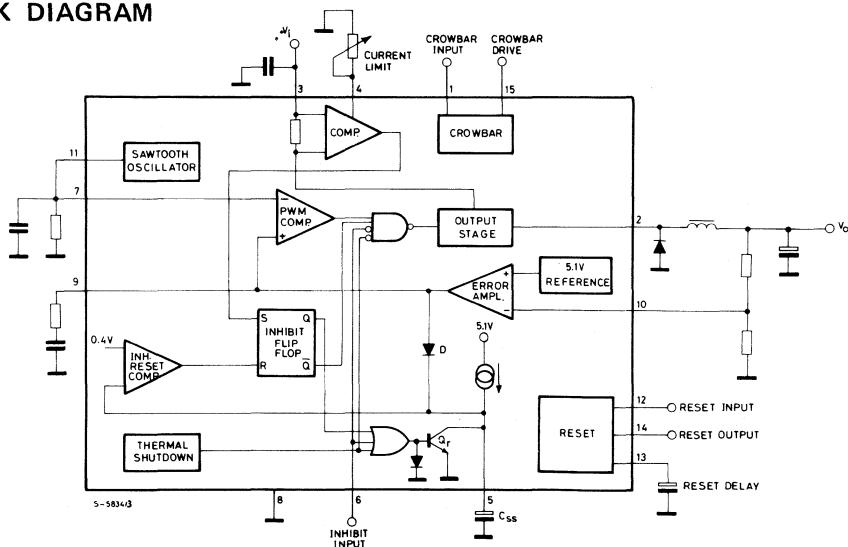


ORDERING NUMBER:

L296
L296P

L296HT
L296PHT

BLOCK DIAGRAM



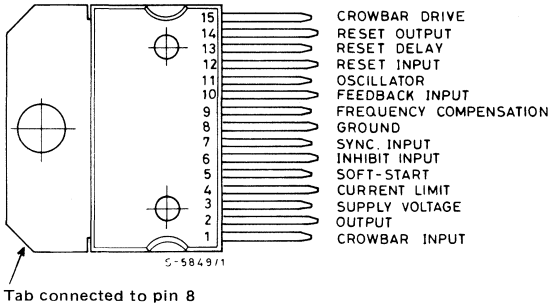
ABSOLUTE MAXIMUM RATINGS

V_i	Input voltage (pin 3)	50	V
$V_i - V_2$	Input to output voltage difference	50	V
V_2	Output DC voltage	-1	V
	Output peak voltage at $t = 0.1 \mu\text{sec}$ $f = 200 \text{ kHz}$	-7	V
V_1, V_{12}	Voltage at pins 1, 12	10	V
V_{15}	Voltage at pin 15	15	V
$V_4, V_5, V_7, V_9, V_{13}$	Voltage at pins 4, 5, 7, 9 and 13	5.5	V
V_{10}, V_6	Voltage at pins 10 and 6	7	V
V_{14}	Voltage at pin 14 ($I_{14} \leq 1 \text{ mA}$)	V_i	
I_9	Pin 9 sink current	1	mA
I_{11}	Pin 11 source current	20	mA
I_{14}	Pin 14 sink current ($V_{14} < 5\text{V}$)	50	mA
P_{tot}	Power dissipation at $T_{\text{case}} \leq 90^\circ\text{C}$	20	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	$^\circ\text{C}$

THERMAL DATA

$R_{\text{th j-case}}$	Thermal resistance junction-case	max	3 $^\circ\text{C/W}$
$R_{\text{th j-amb}}$	Thermal resistance junction-ambient	max	35 $^\circ\text{C/W}$

CONNECTION DIAGRAM
(top view)





L296
L296P

PIN FUNCTIONS

N°	NAME	FUNCTION
1	CROWBAR INPUT	Voltage sense input for crowbar overvoltage protection. Normally connected to the feedback input thus triggering the SCR when V_{out} exceeds nominal by 20%. May also monitor the input and a voltage divider can be added to increase the threshold. Connected to ground when SCR not used.
2	OUTPUT	Regulator output.
3	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the L296's internal logic.
4	CURRENT LIMIT	A resistor connected between this terminal and ground sets the current limiter threshold. If this terminal is left unconnected the threshold is internally set (see electrical characteristics).
5	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
6	INHIBIT INPUT	TTL – level remote inhibit. A logic high level on this input disables the device.
7	SYNC INPUT	Multiple L296s are synchronized by connecting the pin 7 inputs together and omitting the oscillator RC network on all but one device.
8	GROUND	Common ground terminal.
9	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
10	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
11	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.



PIN FUNCTIONS (continued)

N°	NAME	FUNCTION
12	RESET INPUT	Input of the reset circuit. The threshold is roughly 5V. It may be connected to the feedback point or via a divider to the input.
13	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
14	RESET OUTPUT	Open collector reset signal output. This output is high when the supply is safe.
15	CROWBAR OUTPUT	SCR gate drive output of the crowbar circuit.

CIRCUIT OPERATION (refer to the block diagram)

The L296 and L296P are monolithic stepdown switching regulators providing output voltages from 5.1V to 40V and delivering 4A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to $\pm 2\%$). This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage. The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 9. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source.

Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator

resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V. The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network.

The reset circuit generates an output signal when the supply voltage exceeds a threshold programmed by an external divider. The reset signal is generated with a delay time programmed by an external capacitor. When the supply falls below the threshold the reset output goes low immediately. The reset output is an open collector.

The crowbar circuit senses the output voltage and the crowbar output can provide a current of 100 mA to switch on an external SCR. This SCR is triggered when the output voltage exceeds the nominal by 20%. There is no internal connection between the output and crowbar sense input therefore the crowbar can monitor either the input or the output.

A TTL - level inhibit input is provided for applications such as remote on/off control. This input is activated by high logic level and disables circuit operation. After an inhibit the L296 restarts under control of the soft start network.

The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

CIRCUIT OPERATION (continued)

Fig. 1 – Reset output waveforms

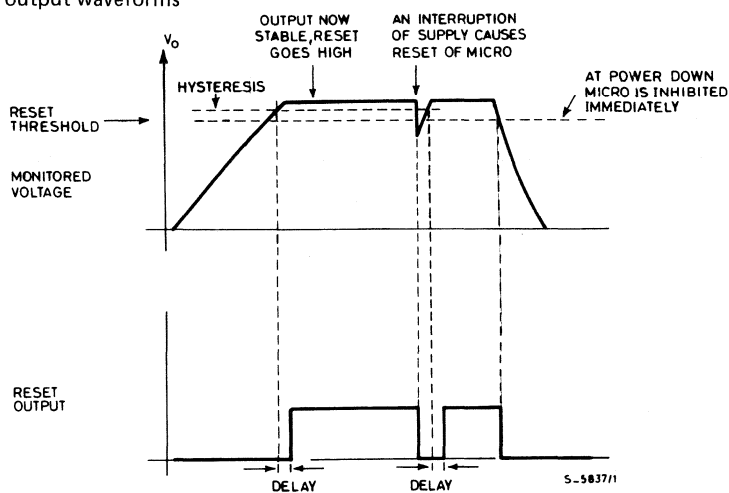


Fig. 2 – Soft start waveforms

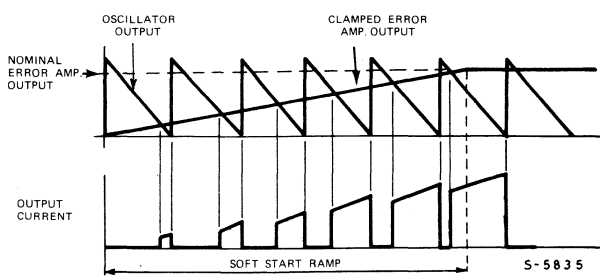
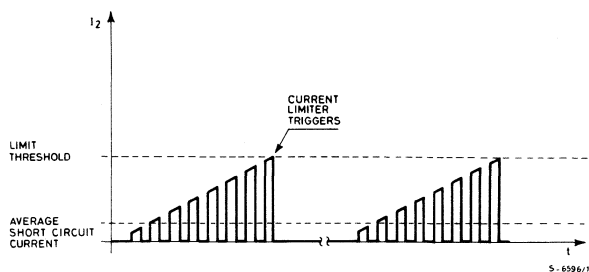


Fig. 3 – Current limiter waveforms





L296
L296P

ELECTRICAL CHARACTERISTICS (Refer to the test circuits $T_J = 25^\circ\text{C}$, $V_I = 35\text{V}$, unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
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DYNAMIC CHARACTERISTICS (pin 6 to GND unless otherwise specified)

V _O	Output voltage range	V _I = 46V I _O = 1 A		V _{ref}		40	V	4
V _I	Input voltage range	V _O = V _{ref} to 36V I _O ≤ 3A		9		46	V	4
V _I	Input voltage range	Note (1) V _O = V _{REF} to 36V I _O = 4A				46	V	4
ΔV _O	Line regulation	V _I = 10V to 40V, V _O = V _{ref} , I _O = 2A			15	50	mV	4
ΔV _O	Load regulation	V _O = V _{ref}	I _O = 2A to 4A		10	30	mV	4
			I _O = 0.5A to 4A		15	45	mV	4
V _{ref}	Internal reference voltage (pin 10)	V _I = 9V to 46V I _O = 2A		5	5.1	5.2	V	4
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of reference voltage	T _j = 0°C to 125°C I _O = 2A			0.4		mV/°C	
V _d	Dropout voltage between pin 2 and pin 3	I _O = 4A			2	3.2	V	4
		I _O = 2A			1.3	2.1	V	4
I _{2L}	Current limiting threshold (pin 2)	L296 pin 4 open V _I = 9V to 40V V _O = V _{ref} to 36V		4.5		7.5	A	4
		L296P V _I = 9V to 40V V _O = V _{ref}	pin 4 open	5		7	A	4
			R _{lim} = 22KΩ	2.5		4.5	A	4
I _{SH}	Input average current	V _I = 46V; Output short-circuited			60	100	mA	4
η	Efficiency	I _O = 3A	V _O = V _{ref}		75		%	4
			V _O = 12V		85		%	4
SVR	Supply voltage ripple rejection	ΔV _i = 2V _{rms} V _O = V _{ref}	f _{ripple} = 100Hz I _O = 2A	50	56		dB	4
f	Switching frequency	∞		85	100	115	KHz	4
$\frac{\Delta f}{\Delta V_i}$	Voltage stability of switching frequency	V _I = 9V to 46V			0.5		%	4
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	T _j = 0°C to 125°C			1		%	4
f _{max}	Maximum operating switching frequency	V _O = V _{ref} ; I _O = 1A		200			KHz	—
T _{sd}	Thermal shutdown junction temperature			135	145		°C	—

DC CHARACTERISTICS

I_{3Q}	Quiescent drain curr.	$V_I = 46\text{V}$ $V_7 = 0\text{V}$ S1 : B S2 : B	$V_6 = 0\text{V}$		66	85	mA	6a
			$V_6 = 3\text{V}$		30	40	mA	6a
$-I_{2L}$	Output leakage curr.	$V_I = 46\text{V}$, $V_6 = 3\text{V}$, S1 : B, S2 : A, $V_7 = 0\text{V}$				2	mA	6a

Note (1) : Using min. 7A schottky diode

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
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SOFT START

$I_{5\text{ so}}$	Source current	$V_6 = 0\text{V}, V_5 = 3\text{V}$	100	130	160	μA	6b
$I_{5\text{ si}}$	Sink current	$V_6 = 3\text{V}, V_5 = 3\text{V}$	50	70	120	μA	6b

INHIBIT

$V_{6\text{L}}$	Low input voltage	$V_1 = 9\text{V to } 46\text{V}$	$S1 : B$	-0.3		0.8	V	6a
$V_{6\text{H}}$	High input voltage	$V_7 = 0\text{V}$	$S2 : B$	2		5.5	V	6a
$-I_{6\text{L}}$	Input current with low input voltage	$V_1 = 9\text{V to } 46\text{V}$	$V_6 = 0.8\text{V}$			10	μA	6a
$-I_{6\text{H}}$	Input current with high input voltage	$V_7 = 0\text{V}$ $S1 : B$ $S2 : B$	$V_6 = 2\text{V}$			3	μA	6a

ERROR AMPLIFIER

$V_{9\text{H}}$	High level output volt.	$V_{10} = 4.7\text{V}, I_9 = 100\mu\text{A}, S1 : A, S2 : A$	3.5				V	6c
$V_{9\text{L}}$	Low level output volt.	$V_{10} = 5.3\text{V}, I_9 = 100\mu\text{A}, S1 : A, S2 : E$			0.5		V	6c
$I_{9\text{ si}}$	Sink output current	$V_{10} = 5.3\text{V}, S1 : A, S2 : B$	100	150			μA	6c
$-I_{9\text{ so}}$	Source output current	$V_{10} = 4.7\text{V}, S1 : A, S2 : D$	100	150			μA	6c
I_{10}	Input bias current	$V_{10} = 5.2\text{V}, S1 : B$		2	10		μA	6c
		$V_{10} = 6.4\text{V}, S1 : B, L296P$		2	10		μA	6c
G_v	DC open loop Gain	$V_9 = 1\text{V to } 3\text{V}, S1 : A, S2 : C$	46	55			dB	6c

OSCILLATOR AND PWM COMPARATOR

$-I_7$	Input bias current of PWM comparator	$V_7 = 0.5\text{V to } 3.5\text{V}$			5		μA	6a
$-I_{11}$	Oscillator source curr.	$V_{11} = 2\text{V}, S1 : A, S2 : B$	5				mA	6A

RESET

V _{12 R}	Rising threshold voltage	V _I = 9V to 46V, S1 : B, S2 : B		V _{ref} -150mV	V _{ref} -100mV	V _{ref} -50mV	V	6d
V _{12 F}	Falling threshold voltage			4.75	V _{ref} -150mV	V _{ref} -100mV	V	6d
V _{13 D}	Delay threshold volt.	V ₁₂ = 5.3V, S1 : A, S2 : B		4.3	4.5	4.7	V	6d
V _{13 H}	Delay threshold voltage hysteresis				100		mV	6d
V _{14 S}	Output saturation volt.	I ₁₄ = 16mA; V ₁₂ = 4.7V; S1, S2 : B				0.4	V	6d
I ₁₂	Input bias current	V ₁₂ = 0V to V _{ref} , S1 : B, S2 : B			1	3	μA	6d
-I _{13 so}	Delay source current	V ₁₃ = 3V S1 : A S2 : B	V ₁₂ = 5.3V	70	110	140	μA	6d
I _{13 si}	Delay sink current		V ₁₂ = 4.7V	10			mA	6d
I ₁₄	Output leakage curr.	V _I = 46V, V ₁₂ = 5.3V, S1 : B, S2 : A				100	μA	6d

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
CROWBAR						
V ₁ Input threshold voltage	S1 : B	5.5	6	6.4	V	6b
V ₁₅ Output saturation voltage	V _i = 9V to 46V, I ₁₅ = 5mA V ₁ = 5.4V S1 : A		0.2	0.4	V	6b
I ₁ Input bias current	V ₁ = 6V, S1 : B			10	μA	6b
-I ₁₅ Output source current	V _i = 9V to 46V, V ₁₅ = 2V V ₁ = 6.5V S1 : B	70	100		mA	6b

Fig. 4 – Dynamic test circuit

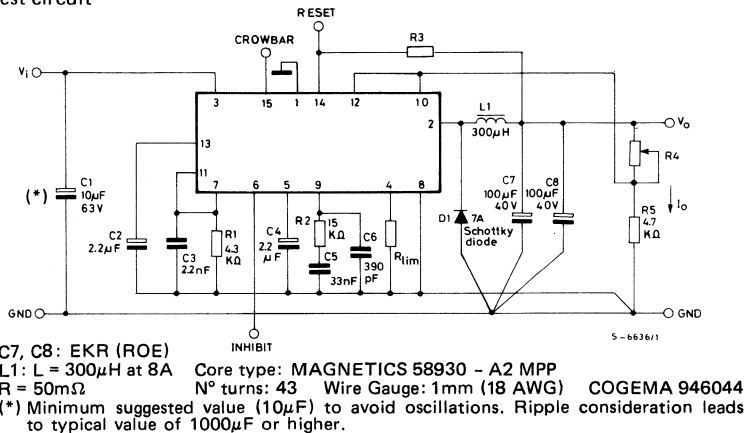


Fig. 5 – PC. board and component layout of the circuit of fig. 4 (1:1 scale)

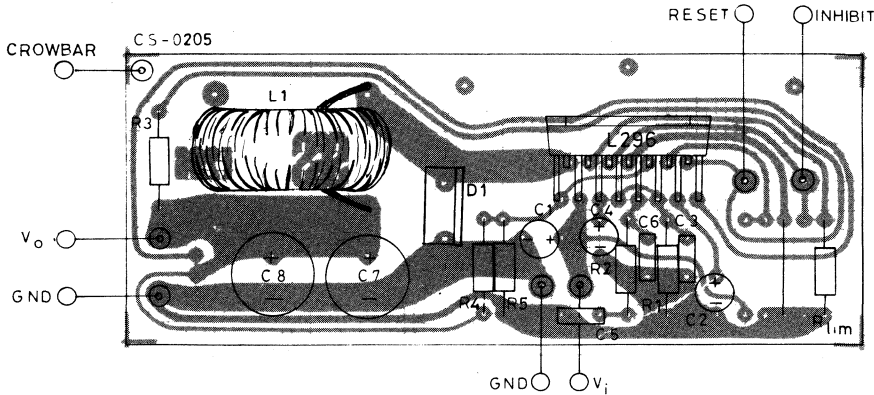


Fig. 6 - DC test circuits

Fig. 6a

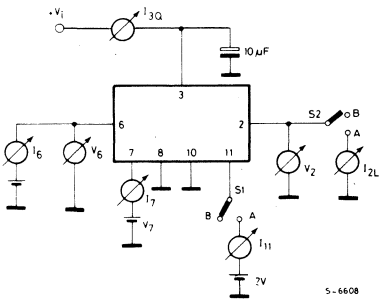


Fig. 6b

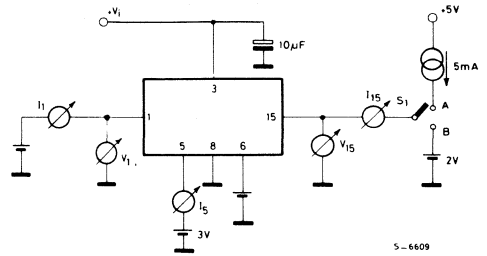


Fig. 6c

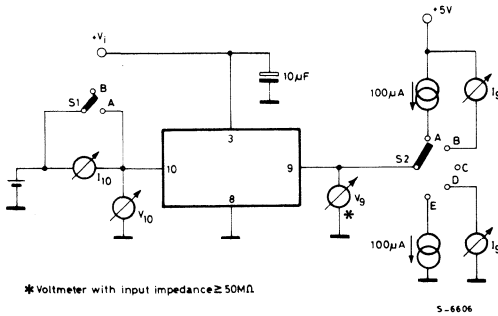
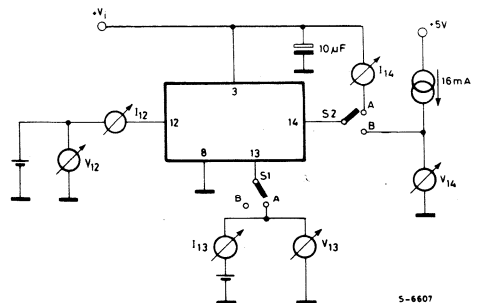


Fig. 6d



- 1 - Set V_{10} for $V_9 = 1V$
- 2 - Change V_{10} to obtain $V_9 = 3V$
- 3 - $G_v = \frac{\Delta V_9}{\Delta V_{10}} = \frac{2V}{\Delta V_{10}}$

Fig. 7 - Quiescent drain current vs. supply voltage (0% duty cycle - see fig. 6a)

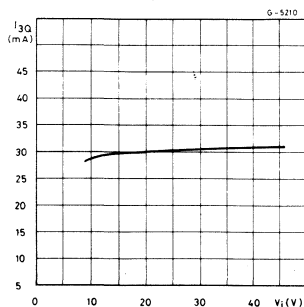


Fig. 8 - Quiescent drain current vs. supply voltage (100% duty cycle see fig. 6a)

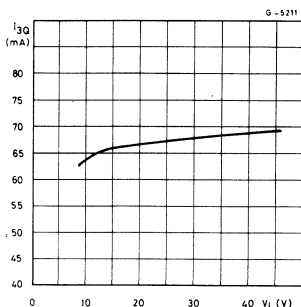


Fig. 9 - Quiescent drain current vs. junction temperature (0% duty cycle - see fig. 6a)

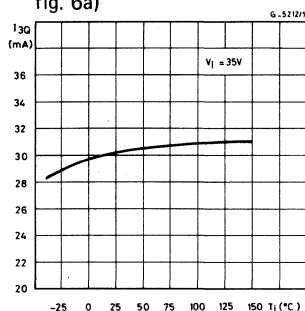


Fig. 10 - Quiescent drain current vs. junction temperature (100% duty cycle - see fig. 6a)

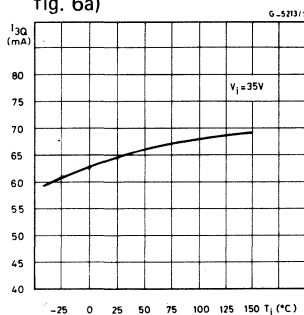


Fig. 11 - Reference voltage (pin 10) vs. V_i (see fig. 4)

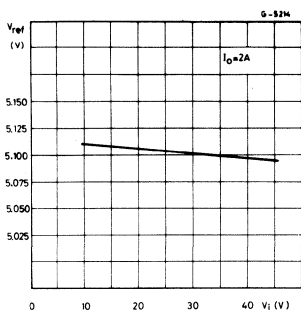


Fig. 12 - Reference voltage (pin 10) vs. junction temperature (see fig. 4)

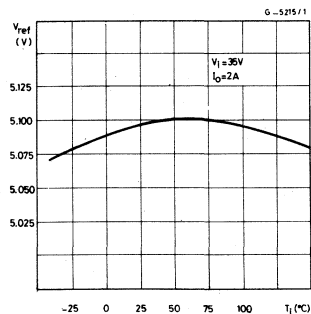


Fig. 13 - Open loop frequency and phase response of error amplifier (see fig. 6c)

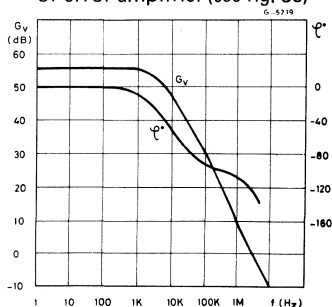


Fig. 14 - Switching frequency vs. input voltage (see fig. 4)

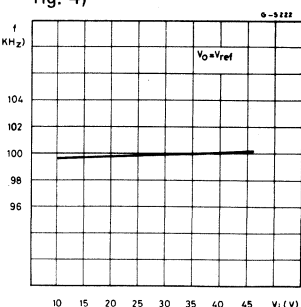


Fig. 15 - Switching frequency vs. junction temperature (see fig. 4)

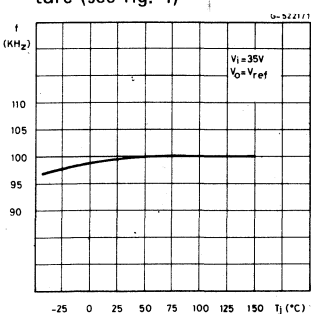


Fig. 16 - Switching frequency vs. R1 (see fig. 4)

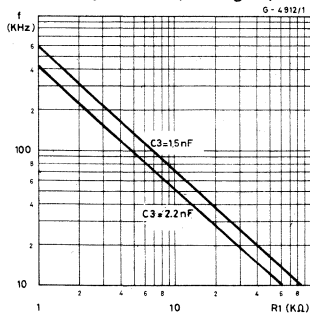


Fig. 17 - Line transient response (see fig. 4)

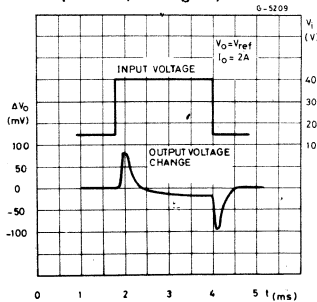


Fig. 18 - Load transient response (see fig. 4)

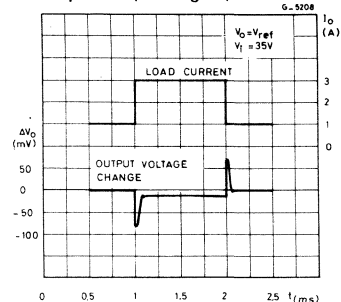


Fig. 19 - Supply voltage ripple rejection vs. frequency (see fig. 4)

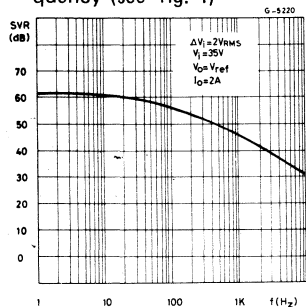


Fig. 20 - Dropout voltage between pin 3 and pin 2 vs. current at pin 2

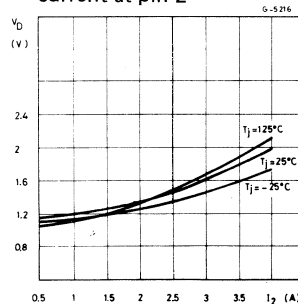


Fig. 21 - Dropout voltage between pin 3 and pin 2 vs. junction temperature

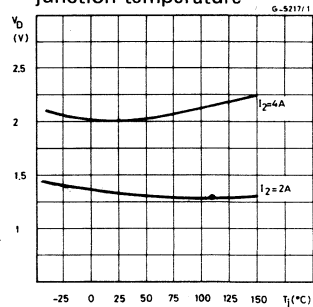


Fig. 22 - Power dissipation derating curve

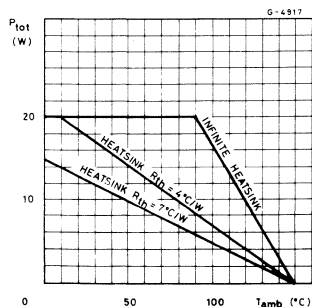


Fig. 23 - Power dissipation (device only) vs. input voltage

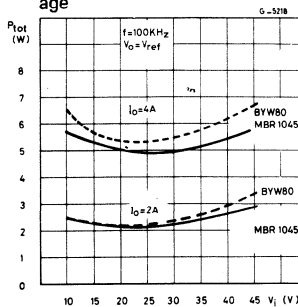


Fig. 24 - Power dissipation (device only) vs. input voltage

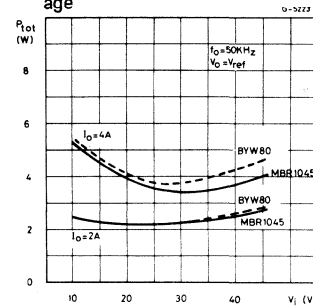


Fig. 25 - Power dissipation (device only) vs. output voltage (see fig. 4)

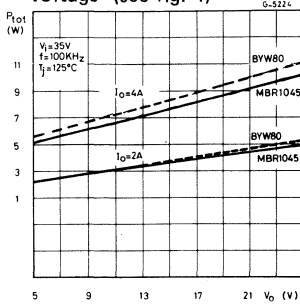


Fig. 26 - Power dissipation (device only) vs. output voltage (see fig. 4)

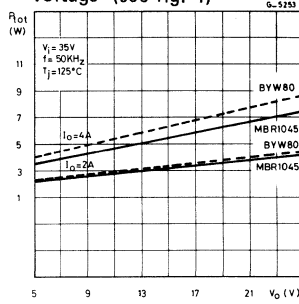


Fig. 27 - Voltage and current waveforms at pin 2 (see fig. 4)

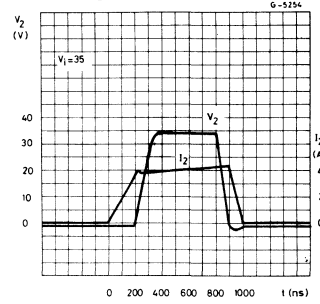


Fig. 28 - Efficiency vs. output current

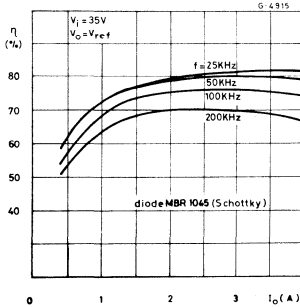


Fig. 29 - Efficiency vs. output current

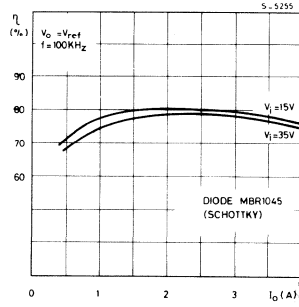


Fig. 30 - Efficiency vs. output voltage

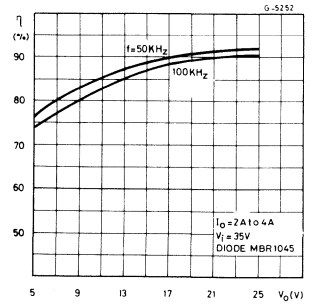


Fig. 31 - Current limiting threshold vs. R_{pin4} (L296P only)

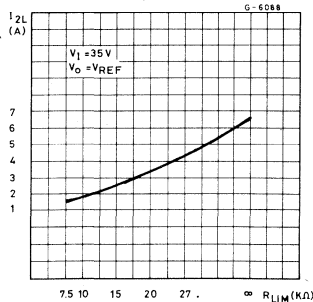


Fig. 32 - Current limiting threshold vs. junction temperature

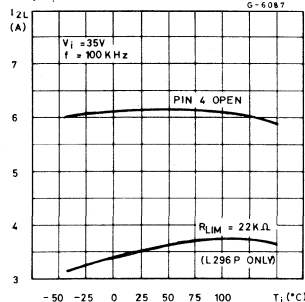
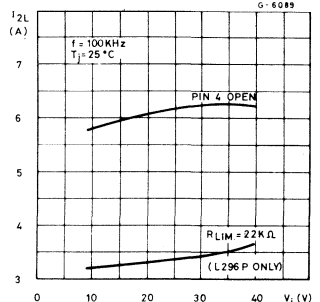


Fig. 33 - Current limiting threshold vs. supply voltage



SELECTION OF COMPONENT VALUES (See fig. 31)

Component	Recommended Value	Purpose	Allowed rage		NOTES
			Min	Max	
R1 R2	— 100 kΩ	Set input voltage threshold for reset.	—	220 kΩ	$R1/R2 = \frac{V_{i \min}}{5} - 1$ If output voltage is sensed R1 and R2 may be limited and pin 12 connected to pin 10.
R3	4.3 kΩ	Sets switching frequency	1 kΩ	100 kΩ	
R4	10 kΩ	Pull-down resistor		22 kΩ	May be omitted and pin 6 grounded if inhibit not used.
R5	15 kΩ	Frequency compensation	10 kΩ		
R6		Collector load for reset output	$\frac{V_o}{0.05A}$		Omitted if reset function not used.
R7 R8	— 4.7 kΩ	Divider to set output voltage	— —	— 10 kΩ	$R7/R8 = \frac{V_o - V_{ref}}{V_{ref}} -$
R _{lim}	—	Sets current limit level	7.5 kΩ		If R _{lim} is omitted and pin 4 left open the current limit is internally fixed.
C1	10 μF	Stability	2.2 μF		
C2	2.2 μF	Sets reset delay	—	—	Omitted if reset function not used.
C3	2.2 nF	Sets switching frequency	1 nF	3.3 nF	
C4	2.2 μF	Soft start	1 μF	—	Also determines average short circuit current.
C5	33 nF	Frequency compensation			
C6	390 pF	High frequency compensation	—	—	Not required for 5V operation
C7,C8 L1	100 μF 300 μH	Output filter	— 100 μH	—	
Q1		Crowbar protection			The SCR must be able to withstand the peak discharge current of the output capacitor and the short circuit current of the device.
D1		Recirculation diode			7A schottky or 35ns t _{rr} diode.

APPLICATION INFORMATION (continued)

Fig. 36 - A minimal 5.1V fixed regulator. Very few components are required

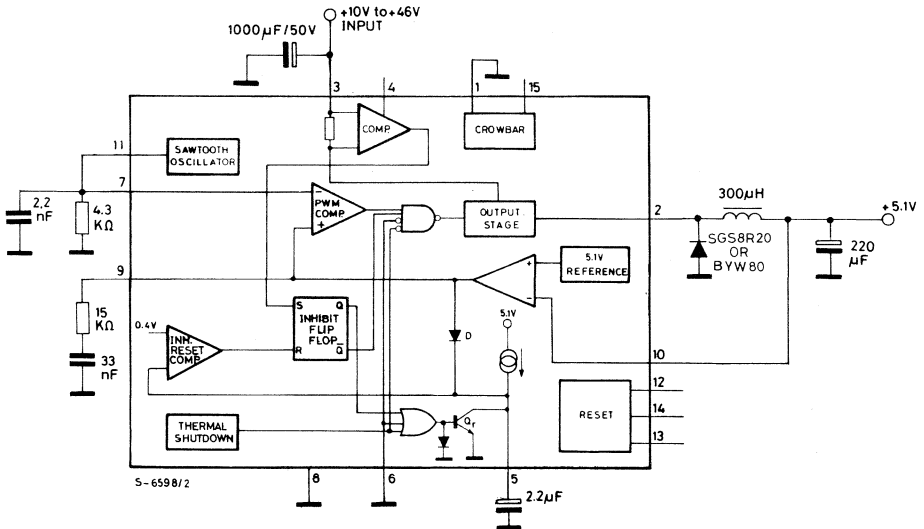
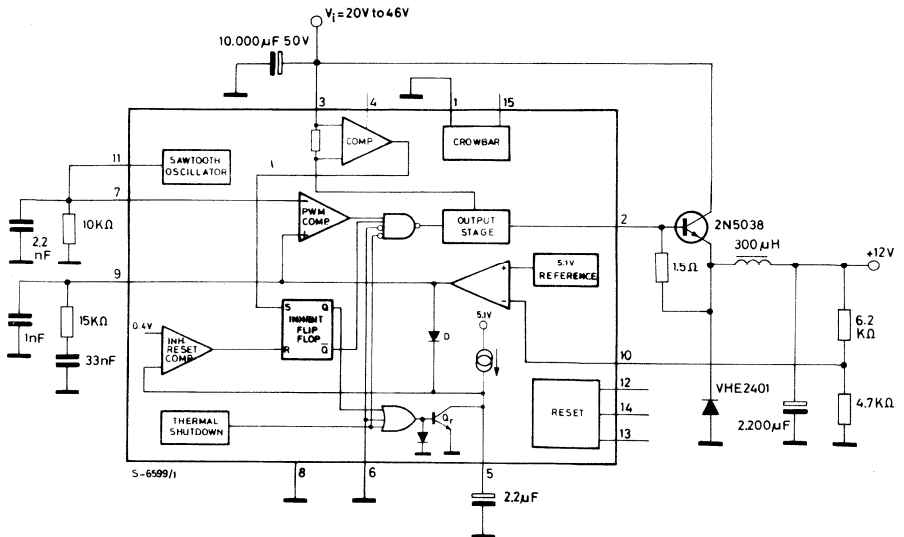
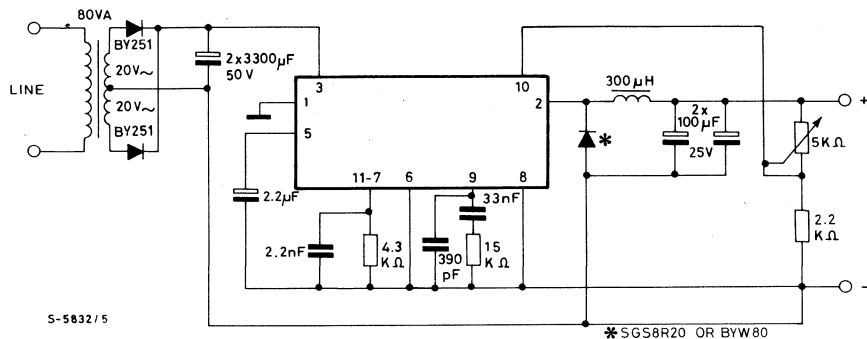


Fig. 37 - 12V/10A Power supply



APPLICATION INFORMATION (continued)

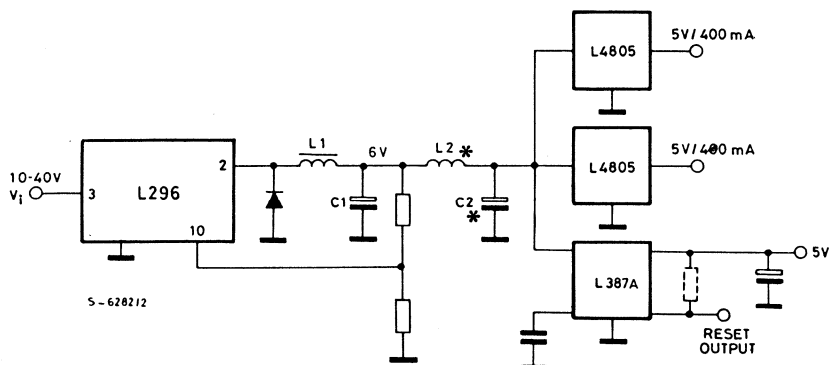
Fig. 38 – Programmable power supply

 $V_0 = 5.1 \text{ to } 15V$ $I_o = 4A$ max. (min. load current = 100 mA) $\text{ripple} \leq 20 \text{ mV}$

load regulation (1A to 4A) = 10 mV ($V_o = 5.1V$)

line regulation (220V $\pm$ 15% and to $I_o = 3A$) = 15 mV ($V_o = 5.1V$)

Fig. 39 – Preregulator for distributed supplies



(*) L2 and C2 are necessary to reduce the switching frequency spikes.

APPLICATION INFORMATION (continued)

Fig. 40 - In multiple supplies several L296s can be synchronized as shown.

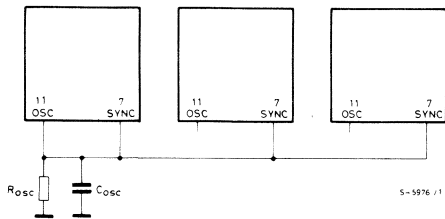


Fig. 41 - Voltage sensing for remote load

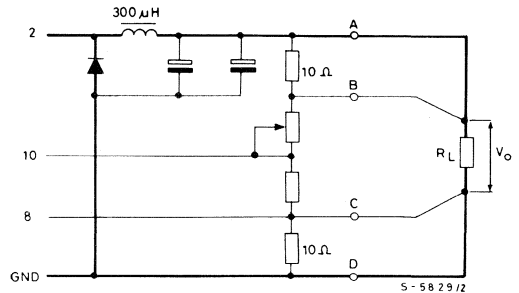
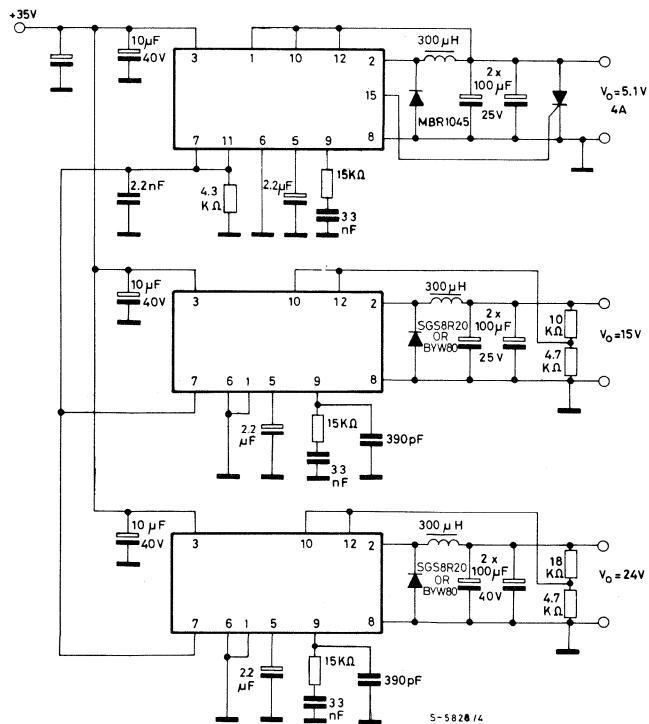


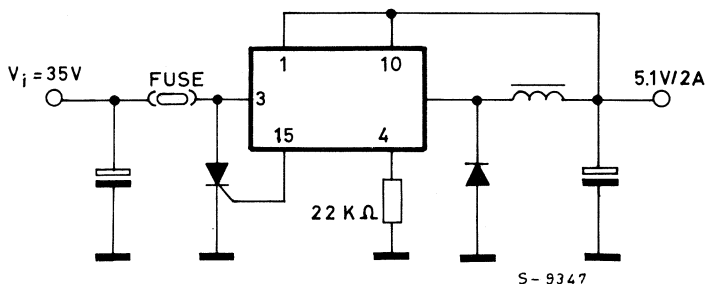
Fig. 42 - A 5.1V/15V/24V multiple supply. Note the synchronization of the three L296s.





L296
L296P

Fig. 43 – 5.1V/2A Power supply using external limiting current resistor and crowbar protection on the supply voltage (L296P only)

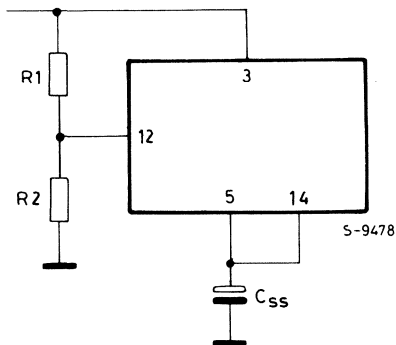


SOFT-START AND REPETITIVE POWER-ON

When the device is repetitively powered-on, the soft-start capacitor, C_{SS} , must be discharged rapidly to ensure that each start is "soft". This can be achieved economically using the reset circuit, as shown in Fig. 44.

In this circuit the divider R_1 , R_2 connected to pin 12 determines the minimum supply voltage, below which the open collector transistor at the pin 14 output discharges C_{SS} .

Fig. 44

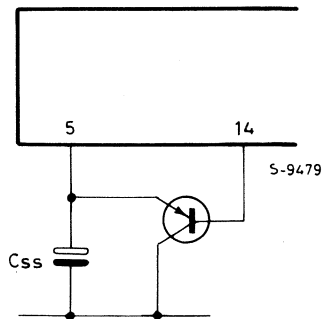


The approximate discharge times obtained with this circuit are:

C_{SS}	t_{DIS}
$2.2\mu F$	$200\mu s$
$4.7\mu F$	$300\mu s$
$10\mu F$	$600\mu s$

If these times are still too long, an external PNP transistor may be added, as shown in Fig. 45; with this circuit discharge times of a few microseconds may be obtained.

Fig. 45



HOW TO OBTAIN BOTH RESET AND POWER FAIL

Figure 46 illustrates how it is possible to obtain at the same time both the power fail and reset functions simply by adding one diode (D) and one resistor (R).

In this case the reset delay time (pin 13) can only start when the output voltage is $V_o \geq V_{REF} - 100\text{mV}$ and the voltage across R2 is higher than 4.5V.

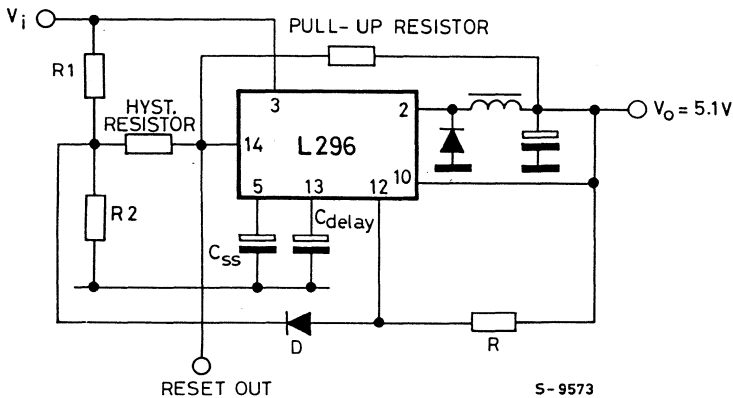
With the hysteresis resistor it is possible to fix the input pin 12 hysteresis in order to increase

immunity to the 100Hz ripple present on the supply voltage.

Moreover, the power fail and reset delay time are automatically locked to the soft start. Soft start and delayed reset are thus two sequential functions.

The hysteresis resistor should be in the range of about $100\text{K}\Omega$ and the pull-up resistor of 1 to $2.2\text{K}\Omega$.

Fig. 46



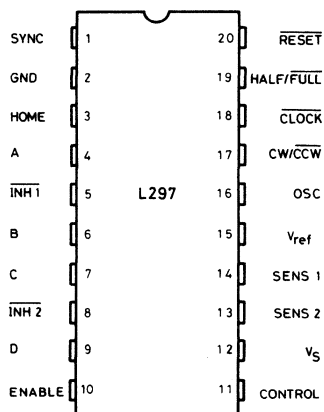
S-9573





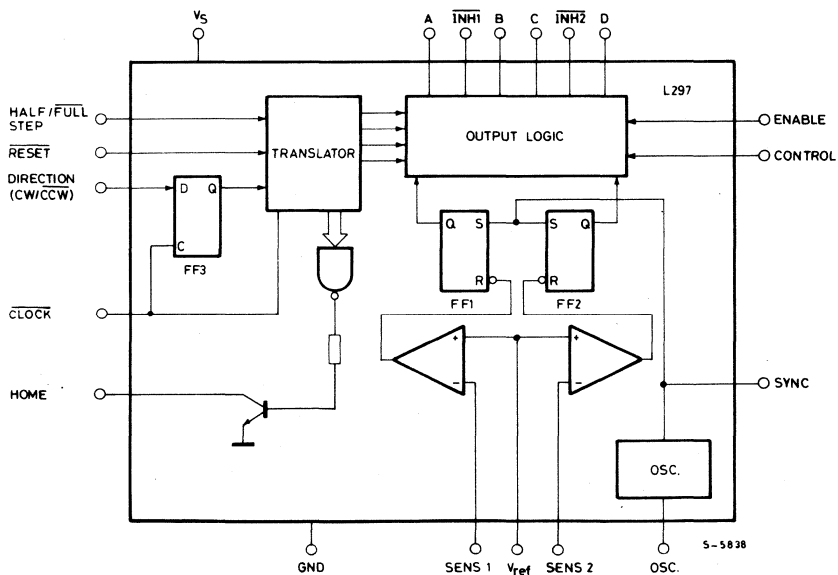
L297
L297A

CONNECTION DIAGRAM



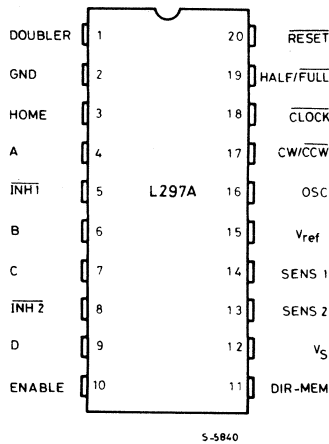
S-5839

BLOCK DIAGRAM

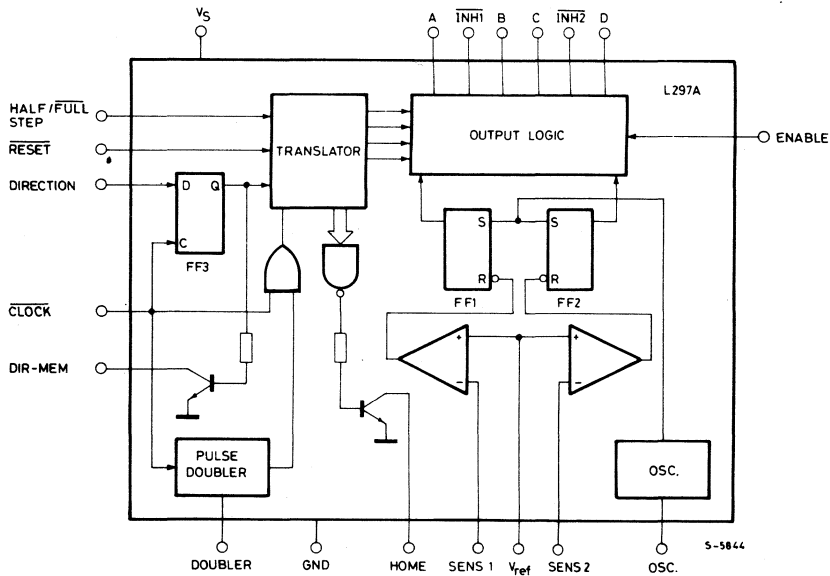


S-5838

CONNECTION DIAGRAM



BLOCK DIAGRAM



THERMAL DATA

R _{th j-amb}	Thermal resistance junction-ambient	max.	80	°C/W
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L297
L297A

PIN FUNCTIONS – L297

N°	NAME	FUNCTION
1	SYNC	Output of the on-chip chopper oscillator. The SYNC connections of all L297s to be synchronized are connected together and the oscillator components are omitted on all but one. If an external clock source is used it is injected at this terminal.
2	GND	Ground connection.
3	HOME	Open collector output that indicates when the L297 is in its initial state (ABCD = 0101). The transistor is open when this signal is active.
4	A	Motor phase A drive signal for power stage.
5	$\overline{\text{INH1}}$	Active low inhibit control for driver stages of A and B phases. When a bipolar bridge is used this signal can be used to ensure fast decay of load current when a winding is de-energized. Also used by chopper to regulate load current if CONTROL input is low.
6	B	Motor phase B drive signal for power stage.
7	C	Motor phase C drive signal for power stage.
8	$\overline{\text{INH2}}$	Active low inhibit control for drive stages of C and D phases. Same functions as $\overline{\text{INH1}}$.
9	D	Motor phase D drive signal for power stage.
10	ENABLE	Chip enable input. When low (inactive) $\overline{\text{INH1}}$, $\overline{\text{INH2}}$, A, B, C and D are brought low.
11	CONTROL	Control input that defines action of chopper. When low chopper acts on $\overline{\text{INH1}}$ and $\overline{\text{INH2}}$; when high chopper acts on phase lines ABCD.
12	V_s	5V supply input.
13	SENS ₂	Input for load current sense voltage from power stages of phases C and D.



L297
L297A

PIN FUNCTIONS – L297(continued)

N°	NAME	FUNCTION
14	SENS ₁	Input for load current sense voltage from power stages of phases A and B.
15	V _{ref}	Reference voltage for chopper circuit. A voltage applied to this pin determines the peak load current.
16	OSC	An RC network (R to V _{CC} , C to ground) connected to this terminal determines the chopper rate. This terminal is connected to ground on all but one device in synchronized multi-L297 configurations. $f \cong 1/0.69 RC$, $R > 10 \text{ k}\Omega$.
17	CW/ $\overline{\text{CCW}}$	Clockwise/counterclockwise direction control input. Physical direction of motor rotation also depends on connection of windings. Synchronized internally therefore direction can be changed at any time.
18	$\overline{\text{CLOCK}}$	Step clock. An active low pulse on this input advances the motor one increment. The step occurs on the rising edge of this signal.
19	HALF/ $\overline{\text{FULL}}$	Half/full step select input. When high selects half step operation; when low selects full step operation. One-phase-on full step mode is obtained by selecting FULL when the L297's translator is at an even-numbered state. Two-phase-on full step mode is set by selecting FULL when the translator is at an odd numbered position. (The home position is designated state 1).
20	$\overline{\text{RESET}}$	Reset input. An active low pulse on this input restores the translator to the home position (state 1, ABCD = 0101).



PIN FUNCTIONS - L297A

Pin function of the L297A are identical to those of the L297 except for pins 1 and 11.

N°	NAME	FUNCTIONS
1	DOUBLER	An RC network connected to this pin determines the delay between an input clock pulse and the corresponding ghost pulse.
11	DIR-MEM	Direction Memory. Inverted output of the direction flip flop. Open collector output.

CIRCUIT OPERATION

The L297(A) is intended for use with a dual bridge driver, quad darlington array or discrete power devices in step motor driving applications. It receives step clock, direction and mode signals from the systems controller (usually a microcomputer chip) and generates control signals for the power stage.

The principal functions are a translator, which generates the motor phase sequences, and a dual PWM chopper circuit which regulates the current in the motor windings. The translator generates three different sequences, selected by the HALF/FULL input. These are normal (two phases energised), wave drive (one phase energised) and half-step (alternately one phase energised/two phases energised). Two inhibit signals are also generated by the L297 in half step and wave drive modes. These signals, which connect directly to the L298's enable inputs, are intended to speed current decay when a winding is de-energised. When the L297 is used to drive a unipolar motor the chopper acts on these lines.

An input called CONTROL determines whether the chopper will act on the phase lines ABCD or the inhibit lines INH1 and INH2. When the phase lines are chopped the non-active phase line of each pair (AB or CD) is activated (rather than interrupting the line then active). In L297 + L298 configurations this technique reduces dissipation in the load current sense resistors.

A common on-chip oscillator drives the dual chopper. It supplies pulses at the chopper rate which set the two flip-flops FF1 and FF2. When the current in a winding reaches the programmed peak value the voltage across the sense resistor (connected to one of the sense inputs SENS₁ or SENS₂) equals V_{ref} and the corresponding comparator resets its flip flop, interrupting the drive current until the next oscillator pulse arrives. The peak current for both windings is programmed by a voltage divider on the V_{ref} input.

Ground noise problems in multiple configurations can be avoided by synchronising the chopper oscillators. This is done by connecting all the SYNC pins together, mounting the oscillator RC network on one device only and grounding the OSC pin on all other devices.

The L297A includes a pulse doubler on the step clock line which is intended to simplify the implementation of multiple stepping. A ghost pulse is generated automatically after each input pulse, delayed by the time $0.75 R_d C_d$.

The RC network should be dimensioned to place the ghost pulse roughly halfway between clock pulses. If pin 1 (DOUBLER) is grounded the doubler function is disabled.



L297
L297A

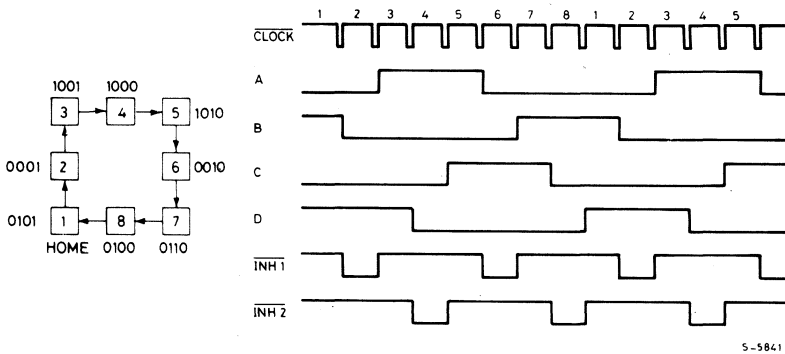
MOTOR DRIVING PHASE SEQUENCES

The L297's translator generates phase sequences for normal drive, wave drive and half step modes. The state sequences and output waveforms for these three modes are shown below. In all cases the translator advances on the low to high transition of $\overline{\text{CLOCK}}$.

Clockwise rotation is indicated; for anticlockwise rotation the sequences are simply reversed. $\overline{\text{RESET}}$ restores the translator to state 1, where $\text{ABCD} = 0101$.

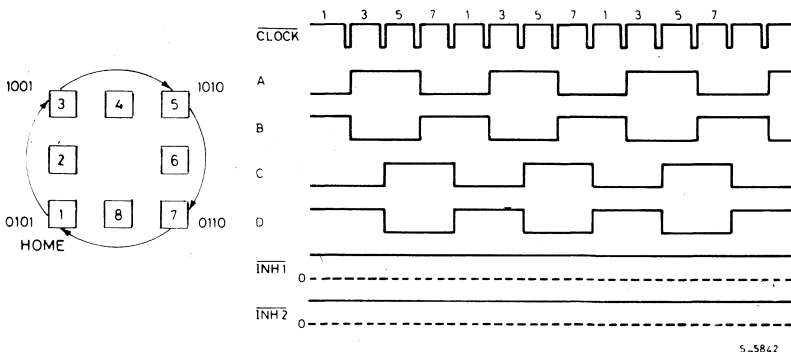
Half step mode

Half step mode is selected by a high level on the $\text{HALF}/\overline{\text{FULL}}$ input.



Normal drive mode

Normal drive mode (also called "two-phase-on" drive) is selected by a low level on the $\text{HALF}/\overline{\text{FULL}}$ input when the translator is at an odd numbered state (1, 3, 5 or 7). In this mode the INH1 and INH2 outputs remain high throughout.



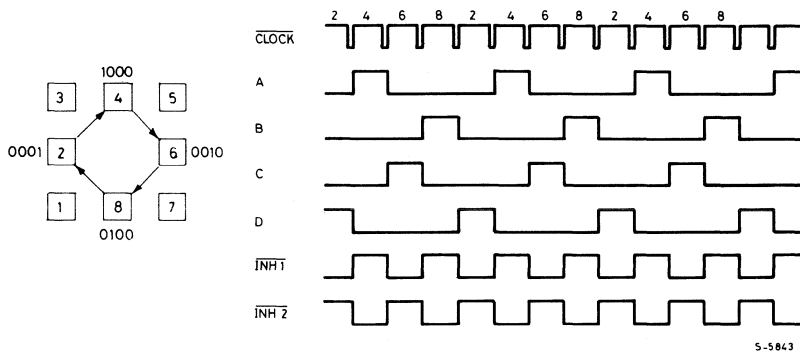


L297
L297A

MOTOR DRIVING PHASE SEQUENCES (continued)

Wave drive mode

Wave drive mode (also called “one-phase-on” drive) is selected by a low level on the HALF/FULL input when the translator is at an even numbered state (2, 4, 6 or 8).



ELECTRICAL CHARACTERISTICS (Refer to the block diagram $T_{amb} = 25^{\circ}\text{C}$, $V_s = 5\text{V}$ unless otherwise specified)

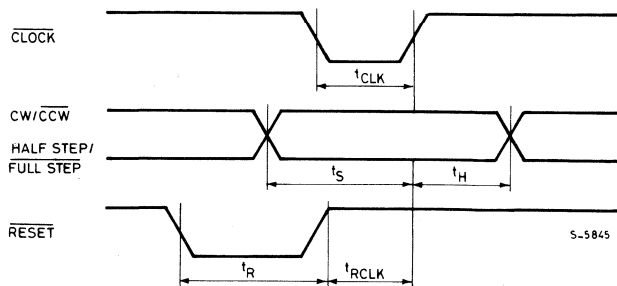
Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s Supply voltage (pin 12)		4.75		7	V
I_s Quiescent supply current (pin 12)	Outputs floating		50	80	mA
V_i Input voltage (pins 11, 17, 18, 19, 20)	Low			0.8	V
	High	2		V_s	V
I_i Input current (pin 11, 17, 18, 19, 20)	$V_i = L$			-100	μA
	$V_i = H$			10	μA
V_{en} Enable input voltage (pin 10)	Low			1.5	V
	High	2		V_s	V
I_{en} Enable input current (pin 10)	$V_{en} = L$			-100	μA
	$V_{en} = H$			10	μA

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_o Phase output voltage (pins 4, 6, 7, 9)	$I_o = 10\text{mA}$ V_{OL}			0.4	V
	$I_o = 5\text{mA}$ V_{OH}	3.9			V
V_{inh} Inhibit output voltage (pins 5, 8)	$I_o = 10\text{mA}$ $V_{inh L}$			0.4	V
	$I_o = 5\text{mA}$ $V_{inh H}$	3.9			V
I_{leak} Leakage current (pins 3, 11 *)	$V_{CE} = 7\text{V}$			1	μA
V_{sat} Saturation voltage (pins 3, 11 *)	$I = 5\text{mA}$			0.4	V
V_{off} Comparators offset voltage (pins 13, 14, 15)	$V_{ref} = 1\text{V}$			5	mV
I_b Comparator bias current (pins 13, 14, 15)		-100		10	μA
V_{ref} Input reference voltage (pin 15)		0		3	V
t_{CLK} Clock time		0.5			μs
t_s Set up time		1			μs
t_H Hold time		4			μs
t_R Reset time		1			μs
t_{RCLK} Reset to clock delay		1			μs

* L297A only.

Fig. 1



APPLICATION INFORMATION

Two phase bipolar stepper motor control circuit

This circuit drives bipolar stepper motors with winding currents up to 2A. The diodes are fast 2A types.

Fig. 2

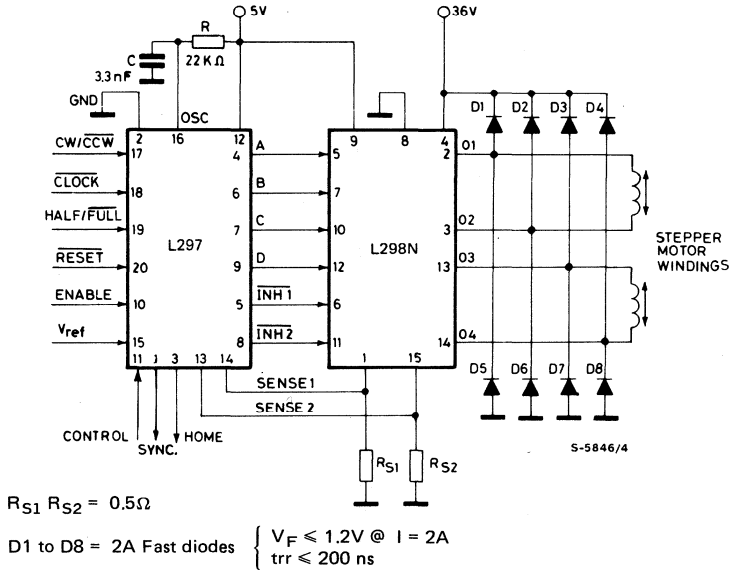


Fig. 3 - Synchronising L297s

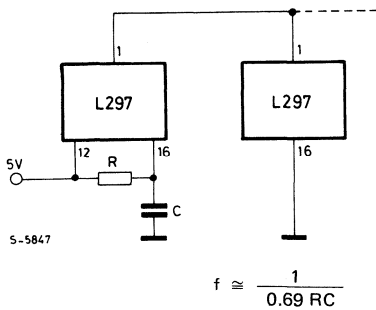
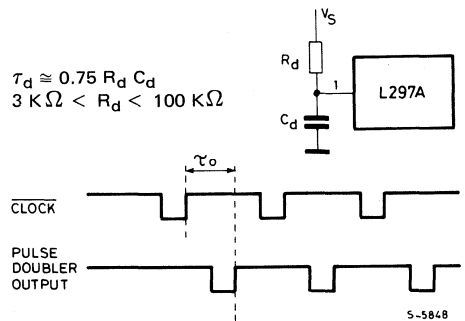


Fig. 4 – Pulse doubler (L297A)

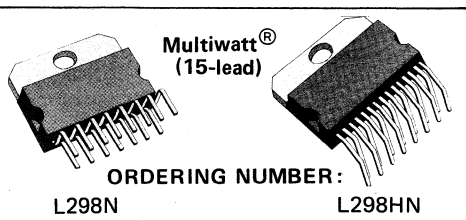




DUAL FULL-BRIDGE DRIVER

- POWER SUPPLY VOLTAGE UP TO 46V
- TOTAL DC CURRENT UP TO 4A
- LOW SATURATION VOLTAGE
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5V (HIGH NOISE IMMUNITY)

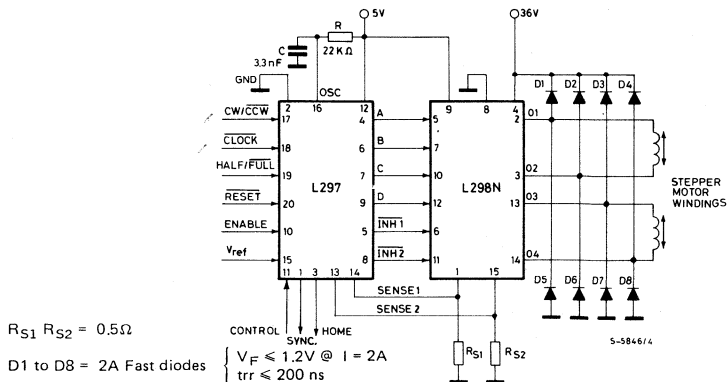
of the input signals. The emitters of the lower transistors of each bridge are connected together and the corresponding external terminal can be used for the connection of an external sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.



ABSOLUTE MAXIMUM RATINGS

V_s	Power supply	50	V
V_{ss}	Logic supply voltage	7	V
V_i, V_{inh}	Input and inhibit voltage	-0.3 to 7	V
I_o	Peak output current (each channel)		
	– non repetitive ($t = 100 \mu s$)	3	A
	– repetitive (80% on - 20% off; $t_{on} = 10 \text{ ms}$)	2.5	A
	– DC operation	2	A
V_{sens}	Sensing voltage	-1 to 2.3	V
P_{tot}	Total power dissipation ($T_{case} = 75^\circ C$)	25	W
T_{stq}, T_j	Storage and junction temperature	-40 to 150	$^\circ C$

STEPPER MOTOR CONTROL CIRCUIT

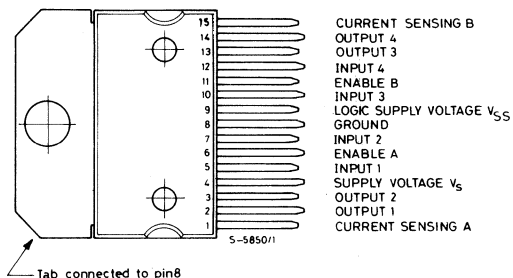




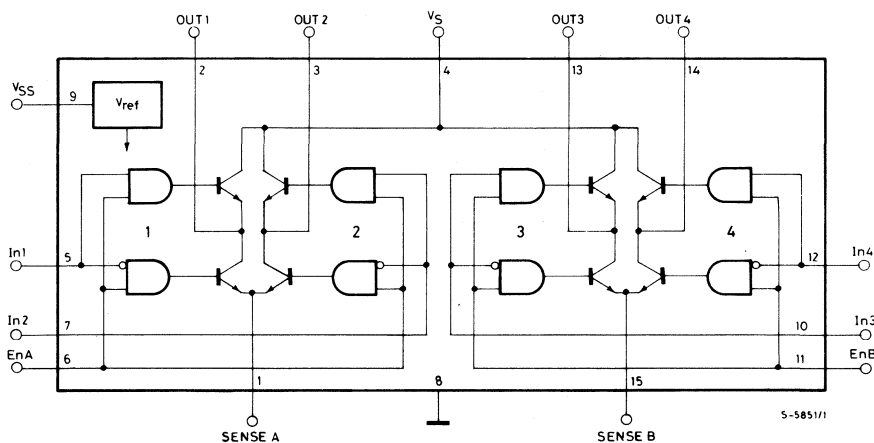
L298N

CONNECTION DIAGRAM

(top view)



BLOCK DIAGRAM

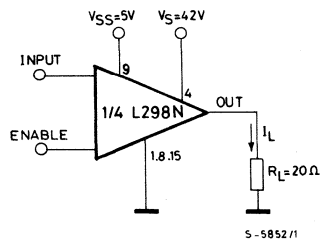


THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case
$R_{th\ j-amb}$	Thermal resistance junction-ambient

max.	3 °C/W
max.	35 °C/W

Fig. 1 - Switching times test circuits



Note: For INPUT chopper, set EN = H

Fig. 1a - Source Current Delay Times vs. Input or Enable Chopper.

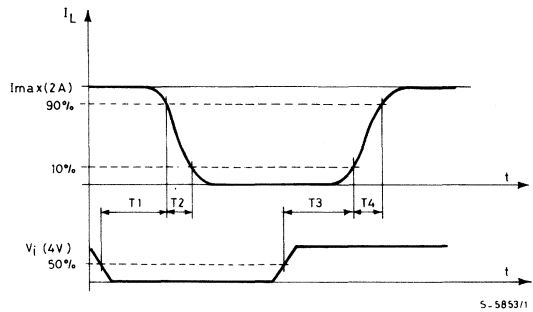
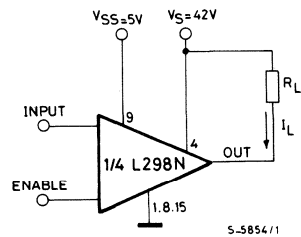
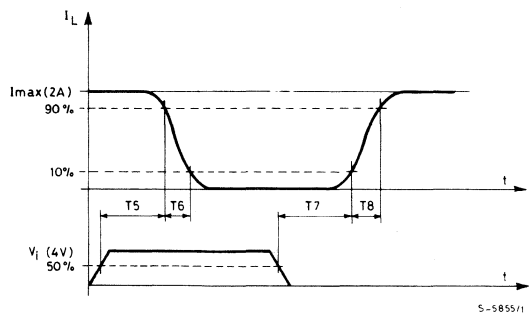


Fig. 2 - Switching times test circuits



Note: For INPUT chopper, set EN = H

Fig. 2a - Sink Current Delay Times vs. Input or Enable Chopper.



**L298N****ELECTRICAL CHARACTERISTICS** (for each channel, $V_s = 42V$, $V_{ss} = 5V$, $T_j = 25^\circ C$)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s Supply voltage (pin 4) *	Operative condition	$V_{IH}+2.5$		46	V
V_{ss} Logic supply voltage (pin 9) *		4.5		7	V
I_s Quiescent supply current (pin 4)	$V_{inh} = H$ $I_L = 0$ $V_i = L$		3	7	mA
	$V_i = H$		15	20	
I_{ss} Quiescent current from V_{ss} (pin 9)	$V_{inh} = L$			1	mA
	$V_{inh} = H$ $I_L = 0$ $V_i = L$		5	10	
	$V_i = H$		1.5	3	
V_{iL} Input low voltage (pins 5, 7, 10, 12)	$V_{inh} = L$			1	V
	$V_{inh} = H$			1.5	
V_{iH} Input high voltage (pins 5, 7, 10, 12)		-0.3		V_{ss}	V
I_{iL} Low voltage input current (pins 5, 7, 10, 12)	$V_i = L$			-10	μA
I_{iH} High voltage input current (pins 5, 7, 10, 12)	$V_i = H \leq V_{ss} - 0.6V$		30	100	
V_{inhL} Inhibit low voltage (pins 6, 11)		-0.3		1.5	V
V_{inhH} Inhibit high voltage (pins 6, 11)		2.3		V_{ss}	
I_{inhL} Low voltage inhibit current (pins 6, 11)	$V_{inh} = L$			-10	μA
I_{inhH} High voltage inhibit current (pins 6, 11)	$V_{inh} = H \leq V_{ss} - 0.6V$		30	100	
$V_{CE sat(H)}$ Source saturation voltage	$I_L = 1A$		1.2	1.8	V
	$I_L = 2A$		1.8	2.8	
$V_{CE sat(L)}$ Sink saturation voltage	$I_L = 1A$		1.2	1.8	V
	$I_L = 2A$		1.7	2.6	
$V_{CE sat}$ Total drop	$I_L = 1A$			3.4	V
	$I_L = 2A$			5.2	
V_{sens} Sensing voltage (pins 1, 15)		$-1^{(1)}$		2	V
$T_1 (V_i)$ Source current turn off delay	$0.5 V_i$ to $0.9 I_L^{(2)}$		1.7		μs
$T_2 (V_i)$ Source current fall time	$0.9 I_L$ to $0.1 I_L^{(2)}$		0.2		μs
$T_3 (V_i)$ Source current turn-on delay	$0.5 V_i$ to $0.1 I_L^{(2)}$		2.5		μs

Fig. 5 - Two phase bipolar stepper motor control circuit (winding currents up to 2A)

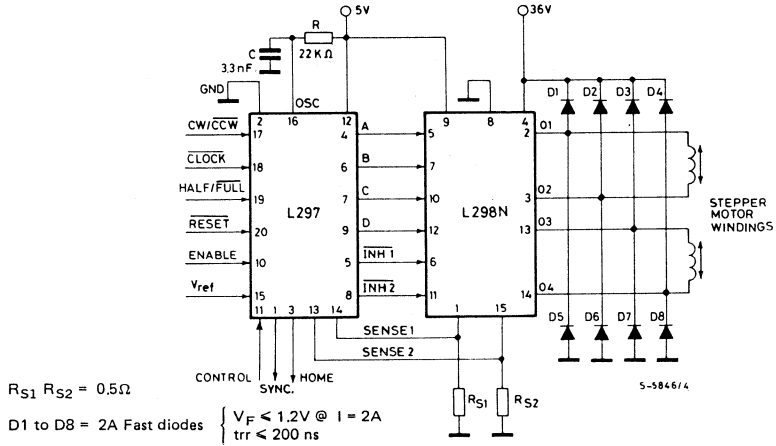
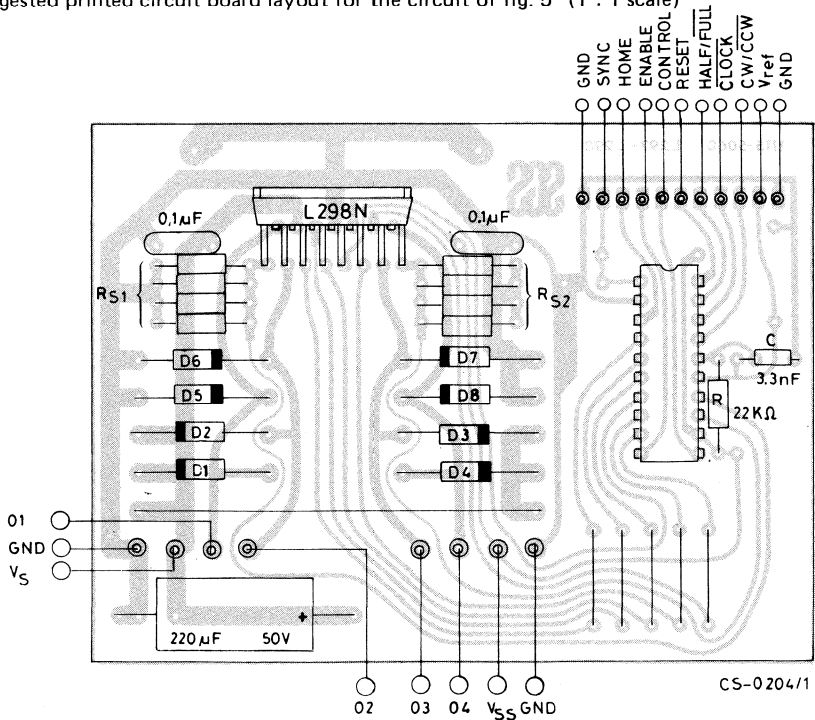


Fig. 6 - Suggested printed circuit board layout for the circuit of fig. 5 (1 : 1 scale)





L387A

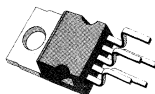
ADVANCE DATA

VERY LOW DROP 5V REGULATOR

- PRECISE OUTPUT VOLTAGE ($5V \pm 4\%$)
- VERY LOW DROPOUT VOLTAGE
- OUTPUT CURRENT IN EXCESS OF 500mA
- POWER-ON, POWER-OFF INFORMATION (RESET FUNCTION)
- HIGH NOISE IMMUNITY ON RESET DELAY CAPACITOR

The L387A is a very low drop voltage regulator in a Pentawatt[®] package specially designed to provide stabilized 5V supplies in consumer and industrial applications. Thanks to its very low input/output voltage drop this device is very useful in battery powered equipment, reducing consumption and prolonging battery life. A reset

output makes the L387A particularly suitable for microprocessor systems. This output provides a reset pulse when power is applied (after an external programmable delay) and goes low when power is removed, inhibiting the microprocessor. An hysteresis on reset delay capacitor raises the immunity to the ground noise.



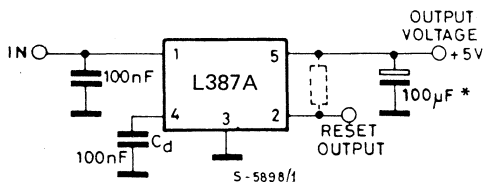
Pentawatt[®]

ORDERING NUMBER: L387A

ABSOLUTE MAXIMUM RATINGS

V_i	Forward input voltage	35	V
V_i	Reverse input voltage	-18	V
T_{op}	Operating junction temperature	-40 to +125	°C
T_{stg}	Storage temperature	-55 to +150	°C

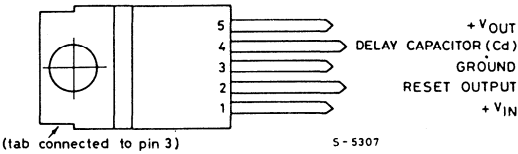
TEST CIRCUIT



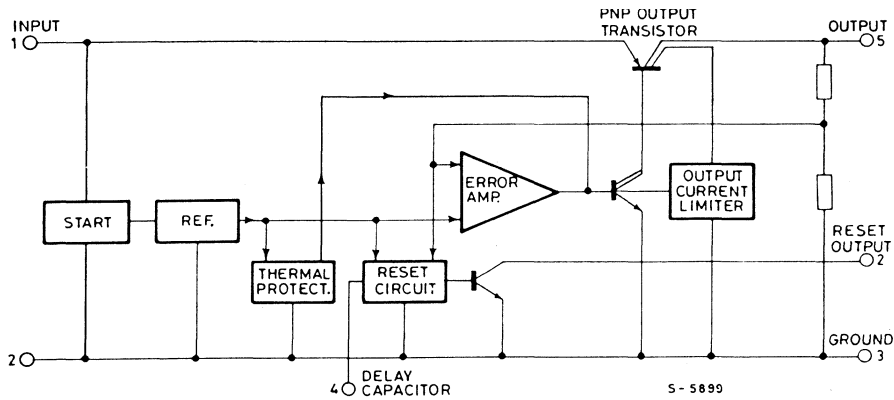
* Min 33µF and max. ESR $\leq 3\Omega$ over temperature range

CONNECTION DIAGRAM

(Top view)



BLOCK DIAGRAM



THERMAL DATA

R _{th j-case}	Thermal resistance junction-case	max	4	°C/W
------------------------	----------------------------------	-----	---	------

**L387A****ELECTRICAL CHARACTERISTICS** (Refer to the test circuit, $V_i = 14.4$ $T_j = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o Output voltage	$I_o = 5\text{mA to } 500\text{mA}$	4.80	5	5.20	V
V_i Operating input voltage	(*)			26	V
ΔV_o Line regulation	$V_i = 6\text{V to } 26\text{V}$ $I_o = 5\text{mA}$		5	50	mV
ΔV_o Load regulation	$I_o = 5\text{mA to } 500\text{mA}$		15	60	mV
$V_i - V_o$ Dropout voltage	$I_o = 500\text{mA}$		0.60	0.8	V
I_q Quiescent current	$I_o = 5\text{mA}$ $I_o = 150\text{mA}$ $I_o = 350\text{mA}$ $I_o = 500\text{mA}$		5 20 60 100	15 35 100 160	mA
	$V_i = 6.2\text{V}$ $I_o = 500\text{mA}$		160	180	
$\frac{\Delta V_o}{\Delta T}$ Temperature output voltage drift			-0.5		mV/ $^\circ\text{C}$
SVR Supply voltage rejection	$I_o = 350\text{mA}$ $C_o = 100\mu\text{F}$		60		dB
I_{sc} Output short circuit current	$f = 120\text{Hz}$ $V_i = 12\text{V} \pm 5\text{Vpp}$		0.8	1.5	A
V_R Reset output voltage	$I_R = 16\text{mA}$ $V_o < 4.75\text{V}$			0.8	V
I_R Reset output leakage current	V_o in regulation			50	μA
t_d Delay time for reset output	$C_d = 100\text{nF}$		30		ms
$V_{RT(\text{off})}$ Reset threshold (delay charging current on)		4.75	$V_o - 0.15$	$V_o - 0.04$	V
I_{C4} Charging current (current generator)	$V_4 = 3\text{V}$	10		30	μA
$V_{RT(\text{on})}$ Reset threshold (low)			$V_{RT(\text{off})} - 10\text{mV}$		V
V_4 Comparator threshold (pin 4)	Reset out = "0"	3.2		3.9	V
	Reset out = "1"	3.7		4.3	V
V_H Hysteresis voltage			500		mV

(*) For a DC voltage $26 < V_i < 35\text{V}$ the device is not operating



L387A

Fig. 1 - Dropout Voltage
vs. output current

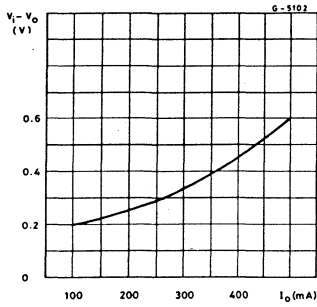


Fig. 2 - Quiescent current
vs. output current

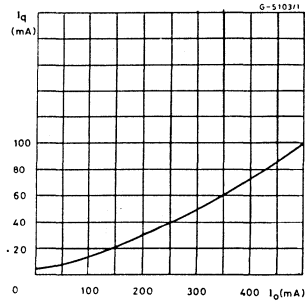
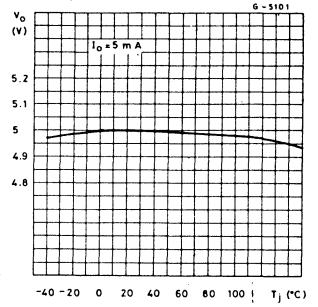


Fig. 3 - Output voltage vs.
temperature





L601 L603
L602 L604

DARLINGTON ARRAYS

- EIGHT DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 400mA PER DRIVER (500mA PEAK)
- OUTPUT VOLTAGE 90V ($V_{CE(sus)} = 70V$)
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL / CMOS / PMOS / DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

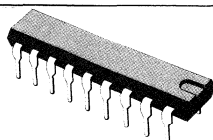
The L601, L602, L603 and L604 are high voltage, high current darlington arrays each containing eight open collector darlington pairs with common emitters. Each channel is rated at 400 mA and can withstand peak currents of 500mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

The four versions interface to all common logic families:

L601	General purpose
L602	14-25V PMOS
L603	5V TTL, CMOS
L604	6 - 15V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads, including solenoids, relays DC motors, LED displays, filament lamps, thermal printheads and high power buffers.

The L601, L602, L603 and L604 are supplied in 18 pin plastic DIP packages with a copper leadframe to reduce thermal resistance.



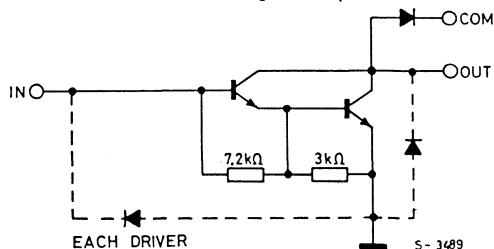
**DIP-18 Plastic
(U7P2)**

ORDERING NUMBERS: L601B, L603B
L602B, L604B

ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Collector emitter voltage (input open)	90	V
I_C	Collector current	0.4	A
I_{Cp}	Collector peak current	0.5	A
V_i	Input voltage (for L602, L603 and L604)	30	V
I_i	Input current (for L601 only)	25	mA
P_{tot}	Total power dissipation at $T_{amb} = 25^\circ C$	1.8	W
T_{op}	Operating junction temperature	-25 to 150	$^\circ C$
T_{stg}	Storage temperature	-55 to 150	$^\circ C$

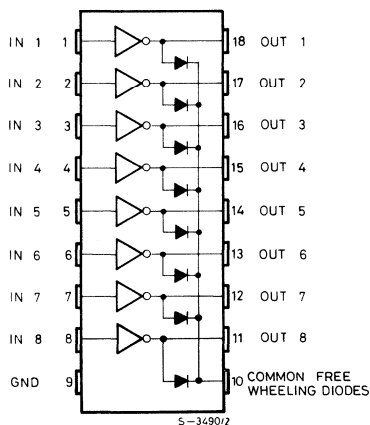
SCHEMATIC DIAGRAM (L601 — One darlington only)





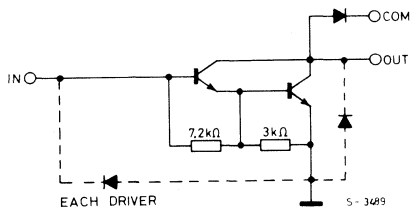
L601 L603
L602 L604

CONNECTION DIAGRAM (top view)

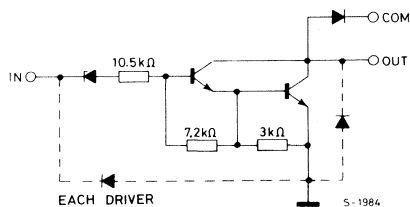


SCHEMATIC DIAGRAMS

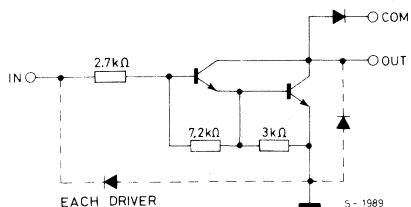
L601



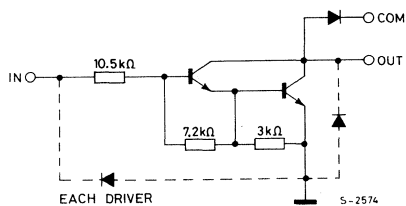
L602



L603



L604



THERMAL DATA

$R_{th\ j-amb}$ Thermal resistance junction-ambient	max 70 °C/W
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ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CEX} Output leakage current	$V_{CE} = 90\text{V}$			10	μA
$V_{CE(sat)}$ Collector emitter saturation voltage	$I_C = 300\text{ mA}$ $I_B = 500\text{ }\mu\text{A}$ $I_C = 200\text{ mA}$ $I_B = 350\text{ }\mu\text{A}$ $I_C = 100\text{ mA}$ $I_B = 250\text{ }\mu\text{A}$			2 1.7 1.2	V V V
h_{FE} DC forward current gain (L601 only)	$V_{CE} = 3\text{V}$ $I_C = 300\text{ mA}$	1000			—
V_i Minimum input voltage (ON condition)	$V_{CE} = 3\text{V}$ for L602 for L603 for L604 $I_C = 300\text{ mA}$			11.5 2.5 2.5	V V V
V_i Maximum input voltage (OFF condition)	$V_{CE} = 90\text{V}$ for L601 for L602 for L603 for L604 $I_C = 25\text{ }\mu\text{A}$	0.55 7 0.75 1			V V V V
I_R Clamp diode reverse current	$V_R = 90\text{V}$			50	μA
V_F Clamp diode forward voltage	$I_F = 300\text{ mA}$		2	2.4	V
t_{on} Turn-on delay	$0.5\text{ }V_i$ to $0.5\text{ }V_o$		0.4		μs
t_{off} Turn-off delay	$0.5\text{ }V_i$ to $0.5\text{ }V_o$		0.4		μs



L702

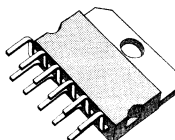
PRELIMINARY DATA

2A QUAD DARLINGTON SWITCH

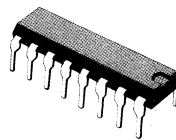
- SUSTAINING VOLTAGE: 70V
- 2A OUTPUT
- HIGH CURRENT GAIN
- IDEAL FOR DRIVING SOLENOIDS, DC MOTORS, STEPPER MOTORS, RELAYS, DISPLAYS, ETC.

The L702 is a monolithic integrated circuit for high current and high voltage switching applications it comprises four darlington transistors with common emitter and open collector suitable for current sinking applications, mounted on the new POWERDIP and Multiwatt[®] packages.

This circuit reduces components, sizes and costs; it can provide direct interface between low level logic and a variety of high current applications.



Multiwatt-11



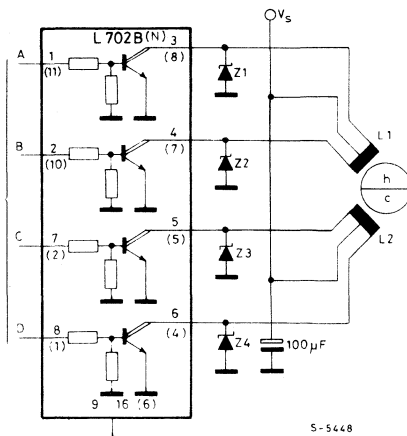
Powerdip 8 + 8
(V6P2)

ORDERING NUMBER: L702B - Powerdip
L702N - Multiwatt

ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Collector-emitter voltage (input open)	90	V
V_i	Input voltage	30	V
I_C	Collector current	3	A
P_{tot}	Total power dissipation at $T_{pin\ 9\ to\ 16} \leq 90^\circ C$	4	W
	Total power dissipation at $T_{amb} \leq 70^\circ C$	1.1	W
	Total power dissipation at $T_{case} \leq 90^\circ C$	20	W
T_{stg}	Storage temperature	-55 to 150	$^\circ C$
T_j	Operating junction temperature	-25 to 150	$^\circ C$

Stepping motor buffer

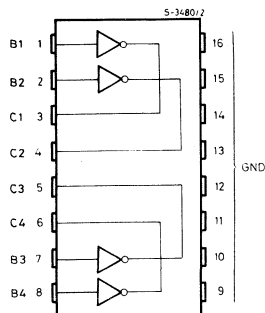


S-5448

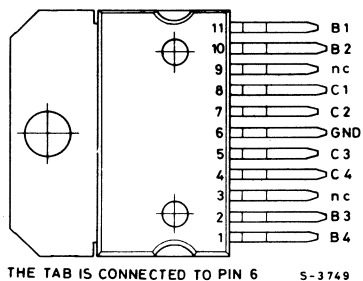


L702

CONNECTION DIAGRAMS (top view)

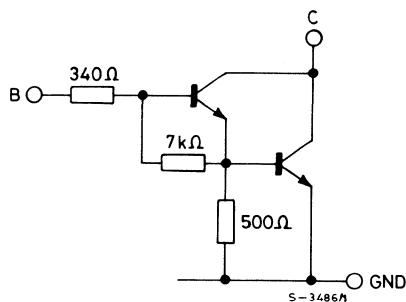


Powerdip



Multiwatt

SCHEMATIC DIAGRAM (each Darlington)



THERMAL DATA

$R_{th j-amb}$	Thermal resistance junction ambient	} Powerdip Multiwatt	max	70	°C/W
$R_{th j-pins 9/16}$	Thermal resistance junction pins 9 to 16		max	14	°C/W
$R_{th j-case}$	Thermal resistance junction-case		max	3	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _C EX Output leakage current	V _{CE} = 90V		10	50	μA
V _{CE} (sust) Collector emitter ^(°) sustaining voltage	I _C = 100 mA	70			V
V _{CE} (sat) Collector emitter saturation voltage	I _C = 1.25A I _i = 2 mA		1.3	1.9	V
h _{FE} DC forward current gain	I _C = 1A V _{CE} = 3V	1000	4000		
I _i Input current	V _i = 3.75V V _i = 2.4V open collector		7 3	11 6	mA mA
V _i Input voltage	off condition	V _{CE} = 70V	I _C ≤ 0.1 mA	0.4	V
	on condition	V _{CE} = 3V	I _C ≥ 1A	2.4	V
t _{on} Turn on time	V _s = 12V		0.3		μs
t _{off} Turn off time	R _L = 10 Ω		1		μs

(°) Pulsed: pulse duration = 300 μs, duty cycle = 1.5%.

Fig. 1 - Switching time

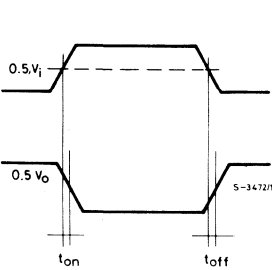


Fig. 2 - t_{on} and t_{off} test circuit

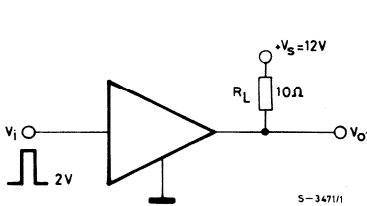


Fig. 3 - Peak collector current vs. duty cycle and number of outputs(L702B only)

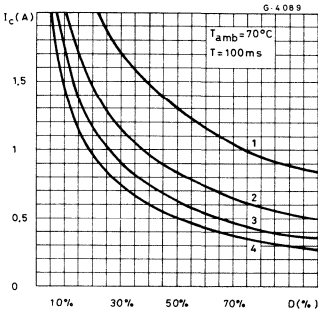


Fig. 4 - Collector emitter saturation voltage vs. collector current

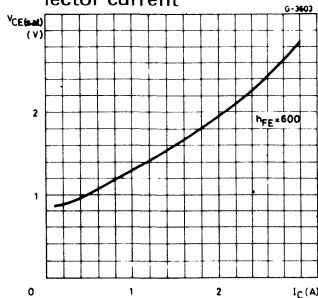


Fig. 5 - Collector current vs. input voltage

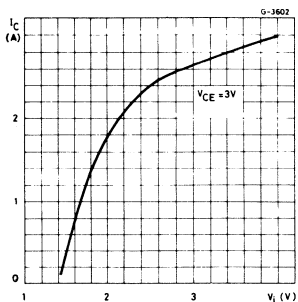


Fig. 6 - Input current vs. input voltage

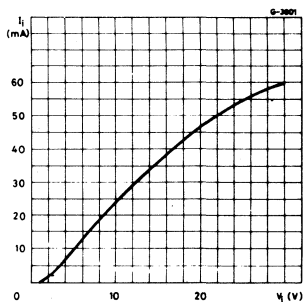


Fig. 7 - Safe operating areas (L702B)

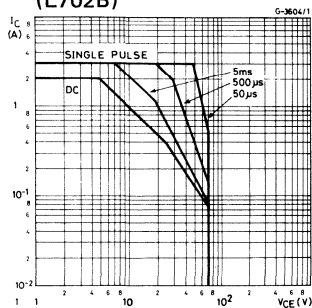


Fig. 8 - Safe operating areas (L702N)

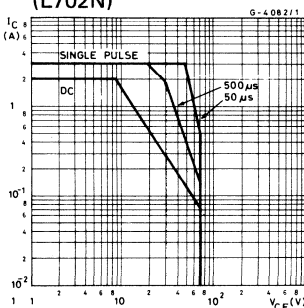
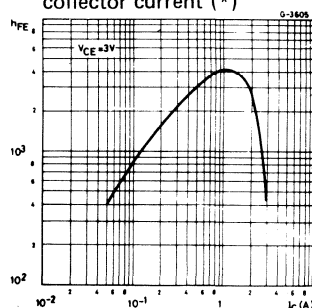


Fig. 9 - DC current gain vs. collector current (*)



(*) Pulse width = 300 μs , duty cycle 1.5%.



L2720 L2722

ADVANCE DATA

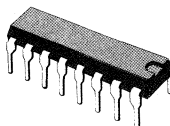
LOW DROP DUAL POWER OPERATIONAL AMPLIFIERS

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

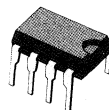
The L2720 and L2722 are monolithic integrated circuits in powerdip and minidip packages, intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies. They are par-

ticularly indicated for driving, inductive loads, as motor and finds applications in compact-disc, VCR automotive, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



Powerdip 8 + 8



Minidip Plastic

ORDERING NUMBERS:

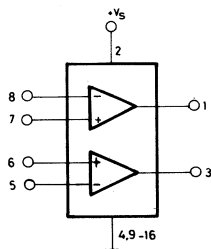
L2720

L2722

ABSOLUTE MAXIMUM RATINGS

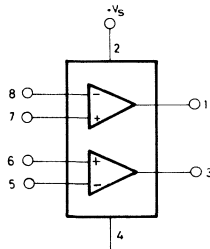
V_s	Supply voltage	28	V
V_s	Peak supply voltage (50ms)	50	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at $T_{amb} = 80^\circ\text{C}$ (L2720), $T_{amb} = 50^\circ\text{C}$ (L2722) $T_{case} = 75^\circ\text{C}$ (L2720)	1	W
		5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

BLOCK DIAGRAMS



S-5906/1

L2720



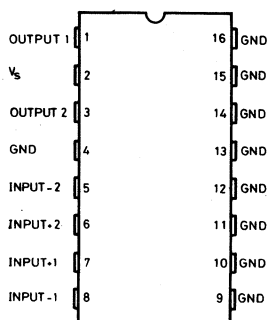
S-5929

L2722



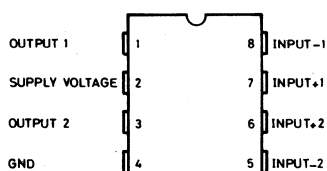
L2720
L2722

CONNECTION DIAGRAMS (Top view)



S-5905

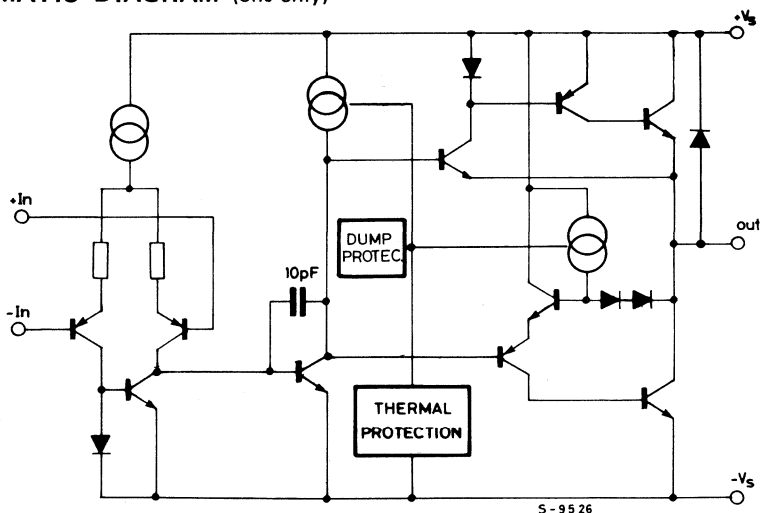
L2720



S-5911

L2722

SCHEMATIC DIAGRAM (one only)



THERMAL DATA

			Powerdip	Minidip
$R_{th\ j-case}$	Thermal resistance junction-pins	max	15°C/W	* 70°C/W
$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	70°C/W	100°C/W

* Thermal resistance junction-pin 4

ELECTRICAL CHARACTERISTICS ($V_s = 24V$, $T_{amb} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s Single supply voltage			4		28	V
V_s Split supply voltage			± 2		± 14	
I_s Quiescent drain current	$V_o = \frac{V_s}{2}$	$V_s = 24V$		10	15	mA
		$V_s = 8V$		9	15	
I_b Input bias current				0.2	1	μA
V_{os} Input offset voltage					15	mV
I_{os} Input offset current				10	50	nA
SR Slew rate				2		V/ μs
B Gain-bandwidth product				1.2		MHz
R_i Input resistance			500			K Ω
G_v O.L. voltage gain	$f = 100Hz$		70	80		dB
	$f = 1KHz$			60		
e_N Input noise voltage	$B = 22Hz \text{ to } 22KHz$			10		μV
I_N Input noise current				200		pA
CMR Common Mode rejection	$f = 1KHz$		66	84		dB
SVR Supply voltage rejection	$f = 100Hz$ $R_G = 10K\Omega$ $V_R = 0.5V$	$V_s = 24V$ $V_s = \pm 12V$ $V_s = \pm 6V$	54	70 75 81		dB dB dB
$V_{DROP (HIGH)}$	$V_s = \pm 2.5V \text{ to } \pm 12V$	$I_p = 100mA$		0.7		V
		$I_p = 500mA$		1.0	1.5	
$V_{DROP (LOW)}$		$I_p = 100mA$		0.3		V
		$I_p = 500mA$		0.5	1.0	
C_s Channel separation	$f = 1KHz$; $R_L = 10\Omega$; $G_v = 30dB$ $V_s = 24V$ $V_s = \pm 6V$			60 60		dB dB
T_{sd} Thermal shutdown junction temperature				145		$^{\circ}C$



L2720
L2722

Fig. 1 - Quiescent current vs. supply voltage

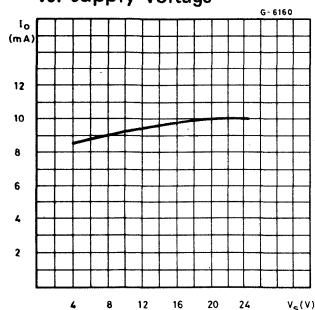


Fig. 2 - Open loop gain vs. frequency

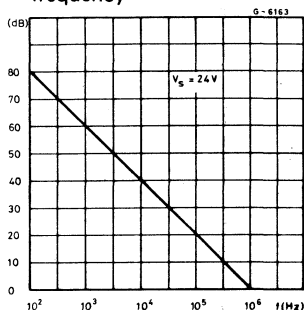


Fig. 3 - Open loop voltage gain

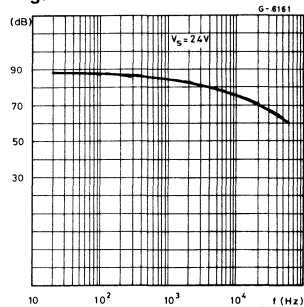


Fig. 4 - Output swing vs. load current ($V_S = \pm 5V$)

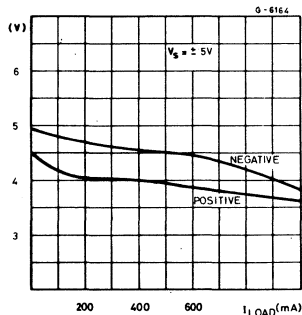


Fig. 5 - Output swing vs. load current ($V_S = \pm 12V$)

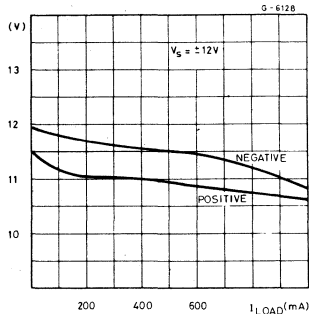


Fig. 6 - Supply voltage rejection vs. frequency

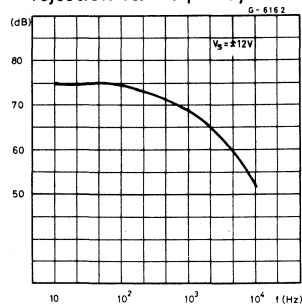
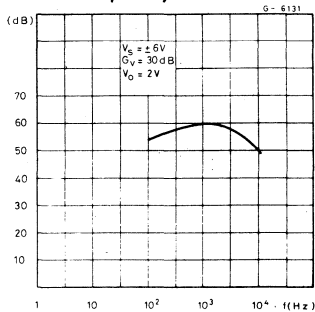


Fig. 7 - Channel separation vs. frequency



APPLICATION SUGGESTION

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

— layout accuracy;

- A 100nF capacitor connected between supply pins and ground;
- boucherot cell (0.1 to 0.2 μ F + 1 Ω series) between outputs and ground or across the load.

Fig. 8 – Bidirectional DC motor control with μ P compatible inputs

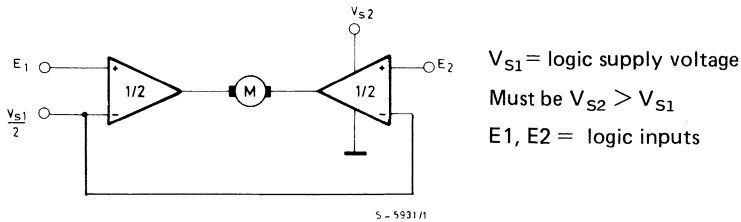


Fig. 9 – Servocontrol for compact-disc

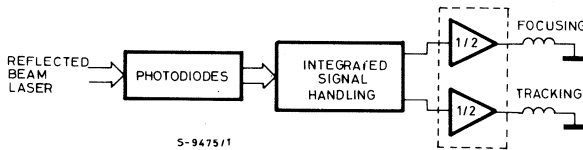


Fig. 10 – Compact-disc motor driver (1/2 section)

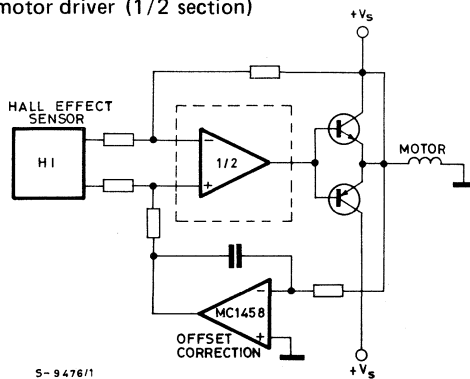


Fig. 11 – Capstan motor control in video recorders

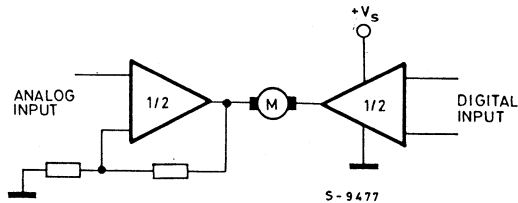
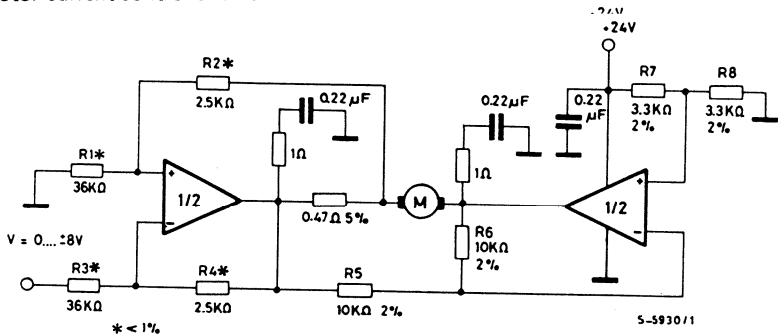


Fig. 12 – Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 13 – Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R_3 \cdot R_1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2 \left(V_1 - \frac{V_s}{2} \right) + |R_o| \cdot I_M$ where $|R_o| = \frac{2R \cdot R_1}{R_X}$ and I_M is the motor current.

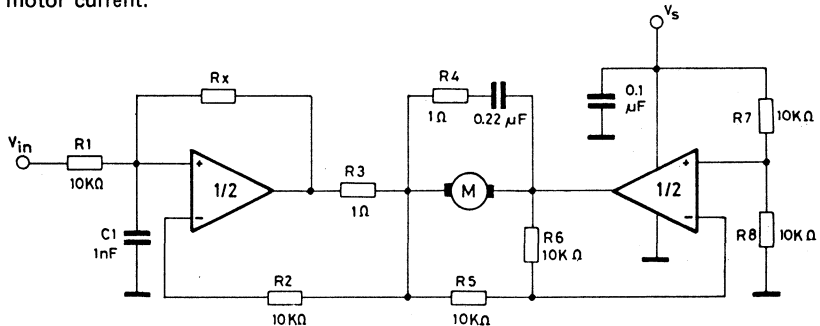
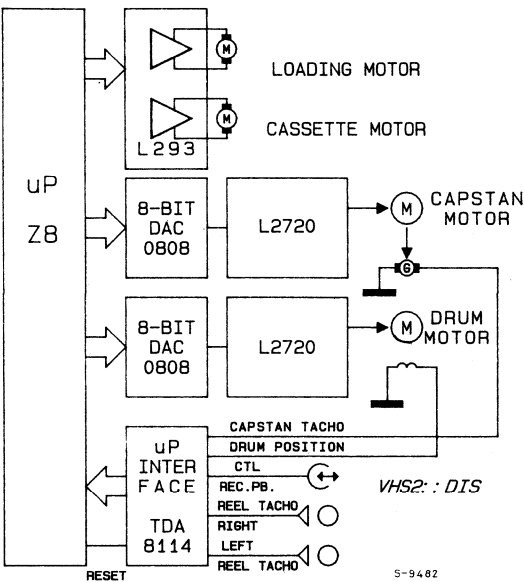


Fig. 14 - VHS-VCR Motor control circuit





L3654S

PRELIMINARY DATA

PRINTER SOLENOID DRIVER

The L3654S is a printer solenoid driver containing ten open-collector driver outputs and a ten-bit serial-in, parallel-out register.

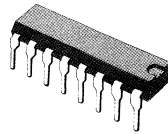
Data is clocked into the shift register serially and transferred to the open-collector outputs by an enable input. Serial input data is loaded by the rising edge of the clock. A serial output from the tenth bit is provided which changes at the falling edge of the clock. This output is not controlled by the enable input and remains active at all time.

The L3654S is pin to pin compatible with the standard L3654, but can work with V_s down to 4.75V.

Each output is rated at 250mA (sink) and is

clamped to ground internally at 50V to dissipate stored energy in inductive loads.

The L3654S is supplied in a 16 lead dual in-line plastic package, and its main fields of application comprise thermal printers, cash registers and printing pocket calculators.



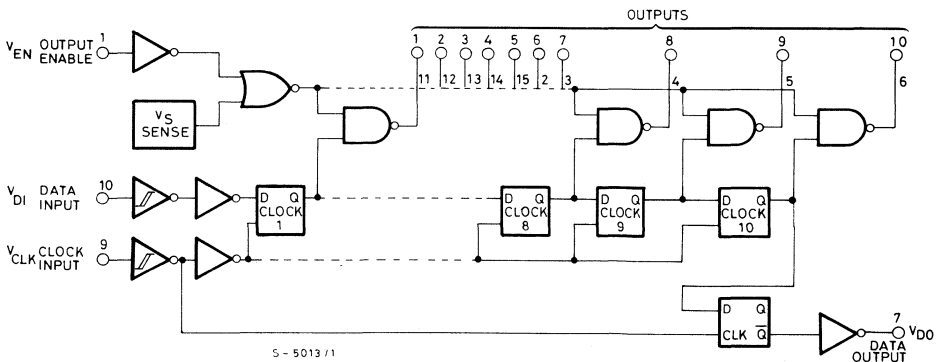
DIP-16 Plastic
(0.25)

ORDERING NUMBER: L3654S

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	9.5	V
V_i	Input voltage	9.5	V
V_E	External supply voltage	45	V
I_o	Output current (single output)	0.4	A
I_g	Ground current	4.0	A
P_{tot}	Total power dissipation ($T_{amb} = 70^\circ\text{C}$)	1	W
T_{stg}, T_j	Storage and junction temperature	-65 to 150	$^\circ\text{C}$

BLOCK DIAGRAM



CONNECTION DIAGRAM (top view)

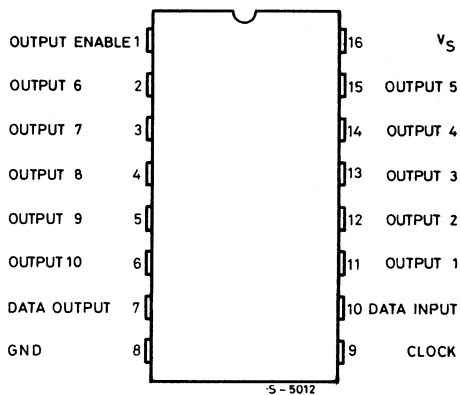
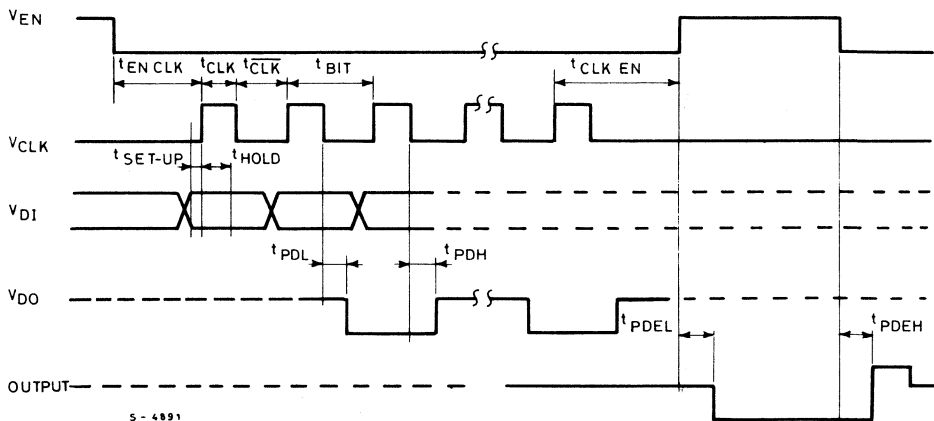


Fig. 1 - Timing diagram



THERMAL DATA

$R_{th\ j-amb}$ Thermal resistance junction-ambient

max 80 °C/W

ELECTRICAL CHARACTERISTICS ($V_s = 5V$, $V_E = 30V$, $T_{amb} = 0^\circ$ to $70^\circ C$, unless otherwise specified)

Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_s Supply voltage			4.75		9.5	V
I_s Supply current	$T_{amb} = 25^\circ C$ $V_s = 9.5V$	$V_{EN} = 0V$; $V_{DO} = 0V$		27	40	mA
		$V_{EN} = 2.6V$ $I_o = 250\text{ mA (each bit)}$		55	70	mA
V_E External operating supply voltage					40	V
I_{leak} Output leakage current (each output)	$V_E = 40V$	$V_{EN} = 0V$			1	mA
V_z Internal clamp voltage	$I_z = 0.3A *$	$V_{EN} = 0V$	45	50	65	V
$V_{CE\ sat}$ Output saturation voltage	$I_o = 250\text{ mA}$	$V_{EN} = 2.6V$			1.6	V
V_{DI} V_{CLK} V_{EN} Input logic levels (pins 1, 9, 10)	Low State (L)				0.8	V
	High state (H)		2.6			
I_{DI} Data input current	$V_{DI} = 2.6V$	$T_{amb} = 70^\circ C$	0.3	0.57		mA
		$T_{amb} = 0^\circ C$		0.57	0.75	
	$V_{DI} = 1V$	$T_{amb} = 70^\circ C$		220		μA
I_{CLK}^* Clock input current	$V_{CLK} = 2.6V$	$T_{amb} = 70^\circ C$	0.2	0.33		mA
		$T_{amb} = 0^\circ C$		0.33	0.5	
	$V_{CLK} = 1V$	$T_{amb} = 70^\circ C$		125		μA
I_{EN} Enable input current	$V_{EN} = 2.6V$	$T_{amb} = 70^\circ C$	0.2	0.33		mA
		$T_{amb} = 0^\circ C$		0.33	0.5	
	$V_{EN} = 1V$	$T_{amb} = 70^\circ C$		125		μA
R_{IN} Input pull-down resistance	Clock input	$T_{amb} = 25^\circ C$ $V_{CLK} < V_s$		8		$K\Omega$
	Enable input	$T_{amb} = 25^\circ C$ $V_{EN} < V_s$		8		
	Data input	$T_{amb} = 25^\circ C$ $V_{DI} < V_s$		4.5		
V_{DO} Output logic levels (pin 7)	Low state (L) $V_{DI} = 0V$ $I_{DO}(\text{pin } 7) = 0$			0.01	0.5	V
	High state (H) $V_{DI} = 2.6V$ $I_{DO}(\text{pin } 7) = -0.75\text{ mA}$		2.6	3.4		V
R_{DO} Output pull-down resistance (pin 7)	$V_{DI} = 0V$	$V_{DO} = 1V$		14		$K\Omega$

* Pulsed: pulse duration = $300\mu s$, duty cycle = 2%

**L3654S****ELECTRICAL CHARACTERISTICS** (see fig. 1 and the section "definition of terms")

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Clock, data and enable input	t_{CLK}	4			μs
	$\overline{t_{CLK}}$	5.5			
	t_{SET-UP}	1			
	t_{HOLD}	3			
Clock to enable delay	$t_{CLK\ EN}$	$2\ t_{BIT}$			
Enable to clock delay	$t_{EN\ CLK}$	t_{BIT}			
Data output delay	t_{PDH}, t_{PDL} $R_L = 5K\Omega, C_L \leq 10\ pF$		0.8	2.5	μs
Output delay	t_{PDEL}		3		μs
	t_{PDEH}		3.5		
Output rise time	$R_L = 100\ \Omega, C_L < 100\ pF$		1.2		μs
Output fall time	$R_L = 100\ \Omega, C_L < 100\ pF$		1.2		μs
V_{DO} rise time			0.4		μs
V_{DO} fall time			0.4		μs

DEFINITION OF TERMS

V_{ss} : External power supply voltage. The return for open-collector relay driver outputs.

V_{DI}, V_{CLK}, V_{EN} : The voltages at the data, clock and enable inputs respectively.

V_{DO} : The voltage at data output.

t_{BIT} : Period of the incoming clock.

t_{CLK} : The portion of t_{BIT} when $V_{CLK} \geq 2.6V$.

$\overline{t_{CLK}}$: The portion of t_{BIT} when $V_{CLK} \leq 0.8V$.

t_{HOLD} : The time following the start of t_{CLK} required to transfer data within the shift register.

t_{SET-UP} : The time prior to the end of $\overline{t_{CLK}}$ required to insure valid data at the shift register input for subsequent clock transitions.



L4901

PRELIMINARY DATA

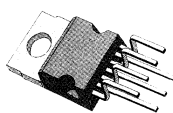
DUAL 5V REGULATOR WITH RESET

- OUTPUT CURRENTS: $I_{O1} = 300\text{mA}$
 $I_{O2} = 400\text{mA}$
- FIXED PRECISION OUTPUT VOLTAGE 5V $\pm 2\%$
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN $1\mu\text{A}$ AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V

- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4901 is a monolithic low drop dual 5V regulator designed mainly for supplying micro-processor systems.

Reset and data save functions during switch on/off can be realized.



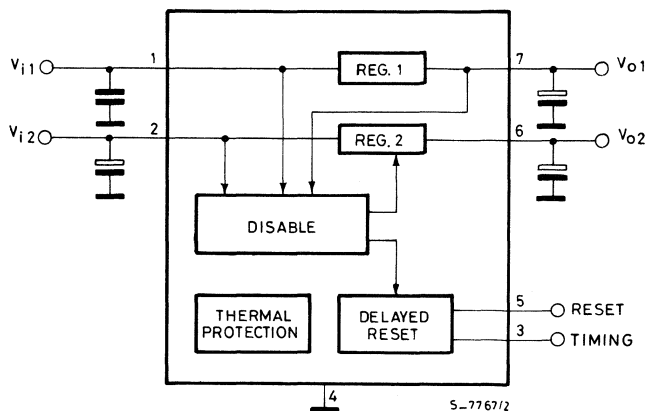
Heptawatt

ORDERING NUMBER: L4901

ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	DC operating input voltage	20	V
	Transient input overvoltage ($t = 40\text{ms}$)	60	V
I_o	Output current	internally limited	
T_j	Storage and junction temperature	-40 to 150	$^{\circ}\text{C}$

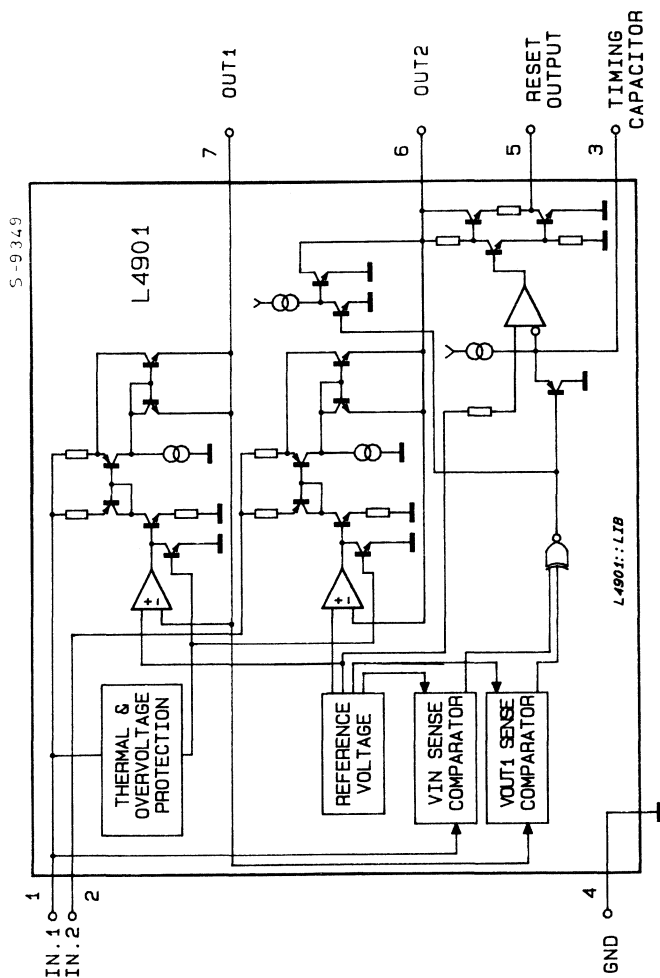
BLOCK DIAGRAM



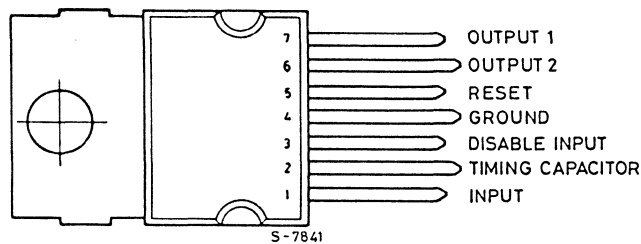


L4901

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



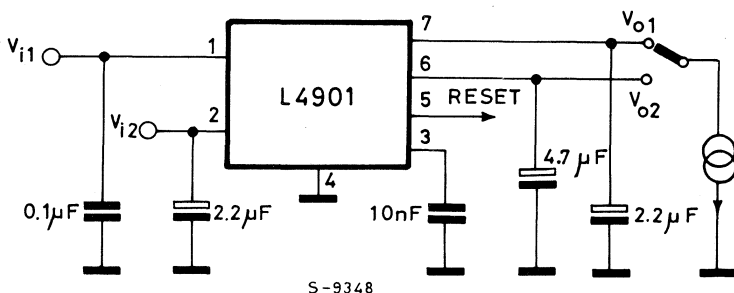
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 300mA regulator input.
2	INPUT 2	400mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5µA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{5\mu A} \right)$; $t_{RD} \text{ (ms)} = C_t \text{ (nF)}$
6	OUTPUT 2	5V - 400mA regulator output. Enabled if $V_{O1} > V_{RT}$ and $V_{IN2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{O2} capacitor is discharged.
7	OUTPUT 1	5V - 300mA regulator output with low leakage (in switch-OFF condition).

THERMAL DATA

$R_{th \text{ j-case}}$	Thermal resistance junction-case	max	4	°C/W
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TEST CIRCUIT



ELECTRICAL CHARACTERISTICS ($V_{IN} = 14.4V$, $T_{amb} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1} Output voltage 1	R load $1K\Omega$	4.95	5.05	5.15	V
V_{O2H} Output voltage 2 HIGH	R load $1K\Omega$	$V_{O1} - 0.1$	5	V_{O1}	V
V_{O2L} Output voltage 2 LOW	$I_{O2} = -5mA$		0.1		V
I_{O1} Output current 1	$\Delta V_{O1} = -100mV$	300			mA
I_{L01} Leakage output 1 current	$V_{IN} = 0$ $V_{O1} \leq 3V$			1	μA
I_{O2} Output current 2	$\Delta V_{O2} = -100mV$	400			mA
V_{i01} Output 1 dropout voltage (*)	$I_{O1} = 10mA$ $I_{O1} = 100mA$ $I_{O1} = 300mA$		0.7 0.8 1.05	0.8 1 1.25	V V V
V_{IT} Input threshold voltage		$V_{O1} + 1.2$	6.4	$V_{O1} + 1.6$	V
V_{ITH} Input threshold voltage hyst.			250		mV
ΔV_{O1} Line regulation 1	$7V < V_{IN} < 18V$ $I_{O1} = 5mA$		5	50	mV
ΔV_{O2} Line regulation 2	$I_{O2} = 5mA$		5	50	mV
ΔV_{O1} Load regulation 1	$V_{IN} = 8V$ $5mA < I_{O1} < 300mA$		40	80	mV
ΔV_{O2} Load regulation 2	$5mA < I_{O2} < 400mA$		50	100	mV
I_Q Quiescent current	$0 < V_{IN} < 13V$ $6.3V < V_{IN} < 13V$ $I_{O2} = 0$ $I_{O1} \leq 5mA$		4.5 1.6	6 3.5	mA mA
I_{Q1} Quiescent current 1	$6.3V < V_{IN1} < 13V$ $V_{IN2} = 0$ $I_{O1} \leq 5mA$ $I_{O2} = 0$		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{RT} Reset threshold voltage		$V_{O2}-0.15$	4.9	$V_{O2}-0.05$	V
V_{RTH} Reset threshold hysteresis			50	160	mV
V_{RH} Reset output voltage HIGH	$I_R = 500\mu A$	$V_{O2}-1$	4.12	V_{O2}	V
V_{RL} Reset output voltage LOW	$I_R = -5mA$		0.25	0.4	V
t_{RD} Reset pulse delay	$C_t = 10nF$	6	10	14	ms
t_d Timing capacitor discharge time	$C_t = 10nF$			20	μs
$\frac{\Delta V_{O1}}{\Delta T}$ Thermal drift	$-20^\circ C \leq T_{amb} \leq 140^\circ C$	-0.8	0.3	+0.8	mV/ $^\circ C$
$\frac{\Delta V_{O2}}{\Delta T}$ Thermal drift	$-20^\circ C \leq T_{amb} \leq 140^\circ C$	-0.8	0.3	+0.8	mV/ $^\circ C$
SVR1 Supply voltage rejection	$f = 100Hz$ $V_R = 0.5V$ $I_o = 100mA$	54	84		dB
SVR2 Supply voltage rejection		50	80		dB
T_{JSD} Thermal shut down			150		$^\circ C$

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4901 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{O1} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{O2}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{O2} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage

- an overload on the output 1 ($V_{O1} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2 ($V_{O2} - V_R = V_{CEsat}$; $I_{O2} = I_{SC2}$) and does not influence Reg. 1.

The V_{O1} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current error even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery without a

CIRCUIT OPERATION (continued)

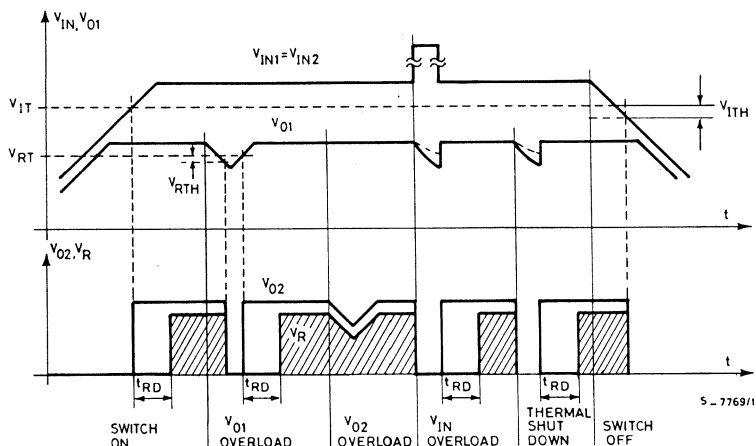
separation diode. The V_{01} regulator also features low consumption (0.6mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits which may be powered down when the system is inactive, or that must be powered

down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system typically used in trip computers or in car radios with programmable tuning.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 4 shows the L4901 with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type N-MOS μP . The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

The L4901 is also ideal for microcomputer systems using battery backup CMOS static RAMs. As shown in fig. 5 the reset output is used both to disable the μP and, through the address decoder M74HC138, to ensure that the RAMs are disabled as soon as the main supply starts to fall.

Another interesting application of the L4901 is in μP system with shadow memories. (see fig. 6)

When the input voltage goes below V_{IT} , the reset output enables the execution of a routine that saves the machine's state in the shadow RAM (xicor x 2201 for example).

Thanks to the low consumption of the Reg. 1 a 680 μF capacitor on its input is sufficient to provide enough energy to complete the operation. The diode on the input guarantees the supply of the equipment even if a short circuit on V_1 occurs.

APPLICATION SUGGESTION (continued)

Fig. 2

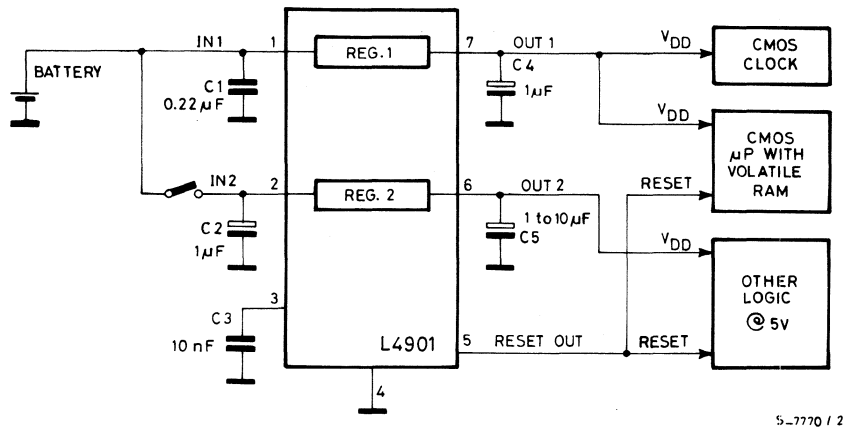
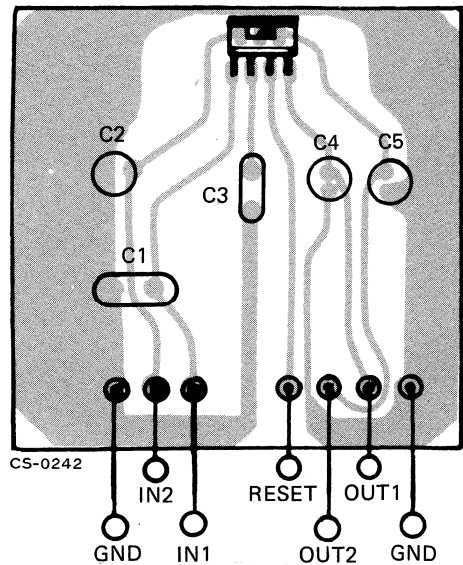


Fig. 3 - P.C. board component layout of fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

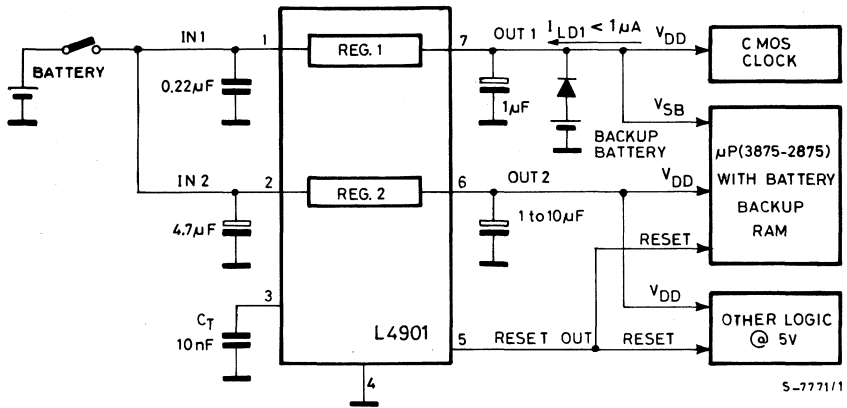
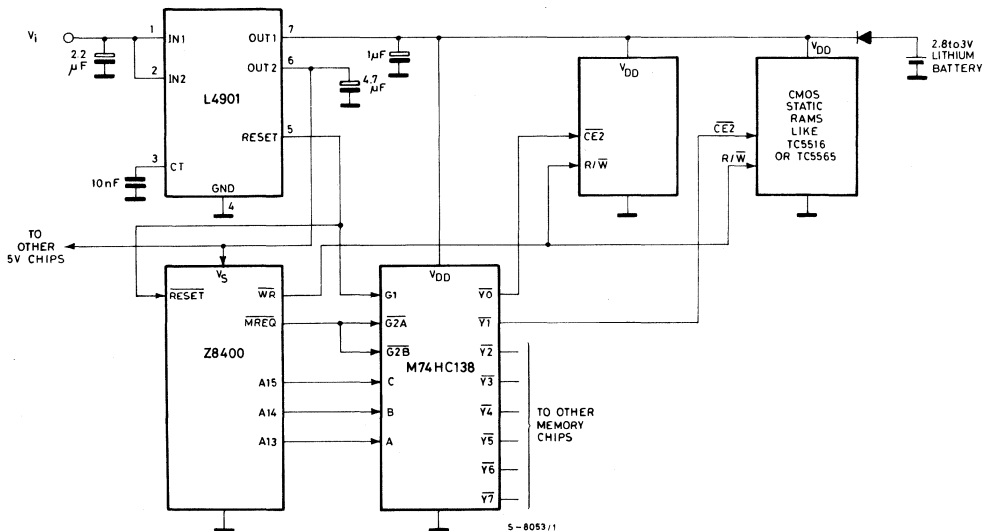


Fig. 5



APPLICATION SUGGESTION (continued)

Fig. 6

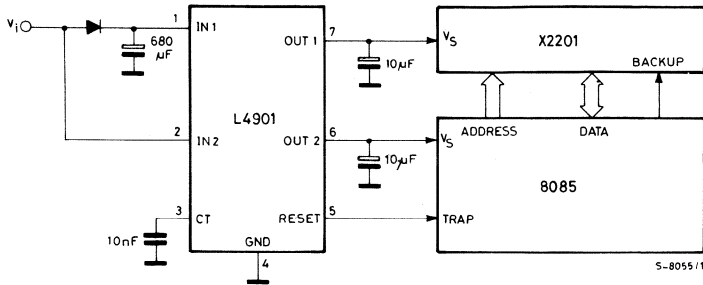


Fig. 7 - Quiescent current (Reg. 1) vs. output current

G-5795

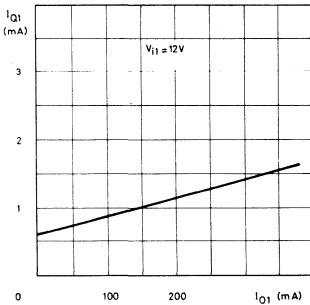


Fig. 8 - Quiescent current (Reg. 1) vs. input voltage

G-5796/2

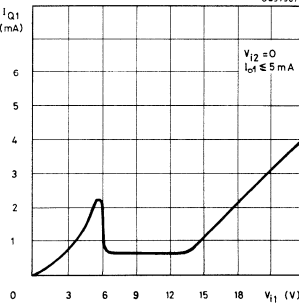


Fig. 9 - Total quiescent current vs. input voltage

G-5797/1

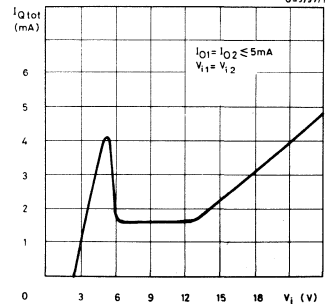


Fig. 10 - Regulator 1 output current and short circuit current vs. input voltage

G-5925

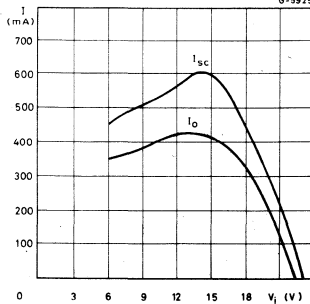


Fig. 11 - Regulator 2 output current and short circuit current vs. input voltage

G-5926

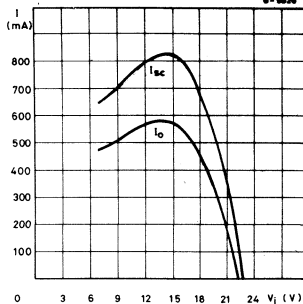
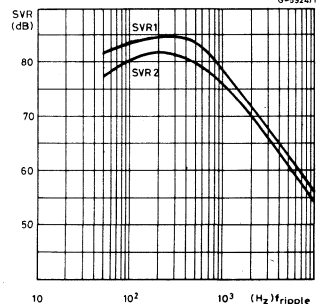


Fig. 12 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequency

G-5924/1





L4902

PRELIMINARY DATA

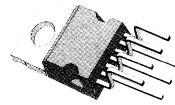
DUAL 5V REGULATOR WITH RESET AND DISABLE FUNCTIONS

- OUTPUT CURRENTS: $I_{O1} = 300\text{mA}$
 $I_{O2} = 400\text{mA}$
- FIXED PRECISION OUTPUT VOLTAGE $5\text{V} \pm 2\%$
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN $1\mu\text{A}$ AT OUTPUT 1
- RESET OUTPUT HIGH

- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4902 is a monolithic low drop dual 5V regulator designed mainly for supplying micro-processor systems.

Reset and data save functions and remote switch on/off control can be realized.



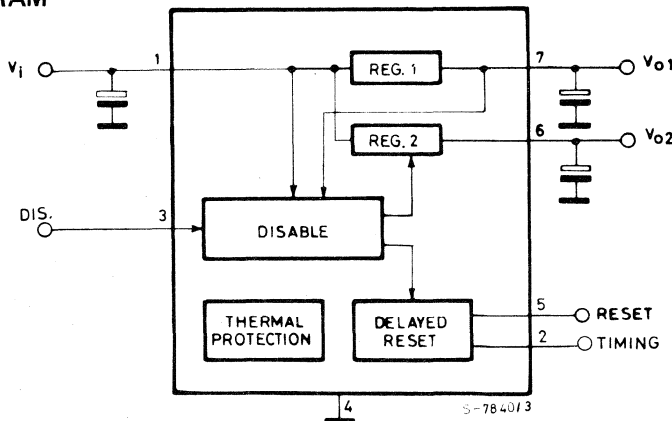
Heptawatt

ORDERING NUMBER : L4902

ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	DC operating input voltage	20	V
	Transient input overvoltage ($t = 40\text{ms}$)	60	V
I_O	Output current	internally limited	
T_{stg}, T_J	Storage and junction temperature	-40 to 150	$^{\circ}\text{C}$

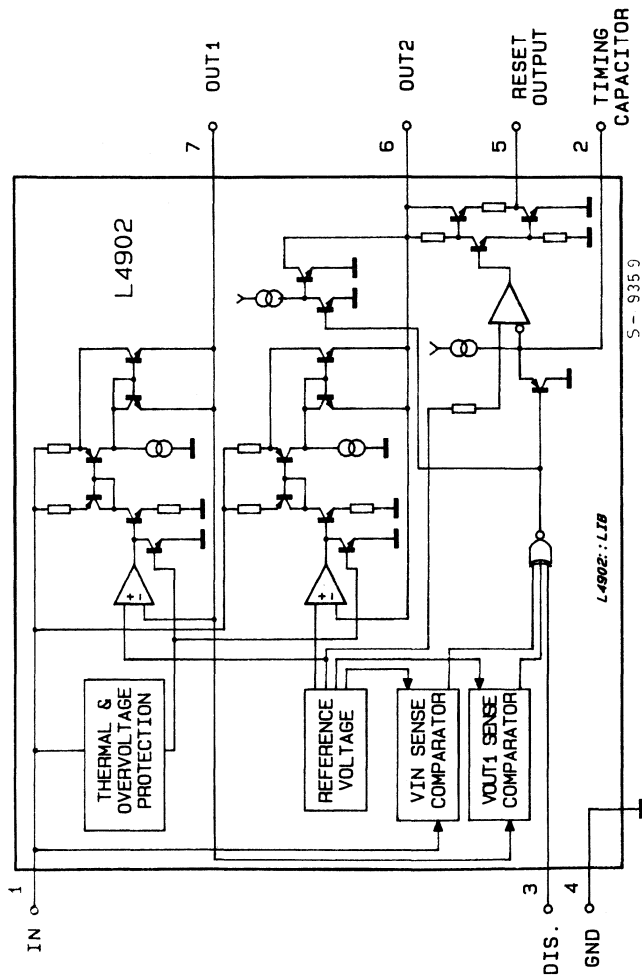
BLOCK DIAGRAM





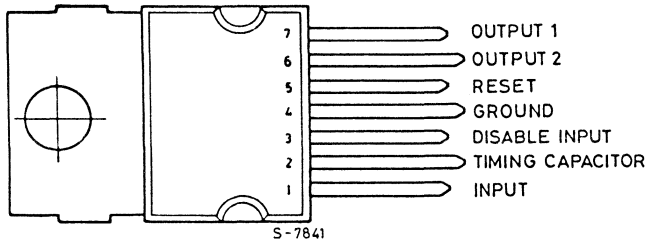
L4902

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM

(Top view)



PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Regulators common input.
2	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a $5\mu\text{A}$ constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
3	V_{O2} DISABLE INPUT	A high level ($> V_{DT}$) disable output Reg. 2.
4	GND	Common ground.
5	RESET OUTPUT	When pin 2 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{5\mu\text{A}} \right)$; $t_{RD} \text{ (ms)} = C_t \text{ (nF)}$.
6	OUTPUT 2	5V - 400mA regulator output. Enabled if $V_{O1} > V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN} > V_{IT}$. If Reg. 2 is switched-OFF the C_{O2} capacitor is discharged.
7	OUTPUT 1	5V - 300mA. Low leakage (in switch-OFF condition) output.

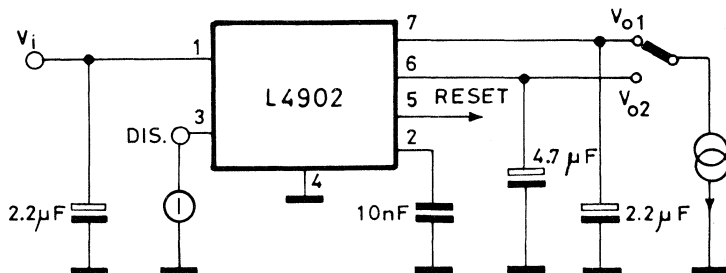
THERMAL DATA

$R_{th \text{ J-case}}$	Thermal resistance junction-case	max	4	$^{\circ}\text{C/W}$
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L4902

TEST CIRCUIT



S-9360 /1

ELECTRICAL CHARACTERISTICS ($V_{IN} = 14.4V$, $T_{amb} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{01} Output voltage 1	R load $1K\Omega$	4.95	5.05	5.15	V
V_{02H} Output voltage 2 HIGH	R load $1K\Omega$	$V_{01}-0.1$	5	V_{01}	V
V_{02L} Output voltage 2 LOW	$I_{02} = -5mA$		0.1		V
I_{01} Output current 1 max.	$\Delta V_{01} = -100mV$	300			mA
I_{L01} Leakage output 1 current	$V_{IN} = 0$ $V_{01} \leq 3V$			1	μA
I_{02} Output current 2 max.	$\Delta V_{02} = -100mV$	400			mA
V_{I01} Output 1 dropout voltage (*)	$I_{01} = 10mA$ $I_{01} = 100mA$ $I_{01} = 300mA$		0.7 0.8 1.05	0.8 1 1.25	V V V
V_{IT} Input threshold voltage		$V_{01}+1.2$	6.4	$V_{01}+1.6$	V
V_{ITH} Input threshold voltage hysteresis			250		mV
ΔV_{01} Line regulation 1	$7V < V_{IN} < 18V$ $I_{01} = 5mA$ $I_{02} = 5mA$		5	50	mV
ΔV_{02} Line regulation 2			5	50	mV
ΔV_{01} Load regulation 1	$V_{IN} = 8V$ $5mA < I_{01} < 300mA$ $5mA < I_{02} < 400mA$		40	80	mV
ΔV_{02} Load regulation 2			50	100	mV
I_Q Quiescent current	$0 < V_{IN} < 13V$ $6.3V < V_{IN} < 13V$ $V_{02} LOW$ $6.3V < V_{IN} < 13V$ $V_{02} HIGH$ $I_{01} = I_{02} \leq 5mA$		4.5 2.7 1.6	6 4 3.5	mA mA mA
V_{RT} Reset threshold voltage		$V_{02}-0.15$	4.9	$V_{02}-0.05$	V
V_{RTH} Reset threshold hysteresis			50	160	mV

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{RH} Reset output voltage HIGH	$I_R = 500\mu A$	$V_{O2}-1$	4.12	V_{O2}	V
V_{RL} Reset output voltage LOW	$I_R = -5mA$		0.25	0.4	V
t_{RD} Reset pulse delay	$C_t = 10nF$	6	10	14	ms
t_d Timing capacitor discharge time	$C_t = 10nF$			20	μs
V_{DT} V_{O2} disable threshold voltage			1.25	2.4	V
I_D V_{O2} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-100 -2		μA μA
$\frac{\Delta V_{O1}}{\Delta T}$ Thermal drift	$-20^\circ C \leq T_{amb} \leq 140^\circ C$	-0.8	0.3	0.8	mV/ $^\circ C$
$\frac{\Delta V_{O2}}{\Delta T}$ Thermal drift	$-20^\circ C \leq T_{amb} \leq 140^\circ C$	-0.8	0.3	0.8	mV/ $^\circ C$
SVR1 Supply voltage rejection	$f = 100Hz$ $V_R = 0.5V$ $I_O = 100mA$	54	84		dB
SVR2 Supply voltage rejection		50	80		dB
T_{JSD} Thermal shut down			150		$^\circ C$

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4902 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with common inputs plus a reset output for the data save function and a Reg. 2 output disable.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{O1} rises to the nominal value.

When the input reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{O2}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{O2} and V_R are switched together at low level when one of the following conditions occurs:

- a high level ($> V_{DT}$) is applied on pin 3;

- an input overvoltage;
- an overload on the output 1 ($V_{O1} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2 ($V_{O2} - V_R = V_{CEsat}$; $I_{O2} = I_{SC2}$) and does not influence Reg. 1.

The V_{O1} output features:

- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current error in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery without a separation diode.

CIRCUIT OPERATION (continued)

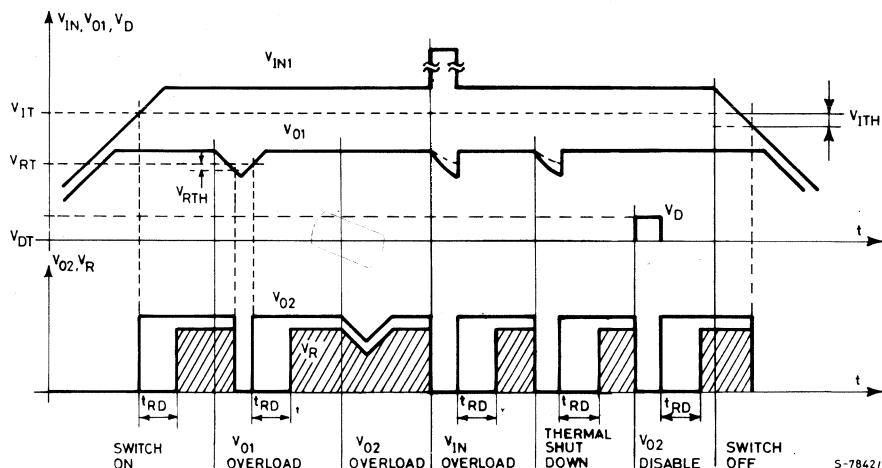
The V_{02} output can supply other non essential 5V circuits which may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access

only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Fig. 1



APPLICATION SUGGESTION

Fig. 2 illustrates how the L4902's disable input may be used in a CMOS μ Computer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μ computer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a μ P unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Another application for the L4902 is supplying a shadow-ram microcomputer chip (SGS M38SH72 for example) where a fast NV memory is backed up on chip by a EEPROM when a low level on

the reset output occurs.

By adding two CMOS CHMIDT-TRIGGER and few external components, also a watch dog function may be realized (see fig. 5). During normal operation the microsystem supplies a periodical pulse waveform; if an anomalous condition occurs (in the program or in the system), the pulses will be absent and the disable input will be activated after a settling time determined by R1 C1. In this condition all the circuitry connected to V_{02} will be disabled, the system will be restarted with a new reset front.

The disable of V_{02} prevent spurious operation during microprocessor malfunctioning.

APPLICATION SUGGESTION (continued)

Fig. 2

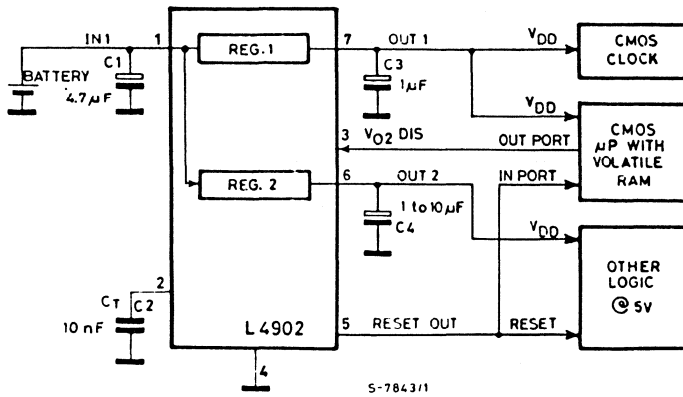
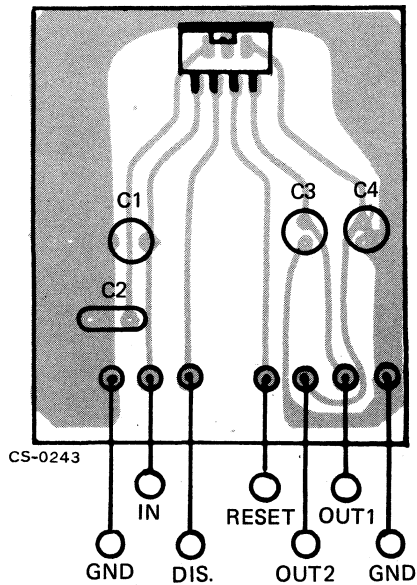


Fig. 3 – P.C. board and component layout of the circuit of Fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

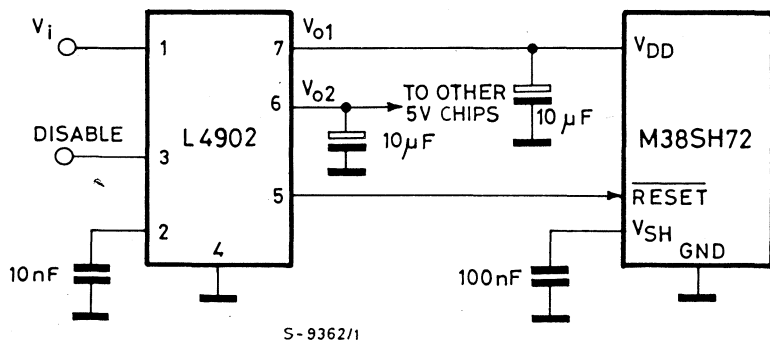
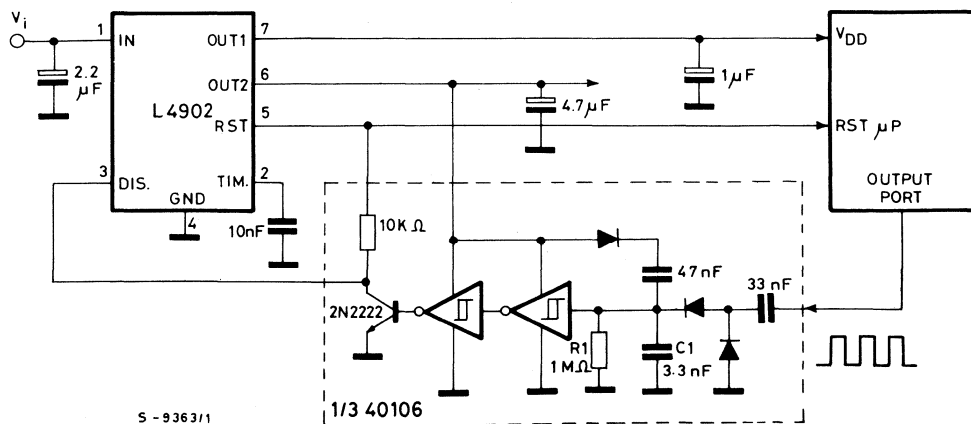


Fig. 5



APPLICATION SUGGESTION (continued)

Fig. 6 - Quiescent current vs. output current

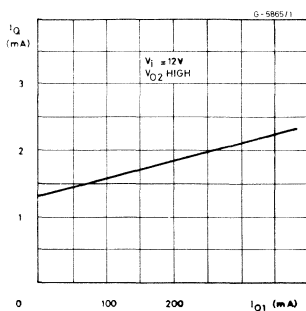


Fig. 7 - Quiescent current vs. input voltage

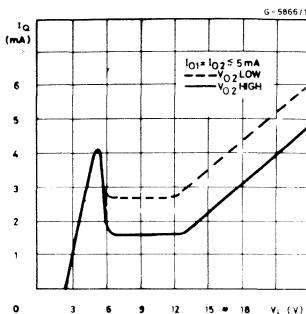


Fig. 8 - Regulator 1 output current and short circuit current vs. input voltage

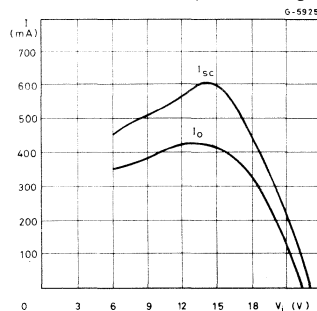


Fig. 9 - Regulator 2 output current and short circuit current vs. input voltage

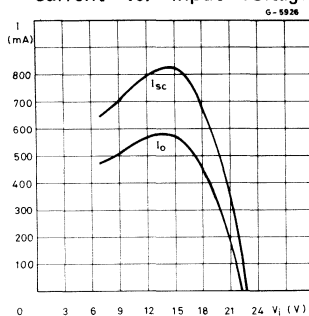
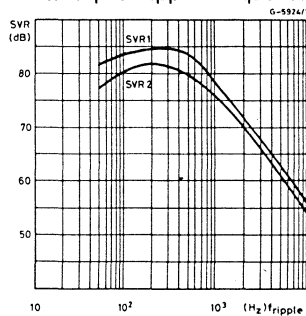


Fig. 10 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequency





L4903

ADVANCE DATA

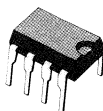
DUAL 5V REGULATOR WITH RESET AND DISABLE FUNCTIONS

- OUTPUT CURRENTS: $I_{O1} = 50\text{mA}$
 $I_{O2} = 100\text{mA}$
- FIXED PRECISION OUTPUT VOLTAGE
 $5\text{V} \pm 2\%$
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN $1\mu\text{A}$ AT OUTPUT 1
- INPUT OVERVOLTAGE PROTECTION UP TO 60V

- RESET OUTPUT LOW
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4903 is a monolithic low drop dual 5V regulator designed mainly for supplying micro-processor systems.

Reset, data save functions and remote switch on/off control can be realized.



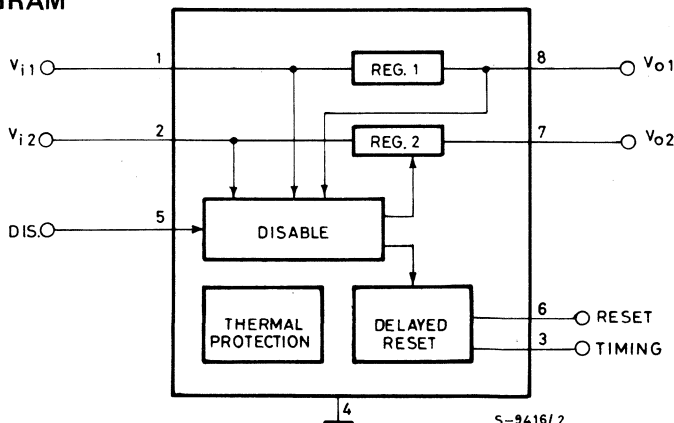
Minidip Plastic

ORDERING NUMBER: L4903

ABSOLUTE MAXIMUM RATINGS

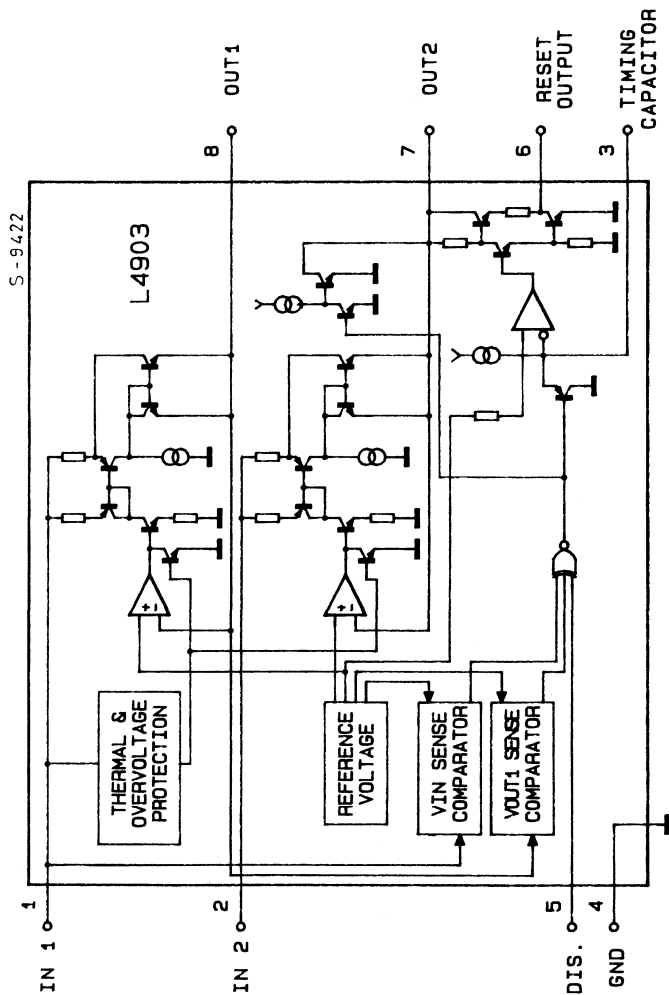
V_{IN}	DC input voltage	24	V
V_{IN}	DC operating input voltage	20	V
V_t	Transient input overvoltage ($t = 40\text{ms}$)	60	V
P_{tot}	Power dissipation at $T_{amb} = 50^\circ\text{C}$	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

BLOCK DIAGRAM



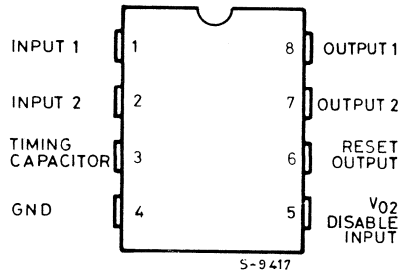
S-9416/2

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM

(Top view)



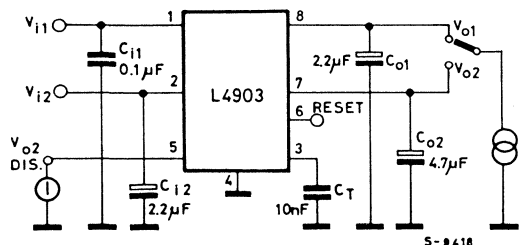
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a $5\mu\text{A}$ constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	V ₀₂ DISABLE INPUT	A high level ($> V_{DT}$) disable output Reg. 2.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched low. Therefore $t_{RD} = C_t \left(\frac{5V}{5\mu\text{A}} \right)$; $t_{RD} \text{ (ms)} = C_t \text{ (nF)}$.
7	OUTPUT 2	5V - 100mA regulator output. Enabled if $V_{O1} > V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN2} > V_{IT}$. If Reg. 2 is switched OFF the C ₀₂ capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

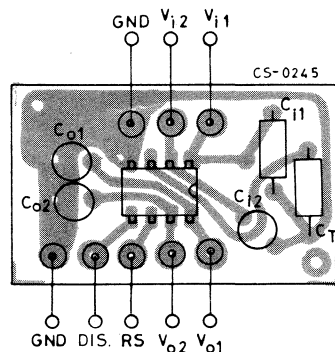
THERMAL DATA

R _{th j-pin}	Thermal resistance junction-pin 4	max	70	°C/W
R _{th j-amb}	Thermal resistance junction-ambient	max	100	°C/W

TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)



ELECTRICAL CHARACTERISTICS ($V_{IN} = 14.4V$, $T_{amb} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1} Output voltage 1	R load 1K Ω	4.95	5.05	5.15	V
V_{O2H} Output voltage 2 HIGH	R load 1K Ω	$V_{O1} - 0.1$	5	V_{O1}	V
V_{O2L} Output voltage 2 LOW	$I_{O2} = -5mA$		0.1		V
I_{O1} Output current 1 max. (*)	$\Delta V_{O1} = -100mV$	50			mA
I_{LO1} Leakage output 1 current	$V_{IN} = 0$ $V_{O1} \leq 3V$			1	μA
I_{O2} Output current 2 max. (*)	$\Delta V_{O2} = -100mV$	100			mA
V_{IO1} Output 1 dropout voltage (*)	$I_{O1} = 10mA$ $I_{O1} = 50mA$		0.7 0.75	0.8 0.9	V V
V_{IT} Input threshold voltage		$V_{O1} + 1.2$	6.4	$V_{O1} + 1.6$	V
V_{ITH} Input threshold voltage hysteresis			250		mV
ΔV_{O1} Line regulation 1	$7V < V_{IN} < 18V$ $I_{O1} = 5mA$		5	50	mV
ΔV_{O2} Line regulation 2	$I_{O2} = 5mA$		5	50	mV
ΔV_{O1} Load regulation 1	$V_{IN1} = 8V$ $5mA < I_{O1} < 50mA$		5	20	mV
ΔV_{O2} Load regulation 2	$5mA < I_{O2} < 100mA$		10	50	mV
I_Q Quiescent current	$0 < V_{IN} < 13V$ $6.3V < V_{IN} < 13V$ V_{O2} LOW $6.3V < V_{IN} < 13V$ V_{O2} HIGH $I_{O1} = I_{O2} \leq 5mA$		4.5 2.7 1.6	6 4 3.5	mA mA mA
I_{Q1} Quiescent current 1	$6.3V < V_{IN1} < 13V$ $V_{IN2} = 0$ $I_{O1} < 5mA$ $I_{O2} = 0$		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{RT} Reset threshold voltage		$V_{02}-0.4$	4.7	$V_{02}-0.2$	V
V_{RTH} Reset threshold hysteresis			50	160	mV
V_{RH} Reset output voltage HIGH	$I_R = 500\mu A$	$V_{02}-1$	4.12	V_{02}	V
V_{RL} Reset output voltage LOW	$I_R = -5mA$		0.25	0.4	V
t_{RD} Reset pulse delay	$C_t = 10nF$	6	10	14	ms
t_d Timing capacitor discharge time	$C_t = 10nF$			20	μs
V_{DT} V_{02} disable threshold voltage			1.25	2.4	V
I_D V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-100 -2		μA μA
$\frac{\Delta V_{01}}{\Delta T}$ Thermal drift	$-20^\circ C \leq T_{amb} \leq 140^\circ C$	-0.8	0.3	0.8	mV/ $^\circ C$
$\frac{\Delta V_{02}}{\Delta T}$ Thermal drift	$-20^\circ C \leq T_{amb} \leq 140^\circ C$	-0.8	0.3	0.8	mV/ $^\circ C$
SVR1 Supply voltage rejection	$f = 100Hz$ $V_R = 0.5V$ $I_o = 50mA$	54	84		dB
SVR2 Supply voltage rejection	$I_o = 100mA$	50	80		dB
T_{JSD} Thermal shut down			150		$^\circ C$

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current conditions.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4903 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function and Reg. 2 output disable.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) goes low after a programmable time T_{RD} (timing capacitor).

V_{02} is switched at low level and V_R at high level when one of the following conditions occurs:

- a high level ($> V_{DT}$) is applied on pin 5;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2 ($V_{02} - V_R = V_{CEsat}$; $I_{02} = I_{SC2}$) and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current error in power down conditions.

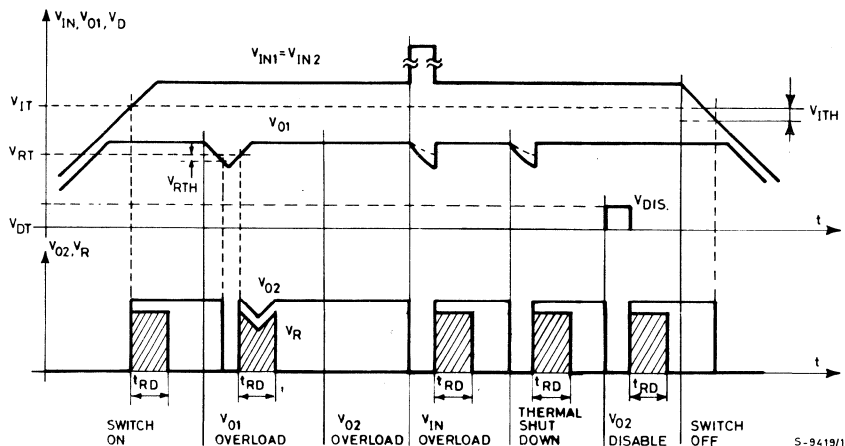
This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery without a separation diode.

CIRCUIT OPERATION (continued)

The V_{O2} output can supply other non essential 5V circuits which may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access

Fig. 1



APPLICATION SUGGESTION

Fig. 2 illustrates how the L4903's disable input may be used in a CMOS μ Computer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μ computer chip with volatile memory. V_{02} output, supplying non-essential circuits, is

turned OFF under control of a μ P unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

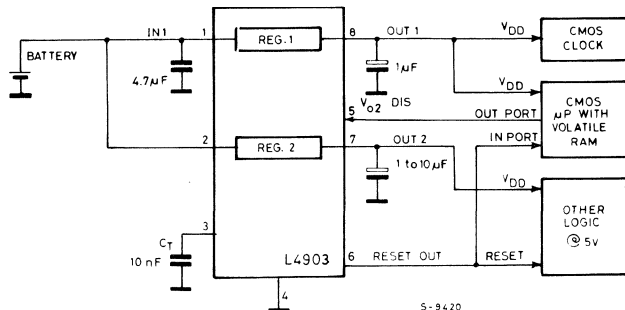


Fig. 3 - Quiescent current (Reg. 1) vs. output current

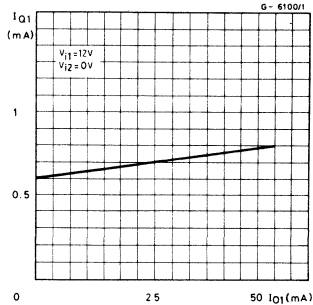


Fig. 4 - Quiescent current (Reg. 1) vs. input voltage

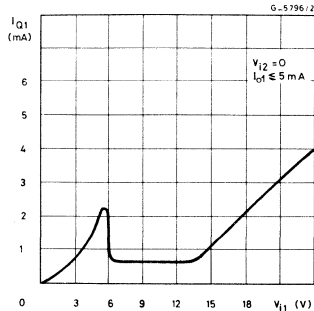


Fig. 5 -- Total quiescent current vs. input voltage

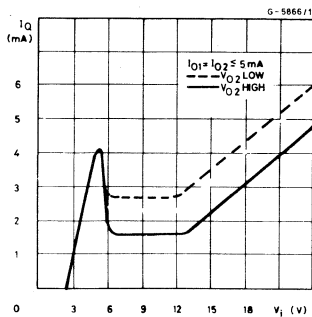
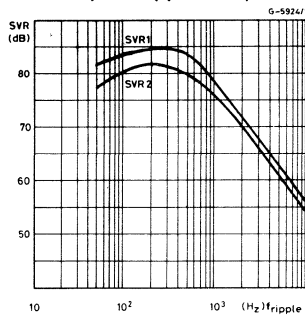


Fig. 6 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequency





L4904

ADVANCE DATA

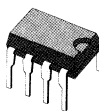
DUAL 5V REGULATOR WITH RESET

- OUTPUT CURRENTS: $I_{O1} = 50\text{mA}$
 $I_{O2} = 100\text{mA}$
- FIXED PRECISION OUTPUT VOLTAGE
 $5\text{V} \pm 2\%$
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN $1\mu\text{A}$ AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V

- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4904 is a monolithic low drop dual 5V regulator designed mainly for supplying micro-processor systems.

Reset and data save functions during switch on/off can be realized.



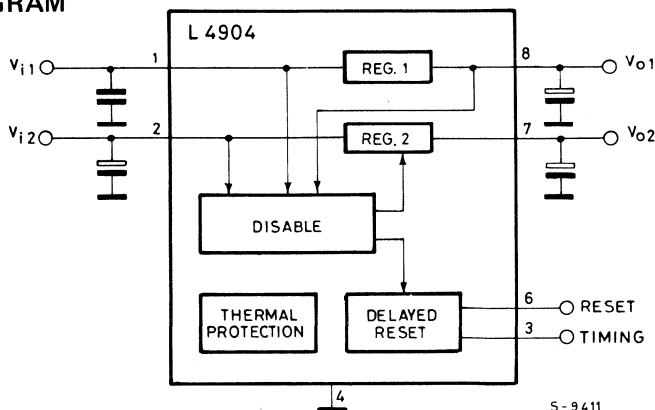
Minidip Plastic

ORDERING NUMBER: L4904

ABSOLUTE MAXIMUM RATINGS

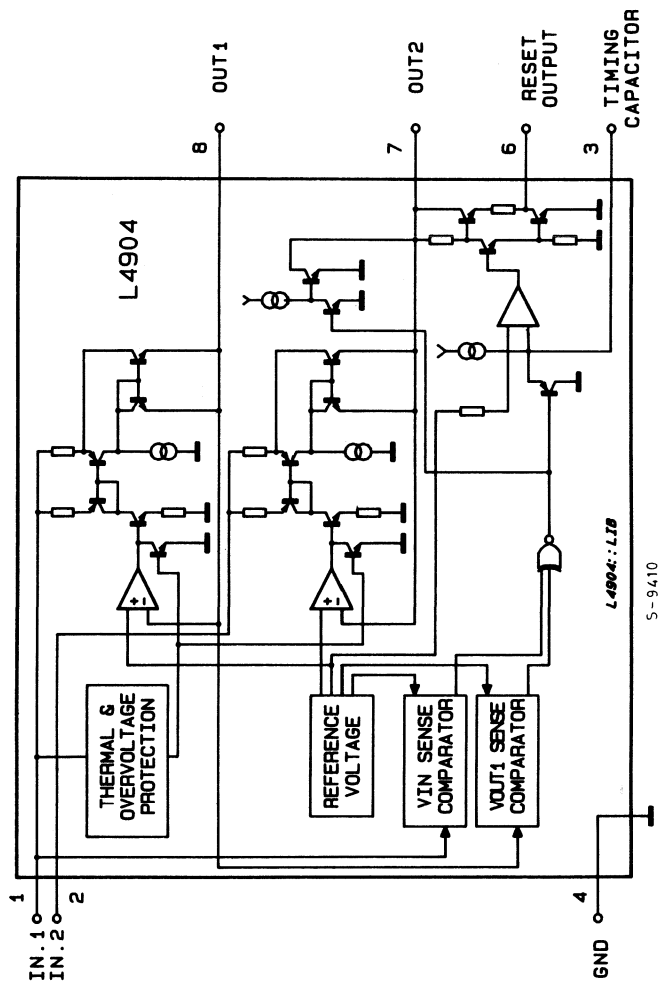
V_{IN}	DC input voltage	24	V
	DC operating input voltage	20	V
	Transient input overvoltage ($t = 40\text{ms}$)	60	V
I_O	Output current	internally limited	
P_{tot}	Power dissipation at $T_{amb} = 50^\circ\text{C}$	1	W
T_j	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

BLOCK DIAGRAM



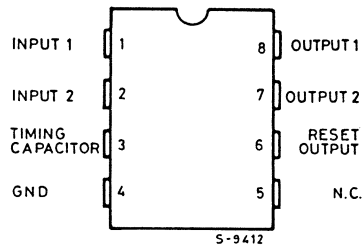
S-9411

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM

(Top view)



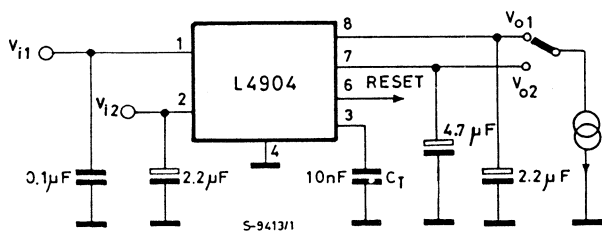
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5µA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{5\mu A} \right)$; $t_{RD} \text{ (ms)} = C_t \text{ (nF)}$.
7	OUTPUT 2	5V - 100mA regulator output. Enabled if $V_{O1} > V_{RT}$ and $V_{IN2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{O2} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

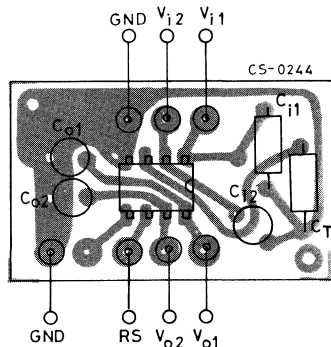
THERMAL DATA

$R_{thJ-amb}$	Thermal resistance junction-ambient	max	100	°C/W
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TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)



ELECTRICAL CHARACTERISTICS ($V_{IN} = 14.4V$, $T_{amb} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1} Output voltage 1	R load $1K\Omega$	4.95	5.05	5.15	V
V_{O2H} Output voltage 2 HIGH	R load $1K\Omega$	$V_{O1} - 0.1$	5	V_{O1}	V
V_{O2L} Output voltage 2 LOW	$I_{O2} = -5mA$		0.1		V
I_{O1} Output current 1	$\Delta V_{O1} = -100mV$	50			mA
I_{L01} Leakage output 1 current	$V_{IN} = 0$ $V_{O1} \leq 3V$			1	μA
I_{O2} Output current 2	$\Delta V_{O2} = -100mV$	100			mA
V_{IO1} Output 1 dropout voltage (*)	$I_{O1} = 10mA$ $I_{O1} = 50mA$		0.7 0.75	0.8 0.9	V V
V_{IT} Input threshold voltage		$V_{O1} + 1.2$	6.4	$V_{O1} + 1.6$	V
V_{ITH} Input threshold voltage hyst.			250		mV
ΔV_{O1} Line regulation	$7V < V_{IN} < 18V$ $I_{O1} = 5mA$ $I_{O2} = 5mA$		5	50	mV
ΔV_{O2} Line regulation 2			5	50	
ΔV_{O1} Load regulation 1	$V_{IN} = 8V$ $5mA < I_{O1} < 50mA$ $5mA < I_{O2} < 100mA$		5	20	mV
ΔV_{O2} Load regulation 2			10	50	
I_Q Quiescent current	$0 < V_{IN} < 13V$ $6.3V < V_{IN} < 13V$ $I_{O2} = I_{O1} \leq 5mA$		4.5 1.6	6 3.5	mA mA
I_{Q1} Quiescent current 1	$6.3V < V_{IN1} < 13V$ $V_{IN2} = 0$ $I_{O1} \leq 5mA$ $I_{O2} = 0$		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{RT} Reset threshold voltage		$V_{O2}-0.15$	4.9	$V_{O2}-0.05$	V
V_{RTH} Reset threshold hysteresis			50	160	mV
V_{RH} Reset output voltage HIGH	$I_R = 500\mu A$	$V_{O2}-1$	4.12	V_{O2}	V
V_{RL} Reset output voltage LOW	$I_R = -5mA$		0.25	0.4	V
t_{RD} Reset pulse delay	$C_t = 10nF$	6	10	14	ms
t_d Timing capacitor discharge time	$C_t = 10nF$			20	μs
$\frac{\Delta V_{O1}}{\Delta T}$ Thermal drift	$-20^\circ C \leq T_{amb} \leq 140^\circ C$	-0.8	0.3	+0.8	mV/ $^\circ C$
$\frac{\Delta V_{O2}}{\Delta T}$ Thermal drift	$-20^\circ C \leq T_{amb} \leq 140^\circ C$	-0.8	0.3	+0.8	mV/ $^\circ C$
SVR1 Supply voltage rejection	$f = 100Hz$ $V_R = 0.5V$ $I_O = 50mA$	54	84		dB
SVR2 Supply voltage rejection	$I_O = 100mA$	50	80		dB
T_{JSD} Thermal shut down			150		$^\circ C$

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4904 makes it very easy to supply such equipments; it provides two voltage regulators (booth 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{O1} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{O2}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{O2} and V_R are switched together at low level when one of the following conditions occurs:

— an input overvoltage

- an overload on the output 1 ($V_{O1} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2 ($V_{O2} - V_R = V_{CEsat}$; $I_{O2} = I_{SC2}$) and does not influence Reg. 1.

The V_{O1} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current error in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery without a separation diode. The V_{O1} regulator also features



L4904

CIRCUIT OPERATION (continued)

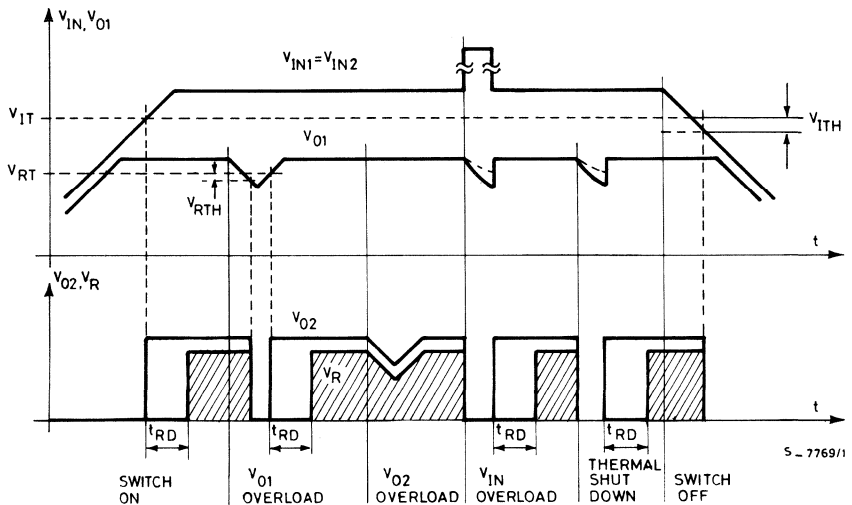
low consumption (0.6mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits which may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply

voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 3 shows the L4904 with a back up battery

on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type C-MOS μP . The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

APPLICATION SUGGESTIONS (continued)

Application Circuits of a Microprocessor system (Fig. 2) or with data save battery (Fig. 3). The reset output provide delayed rising front at the turn-off of the regulator 2.

Fig. 2

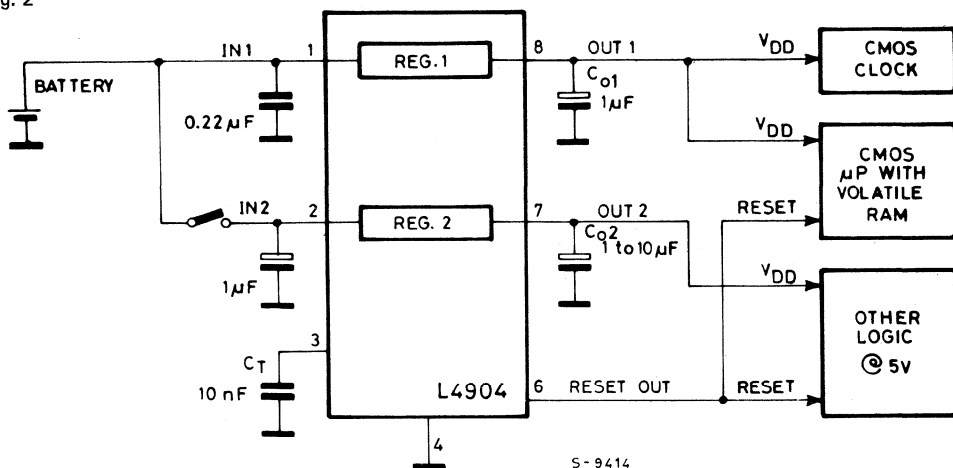
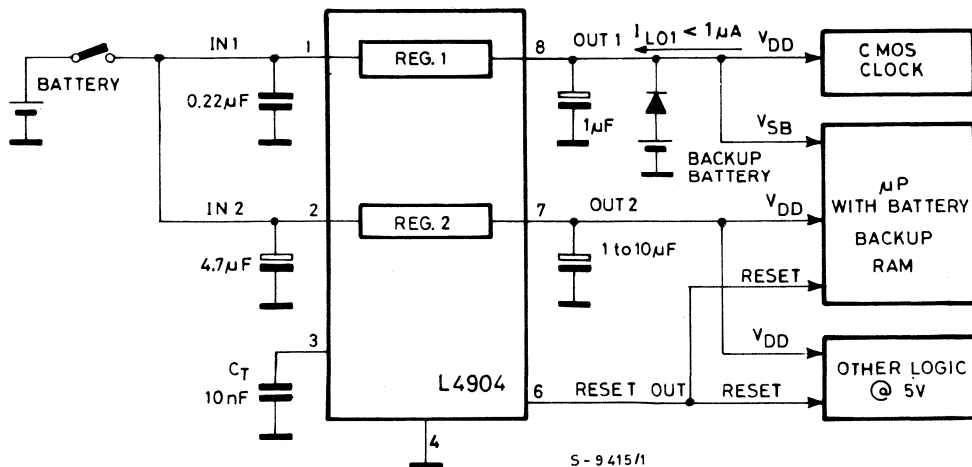


Fig. 3





L4904

APPLICATION SUGGESTIONS (continued)

Fig. 4 - Quiescent current (Reg. 1) vs. output current

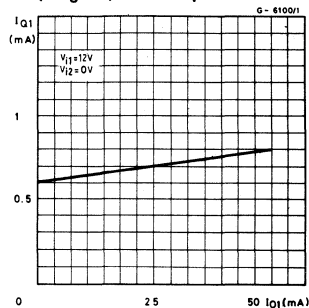


Fig. 5 - Quiescent current (Reg. 1) vs. input voltage

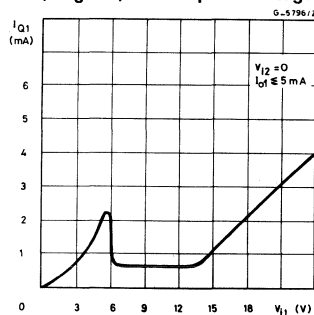


Fig. 6 - Total quiescent current vs. input voltage

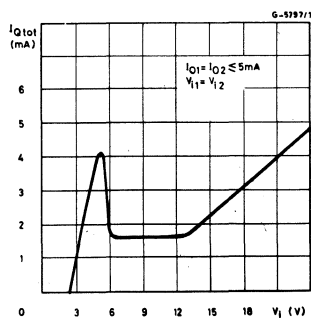
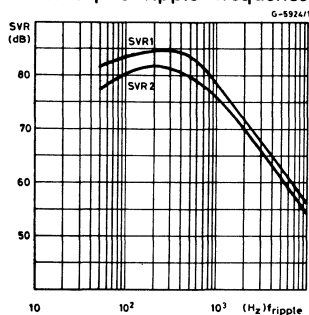


Fig. 7 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequency





L4920 L4921

PRELIMINARY DATA

VERY LOW DROP ADJUSTABLE REGULATOR

- VERY LOW DROP VOLTAGE
- ADJUSTABLE OUTPUT VOLTAGES FROM 1.25V TO 20V
- 400mA OUTPUT CURRENT
- LOW QUIESCENT CURRENT
- OVERVOLTAGE AND REVERSE VOLTAGE PROTECTION
- +60/-60 TRANSIENT PEAK VOLTAGE
- SHORT CIRCUIT PROTECTION WITH FOLDBACK CHARACTERISTICS
- THERMAL SHUT-DOWN

The L4920 and L4921 are adjustable voltage regulators with a very low voltage drop (0.4V typ. at 0.4A), low quiescent current and comprehensive on-chip protection.

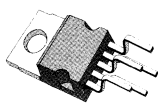
These devices are protected against load dump transients of $\pm 60V$, input overvoltage, polarity reversal and over heating.

A foldback current limiter protects against load short circuits.

The output voltage is adjustable through an external divider from 1.25V to 20V. The minimum operating input voltage is 5.2V.

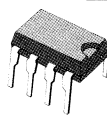
These regulators are designed for automotive, industrial and consumer applications where low consumption is particularly important.

In battery backup and standby applications the low consumption of these devices extends battery life.



Pentawatt®

L4920

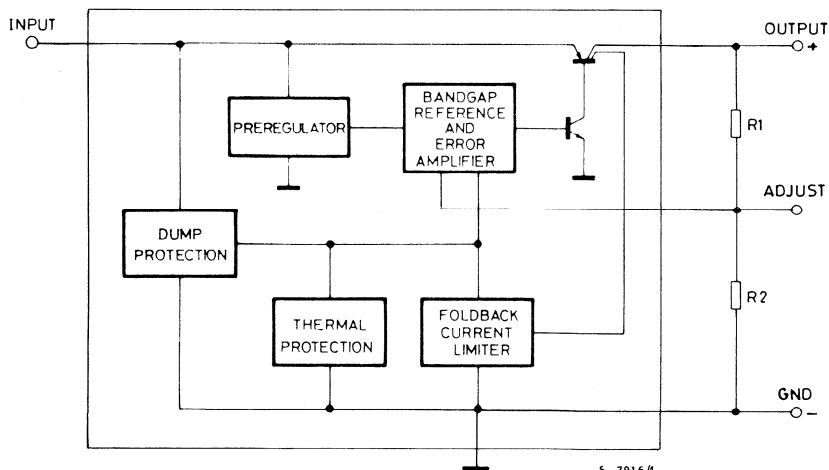


Minidip (4 + 4)

L4921

ORDERING NUMBERS:

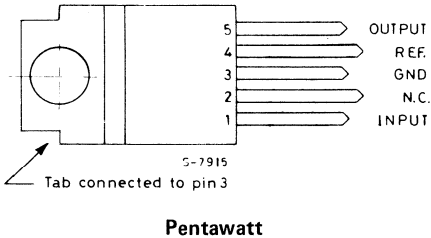
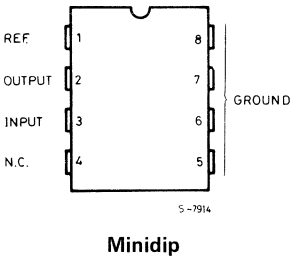
BLOCK DIAGRAM



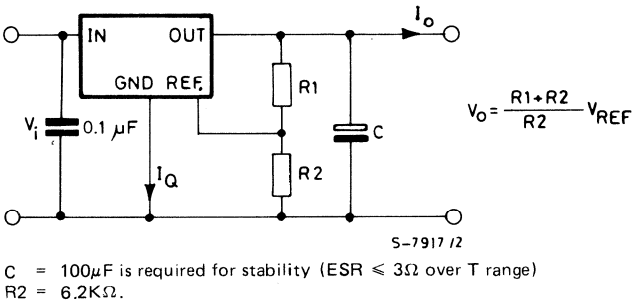
ABSOLUTE MAXIMUM RATINGS

V_i	DC input operating voltage	26	V
V_t	Positive transient peak voltage (t = 300ms 1% duty cycle)	+60	V
V_t	Negative transient peak voltage (t = 100ms 1% duty cycle)	-60	V
V_i	Reverse input voltage	-18	V
T_{stg}	Storage temperature	-55 to 150	°C
T_{op}	Operating junction temperature	-40 to 150	°C

CONNECTION DIAGRAMS (top view)



APPLICATION CIRCUIT



THERMAL DATA			Minidip (4 + 4)	Pentawatt
$R_{th \text{ j-amb}}$	Thermal resistance junction ambient	max	80°C/W	60°C/W
$R_{th \text{ j-pins}}$	Thermal resistance junction pins	max	15°C/W	—
$R_{th \text{ j-case}}$	Thermal resistance junction case	max	—	4°C/W



L4920
L4921

ELECTRICAL CHARACTERISTICS (For $V_i = 14.4V$ $V_o = 5V$; $T_j = 25^\circ C$; $C = 100\mu F$; $R_2 = 6.2K\Omega$ unless otherwise noted)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i Operating input voltage	$V_o \geq 4.5V$ $I_o = 400mA$	$V_o + 0.7$		26	V
	$V_{REF} \leq V_o < 4.5V$ $I_o = 400mA$	5.2		26	V
V_{REF} Reference voltage	$5.2V < V_i < 26V$ $I_o \leq 400mA$ (*)	1.20	1.25	1.30	V
ΔV_o Line regulation	$V_o + 1V < V_i < 26V$ $V_o \geq 4.5V$ $I_o = 5mA$		1	10	mV/ V_o
ΔV_o Load regulation	$5mA < I_o < 400mA$ (*) $V_o \geq 4.5V$		3	15	mV/ V_o
V_D Dropout voltage	$I_o = 10mA$		0.05		V
	$I_o = 150mA$		0.2	0.4	V
	$I_o = 400mA$		0.4	0.7	V
I_D Quiescent current	$I_o = 0mA$ $V_o + 1V < V_i < 26V$		0.8	3	mA
	$I_o = 400mA$ (*) $V_o + 1V < V_i < 26V$		65	100	mA
I_o Maximum output current			650	900	mA
I_{OSC} Short circuit output current (*)		200	350	500	mA
V_R Reverse polarity input voltage (DC)	$V_o \geq -1.5V$ $R_L \leq 500\Omega$			-18	V

(*) Foldback protection



L4920
L4921

Fig. 1 - Output voltage vs. temperature

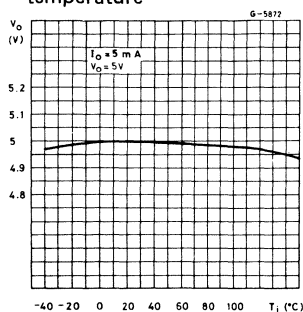


Fig. 2 - Foldback current limiting

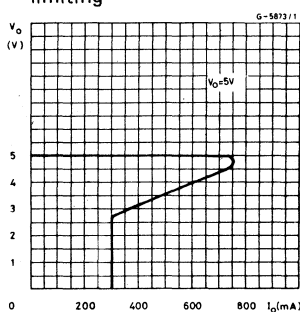
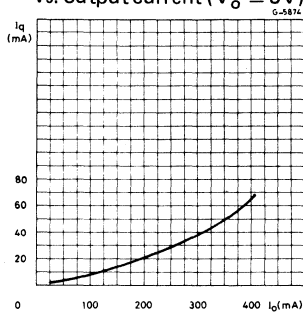


Fig. 3 - Quiescent current vs. output current ($V_o = 5 \text{ V}$)



APPLICATION INFORMATION

- 1) The L4920 and L4921 have $V_{REF} \cong 1.25 \text{ V}$. Then the output voltage can be set down to V_{REF} but V_i must be greater than 5.2 V .
- 2) As the regulator reference voltage source works in closed loop, the reference voltage may change in foldback condition.
- 3) For applications with high V_i the total power dissipation of the device with respect to the thermal resistance of the package may be limiting the application. The total power dissipation is:

$$P_{tot} = V_i I_q + (V_i - V_o) I_o$$

A typical curve giving the quiescent current I_q as a function of the output current I_o is shown in fig. 3.



L4941

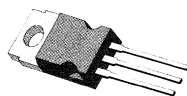
ADVANCE DATA

VERY LOW DROP 1A REGULATOR

- PRECISE 5V OUTPUT ($\pm 2\%$)
- LOW DROPOUT VOLTAGE (450mV TYP. AT 1A)
- VERY LOW QUIESCENT CURRENT
- THERMAL SHUT DOWN
- SHORT CIRCUIT CURRENT LIMITER
- OVERVOLTAGE PROTECTION
- REVERSE POLARITY PROTECTION

current capability IC particularly useful in applications such as battery powered systems where power dissipation is a design constraint.

Standard regulator features such as thermal shut down, current limiter and overvoltage protection are also provided.

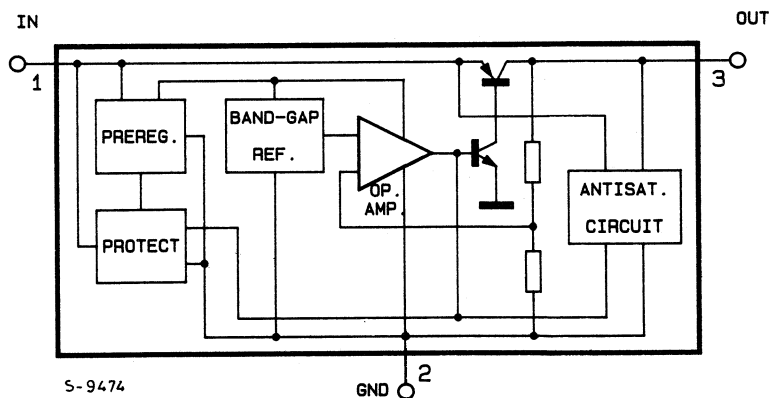


TO-220

ORDERING NUMBER: L4941BV

The L4941 is a very low input/output voltage drop, low quiescent current and high output

BLOCK DIAGRAM





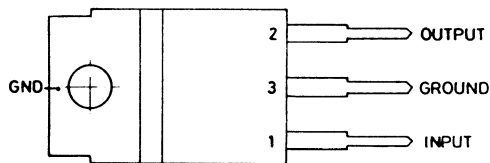
L4941

ABSOLUTE MAXIMUM RATINGS

V_i	Forward input voltage ($R_O = 100\Omega$)	40	V
V_i	Reverse input voltage ($R_O = 100\Omega$)	-15	V
T_{op}	Operating junction temperature range	-40 to 125	$^{\circ}\text{C}$
T_j	Maximum junction temperature	150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-65 to 150	$^{\circ}\text{C}$

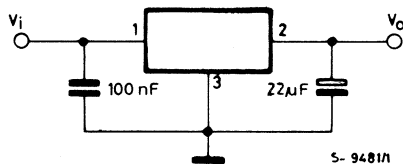
CONNECTION DIAGRAM

(Top view)



S- 2568/1

TEST AND APPLICATION CIRCUIT



THERMAL DATA

$R_{th j-case}$	Thermal resistance junction-case	max	4	$^{\circ}\text{C/W}$
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ELECTRICAL CHARACTERISTICS ($V_i = 14V$, $T_j = 25^\circ C$)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	$I_O = 5mA$	4.9	5	5.1	V
V_O	Output voltage	$V_i = 6V$ to $14V$ $I_O = 5mA$ to $1A$	4.8	5	5.2	V
V_i	Operating input voltage	(*) See note			16	V
V_O	Line regulation	$6V \leq V_i \leq 16V$ $I_O = 5mA$		5	25	mV
V_O	Load regulation	$I_O = 50mA$ to $1A$		15	35	mV
I_d	Quiescent current	$6V \leq V_i \leq 16V$ $I_O = 5mA$		3.5	10	mA
		$I_O = 1A$		20	50	
$V_i - V_O$	Dropout voltage	$I_O = 1A$		450	700	mV
		$I_O = 100mA$		150	250	
$\Delta V_O / \Delta T$	Output voltage drift			0.6		mV/ $^\circ C$
SVR	Supply voltage rejection	$f = 120Hz$ $I_O = 1A$	60			dB
I_O	Current limit			1.3		A
Z_O	Output impedance	$I_O = 200mA$ $f = 120Hz$		30		m Ω
E_N	Output noise voltage	$f = 100Hz$ to $100KHz$ $I_O = 10mA$		100		μV_{rms}

(*) For a DC input voltage $16V < V_i < 40V$ the device is not operating

Fig. 1 - Dropout output voltage vs. current

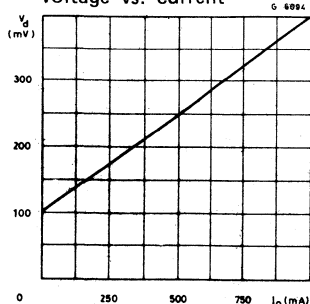


Fig. 2 - Quiescent current vs. output current

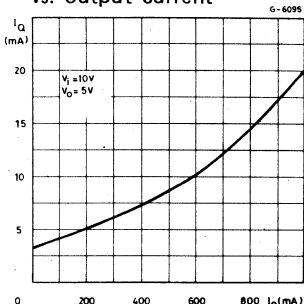


Fig. 3 - Quiescent current vs. load current

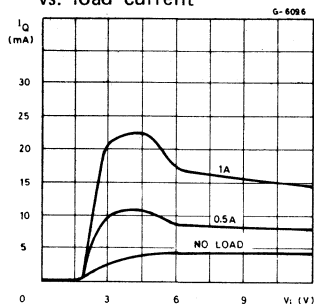


Fig. 4 - Low voltage behaviour

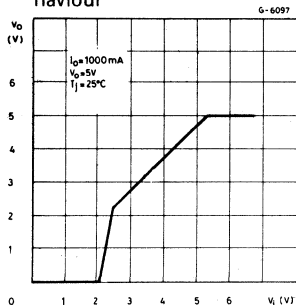


Fig. 5 - Output at voltage extremes

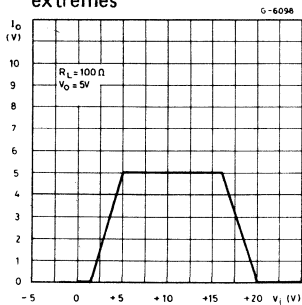


Fig. 6 - Line transient response

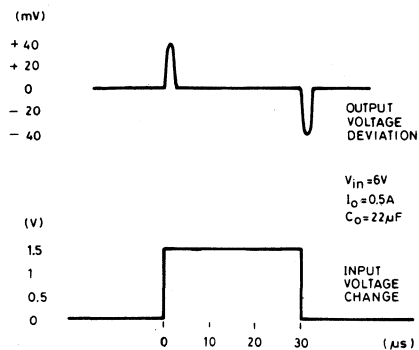
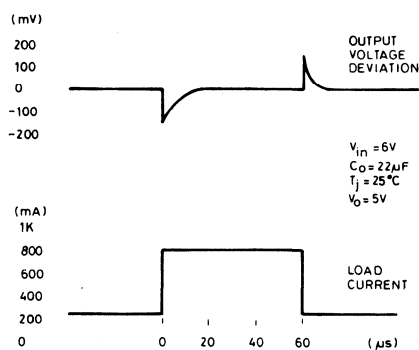
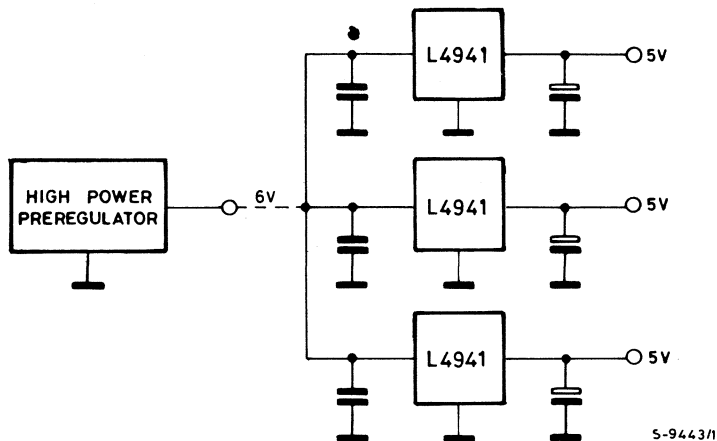


Fig. 7 - Load transient response



APPLICATION INFORMATION

Fig. 8 - Distributed supply with on-card L4941 low-drop regulators



Advantages of this application are:

- Card isolation
- Thermal and short-circuit protection
- High efficiency (80%), like switching regulators, but without radiation and intermodulation problems



L4960

PRELIMINARY DATA

2.5A POWER SWITCHING REGULATOR

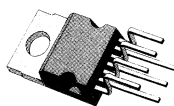
- 2.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE ($\pm 2\%$) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

The L4960 is a monolithic power switching regulator delivering 2.5A at a voltage variable from 5V to 40V in step down configuration. Features of the device include current limiting,

soft start, thermal protection and 0 to 100% duty cycle for continuous operation mode.

The L4960 is mounted in a Heptawatt plastic power package and requires very few external components.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.



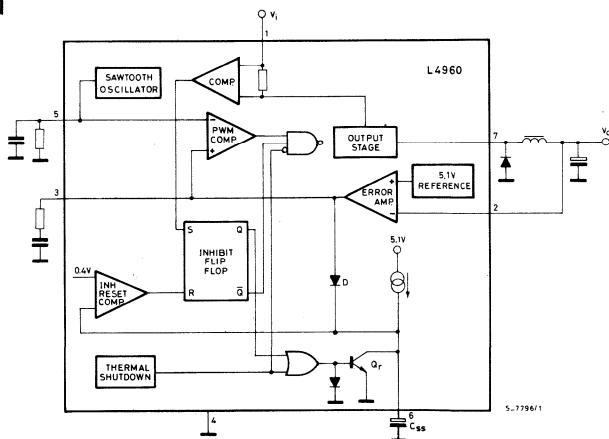
Heptawatt

ORDERING NUMBER: L4960 (Vertical)
L4960H (Horizontal)

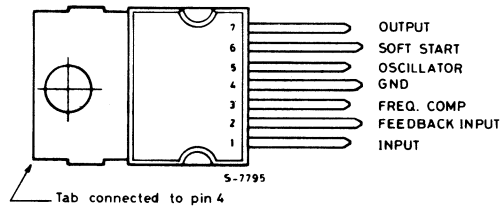
ABSOLUTE MAXIMUM RATINGS

V_1	Input voltage	50	V
$V_1 - V_7$	Input to output voltage difference	50	V
V_7	Negative output DC voltage	-1	V
	Negative output peak voltage at $t = 0.1\mu s$; $f = 100KHz$	-5	V
V_3, V_6	Voltage at pin 3 and 6	5.5	V
V_2	Voltage at pin 2	7	V
I_3	Pin 3 sink current	1	mA
I_5	Pin 5 source current	20	mA
P_{tot}	Power dissipation at $T_{case} \leq 90^\circ C$	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	$^\circ C$

BLOCK DIAGRAM



CONNECTION DIAGRAM



THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max	4	°C/W
$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	50	°C/W

PIN FUNCTIONS

N°	NAME	FUNCTION
1	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
4	GROUND	Common ground terminal.
5	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency.
6	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
7	OUTPUT	Regulator output.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_j = 25^{\circ}\text{C}$, $V_i = 35\text{V}$, unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
-----------	-----------------	------	------	------	------

DYNAMIC CHARACTERISTICS

V_o	Output voltage range	$V_i = 46\text{V}$	$I_o = 1\text{A}$	V_{ref}		40	V
V_i	Input voltage range	$V_o = V_{ref}$ to 36V	$I_o = 2.5\text{A}$	9		46	V
ΔV_o	Line regulation	$V_i = 10\text{V}$ to 40V	$V_o = V_{ref}$ $I_o = 1\text{A}$		15	50	mV
ΔV_o	Load regulation	$V_o = V_{ref}$	$I_o = 0.5\text{A}$ to 2A		10	30	mV
V_{ref}	Internal reference voltage (pin 2)	$V_i = 9\text{V}$ to 46V	$I_o = 1\text{A}$	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	$T_j = 0^{\circ}\text{C}$ to 125°C $I_o = 1\text{A}$			0.4		mV/ $^{\circ}\text{C}$
V_d	Dropout voltage	$I_o = 2\text{A}$			1.4	3	V
I_{om}	Maximum operating load current	$V_i = 9\text{V}$ to 46V $V_o = V_{ref}$ to 36V		2.5			A
I_{7L}	Current limiting threshold (pin 7)	$V_i = 9\text{V}$ to 46V $V_o = V_{ref}$ to 36V		3		4.5	A
I_{SH}	Input average current	$V_i = 46\text{V}$; output short-circuit			30	60	mA
η	Efficiency	$f = 100\text{KHz}$	$V_o = V_{ref}$		75		%
		$I_o = 2\text{A}$	$V_o = 12\text{V}$		85		%
SVR	Supply voltage ripple rejection	$\Delta V_i = 2V_{rms}$ $f_{ripple} = 100\text{Hz}$ $V_o = V_{ref}$	$I_o = 1\text{A}$	50	56		dB
f	Switching frequency			85	100	115	KHz
$\frac{\Delta f}{\Delta V_i}$	Voltage stability of switching frequency	$V_i = 9\text{V}$ to 46V			0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	$T_j = 0^{\circ}\text{C}$ to 125°C			1		%
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$	$I_o = 2\text{A}$	120	150		KHz
T_{sd}	Thermal shutdown junction temperature				150		$^{\circ}\text{C}$

**L4960****ELECTRICAL CHARACTERISTICS** (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
-----------	-----------------	------	------	------	------

DC CHARACTERISTICS

I_{1Q}	Quiescent drain current	100% duty cycle pins 5 and 7 open	$V_1 = 46V$		30	40	mA
		0% duty cycle			15	20	mA
$-I_{7L}$	Output leakage current	0% duty cycle				1	mA

SOFT START

I_{6SO}	Source current		100	130	150	μA
I_{6SI}	Sink current		50	70	120	μA

ERROR AMPLIFIER

V_{3H}	High level output voltage	$V_2 = 4.7V$	$I_3 = 100\mu A$	3.5			V
V_{3L}	Low level output voltage	$V_2 = 5.3V$	$I_3 = 100\mu A$			0.5	V
I_{3SI}	Sink output current	$V_2 = 5.3V$		100	150		μA
$-I_{3SO}$	Source output current	$V_2 = 4.7V$		100	150		μA
I_2	Input bias current	$V_2 = 5.2V$			2	10	μA
G_v	DC open loop gain	$V_3 = 1V$ to $3V$		46	55		dB

OSCILLATOR

$-I_5$	Oscillator source current		5			mA
--------	---------------------------	--	---	--	--	----

CIRCUIT OPERATION (refer to the block diagram)

The L4960 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 2.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to $\pm 2\%$).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 3. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor

C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Fig. 1 - Soft start waveforms

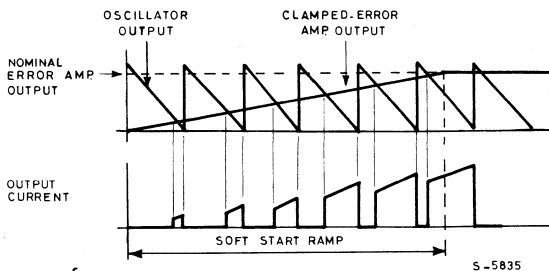


Fig. 2 - Current limiter waveforms

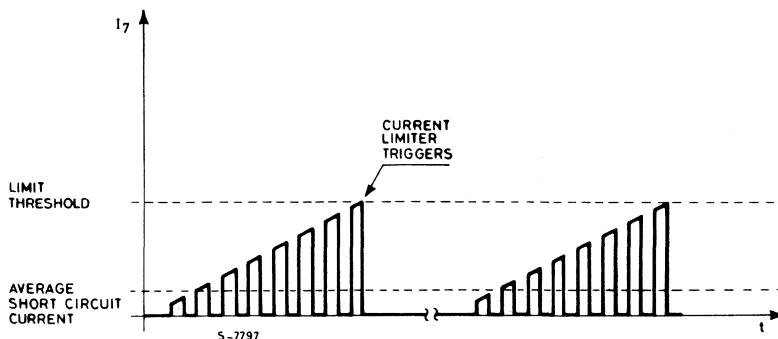
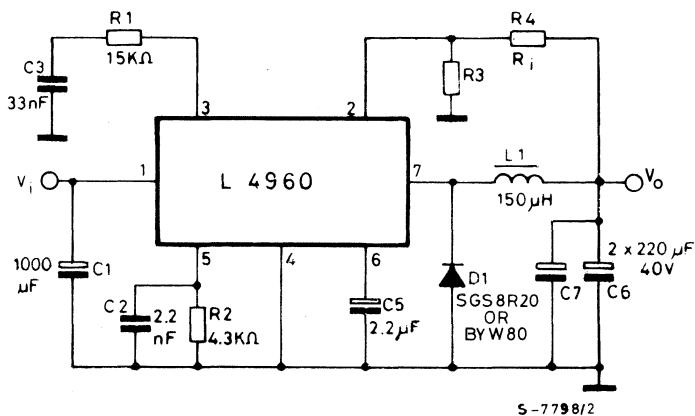


Fig. 3 - Test and application circuit



C6, C7: EKR (ROE)
 L1 = 150μH at 5A (COGEMA 946042)
 CORE TYPE: MAGNETICS 58206-A2 MPP
 N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)

Fig. 4 - Quiescent drain current vs. supply voltage (0% duty cycle)

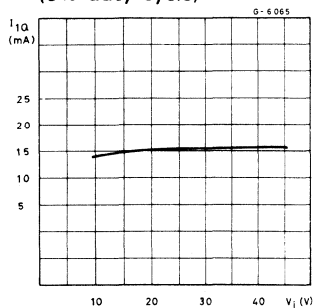


Fig. 5 - Quiescent drain current vs. supply voltage (100% duty cycle)

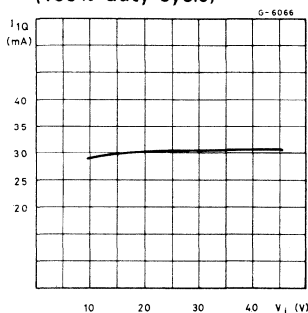


Fig. 6 - Quiescent drain current vs. junction temperature (0% duty cycle)

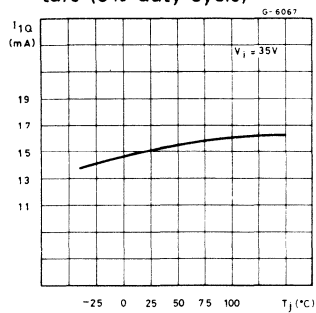


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

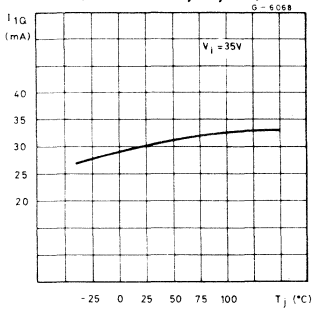


Fig. 8 - Reference voltage (pin 2) vs. V_I

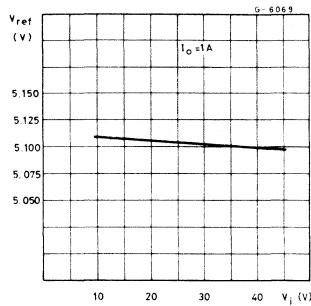


Fig. 9 - Reference voltage vs. junction temperature (pin 2)

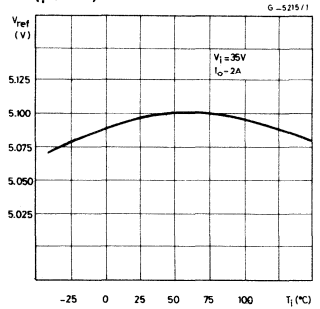


Fig. 10 - Open loop frequency and phase response of error amplifier

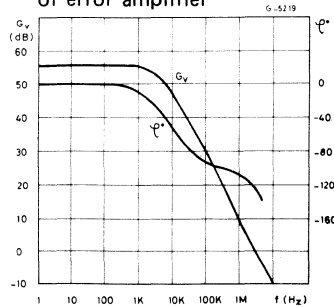


Fig. 11 - Switching frequency vs. input voltage

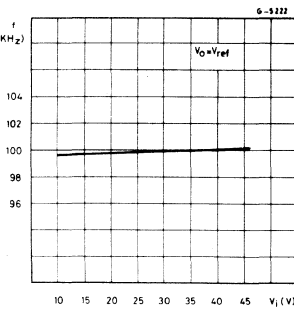


Fig. 12 - Switching frequency vs. junction temperature

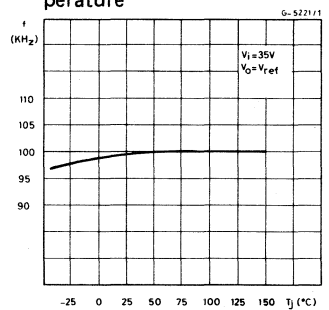


Fig. 13 - Switching frequency vs. R_2 (see test circuit)

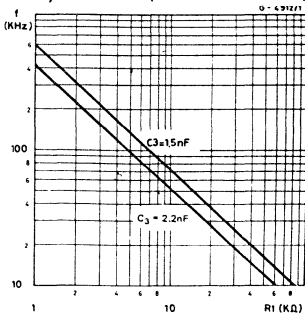


Fig. 14 - Line transient response

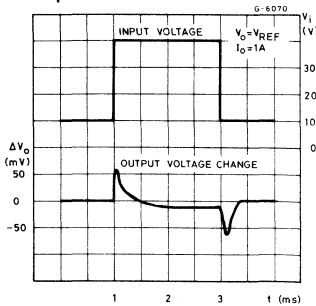
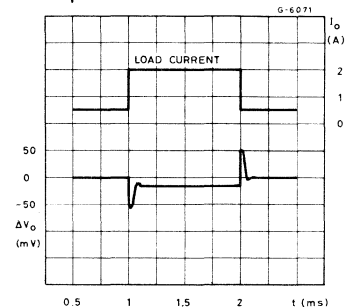


Fig. 15 - Load transient response





L4960

Fig. 16 - Supply voltage ripple rejection vs. frequency

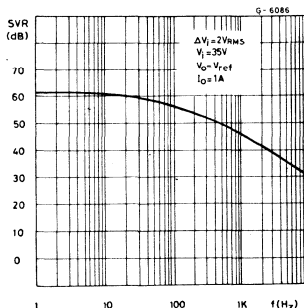


Fig. 17 - Dropout voltage between pin 1 and pin 7 vs. current at pin 7

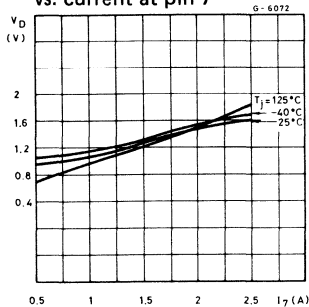


Fig. 18 - Dropout voltage between pin 1 and 7 vs. junction temperature

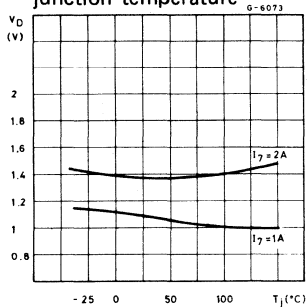


Fig. 19 - Power dissipation derating curve

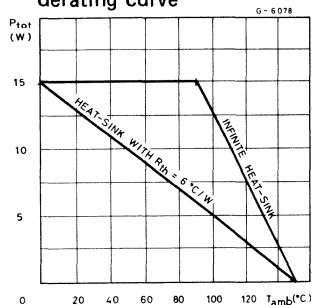


Fig. 20 - Efficiency vs. output current

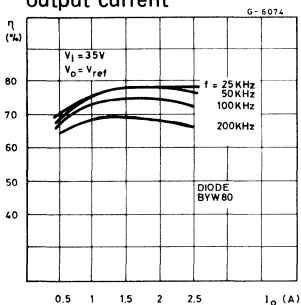


Fig. 21 - Efficiency vs. output current

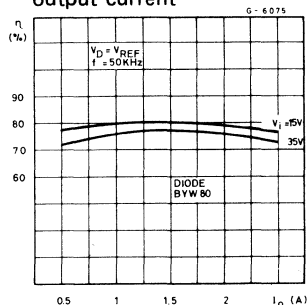


Fig. 22 - Efficiency vs. output current

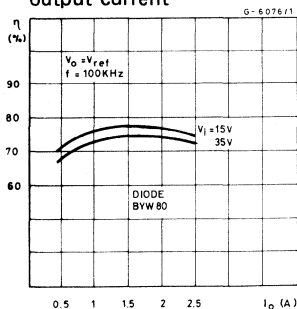
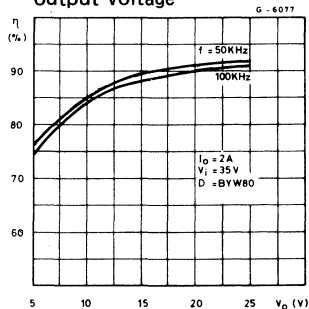
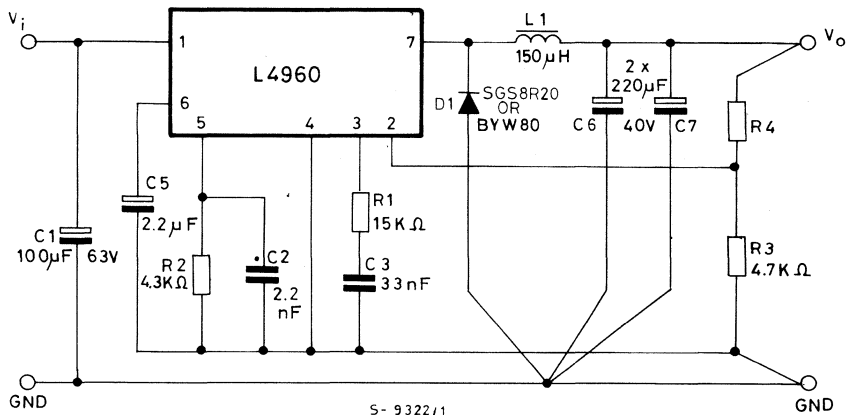


Fig. 23 - Efficiency vs. output voltage



APPLICATION INFORMATION

Fig. 24 – Typical application circuit



C₁, C₆, C₇: EKR (ROE)

D₁: BYW80 OR 5A SCHOTTKY DIODE

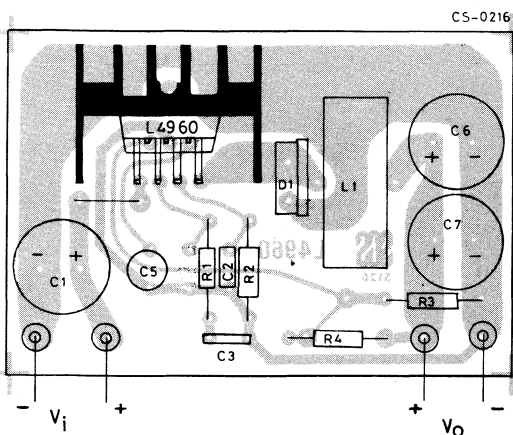
SUGGESTED INDUCTOR: L₁ = 150µH at 5A

CORE TYPE: MAGNETICS 58206 - A2 - MPP

N° TURNS: 45, WIRE GAUGE: 0.8mm (20 AWG), COGEMA 946042

U15/GUP15: N° TURNS: 60, WIRE GAUGE: 0.8mm (20 AWG), AIR GAP: 1mm, COGEMA 969051.

Fig. 25 – P.C. board and component layout of the Fig. 24 (1 : 1 scale)



Resistor values for standard output voltages

V _O	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

APPLICATION INFORMATION (continued)

Fig. 26 - A minimal 5.1V fixed regulator; Very few component are required

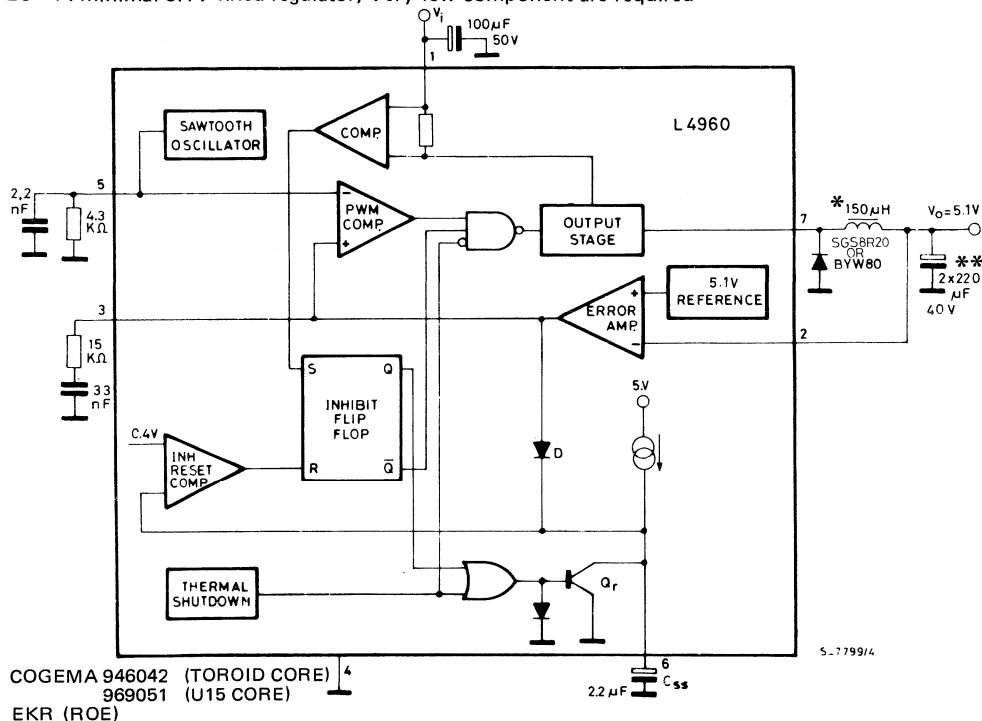
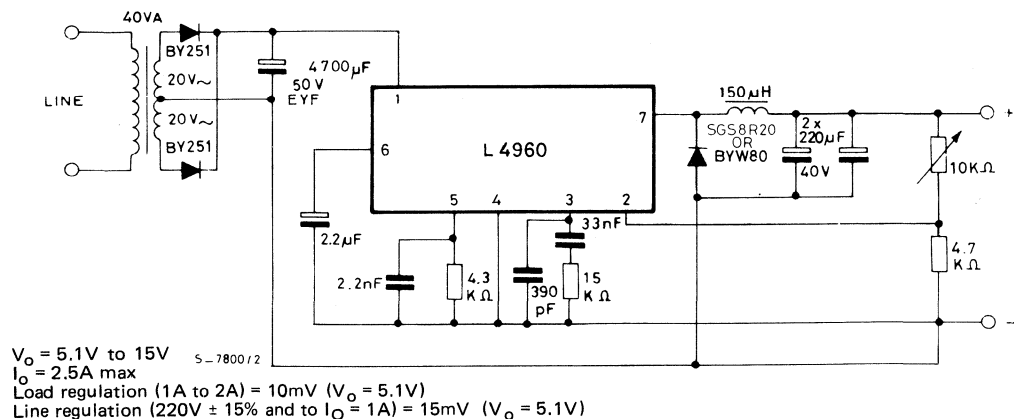
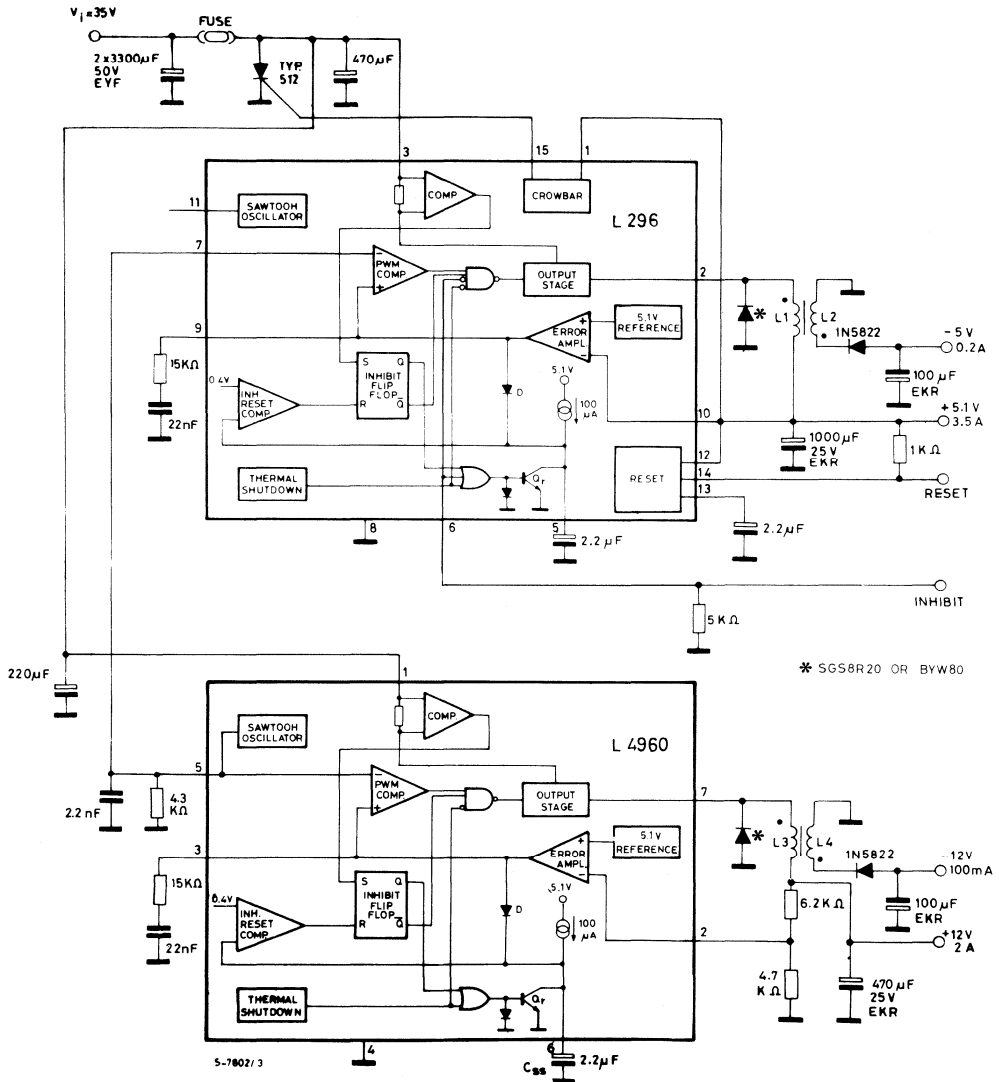


Fig. 27 - Programmable power supply



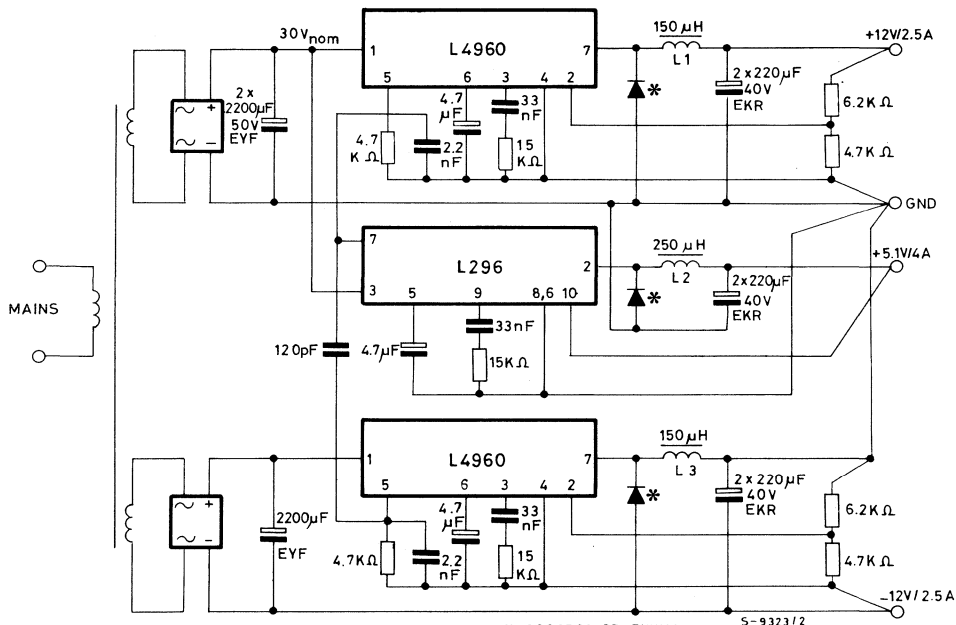
APPLICATION INFORMATION (continued)

Fig. 28 - Microcomputer supply with + 5.1V, -5V, +12V and -12V outputs



APPLICATION INFORMATION (continued)

Fig. 29 - DC-DC converter 5.1V/4A, $\pm 12V/2.5A$; a suggestion how to synchronize a negative output



L1, L3 = COGEMA 946042 (969051)

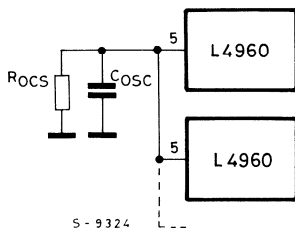
L2 = COGEMA 946044 (946045)

D₁, D₂, D₃ = SGS8R20 or BYW80

* SGS8R20 OR BYW80

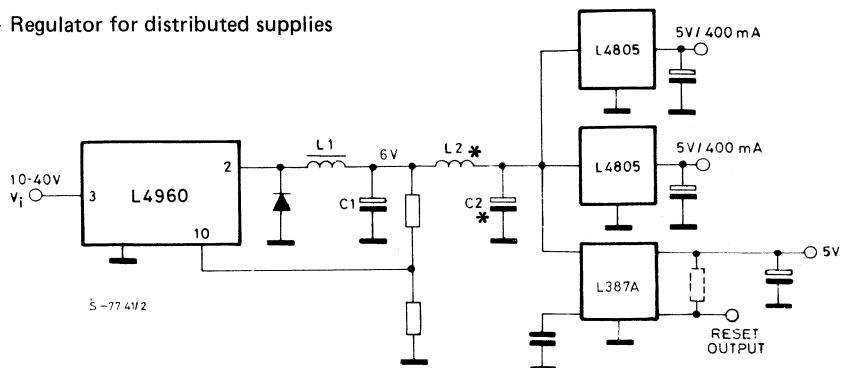
S-9323/2

Fig. 30 - In multiple supplies several L4960s can be synchronized as shown



APPLICATION INFORMATION (continued)

Fig. 31 - Regulator for distributed supplies



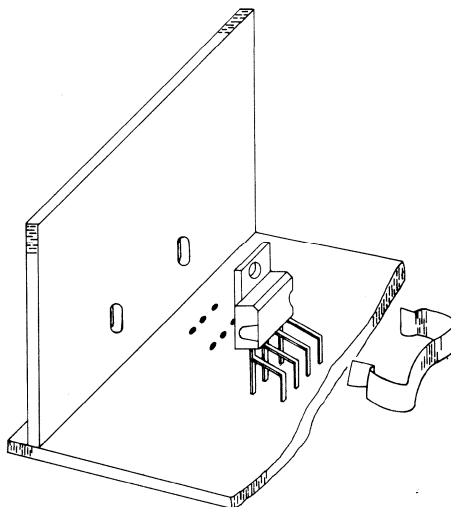
* L2 and C2 are necessary to reduce the switching frequency spikes when linear regulators are remote from L4960

MOUNTING INSTRUCTION

The power dissipated in the circuit must be removed by adding an external heatsink. Thanks to the Heptawatt package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink

and the package it is better to insert a layer of silicon grease, to optimize the thermal contact, no electrical isolation is needed between the two surfaces.

Fig. 32 - Mounting example





L4962

PRELIMINARY DATA

1.5A POWER SWITCHING REGULATOR

- 1.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE ($\pm 20\%$) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT-START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

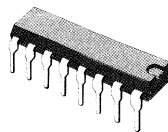
The L4962 is a monolithic power switching regulator delivering 1.5A at a voltage variable from 5V to 40V in step down configuration.

Features of device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operating mode.

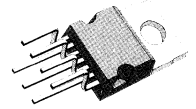
The L4962 is mounted in a 16-lead Powerdip

plastic package and Heptawatt package and requires very few external components.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.



Powerdip
(12 + 2 + 2)



Heptawatt

ORDERING NUMBER :

L4962 (12 + 2 + 2 Powerdip)

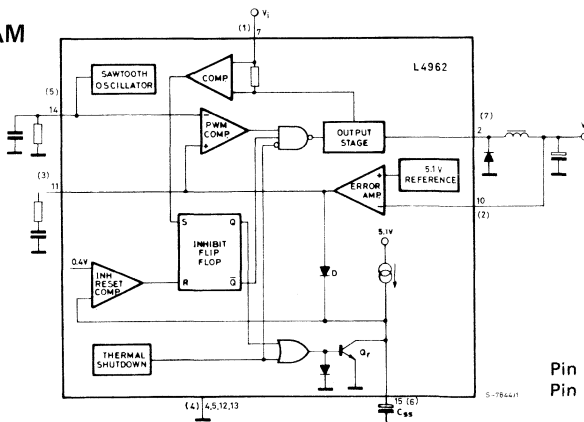
L4962E (Heptawatt)

L4962EH (Horizontal Heptawatt)

ABSOLUTE MAXIMUM RATINGS

V_7	Input voltage	50	V
$V_7 - V_2$	Input to output voltage difference	50	V
V_2	Negative output DC voltage	-1	V
	Output peak voltage at $t = 0.1\mu s, f = 100KHz$	-5	V
V_{11}, V_{15}	Voltage at pin 11, 15	5.5	V
V_{10}	Voltage at pin 10	7	V
I_{11}	Pin 11 sink current	1	mA
I_{14}	Pin 14 source current	20	mA
P_{tot}	Power dissipation at $T_{pins} \leq 90^\circ C$ (Powerdip)	4.3	W
	$T_{case} \leq 90^\circ C$ (Heptawatt)	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	$^\circ C$

BLOCK DIAGRAM



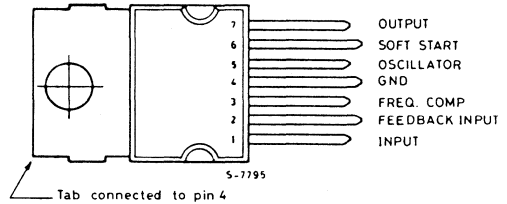
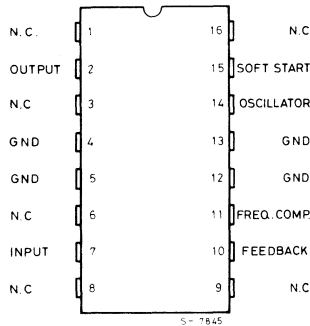
Pin X = Powerdip
Pin (X) = Heptawatt



L4962

CONNECTION DIAGRAMS

(Top view)



THERMAL DATA

			Heptawatt	Powerdip
$R_{th\ J-case}$	Thermal resistance junction-case	max	$4^{\circ}C/W$	$14^{\circ}C/W$
$R_{th\ J-plns}$	Thermal resistance junction-pins	max	$50^{\circ}C/W$	$80^{\circ}C/W^*$
$R_{th\ J-amb}$	Thermal resistance junction-ambient	max		

* Obtained with the GND pins soldered to printed circuit with minimized copper area.

PIN FUNCTIONS

HEPTAWATT	POWERDIP	NAME	FUNCTION
1	7	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	10	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	11	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
4	4, 5, 12, 13	GROUND	Common ground terminal.
5	14	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.
6	15	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. The capacitor also determines the average short circuit output current.
7	2	OUTPUT	Regulator output.
	1, 3, 6, 8, 9, 16		N.C.

**L4962****ELECTRICAL CHARACTERISTICS** (Refer to the test circuit, $T_J = 25^{\circ}\text{C}$, $V_I = 35\text{V}$, unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
-----------	-----------------	------	------	------	------

DYNAMIC CHARACTERISTICS

V_O	Output voltage range	$V_I = 46\text{V}$ $I_O = 1\text{A}$	V_{ref}		40	V
V_I	Input voltage range	$V_O = V_{ref}$ to 36V $I_O = 1.5\text{A}$	9		46	V
ΔV_O	Line regulation	$V_I = 10\text{V}$ to 40V $V_O = V_{ref}$ $I_O = 1\text{A}$		15	50	mV
ΔV_O	Load regulation	$V_O = V_{ref}$ $I_O = 0.5\text{A}$ to 1.5A		8	20	mV
V_{ref}	Internal reference voltage (pin 10)	$V_I = 9\text{V}$ to 46V $I_O = 1\text{A}$	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	$T_J = 0^{\circ}\text{C}$ to 125°C $I_O = 1\text{A}$		0.4		mV/ $^{\circ}\text{C}$
V_d	Dropout voltage	$I_O = 1.5\text{A}$		1.5	2	V
I_{om}	Maximum operating load current	$V_I = 9\text{V}$ to 46V $V_O = V_{ref}$ to 36V	1.5			A
I_{2L}	Current limiting threshold (pin 2)	$V_I = 9\text{V}$ to 46V $V_O = V_{ref}$ to 36V	2		3.3	A
I_{SH}	Input average current	$V_I = 46\text{V}$; output short-circuit		15	30	mA
η	Efficiency	$f = 100\text{KHz}$ $I_O = 1\text{A}$	$V_O = V_{ref}$		70	%
			$V_O = 12\text{V}$		80	%
SVR	Supply voltage ripple rejection	$\Delta V_I = 2V_{rms}$ $f_{ripple} = 100\text{Hz}$ $V_O = V_{ref}$ $I_O = 1\text{A}$	50	56		dB
f	Switching frequency		85	100	115	KHz
$\frac{\Delta f}{\Delta V_I}$	Voltage stability of switching frequency	$V_I = 9\text{V}$ to 46V		0.5		%
$\frac{\Delta f}{\Delta T_J}$	Temperature stability of switching frequency	$T_J = 0^{\circ}\text{C}$ to 125°C		1		%
f_{max}	Maximum operating switching frequency	$V_O = V_{ref}$ $I_O = 1\text{A}$	120	150		KHz
T_{sd}	Thermal shutdown junction temperature			150		$^{\circ}\text{C}$

**L4962****ELECTRICAL CHARACTERISTICS** (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
-----------	-----------------	------	------	------	------

DC CHARACTERISTICS

I_{7Q}	Quiescent drain current	100% duty cycle pins 2 and 14 open	$V_I = 46V$		30	40	mA
		0% duty cycle			15	20	mA
$-I_{2L}$	Output leakage current	0% duty cycle				1	mA

SOFT START

I_{15SO}	Source current		100	130	160	μA
I_{15SI}	Sink current		50	70	120	μA

ERROR AMPLIFIER

V_{11H}	High level output voltage	$V_{10} = 4.7V$	$I_{11} = 100\mu A$	3.5			V
V_{11L}	Low level output voltage	$V_{10} = 5.3V$	$I_{11} = 100\mu A$			0.5	V
I_{11SI}	Sink output current	$V_{10} = 5.3V$		100	150		μA
$-I_{11SO}$	Source output current	$V_{10} = 4.7V$		100	150		μA
I_{10}	Input bias current	$V_{10} = 5.2V$			2	10	μA
G_V	DC open loop gain	$V_{11} = 1V$ to $3V$		46	55		dB

OSCILLATOR

$-I_{14}$	Oscillator source current		5			mA
-----------	---------------------------	--	---	--	--	----

CIRCUIT OPERATION (refer to the block diagram)

The L4962 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 1.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to $\pm 2\%$).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 11. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor

citor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Fig. 1 - Soft start waveforms

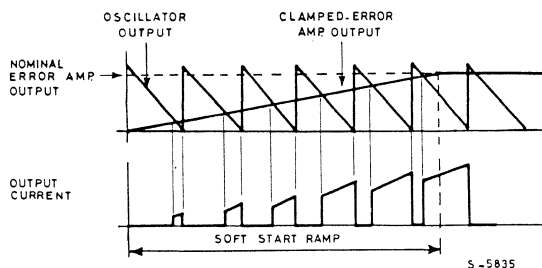


Fig. 2 - Current limiter waveforms

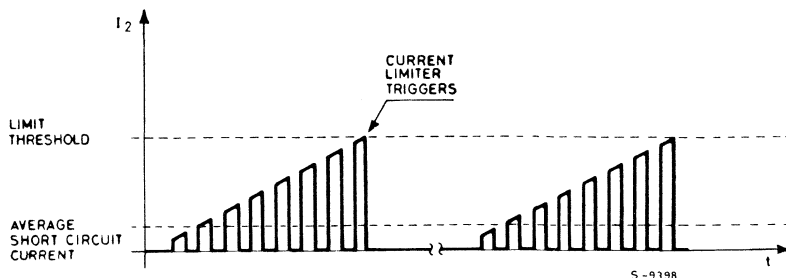
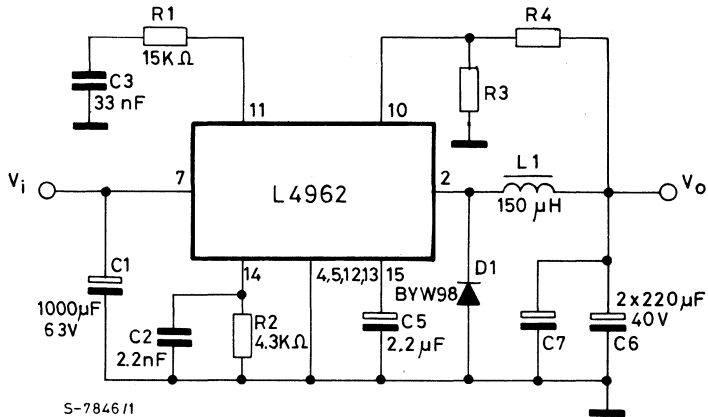


Fig. 3 - Test and application circuit (Powerdip)



- 1) D₁: BYW98 or 3A Schottky diode, 45V of VRRM;
- 2) L₁: CORE TYPE - MAGNETICS 58120 - A2 MPP
N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)
- 3) C₆, C₇: ROE, EKR 220μF 40V

Fig. 4 - Quiescent drain current vs. supply voltage (0% duty cycle)

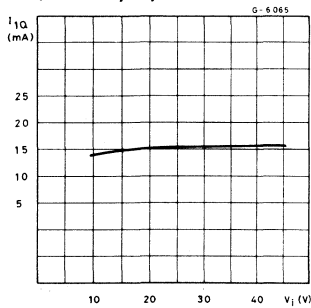


Fig. 5 - Quiescent drain current vs. supply voltage (100% duty cycle)

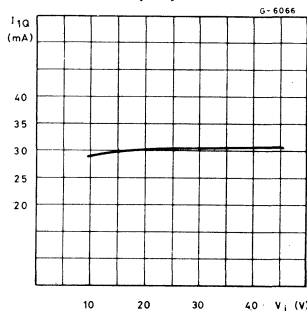


Fig. 6 - Quiescent drain current vs. junction temperature (0% duty cycle)

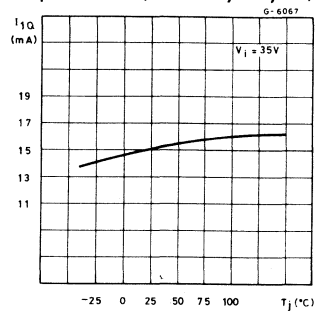


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

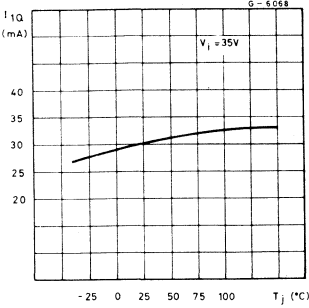


Fig. 8 - Reference voltage (pin 10) vs. V_I rdip) vs. V_I

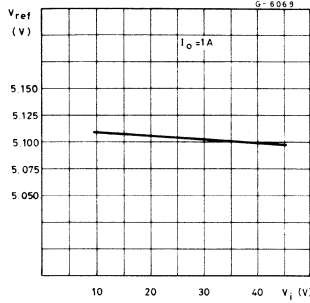


Fig. 9 - Reference voltage (pin 10) vs. junction temperature

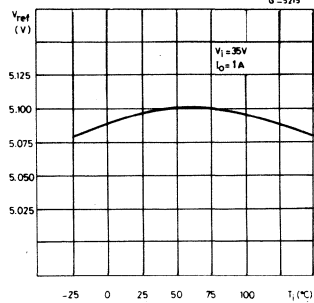


Fig. 10 - Open loop frequency and phase response of error amplifier

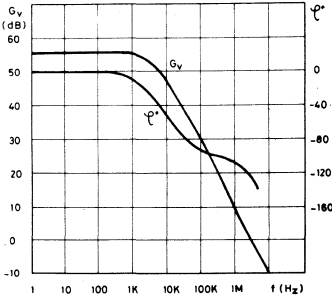


Fig. 11 - Switching frequency vs. input voltage

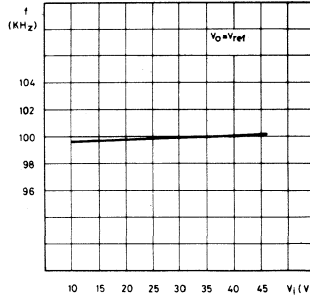


Fig. 12 - Switching frequency vs. junction temperature

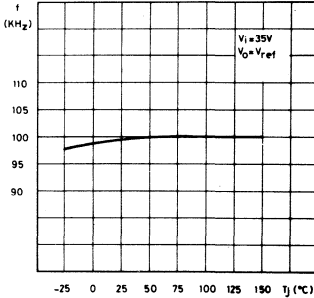


Fig. 13 - Switching frequency vs. R2 (see test circuit)

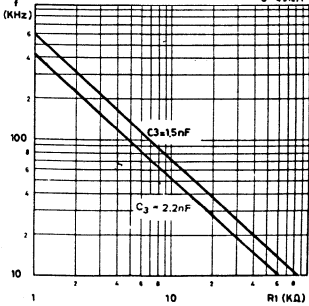


Fig. 14 - Line transient response

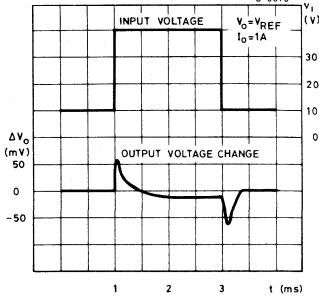


Fig. 15 - Load transient response

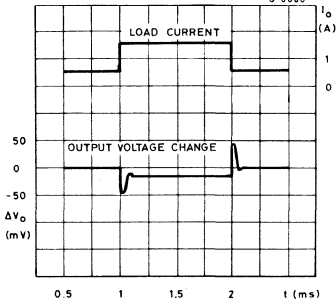


Fig. 16 - Supply voltage ripple rejection vs. frequency

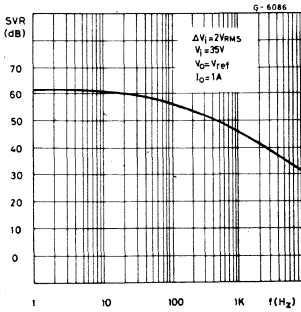


Fig. 17 - Dropout voltage between pin 7 and pin 2 vs. current at pin 2

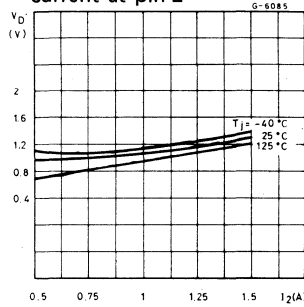


Fig. 18 - Dropout voltage between pin 7 and 2 vs. junction temperature

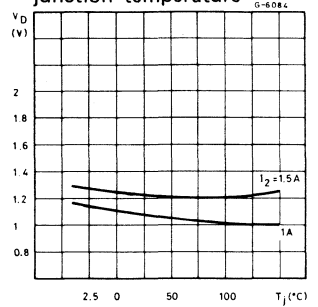


Fig. 19 - Efficiency vs. output current

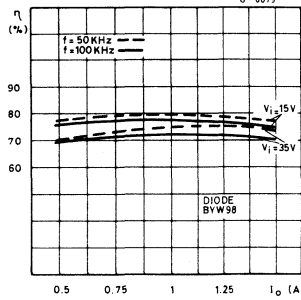


Fig. 20 - Efficiency vs. output current

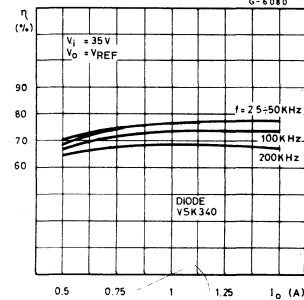


Fig. 21 - Efficiency vs. output current

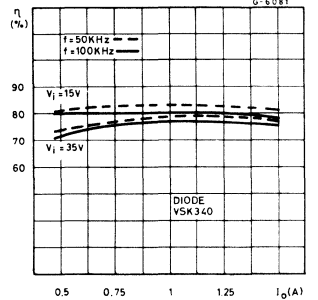


Fig. 22 - Efficiency vs. output voltage

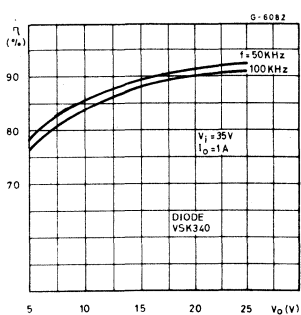


Fig. 23 - Efficiency vs. output voltage

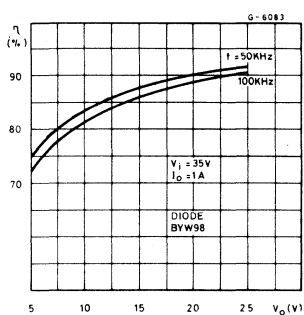
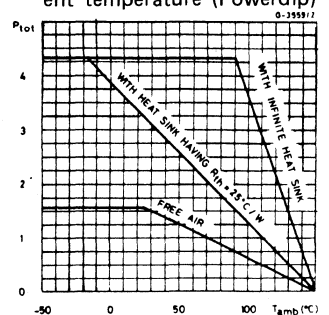
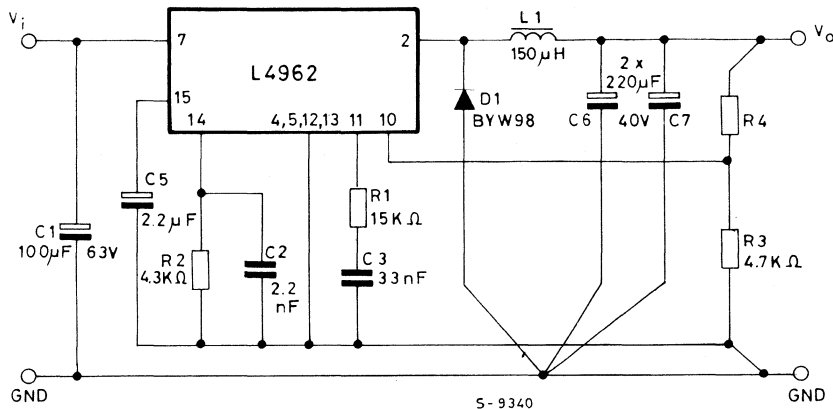


Fig. 24 - Maximum allowable power dissipation vs. ambient temperature (Powerdip)



APPLICATION INFORMATION

Fig. 25 - Typical application circuit



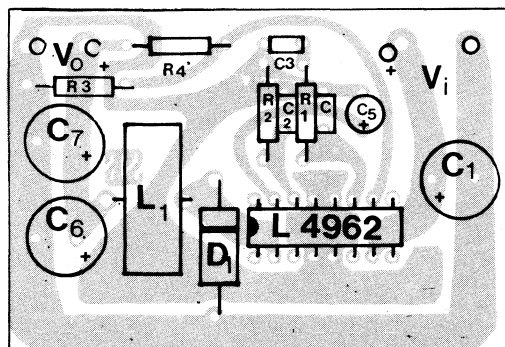
C₁, C₆, C₇: EKR (ROE)

D₁: BYW98 OR VISK340 (SCHOTTKY)

SUGGESTED INDUCTORS (L₁): MAGNETICS 58120 - A2MPP - 45 TURNS - WIRE GAUGE 0.8mm (20AWG) - COGEMA 946043

OR U15, GUP15, 60 TURNS 1mm, AIR GAP 0.8mm (20AWG) - COGEMA 969051

Fig. 26 - P.C. board and component layout of the circuit of Fig. 25 (1 : 1 scale)



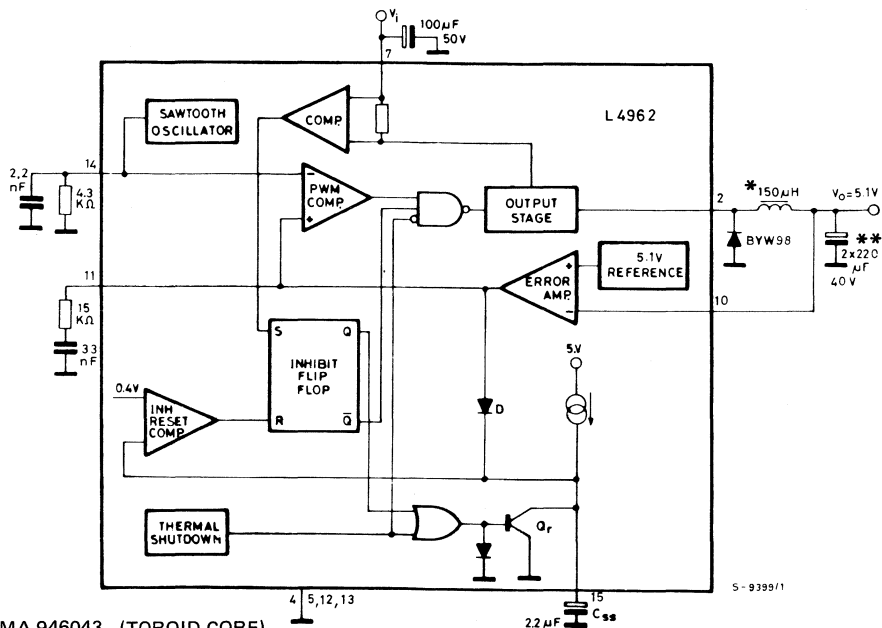
CS-0241

Resistor values for
standard output 7 voltages

V _o	R ₈	R ₇
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

APPLICATION INFORMATION (continued)

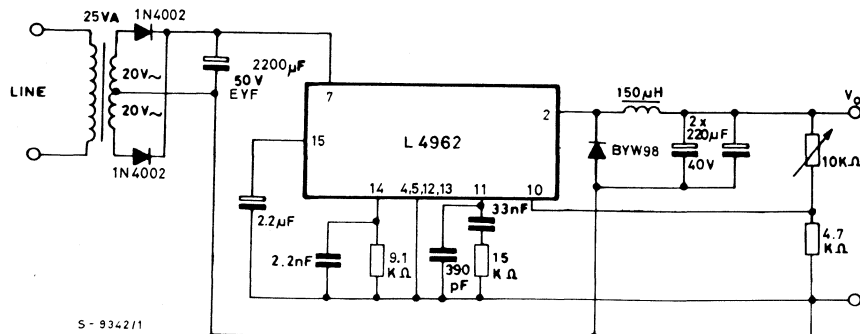
Fig. 27 - A minimal 5.1V fixed regulator; very few components are required



* COGEMA 946043 (TOROID CORE)
969051 (U15 CORE)

** EKR (ROE)

Fig. 27 - Programmable power supply



$V_O = 5.1V$ to $15V$

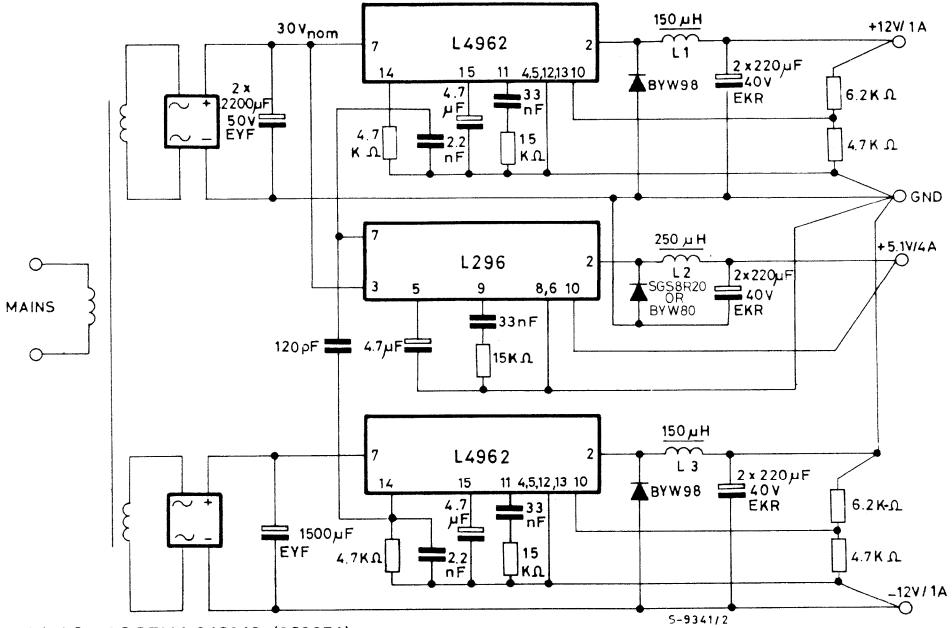
$I_O = 1.5A$ max

Load regulation ($0.5A$ to $1.5A$) = $10mV$ ($V_O = 5.1V$)

Line regulation ($220V \pm 15\%$ and to $I_O = 1A$) = $15mV$ ($V_O = 5.1V$)

APPLICATION INFORMATION (continued)

Fig. 29 - DC-DC converter 5.1V/4A, $\pm 12V/1A$. A suggestion how to synchronize a negative output



L1, L3 = COGEMA 946043 (969051)
L2 = COGEMA 946044 (946045)

Fig. 30 - In multiple supplies several L4962s can be synchronized as shown

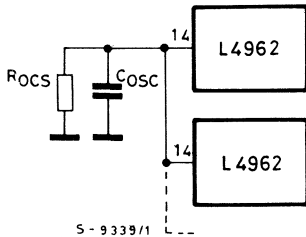
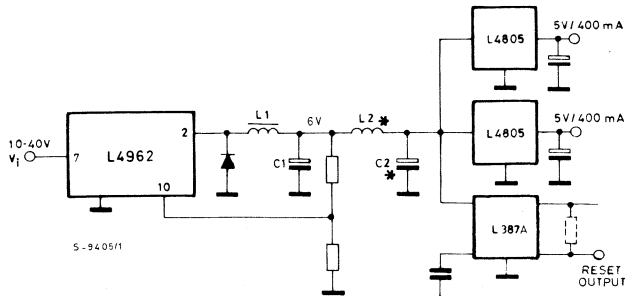


Fig. 31 - Preregulator for distributed supplies



* L2 and C2 are necessary to reduce the switching frequency spikes when linear regulators are remote from L4962

MOUNTING INSTRUCTION

The $R_{thj-amb}$ of the L4962 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 32). The diagram of figure 33 shows the $R_{thj-amb}$ as a function of the side "l" of two equal square copper areas having the thickness of 35μ (1.4

mils). During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds. The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 32 – Example of P.C. board copper area which is used as heatsink

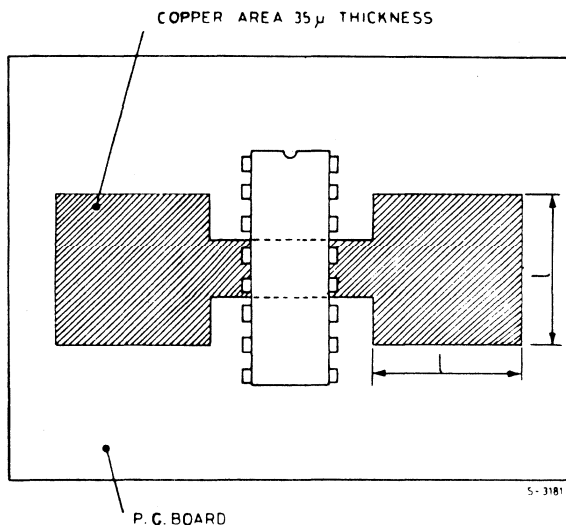
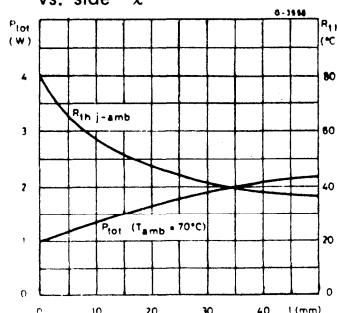


Fig. 33 – Maximum dissippable power and junction to ambient thermal resistance vs. side "l"





L5832

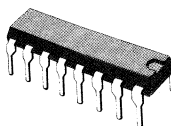
SOLENOID CONTROLLER

- DRIVES ONE OR TWO EXTERNAL DARLINGTONS
- DUAL AND SINGLE LEVEL CURRENT CONTROL
- SWITCHMODE CURRENT REGULATION
- ADJUSTABLE PEAK DURATION
- WIDE SUPPLY RANGE (4.75-46V)
- TTL-COMPATIBLE LOGIC INPUTS
- THERMAL PROTECTION

The L5832 Solenoid Controller is designed for use with one or two external darlington transistors in solenoid and relay driving applications. The device is controlled by two logic inputs and features switchmode regulation of the load current. A key feature of the L5832 is flexibility. It can be used with a variety of darlington transistors to

match the requirements of the load and it allows both simple and two level current control. Moreover, the drive waveshape can be adjusted by external components. Other features of the device include thermal shutdown, a supply voltage range of 4.75-46V and TTL-compatible inputs.

The L5832 is supplied in a 12 + 2 + 2 - lead Powerdip package which uses the four center pins to conduct heat to the PC board copper.



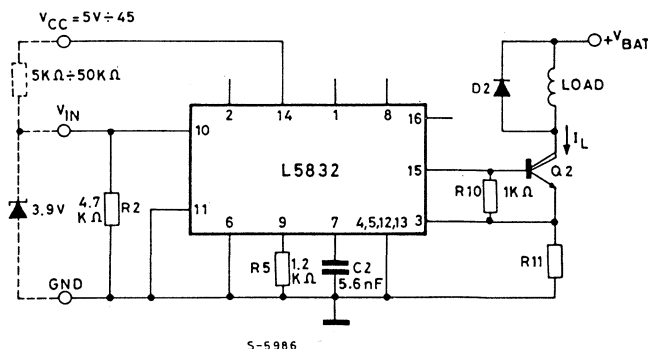
Powerdip
12 + 2 + 2

ORDERING NUMBER: L5832

ABSOLUTE MAXIMUM RATINGS

V_s	DC Supply voltage	46	V
V_g	(Positive transient voltage at pin 8)	60	V
V_{en}	Enable input voltage (pin 11)	7	V
V_i	Input voltage (pin 10)	7	V
V_R	External reference voltage (pin 2)	2	V
P_d	Power dissipation ($T_{case} = 80^\circ\text{C}$)	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

APPLICATION CIRCUIT USING ONE DARLINGTON

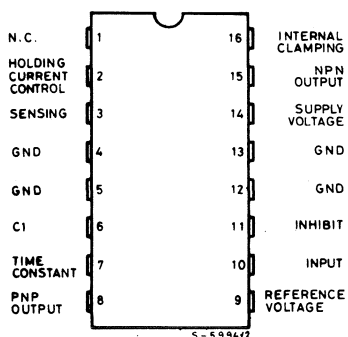


S-5986

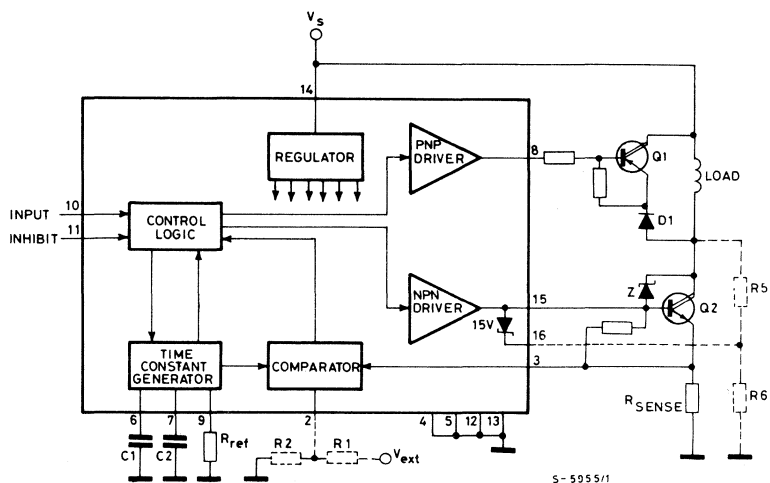


L5832

CONNECTION DIAGRAM



BLOCK DIAGRAM



THERMAL DATA

$R_{th \text{ j-case}}$	Thermal resistance junction-case	max	14	°C/W
$R_{th \text{ j-amb}}$	Thermal resistance junction-ambient	max	80	°C/W



PIN FUNCTIONS

N°	NAME	FUNCTION
1	NC	Not connected. Must be left open circuit.
2	HOLDING CURRENT CONTROL	A voltage applied to this pin sets the holding current level. If left open circuit an internal 75 mV reference is used and $I_h = I_p/6$.
3	SENSING	Connection for load current sense resistor. Value sets the maximum load current. $I_p = 0.45/R_s$.
4	GROUND	Ground connection. With pins 5, 12 and 13 conducts heat to printed circuit board copper.
5	GROUND	See pin 4.
6	C1	A capacitor connected between this pin and ground sets the duration of the current peak (t_2 in fig. 3). If left open, the switchmode control of the peak is suppressed. If grounded, the current does not fall to the holding level.
7	DISCHARGE TIME CONSTANT	A capacitor connected between this pin and ground sets the duration of t_{off} (fig. 3). If grounded, switchmode control is suppressed.
8	PNP DRIVING OUTPUT	Current drive output for external PNP darlington (for recirculation). $I = 35 I_{ref}$.
9	REFERENCE VOLTAGE	A resistor connected between this pin and ground sets the internal current reference, I_{ref} . The recommended value is 1.2 k Ω , giving $I_{ref} = 1$ mA.
10	INPUT	TTL-compatible input. A high level on this pin activates the output, driving the load.
11	INHIBIT	TTL-compatible inhibit input. A high level on this input disables the output stages and logic circuitry, irrespective of the state of pin 10.
12	GROUND	See pin 4.
13	GROUND	See pin 4.
14	SUPPLY VOLTAGE	Supply voltage input.
15	NPN DRIVING OUTPUT	Current drive for external NPN darlington (in series with the load). $I = 100 I_{ref}$.
16	INTERNAL CLAMPING	Internal zener clamp available for fast turnoff.

ELECTRICAL CHARACTERISTICS (V_s (pin 14) = 14V, T_{amb} = 25°C, R_{ref} = 1.2K Ω , unless otherwise specified. Refer to Fig. 2)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s Operating supply voltage (Pin 14)		4.75		46	V
I_s Quiescent current (Pin 14)	$V_{pin10} = V_{pin11} = \text{Low State}$		21	40	mA
V_{in} Input voltage (Pin 10)	Low state			0.8	V
V_{en} Enable input voltage (Pin 11)	High state	2.4			V
I_{in} Input current (Pin 10)	Low state			100	μA
I_{en} Enable input current (Pin 11)	High state			10	μA
V_{ref} Internal reference voltage (Pin 9)		1.2	1.25	1.3	V
I_{ref} Reference current (Pin 9)	$I_{ref} = V_{ref}/R_{ref}$ $R_{ref} = 1.2K\Omega$			1300	μA
I_{pd} Peak duration control current (Pin 6)	$I_{pd} = I_{ref}/8$	110	130	180	μA
t_{pd} Peak duration time (Pin 6)	$t_{pd} = C_1 V_{th}/I_{pd}$ $V_{th} = 1.4V$ $C_1 = 4.7nF$		500		μs
I_{od} Off duration control current (Pin 7)	$I_{od} = I_{ref}/8$	110	130	180	μA
t_{off} Off duration time (Pin 7)	$t_{od} = C_2 V_{th}/I_{od}$ $V_{th} = 1.4V$ $C_2 = 4.7nF$		50		μs
I_{d1} NPN driving current (Pin 15)	$I_{d1} = 100 I_{ref}$ (only present during charging phase)	80	100	130	mA
I_{d2} PNP driving current (Pin 8)	$I_{d2} = 35 I_{ref}$	28	35	48	mA
I_p Peak current (emitter of NPN Darlington)	$I_p = 450mV/R_{sens}$ $R_{sens} = 0.1\Omega$	4.2	4.5	4.8	A
V_h Holding current control voltage	$V_h = R_{sens} I_h$ $I_h = \text{Emitter current of NPN Darlington}$ Pin 2 Floating	70	75	85	mV
	Pin 2 externally biased			2	V
R_{in} Holding current control input impedance (Pin 2)		100	150	200	Ω
r Peak to hold current ratio	Pin 2 floating	5.8	6	6.2	
	Pin 6 shorted	0.97	1	1.03	
I_B Sense input bias current (Pin 3)				100	μA
V_{clamp} Internal clamping (Pin 16 to 15)	$I = 200\mu\text{A}$	14	16	18	V
V_{dt} Dump protection threshold voltage (Pin 1)		28	32	34	V
R_{dt} Dump protection threshold input impedance (Pin 1)		22	32	42	K Ω
Thermal drift of reference voltage			0.5		mV/°C

APPLICATION INFORMATION

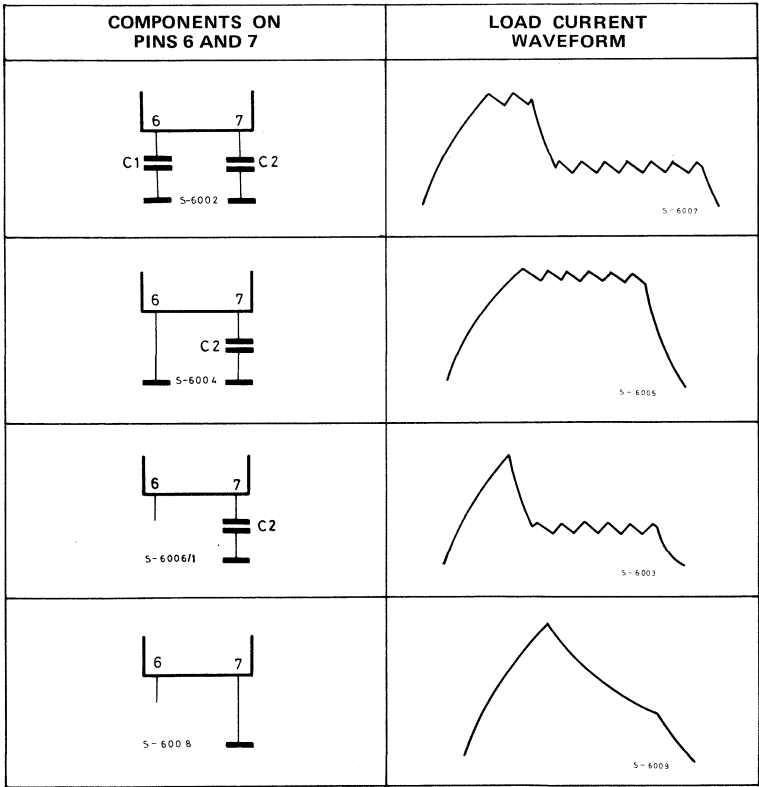
The L5832 solenoid controller is intended for use with one or two external darlington transistors to drive inductive loads such as solenoids, relays, electric valves and DC motors.

Controlled by a logic input and an inhibit input (both TTL compatible), the device drives the external darlington(s) to produce a load current waveform as shown in figure 3. This basic waveform shows that the device produces an initial current peak followed by a lower holding current. Both the peak and holding current levels are regulated by the L5832's switchmode circuitry.

The duration of the peak, the peak current level and holding current level can all be adjusted by external components.

Moreover, by omitting C1, C2 or both it is possible to realize single-level current control, a transitory peak followed by a regulated holding current or a simple peak (figure 1).

Fig. 1 – Components connected to pins 6 and 7 determine the load current waveshape



APPLICATION INFORMATION (continued)

The peak current level I_p , is set by the sensing resistor, R_{sens} , and is found from:

$$I_p = \frac{0.45}{R_{sens}}$$

The holding current level, I_h , is set by a voltage applied to pin 2. If this pin is left open circuit an internal reference of 75 mV supervenes and the holding current is given by:

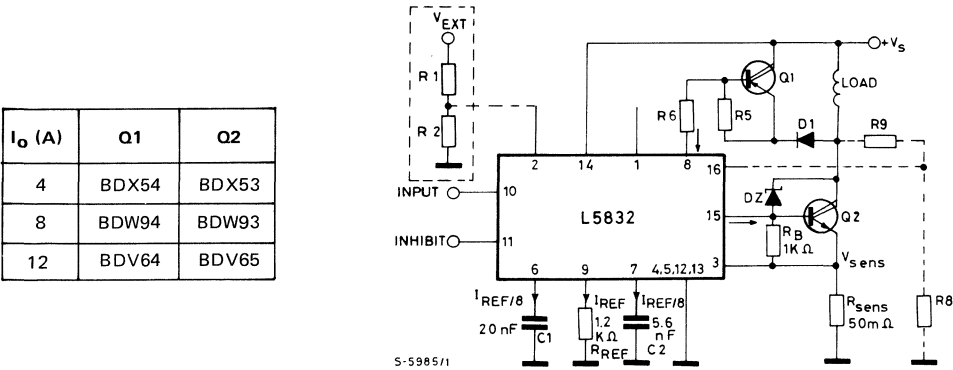
$$I_h = \frac{I_p}{6}$$

Alternatively, this level may be varied by adding a divider to pin 2 ($R1$, $R2$) and suitable values are found from:

$$\frac{I_{h\ max}}{I_p} = \frac{1}{0.45V} \left(\frac{R2 // R_{in}}{R1 + R2 // R_{in}} V_{ext} + \frac{R2 // R_{in}}{R_x + R2 // R_{in}} V_x \right)$$

where $V_x = 3V$, $R_x = 5850\Omega$. $R_{in} = 150\Omega$ (R_{in} of pin 2) and V_{ext} is the external voltage applied to the divider.

Fig. 2 - Application circuit showing all the optional components. In particular it illustrates how the holding current level is adjusted independently of the peak current (with $R1$, $R2$, V_{ext}) and how the internal zener clamp is connected. This circuit produces the waveforms shown in Fig. 3.



The drive currents for the two darlingtonts and the waveform time constants are all defined by a reference current, I_{ref} , which is defined in turn by a resistor between pin 9 and ground. The recommended value for I_{ref} is 1 mA which is obtained with a 1.2 kΩ resistor. From I_{ref} the darlington drive currents are given by:

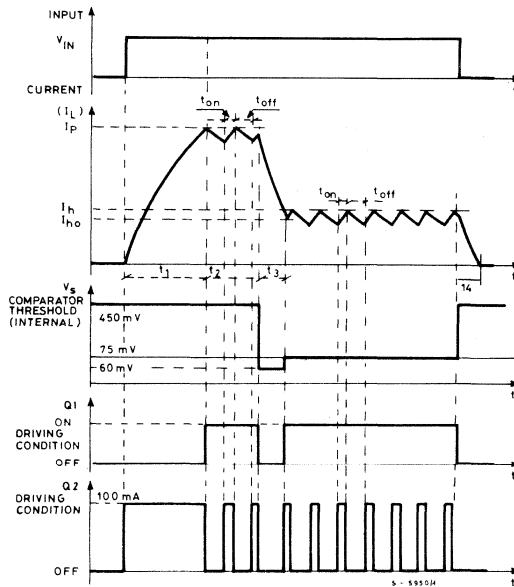
PNP : $I = 35 I_{ref}$

NPN : $I = 100 I_{ref}$

The duration of the high current level (t_2 in figure 3) is set by a capacitor connected between pin 6 and ground. This capacitor, $C1$, is related to the duration, T , by:

$$C1 = \frac{I_{ref} T}{12}$$

Fig. 3 - Waveforms of the typical application circuit of fig. 2.



The discharge time constant (t_{off} in figure 3) is set by a capacitor between pin 7 and ground and is found from:

$$t_{off} = \frac{12C2}{I_{ref}}$$

The t_{off} and t_{on} times are also related to the current ripple, ΔI :

$$t_{off} = \frac{L \Delta I}{V_{off}} \quad \text{and} \quad t_{on} = \frac{L \Delta I}{V_{on}}$$

where

$$\begin{aligned} V_{off} &= V_{diode} + V_{CEQ1} + R_L I_L \\ V_{on} &= V_s - V_{CEQ2} - V_{RS} - R_L I_L \\ L &= \text{load inductance} \\ R_L &= \text{load resistance} \\ \Delta I &= \text{load current ripple.} \end{aligned}$$

Note that t_{off} is the same for both the peak and holding currents.

Fig. 4 – When pin 6 in grounded, as shown here, the load current is regulated at a single level.

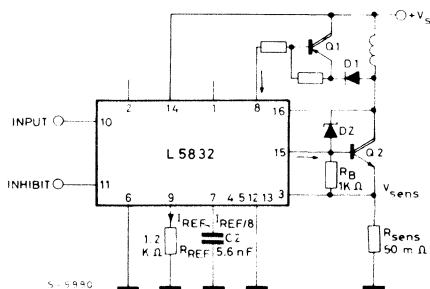
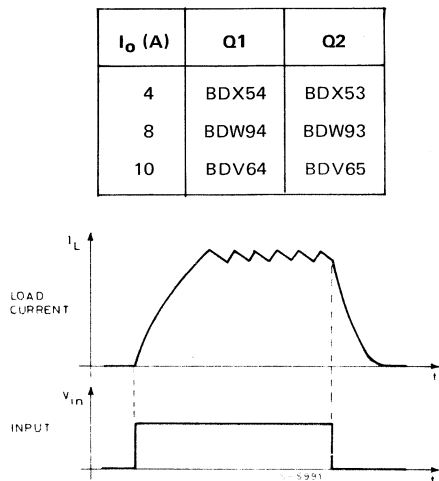


Fig. 5 – In this application circuit, pin 6 is left open to give a single peak followed by a regulated holding current.

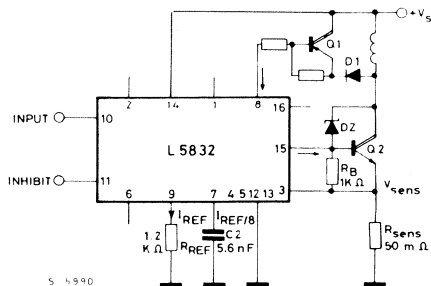
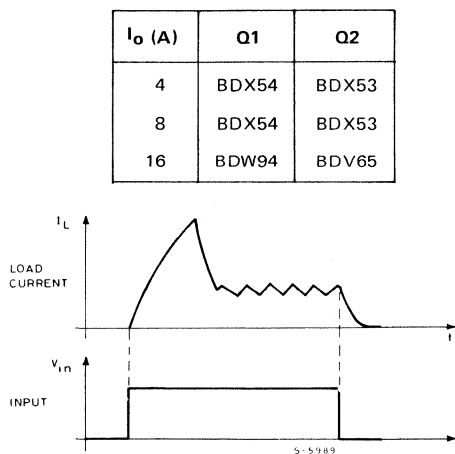
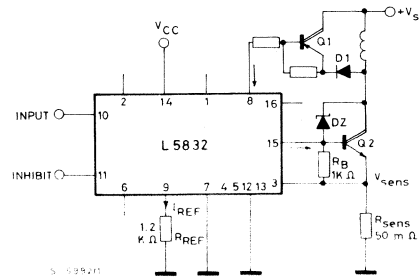
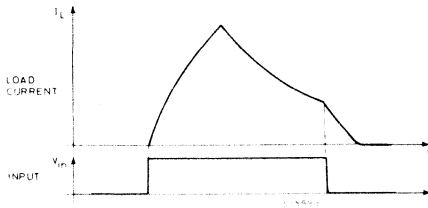


Fig. 6 – Switchmode control of the current can be suppressed entirely by leaving pin 6 open and grounding pin 7. The peak current is still controlled.

I_o (A)	Q1	Q2
4	BDX54	BDX53
8	BDW94	BDW93
10	BDV64	BDV65



For fast turnoff an internal zener clamp is available on pin 16.

This is used with an external divider, R8 R9, as shown in figure 2. Suitable values can be found from:

$$V_{\text{pin } 16} \cong 15V + V_{BEQ2} + VR_{\text{sense}}$$

$$V_{CQ2} \cong V_{\text{pin } 16} \cdot \frac{R9 + R8}{R8}$$

(V_{CQ2} is the voltage at the collector of Q2).

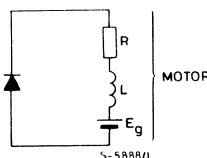
To ensure stability, a small capacitor (about 200 pF) must be connected between the base and collector of Q2 when pin 16 is used.

For the application circuit of figure 7 $t_{\text{off}} = 12C2/I_{\text{ref}}$, as before, and the current ripple is given by:

$$t_{\text{off}} = - \frac{L}{R} \frac{\ln(I_{LP} - \Delta I) \cdot R_L + V_L}{I_{LP} \cdot R_L + V_L}$$

where V_L is the voltage across the inductor during recirculation.

Note that if the load is a motor $V_L = E_g + V_D$.



Normally ΔI is a design parameter therefore C2 can be calculated directly from:

$$C2 = \frac{-I_{ref} \cdot L}{12R_L} \cdot \frac{\ln(I_{LP} - \Delta I) R_L + V_L}{I_{LP} \cdot R_L + V_L}$$

This application is particularly important because it allows the use of inductive loads with the lowest possible series resistance (compatible with constructional requirements) and therefore reduces notably the power dissipation.

For example, an electric valve driven from 24V which draws 2A has a series resistance of 12Ω and dissipates 48W. Using this circuit a valve with a 2Ω series resistance can be used and the power dissipation is:

$$P_d = R_L I_L^2 + V_D I_L (1 - \delta) + V_{\text{sat}} \cdot I_L \cdot \delta + R_S I_L^2 \delta$$

where R_L = resistance of valve = 2Ω
 V_D = drop across diode, $V_D \cong 1V$
 V_{sat} = saturation voltage of Q2, $\cong 1V$
 R_S = $11 = 220\text{ m}\Omega$
 δ = duty cycle = 20%

therefore:

$$P_d = 8 + 1.6 + 0.4 + 0.16 = 10.16W$$

This given two advantages: the size (and cost) of the valve is reduced and the drive current is reduced from 2A to about 0.4A.

The same consideration is also true for DC motors.

Fig. 7 – Application circuit using only one darlington. The resistor and zener shown dotted activate the load when power is applied.

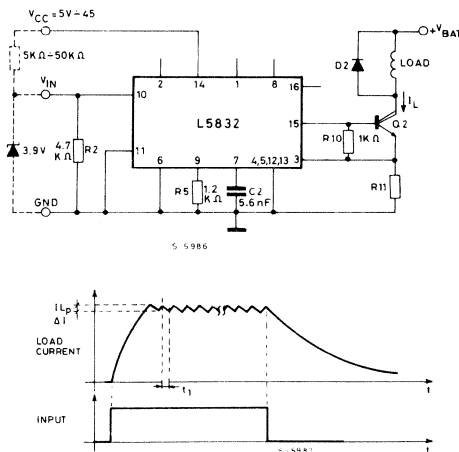


Fig. 8 – P.C. board and component layout of the circuit of fig. 7 (1:1 scale)

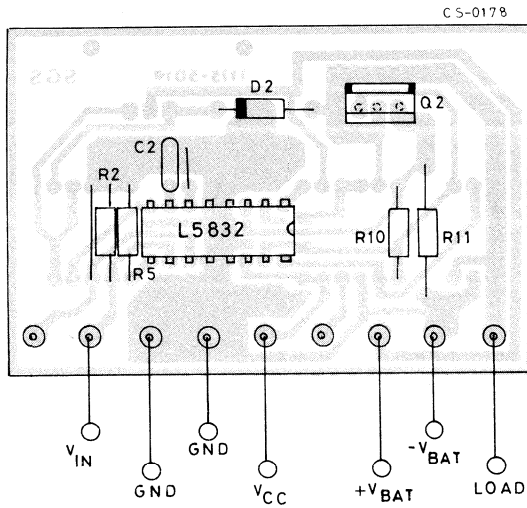
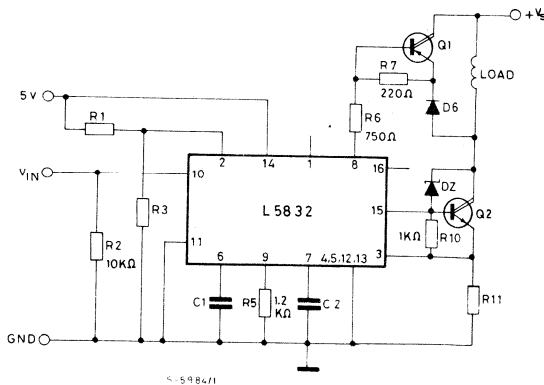


Fig. 9 – Application circuit showing how two separate supplies can be used.





The application circuit of figure 9 is very similar to figure 2 except that it shows the use of two supplies — one for the control circuit, one for the power stage.

Choose R6 so that the voltage on pin 8 does not exceed 46V DC. This can be done simply bearing in mind that the pin 8 current is $35 I_{ref}$.

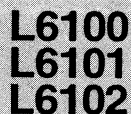
R6 must not be too high if a very low supply voltage is used because:

$$V_{smin} = R6 \cdot I6 + 4.75$$

therefore

$$V_{smin} = 750 \cdot 35 \cdot 10^{-3} + 4.75 = 31V$$

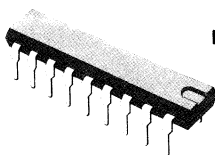
The zener diode DZ can not exceed 62V because when Q1 is off and DZ triggered — the fast recirculation — the voltage on pin 8 may not exceed 60V.



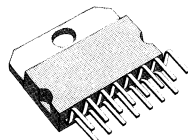
100V-1A, QUAD DMOS POWER SWITCH

The device is assembled in three package: 12+3+3 lead powerdip; 11-lead Multiwatt® and 15-lead Multiwatt®.

Powerdip 12 + 3 + 3
L6100

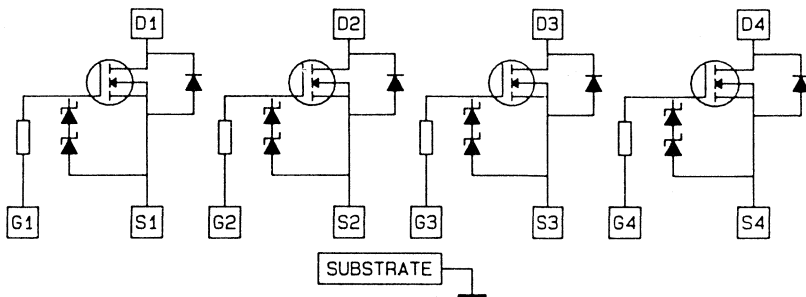


Multiwatt-11
L6101



Multiwatt-15
L6102

V_{DS}	Drain-source voltage	100	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 14K\Omega$)	100	V
V_{GS}	Gate-source voltage	+14 to -0.6	V
I_D	Drain current		
	— DC operation	1	A
	— Pulsed (300 μ s, 1% duty cycle)	2.5	A
T_{stg}, T_j	Storage and junction temperature range	-40 to +150	$^{\circ}$ C



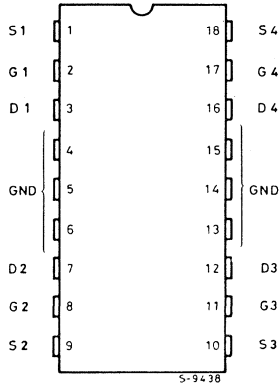


L6100
L6101
L6102

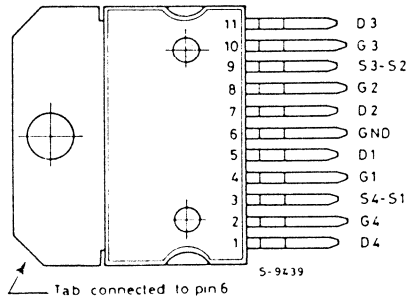
CONNECTION DIAGRAMS

(Top view)

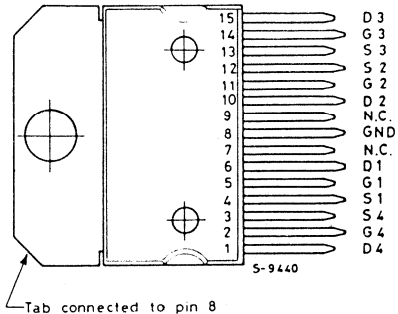
L6100
(Powerdip)



L6101
(Multiwatt-11)



L6102
(Multiwatt-15)



THERMAL DATA

			Powerdip	Multiwatt-11	Multiwatt-15
$R_{th j-amb}$	Thermal resistance junction-ambient	max	65°C/W	35°C/W	35°C/W
$R_{th j-case}$	Thermal resistance junction-case	max	11°C/W	3°C/W	3°C/W

ELECTRICAL CHARACTERISTICS ($T_{\text{case}} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-source breakdown voltage	@ $I_{\text{D}} = 1\text{mA}$ $V_{\text{GS}} = 0\text{V}$	100		V
$V_{\text{GS}}(\text{TH})$	Threshold voltage	@ $I_{\text{D}} = 1\text{mA}$ $V_{\text{GS}} = V_{\text{DS}}$	2	4	V
I_{GSS}	Gate-source leakage	@ $V_{\text{GSS}} = 10\text{V}$		1	μA
$R_{\text{DS}}(\text{ON})$	Static drain-source on-state resistance	@ $V_{\text{GS}} = 10\text{V}$ $I_{\text{D}} = 1\text{A}$		1.2	Ω

Fig. 1 – Saturation characteristics

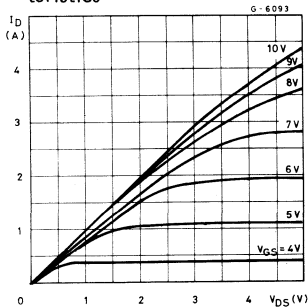


Fig. 2 – Normalized ON-resistance vs. temperature

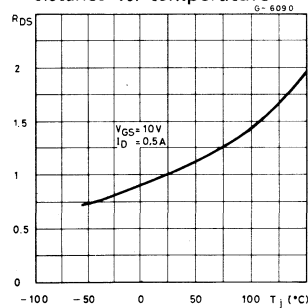


Fig. 3 – Transconductance vs. drain current

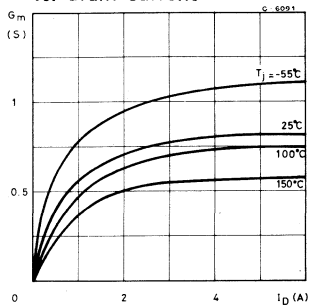
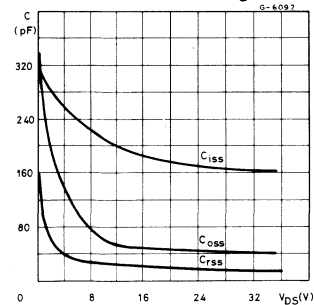


Fig. 4 – Capacitance vs. drain to source voltage





L6202

ADVANCE DATA

1.5A DMOS FULL BRIDGE DRIVER

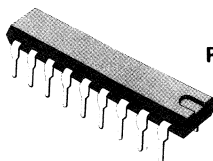
- POWER SUPPLY VOLTAGE UP TO 52V
- TOTAL DC CURRENT UP TO 1.5A
- LOW SATURATION VOLTAGE
- LOW POWER DISSIPATION
- NO CROSS CONDUCTION
- TTL COMPATIBLE INPUTS
- OVERTEMPERATURE PROTECTION

Realized with mixed bipolar/CMOS/DMOS technology, the L6202 is a full bridge driver for motor control applications. Delivering up to 1.5A output current at motor supply voltages up to 52V, the device uses DMOS output transistors to obtain very high efficiency and fast switching speed.

Each channel (half-bridge) of the device is controlled by a separate logic input, while a common enable input controls both channels. All inputs are TTL, CMOS and μ C-compatible.

The L6202 is assembled in a Powerdip 12+3+3 package an 18-lead DIP using the six center pins to conduct heat to the PCB. Thanks to the very high efficiency of the DMOS output stage no external heatsink is necessary, even when operating at the full rated current and voltage.

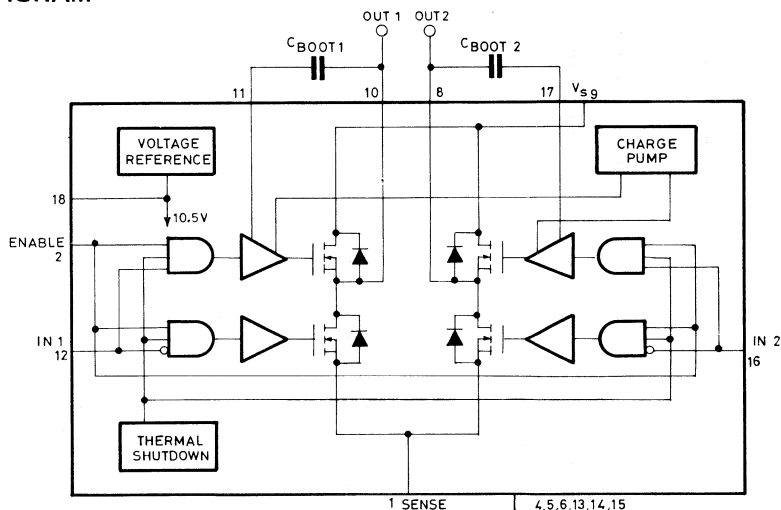
MultiPower BCD Technology



Powerdip 12 + 3 + 3

ORDERING NUMBER: L6202

BLOCK DIAGRAM



S-9392

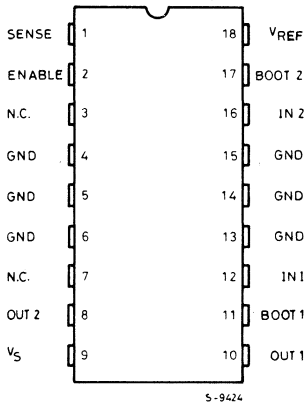
Note: suggested value for $C_{BOOT1,2}$: 10nF

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_S	Power supply	60	V
V_{IN}, V_{EN}	Input or enable voltage	-0.3 to 7	V
I_O	Peak output current		
	— non repetitive	5	A
	— DC operation	1.5	A
V_{sens}	Sensing voltage	-1 to 4	V
P_{tot}	Total power dissipation ($T_{case} = 75^{\circ}C$)	6	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^{\circ}C$

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j-pins}$	Thermal resistance junction-pins	max	12	$^{\circ}C/W$
$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	65	$^{\circ}C/W$

**PIN FUNCTIONS**

N°	NAME	FUNCTION
1	SENSE	A resistance R_{sense} , connected to this pin, allows motor current control.
2	ENABLE	Enable Input. A logic low level on this pin switches off the DMOS POWER transistors.
3	NOT CONNECTED	
4	GROUND	Common ground terminal.
5	GROUND	Common ground terminal.
6	GROUND	Common ground terminal.
7	NOT CONNECTED	
8	OUT 2	Output of the half bridge.
9	V_S	Supply voltage.
10	OUT 1	Output of the half bridge.
11	BOOT 1	A capacitor $C_{\text{BOOT 1}}$, connected to this terminal allows the upper DMOS transistor driving for high switching frequencies.
12	IN 1	Input from the controller device.
13	GND	Common ground terminal.
14	GND	Common ground terminal
15	GND	Common ground terminal.
16	IN 2	Input from the controller device.
17	BOOT 2	A capacitor $C_{\text{BOOT 2}}$, connected to this terminal, allow the upper DMOS transistor driving for high switching frequencies.
18	V_{ref}	Internal reference voltage.

ELECTRICAL CHARACTERISTICS ($V_S = 42V$, $T_J = 25^\circ C$)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S Supply voltage	Operating condition	12 (*)		52	V
V_{ref} Reference voltage			10.5		V
I_S Quiescent supply current	$V_{EN} = H$ $V_{IN} = L$		7		mA
	$I_L = 0$ $V_{IN} = H$		7		
	$V_{EN} = L$		6		
V_{INL} Input low voltage		-0.3		0.8	V
V_{INH} Input high voltage		2		7	V
V_{INL} Input low current				-10	μA
I_{INH} Input high current			30		μA
V_{ENL} Enable low voltage		-0.3		0.8	V
V_{ENH} Enable high voltage		2		7	V
I_{ENL} Enable low current				-10	μA
I_{ENH} Enable high current			30		μA
$R_{DS(ON)}$			0.3		Ω
$V_{DS(sat)}$ Saturation voltage	$I_L = 1A$		0.3		V
	$I_L = 1.2A$		0.45		
$t_1 (V_i)$ Source current turn-off delay			300		ns
$t_2 (V_i)$ Source current fall time			200		ns
$t_3 (V_i)$ Source current turn-on delay			400		ns
$t_4 (V_i)$ Source current rise time			200		ns
$t_5 (V_i)$ Sink current turn-off delay			300		ns
$t_6 (V_i)$ Sink current fall time			200		ns
$t_7 (V_i)$ Sink current turn-on delay			400		ns
$t_8 (V_i)$ Sink current rise time			200		ns
F_C Commutation frequency	$I_L = 1.2A$		50	100	KHz

 (*) If $V_S < 12V$, $V_{ref} = V_S - 2V_{BE}$

CIRCUIT OPERATION

The L6202 is a monolithic full bridge switching motor driver realized in the new Multipower-BCD technology which allows the integration of multiple, isolated DMOS power transistors plus mixed CMOS/bipolar control circuits.

The power stage of the L6202 consists of four N-channel DMOS transistors with an $R_{DS(ON)} \cong 0.3\Omega$ over whole current range. Each transistor has an intrinsic drain-source diode. During recirculation the behaviour of these diodes depends on the operating mode.

When one of the POWER DMOS transistor is ON it behaves almost symmetrically in terms of current - like, in fact, a resistor with the value $R_{DS(ON)}$ in parallel with the drain-source diode.

During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS(ON)} \times I_L$ for voltages less than 0.7V and is clamped at a voltage depending on the characteristics of the diode for greater voltages.

When the ENABLE input is low, the POWER MOS is OFF and the diode carry the whole recirculation.

Although the device guarantees the absence of cross-conduction, the presence of the intrinsic diodes in the POWER DMOS structure causes the generation of current spikes on the sensing terminals due to charge-discharge phenomena in the capacitors C1 & C2 associated with the drain source junctions (Fig. 1). When the output switches from high to low a current spike is generated associated with the capacitor C1. On the low-to-high transition a spike of the same polarity is generated by C2, preceded by a spike of the opposite polarity due to the charging of the input capacity of the lower POWER DMOS transistor. (Fig. 2)

To ensure that the POWER DMOS transistors are driven correctly a gate-source voltage of about 10V must be guaranteed for all of the N-channel DMOS transistors. While there is no problem in driving the lower POWER DMOS devices (their source terminals are referred to ground) it is necessary to provide a gate voltage higher than the positive supply for the upper transistors because they have the drain connected to the supply itself.

This obtained by a system that combines a charge pump circuit, which assures correct DC operation, with a bootstrapping technique suitable for high switching frequencies.

In the bootstrap circuit the external C_B capacitors are charged to a voltage of about 10V when the upper power transistor is OFF and the lower one is ON. To guarantee efficient driving of the upper power transistor in the conduction condition the value of C_B must be greater than the value of the input capacitance, C_{IN} , of the power transistor itself. Since the estimated value of the input capacity is about 1nF, C_B should be $\geq 10nF$ to guarantee correct operation.

An ON-OFF synchronisation circuit provides a dead time (the period in which all four power transistors are OFF) of 40ns, sufficient to prevent simultaneous conduction with obvious advantages in terms of power dissipation and of spurious signals on the ground and in the sensing resistors.

A thermal protection circuit has been included that will disable the device if the junction temperature reaches 150°C. When the temperature has fallen to a safe value the device restarts under the control of the input and enable signals.

Fig. 1 - Intrinsic structures in the POWER DMOS transistors

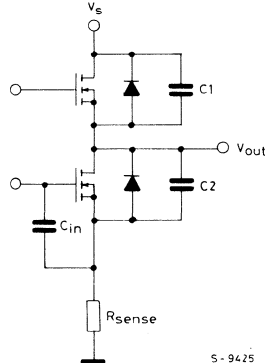


Fig. 2 - Current typical spikes on the sensing pin

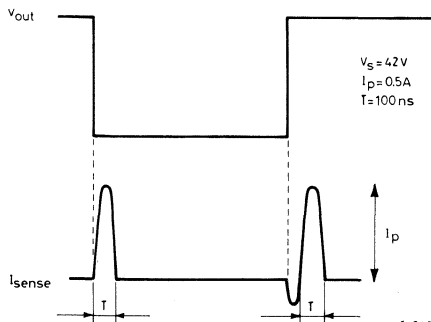
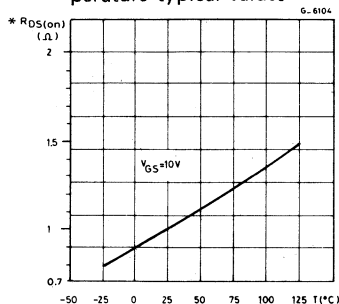
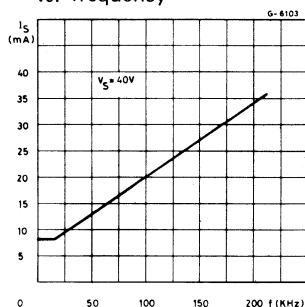


Fig. 3 - $R_{DS(ON)}$ vs. temperature typical values



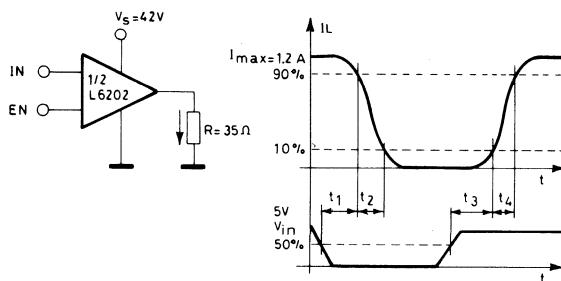
* Normalized at 25°C

Fig. 4 - Quiescent current vs. frequency



SWITCHING TIMES TEST CIRCUITS

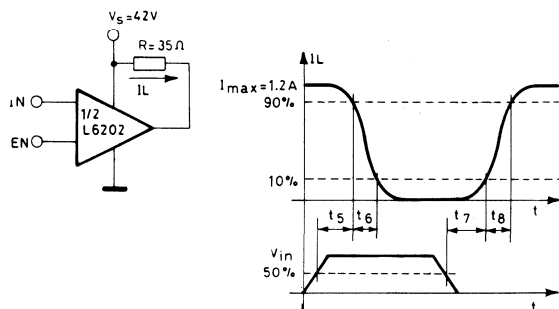
Fig. 5 - Source current delay times vs. input or enable chopper



NOTE: for INPUT chopper SET EN = H

S-9430

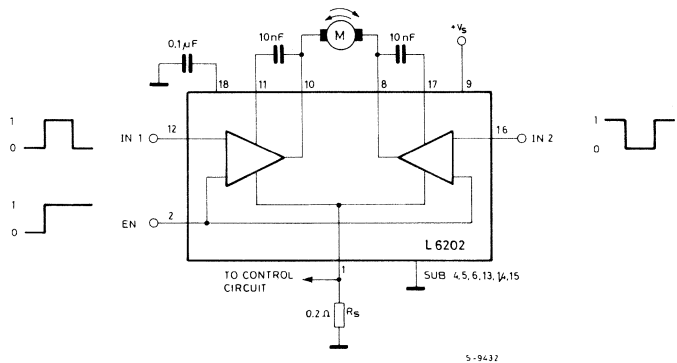
Fig. 6 - Sink current delay times vs. input or enable chopper



NOTE: for INPUT chopper SET EN = H

S-9431

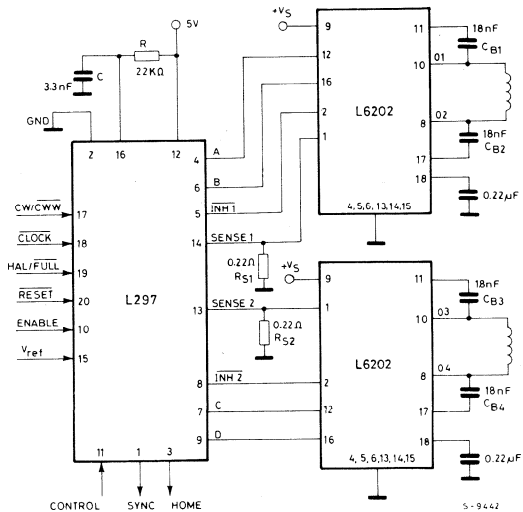
Fig. 7 - Bidirectional DC motor control



	INPUTS	FUNCTION
$V_{EN} = H$	IN1 = H IN2 = L	Turn right
	IN1 = L IN2 = H	Turn left
	IN1 = IN2	Fast motor stop
$V_{EN} = L$	IN1 = X IN1 = IN2	Free running motor stop

L = Low H = High X = Don't care

Fig. 8 - Application circuit





L6203

ADVANCE DATA

3A DMOS FULL BRIDGE DRIVER

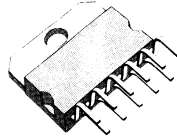
- OPERATING SUPPLY VOLTAGE UP TO 52V
- TOTAL DC CURRENT UP TO 3A
- LOW SATURATION VOLTAGE
- LOW POWER DISSIPATION
- NO CROSS CONDUCTION
- TTL COMPATIBLE INPUTS
- OVER TEMPERATURE PROTECTION

Realized with mixed bipolar/CMOS/DMOS technology, the L6203 is a full bridge driver for motor control applications. Delivering up to 3A output current at motor supply voltages up to 52V, the device uses DMOS output transistors to obtain very high efficiency and fast switching speed.

Each channel (half-bridge) of the device is controlled by a separate logic input, while a common enable input controls both channels. All inputs are TTL, CMOS and μ C-compatible.

The L6203 is assembled in a 11-lead Multiwatt[®] package.

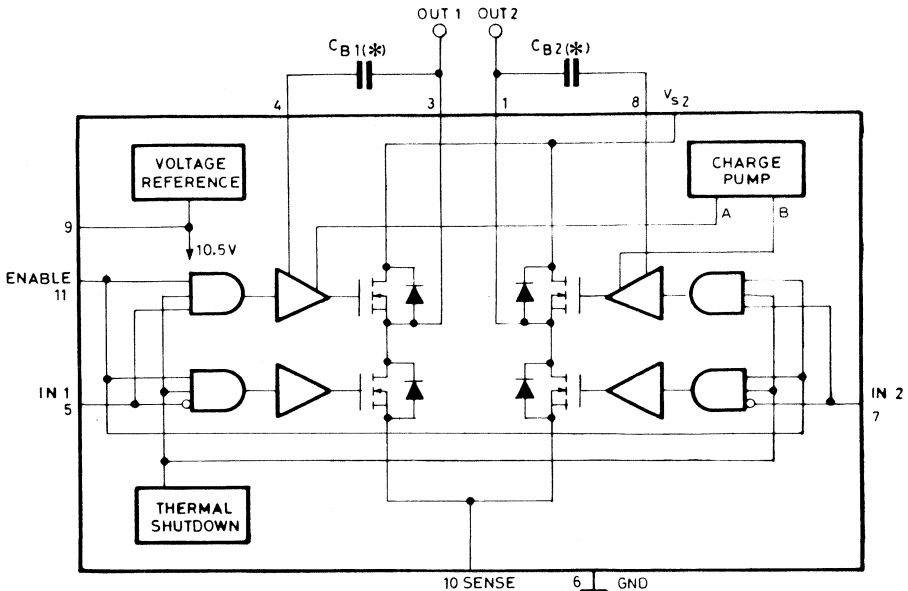
MultiPower BCD Technology



Multiwatt-11

ORDERING NUMBER: L6203

BLOCK DIAGRAM



S-9520

(*) Suggested value for C_{BOOT1} and C_{BOOT2} : 10nF

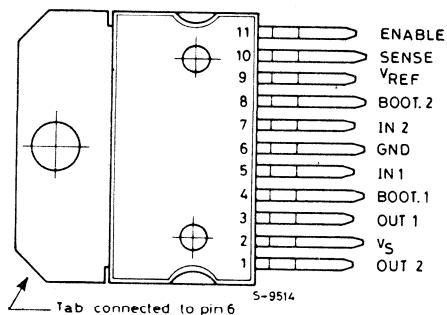
This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_s	Power supply	60	V
V_{IN}, V_{EN}	Input or enable voltage	-0.3 to 7	V
I_o	Output current		
	— peak non repetitive	5	A
	— DC operation	3	A
V_{sens}	Sensing voltage	-1 to 4	V
P_{tot}	Total power dissipation ($T_{case} = 75^\circ\text{C}$)	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

CONNECTION DIAGRAM

(Top view)



THERMAL DATA

$R_{th\ J-case}$	Thermal resistance junction-case	max	3	$^\circ\text{C/W}$
$R_{th\ J-amb}$	Thermal resistance junction-ambient	max	35	$^\circ\text{C/W}$



PIN FUNCTIONS

N°	NAME	FUNCTION
1	OUT 2	Output of the half bridge.
2	V_S	Supply voltage.
3	OUT 1	Output of the half bridge.
4	BOOT. 1	A capacitor C_{B1} , connected to this terminal allows the upper DMOS transistor driving for high switching frequencies.
5	IN 1	Input from the controller device.
6	GND	Common ground terminal.
7	IN 2	Input from the controller device.
8	BOOT. 2	A capacitor C_{B2} , connected to this terminal allows the upper DMOS transistor driving for high switching frequencies.
9	V_{REF}	Internal reference voltage.
10	SENSE	A resistance R_{SENSE} , connected to this terminal, allows motor current control.
11	ENABLE	Enable input. A logic low level on this pin switches off the DMOS power transistors.

ELECTRICAL CHARACTERISTICS ($V_S = 42V$, $T_J = 25^\circ C$)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S Supply voltage	Operating condition	12 (*)		52	V
V_{ref} Reference voltage			10.5		V
I_S Quiescent supply current	$V_{EN} = H$ $V_{IN} = L$		7		mA
	$I_L = 0$ $V_{IN} = H$		7		
	$V_{EN} = L$		6		
V_{INL} Input low voltage		-0.3		0.8	V
V_{INH} Input high voltage		2		7	V
V_{INL} Input low current				-10	μA
I_{INH} Input high current			30		μA
V_{ENL} Enable low voltage		-0.3		0.8	V
V_{ENH} Enable high voltage		2		7	V
I_{ENL} Enable low current				-10	μA
I_{ENH} Enable high current			30		μA
$R_{DS(ON)}$			0.3		Ω
$V_{DS(sat)}$ Saturation voltage	$I_L = 1A$		0.3		V
	$I_L = 3A$		0.9		
$t_1 (V_i)$ Source current turn-off delay			300		ns
$t_2 (V_i)$ Source current fall time			200		ns
$t_3 (V_i)$ Source current turn-on delay			400		ns
$t_4 (V_i)$ Source current rise time			200		ns
$t_5 (V_i)$ Sink current turn-off delay			300		ns
$t_6 (V_i)$ Sink current fall time			200		ns
$t_7 (V_i)$ Sink current turn-on delay			400		ns
$t_8 (V_i)$ Sink current rise time			200		ns
F_C Commutation frequency	$I_L = 3A$		50	100	KHz

 (*) If $V_S < 12V$, $V_{ref} = V_S - 2V_{BE}$

CIRCUIT OPERATION

The L6203 is a monolithic full bridge switching motor driver realized in the new Multipower-BCD technology which allows the integration of multiple, isolated DMOS power transistors plus mixed CMOS/bipolar control circuits.

The power stage of the L6203 consists of four N-channel DMOS transistors with an $R_{DS(ON)} \cong 0.3\Omega$ over the whole current range. Each transistor has an intrinsic drain source diode. During recirculation the behaviour of these diodes depends on the operating mode.

When one of the POWER DMOS transistors is ON it behaves almost symmetrically in terms of current like, in fact, a resistor with the value $R_{DS(ON)}$ in parallel with the drain-source diode.

During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS(ON)} \times I_L$ for voltages less than 0.7V and is clamped at a voltage depending on the characteristics of the diode for greater voltages.

When the enable input is low, the POWER MOS is off and the diode carry the whole recirculation.

Although the device guarantees the absence of cross-conduction, the presence of the intrinsic diodes in the POWER MOS structure causes the generation of current spikes on the sensing pin due to charge-discharge phenomena in the reverse capacitor, C1 & C2 associated with the drain-source junctions (Fig. 1). When the output switches from high to low, a current spike is generated associated with the capacitor C1. On the low-to-high transition, a spike of the same polarity is generated by C2, preceded by a spike of the opposite polarity due to the charging of the input capacity of the lower POWER DMOS transistor (Fig. 2).

To ensure that the POWER DMOS transistors are driven correctly a gate-source voltage of about 10V must be guaranteed for all of the N-channel DMOS transistors. While there is no problem in driving the lower POWER DMOS devices (their source terminals are referred to ground) it is necessary to provide a gate voltage higher than the positive supply for the upper transistors because they have the drain connected to the supply itself.

This is obtained by a system that combines a charge pump circuit, which assures correct DC operation, with a bootstrapping technique suitable for high switching frequencies.

In the bootstrap circuit the external C_B capacitors are charged to a voltage of about 10V when the upper power transistor is OFF and the

lower one is ON. To guarantee efficient driving of the upper power transistor in the conduction condition, the value of C_B must be greater than the value of the input capacitance, C_{IN} , of the power transistor itself. Since the estimated value of the input capacity is about 1nF, C_B should be $> 10nF$ to guarantee correct operation.

An ON-OFF synchronization circuit provides a dead time (the period in which all four power transistors are OFF) of 40ns, sufficient to prevent simultaneous conduction with obvious advantages in terms of power dissipation and of spurious signals on the ground and in the sensing resistors.

A thermal protection circuit has been included that will disable the device if the junction temperature reaches 150°C. When the temperature has fallen to a safe value the device restarts under the control of the input and enable signals.

Fig. 1 - Intrinsic structures in the POWER DMOS transistors

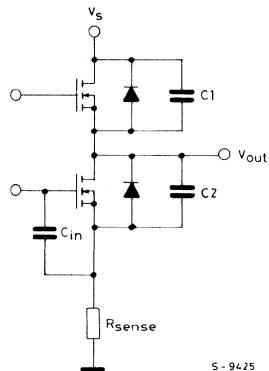


Fig. 2 - Typical current spikes on the sensing pin

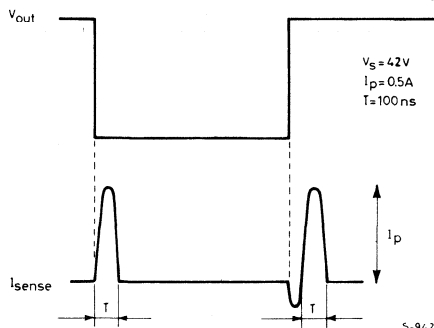
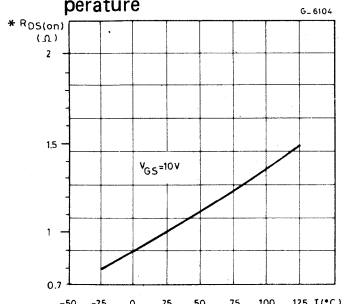
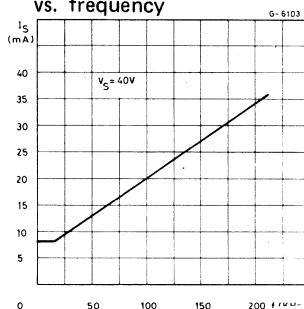


Fig. 3 - $R_{DS(ON)}$ vs. temperature



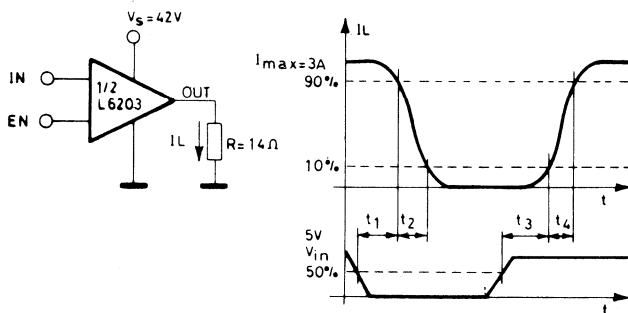
* Normalized at 25°C

Fig. 4 - Quiescent current vs. frequency



SWITCHING TIMES TEST CIRCUITS

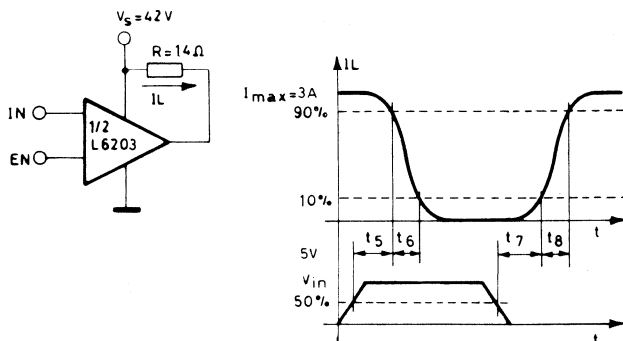
Fig. 5 - Source current delay time vs. input or enable chopper



NOTE: for INPUT chopper SET EN = H

S-9522

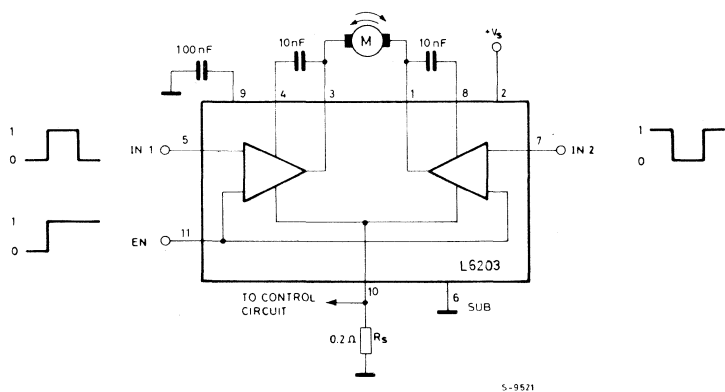
Fig. 6 - Sink current delay time vs. input or enable chopper



NOTE: for INPUT chopper SET EN = H

S-9523

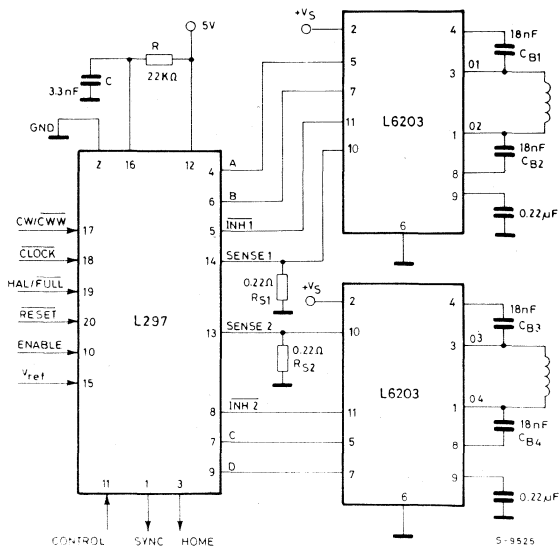
Fig. 7 – Bidirectionale DC motor control



INPUTS			FUNCTION
$V_{EN} = H$	IN1 = H	IN2 = L	Turn right
	IN1 = L	IN2 = H	Turn left
	IN1 = IN2		Fast motor stop
$V_{EN} = L$	IN1 = X	IN1 = IN2	Free running motor stop

L = Low H = High X = Don't care

Fig. 8 – Application circuit





L6207

ADVANCE DATA

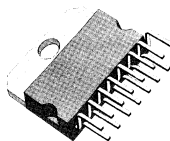
DUAL FULL BRIDGE DRIVER

- POWER SUPPLY VOLTAGE UP TO 46V
- LOW SATURATION VOLTAGE
- OVERTEMPERATURE PROTECTION
- LOGIC "0" INPUT VOLTAGE UP TO 1.5V (HIGH NOISE IMMUNITY)

The L6207 is an integrated monolithic circuit in a 15-lead multiwatt package. It is a high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive load such as relays, solenoids, DC and stepper motors.

Two inhibit inputs are provided to disable the device independently of the input signals. The

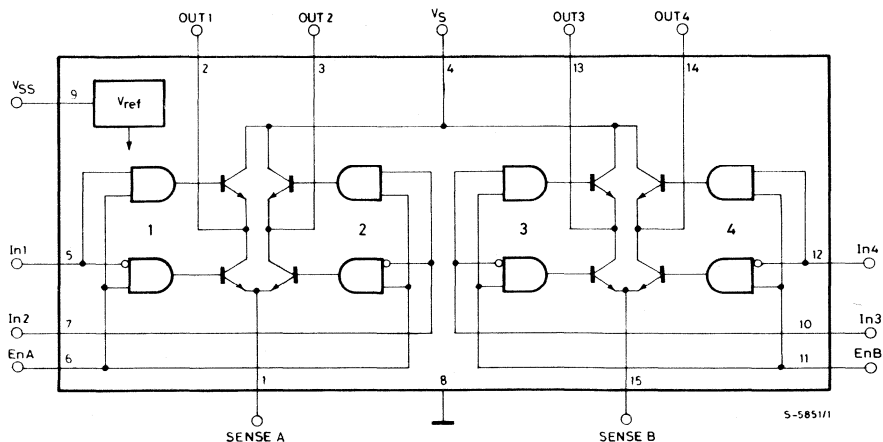
emitters of the lower transistors of each bridge are connected together and the corresponding external terminal can be used for the connection of an external sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.



Multiwatt 15

ORDERING NUMBER: L6207

BLOCK DIAGRAM





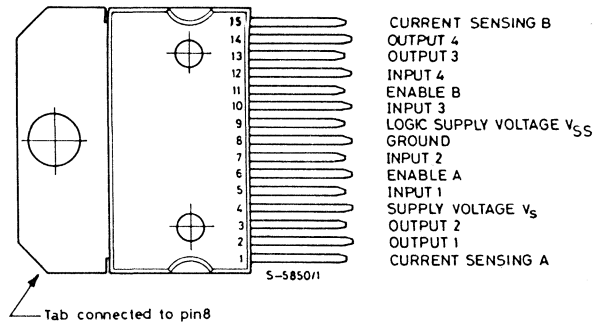
L6207

ABSOLUTE MAXIMUM RATINGS

V_s	Power supply	50	V
V_{ss}	Logic supply voltage	7	V
V_i, V_{EN}	Input and enablet voltage	0.3 to 7	V
I_o	Peak output current (each channel)		
	– non repetitive ($t = 100\mu s$)	1.8	A
	– repetitive (80% on 20% off; $t_{on} = 10ms$)	1.5	A
	– DC operation	1.25	A
V_{sens}	Sensing voltage	-1 to 2.3	V
P_{tot}	Total power dissipation ($T_{case} = 75^\circ C$)	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^\circ C$

CONNECTION DIAGRAM

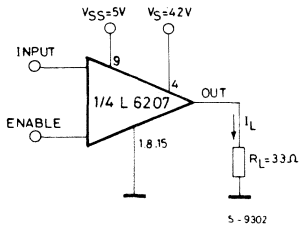
(Top view)



THERMAL DATA

$R_{th j-case}$	Thermal resistance junction-case	max	3	$^\circ C/W$
$R_{th j-amb}$	Thermal resistance junction-ambient	max	35	$^\circ C/W$

Fig. 1 - Switching times test circuit



note: For INPUT chopper, set EN = H

Fig. 1a - Source current delay times vs. input chopper

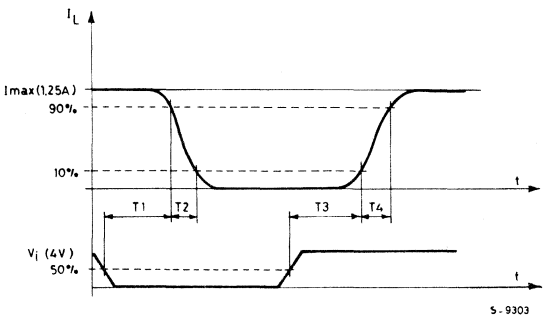
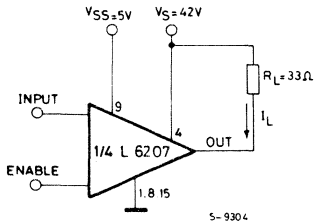
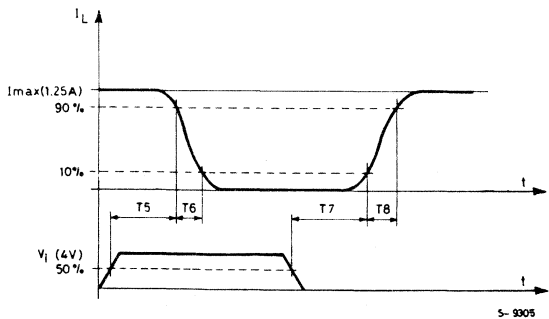


Fig. 2 - Switching time test circuits



note: For INPUT chopper, set EN = H

Fig. 2a - Sink current delay times vs. input chopper



ELECTRICAL CHARACTERISTICS (For each channel, $V_s = 42V$, $V_{ss} = 5V$, $T_j = 25^\circ C$)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s Supply voltage (pin 4) •	Operative condition	$V_{IH}+2.5$		46	V
V_{ss} Logic supply voltage (pin 9) •		4.5		7	V
I_s Quiescent supply current (pin 4) (1)	$V_{EN} = H$ $I_L = 0$ $V_i = L$		3	7	mA
	$V_i = H$		15	20	mA
	$V_{EN} = L$			1	mA
I_{ss} Quiescent current from V_{ss} (pin 9) (1)	$V_{EN} = H$ $I_L = 0$ $V_i = L$		5	10	mA
	$V_i = H$		1.5	3	mA
	$V_{EN} = L$		1	1.5	mA
V_{iL} Input low voltage (pins 5, 7, 10, 12)		-0.3		1.5	V
V_{iH} Input high voltage (pins 5, 7, 10, 12)		2.3		V_{ss}	V
I_{iL} Low voltage input current (pins 5, 7, 10, 12)	$V_i = L$			-10	μA
I_{iH} High voltage input current (pins 5, 7, 10, 12)	$V_i = H \leq V_{ss} - 0.6V$		30	100	μA
V_{ENL} Enable low voltage (pins 6, 11)		-0.3		1.5	V
V_{ENH} Enable High voltage (pins 6, 11)		2.3		V_{ss}	V
I_{ENL} Low voltage enable current (pins 6, 11)	$V_{EN} = L$			-10	μA
I_{ENH} High voltage enable current (pins, 6, 11)	$V_{EN} = H < V_{ss} - 0.6V$		30	100	μA
$V_{CE(sat)H}$ Source saturation voltage	$I_L = 1.25A$		1.5	2.3	V
$V_{CE(sat)L}$ Sink saturation voltage	$I_L = 1.25A$		1.5	2.3	V
$V_{CE(sat)}$ Total drip	$I_L = 1.25A$			4.4	V
V_{sens} Sensing voltage (pins 1, 15)		-1 (*)		2	V
T1 (V_i) Source current turn off delay	$0.5 V_i$ to $0.9 I_L$ (**)		1.7		μs
T2 (V_i) Source current fall time	$0.9 I_L$ to $0.1 I_L$ (**)		0.2		μs
T3 (V_i) Source current turn on delay	$0.5 V_i$ to $0.1 I_L$ (**)		2.5		μs
T4 (V_i) Dource current rise time	$0.1 I_L$ to $0.9 I_L$ (**)		0.35		μs

ELECTRICAL CHARACTERISTICS (continued)

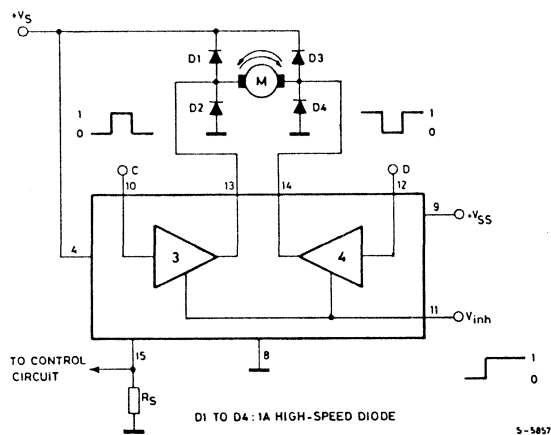
Parameter		Test Conditions	Min.	Typ.	Max.	Unit
T5 (V _I)	Sink current turn-off delay	0.5 V _I to 0.9 I _L (***)		0.7		μs
T6 (V _I)	Sink current fall time	0.9 I _L to 0.1 I _L (***)		0.2		μs
T7 (V _I)	Sink current turn on delay	0.5 V _I to 0.1 I _L (***)		1.5		μs
T8 (V _I)	Sink current rise time	0.1 I _L to 0.9 I _L (***)		0.2		μs
f _C	Commutation frequency	I _L = 1.25A		25	40	KHz

(*) Sensing voltage can be -1V for $t < 50\mu s$; in steady state $V_{sens\ min} > -0.5V$; (**) See fig. 1a; (***) See fig. 2a

(1) The value of the current is related to only one channel

- The correct sequence for power on is:
 1. V_{SS} ON with $EN = L$
 2. V_S ON
 3. $EN = H$

Fig. 3 - Bidirectional DC motor control



TRUTH TABLE

	INPUTS	FUNCTION
$V_{EN} = H$	$C = H \quad D = L$	Turn right
	$C = L \quad D = H$	Turn left
	$C = D$	Fast motor stop
$V_{EN} = L$	$C = X \quad D = X$	Free running motor stop

L = Low H = High X = Don't care

Fig. 4 - Two phase bipolar stepper motor control circuit

This circuit drives bipolar stepper motors with winding currents up to 1.25A. The diodes are fast 1A types.

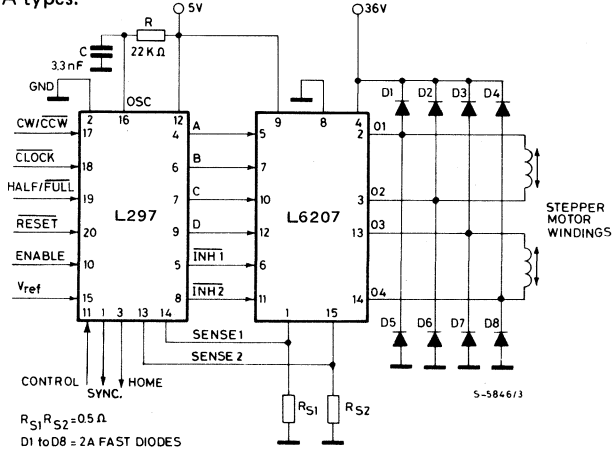
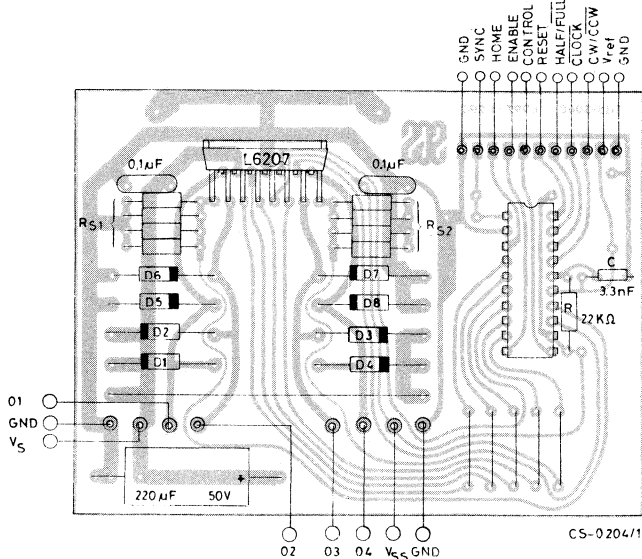


Fig. 5 - Suggested printed circuit board layout for the circuit of fig. 4 (1.1 scale)





L6209

ADVANCE DATA

3A FULL BRIDGE DRIVER WITH DIODES

- SUPPLY VOLTAGE UP TO 46V
- OUTPUT CURRENT UP TO 3A (4A PEAK)
- SEPARATE CONNECTIONS FOR SUPPLIES AND DIODES
- CONNECTION FOR EXTERNAL SENSE RESISTOR
- LOW SATURATION VOLTAGE (3.5V TYP AT 3A)
- THERMAL SHUT DOWN WITH HYSTERESIS
- μ P COMPATIBLE LOGIC INPUTS W'ITH HIGH NOISE IMMUNITY
- LOW LEAKAGE FAST RECOVERY DIODES
- NO CURRENT FROM HIGH VOLTAGE SUPPLIES WHEN ENABLE PIN IS LOW

An enable input allows all four transistors of the bridge to be switched off independently of the input commands.

Each half bridge can be connected to an external sense resistor and have a separate high voltage supply.

An additional supply input is provided so that the logic can operate at a lower voltage, reducing dissipation.

The device is equipped with a thermal protection which, switches off the input and output stages when the temperature reaches 150°C and switches on with hysteresis when the temperature decreases.

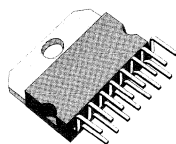
Another important feature is the switching speed (less than 1.5 μ s).

The L6209 is supplied in a 15-lead Multiwatt[®] package.

The L6209 is a high voltage, high current full-bridge driver with internal fast recovery diodes.

The cathodes of the upper recirculation diodes and the anodes of the lower ones are externally available to allow flexibility in application.

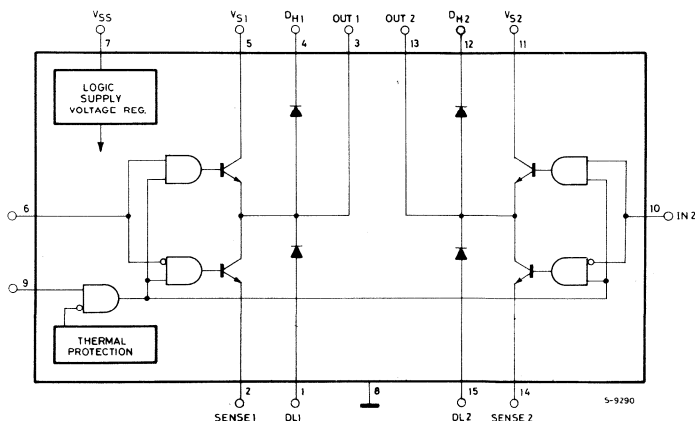
The device is designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC motors and stepping motors.



Multiwatt-15

ORDERING NUMBER: L6209

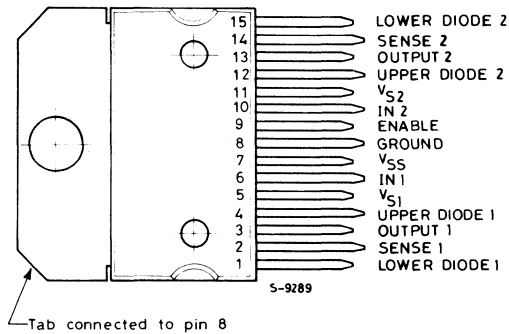
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{S1}, V_{S2}	Power supply	46	V
V_{SS}	Logic supply voltage	7	V
V_{IN}, V_{EN}	Input and enable voltage	-0.3 to 7	V
I_O	Peak output current		
	— non repetitive ($t = 100\mu s$)	5	A
	— repetitive (80% on - 20% off; $t_{on} = 10ms$)	4.5	A
	— DC operation	4	A
V_{sens}	Sensing voltage	-1 to 2.3	V
P_{tot}	Total power dissipation ($T_{case} = 75^{\circ}C$)	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^{\circ}C$
V_{DH}	Maximum recirculation voltage	46	V

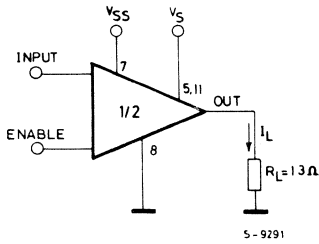
CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max	3	$^{\circ}C/W$
$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	35	$^{\circ}C/W$

Fig. 1 - Switching times test circuits



Note: For INPUT chopper, set EN = H

Fig. 1a - Source current delay times vs. input chopper

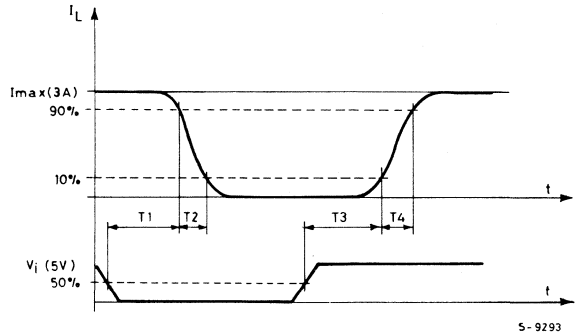
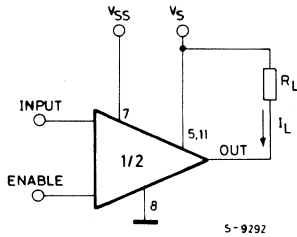


Fig. 2 - Switching times test circuits



Note: For INPUT chopper, set EN = H

Fig. 2a - Sink current delay times vs. input chopper

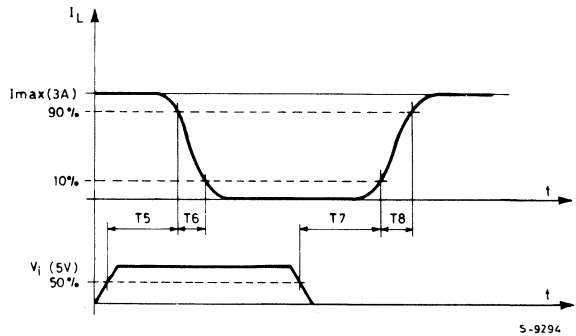
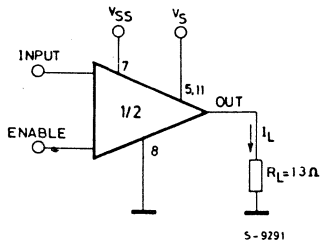


Fig. 3 - Switching times test circuits



Note: For enable chopper in this configuration, set, INPUT = H

Fig. 3a - Source current delay times vs. enable chopper.

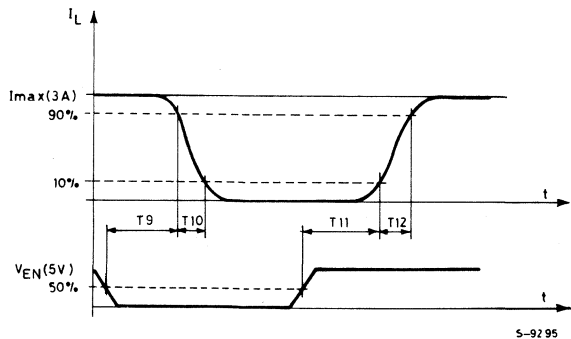
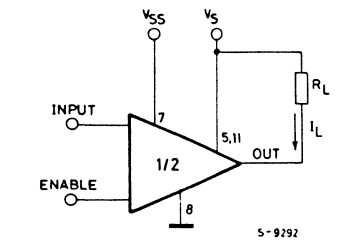
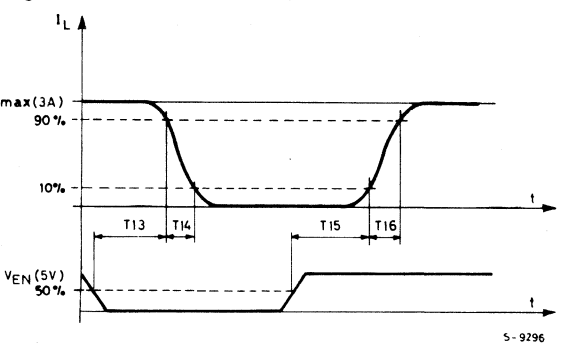


Fig. 4 - Switching times test circuits



Note: For enable chopper in this configuration, set INPUT = L

Fig. 4a - Sink current delay times vs. enable chopper



ELECTRICAL CHARACTERISTICS (for each channel, $V_s = 42V$, $V_{ss} = 5V$, $T_j = 25^{\circ}C$)

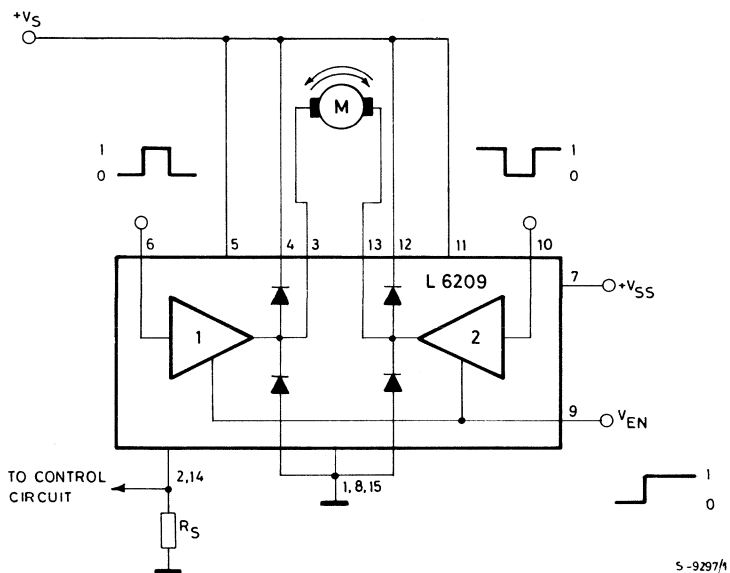
Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s Supply voltage (pin 5, 11)	Operative condition	9		42	V
V_{ss} Logical supply voltage (pin 7)		4.5		5.5	V
I_s Quiescent supply current (pin 5, 11)	$V_{EN} = H$ $I_L = 0$ $V_{IN} = L$		0	1	mA
	$V_{IN} = H$		3	10	
	$V_{EN} = L$		0	1	
I_{ss} Quiescent current from V_{ss} (pin 7)	$V_{EN} = H$ $I_L = 0$ $V_{IN} = L$		40		mA
	$V_{IN} = H$		20		
	$V_{EN} = L$		7		
$V_{IN L}$ Input low voltage (pins 10, 6)		-0.3		0.8	V
$V_{IN H}$ Input high voltage (pins 10, 6)		2		V_{ss}	
$I_{IN L}$ Low voltage input current (pins 10, 6)	$V_{IN} = L$		-20	-50	μA
$I_{IN H}$ High voltage input current (pins 10, 6)	$V_{IN} = H$			50	
$V_{EN L}$ Enable low voltage (pin 9)		-0.3		0.8	V
$V_{EN H}$ Enable high voltage (pin 9)		2		V_{ss}	
$I_{EN L}$ Low voltage enable current (pin 9)	$V_{EN} = L$		-20	-50	μA
$I_{EN H}$ High voltage enable current (pin 9)	$V_{EN} = H \leq V_{ss}$			50	
$V_{CE sat (H)}$ Source saturation voltage	$I_L = 1A$		1.1		V
	$I_L = 3A$		2		

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{CE\ sat}$ (L) Saturation voltage	$I_L = 1A$		1		V
	$I_L = 3A$				
$V_{CE\ sat}$ Total drop	$I_L = 1A$		2.1	3	V
	$I_L = 3A$		3.5	4.5	
V_F Diode forward voltage drop	$I_O = 1A$		1		V
	$I_O = 3A$		1.5		
t_{rr} Diode reverse recovery time	$I_f = 1A$ $dI_f/dt = -50A/\mu s$ $I_{RM} = 2.5A$ $V_R = 42V$		100		ns
t_{fr} Diode forward recovery time	$I_f = 1A$ $dI_f/dt = 100A/\mu s$ Measured at $V_F = 1V$		100		ns
T1 (V_{IN}) Source current turn-off delay	$0.5 V_i$ to $0.9 I_L$ (2)		750		ns
T2 (V_{IN}) Source current fall time	$0.9 I_L$ to $0.1 I_L$ (2)		430		ns
T3 (V_{IN}) Source current turn-on delay	$0.5 V_i$ to $0.1 I_L$ (2)		1.1		μs
T4 (V_{IN}) Source current rise time	$0.1 I_L$ to $0.9 I_L$ (2)		500		ns
T5 (V_{IN}) Sink current turn-off delay	$0.5 V_i$ to $0.9 I_L$ (3)		700		ns
T6 (V_{IN}) Sink current fall time	$0.9 I_L$ to $0.1 I_L$ (3)		500		ns
T7 (V_{IN}) Sink current turn-on delay	$0.5 V_i$ to $0.1 I_L$ (3)		950		ns
T8 (V_{IN}) Sink current rise time	$0.1 I_L$ to $0.9 I_L$ (3)		400		ns
T9 (V_{IN}) Source current turn-off delay	$0.5 V_i$ to $0.9 I_L$ (4)		450		ns
T10 (V_{IN}) Source current fall time	$0.9 I_L$ to $0.1 I_L$ (4)		250		ns
T11 (V_{IN}) Source current turn-on delay	$0.5 V_i$ to $0.1 I_L$ (4)		550		ns
T12 (V_{IN}) Source current rise time	$0.1 I_L$ to $0.9 I_L$ (4)		250		ns
T13 (V_{IN}) Sink current turn-off delay	$0.5 V_i$ to $0.9 I_L$ (5)		350		ns
T14 (V_{IN}) Sink current fall time	$0.9 I_L$ to $0.1 I_L$ (5)		200		ns
T15 (V_{IN}) Sink current turn-on delay	$0.5 V_i$ to $0.1 I_L$ (5)		800		ns
T16 (V_{IN}) Sink current rise time	$0.1 I_L$ to $0.9 I_L$ (5)		200		ns
f_c Commutation frequency	$I_L = 3A$		35	60	KHz

NOTE: (1) Sensing voltage can be -1V for $t \leq 50\mu s$; in steady state $V_{sens\ min} \geq -0.5V$
(2) See fig. 1a. (INPUT chopper)
(3) See fig. 2a. (INPUT chopper)
(4) See fig. 3a. (ENABLE chopper)
(5) See fig. 4a. (ENABLE chopper)

Fig. 5 - Bidirectional DC motor control



TRUTH TABLE

	INPUTS	FUNCTION
$V_{EN} = H$	INA = H INB = L	Turn right
	INA = L INB = H	Turn left
	INA = INB	Fast motor stop
$V_{EN} = L$	INA = X INB = X	Free running motor stop

L = Low H = High X = Don't care



L6210

ADVANCE DATA

DUAL SCHOTTKY DIODE BRIDGE

- MONOLITHIC ARRAY OF EIGHT SCHOTTKY DIODES
- HIGH EFFICIENCY
- 4A PEAK CURRENT
- LOW FORWARD VOLTAGE
- FAST RECOVERY TIME
- TWO SEPARATED DIODE BRIDGES

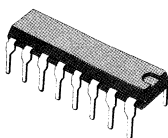
The L6210 is a monolithic IC containing eight Schottky diodes arranged as two separated diode bridges.

This diodes connection makes this device versatile in many applications.

They are used particular in bipolar stepper motor applications, where high efficient operation,

due to low forward voltage drop and fast reverse recovery time, are required.

The L6210 is available in a 16 Pin Powerdip Package (12+2+2) designed for the 0 to 70°C ambient temperature range.



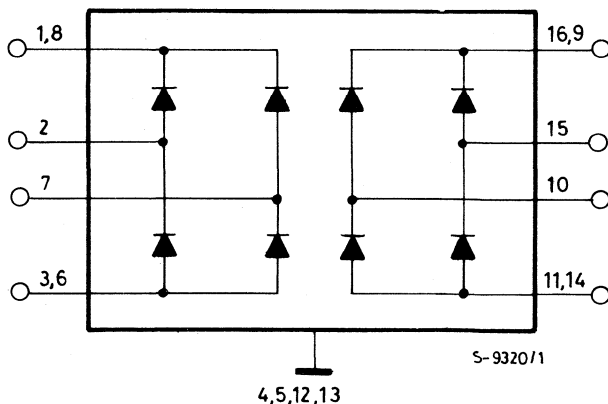
Powerdip 12 + 2 + 2
(V6P2)

ORDERING NUMBER: L6210

ABSOLUTE MAXIMUM RATINGS

I_f	Repetitive forward current peak	2	A
V_r	Peak reverse voltage (per diode)	50	V
T_{amb}	Operating ambient temperature	70	°C
T_{stg}	Storage temperature range	-55 to 150	°C

BLOCK DIAGRAM





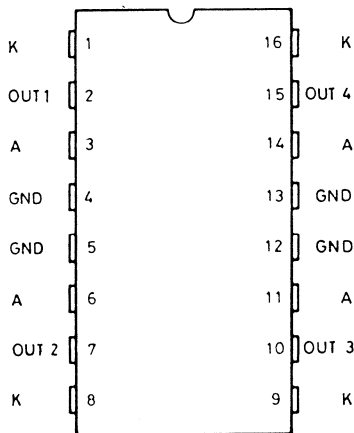
L6210

THERMAL DATA

$R_{th\ j-case}$	Thermal impedance junction-case	max	14	$^{\circ}C/W$
$R_{th\ j-amb}$	Thermal impedance junction-ambient without external heatsink	max	65	$^{\circ}C/W$

CONNECTION DIAGRAM

(Top view)



S-9321

ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}C$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_f Forward voltage drop	$I_f = 500mA$		0.8	1	V
	$I_f = 1A$		1	1.2	V
t_{rr} Reverse recovery time	0.5A forward to 0.5A reverse		15	60	ns
t_{fr} Forward recovery time	1A forward to 1.1V recovery		30	90	ns
I_L Leakage current	$V_R = 40V$ $T_{amb} = 25^{\circ}C$			100	μA

NOTE: At forward currents of greater than 1A, a parasitic current of approximately 1mA may be collected by adjacent diodes.

Fig. 1 - Reverse current vs. voltage

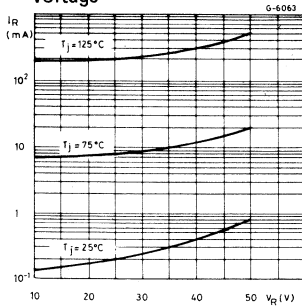
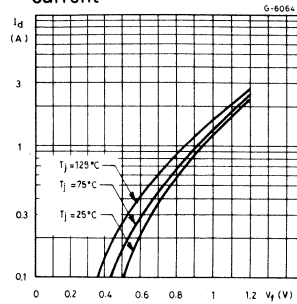


Fig. 2 - Forward voltage vs. current



MOUNTING INSTRUCTIONS

The $R_{thj-amb}$ of the L6210 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board as shown in figure 3 or to an external heatsink (Figure 4).

During soldering the pin temperature must not exceed 260°C and the soldering time must not be longer than 12s. The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 3 - Example of P.C. board copper area which is used as heatsink

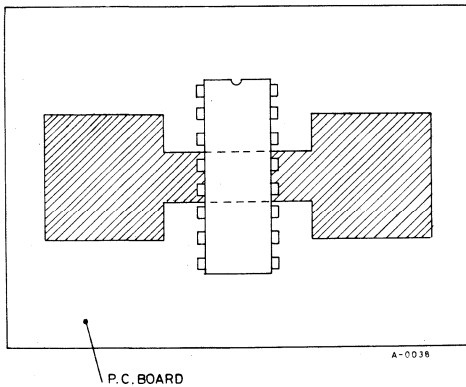
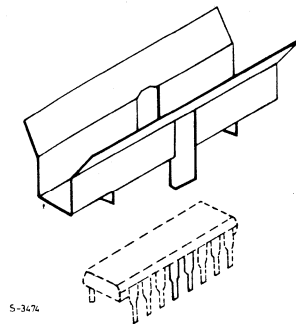


Fig. 4 - Example of an external heatsink





L6212

ADVANCE DATA

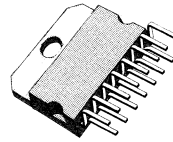
HIGH CURRENT SOLENOID DRIVER

- HIGH VOLTAGE OPERATION (UP TO 50V)
- HIGH OUTPUT CURRENT CAPABILITY (UP TO 6A)
- LOW SATURATION VOLTAGE
- TTL-COMPATIBLE INPUT
- OUTPUT SHORT CIRCUIT PROTECTION (TO GROUND, TO SUPPLY AND ACROSS THE LOAD)
- THERMAL SHUTDOWN
- OVERDRIVING PROTECTION
- LATCHED DIAGNOSTIC OUTPUT

The L6212 is a monolithic switch-mode solenoid driver designed for fast, high-current applications

such as hammer driving in printers and electronic typewriters. Power dissipation is reduced by efficient switch-mode operation. An extra feature of the L6212 is a latched diagnostic output which indicates when the output is short circuit.

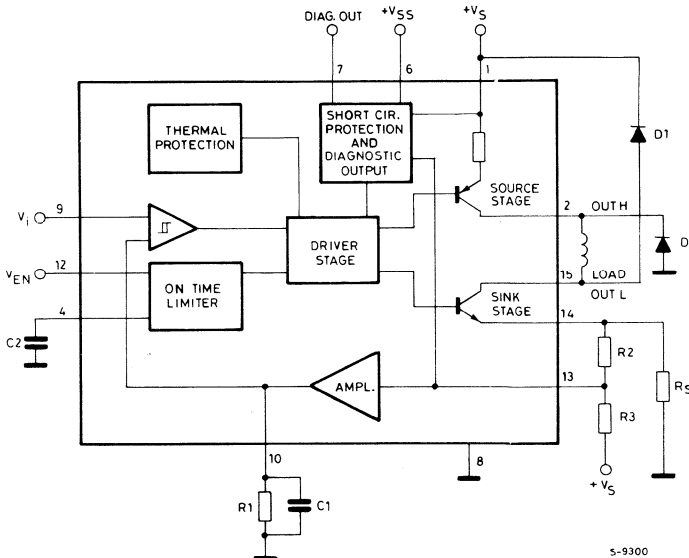
The L6212 is supplied in an 15-lead Multiwatt plastic power package.



Multiwatt-15

ORDERING NUMBER: L6212

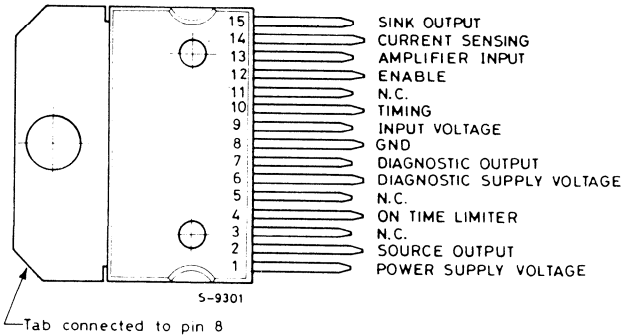
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_s	Power supply voltage	50	V
V_{ss}	Logic supply voltage	7	V
V_{EN}	Enable voltage	7	V
V_i	Input voltage	7	V
I_p	Peak output current (repetitive)	6.5	A
P_{tot}	Total power dissipation (at $T_{case} = 75^{\circ}C$)	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^{\circ}C$

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max	3	$^{\circ}C/W$
$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	35	$^{\circ}C/W$

**L6212**

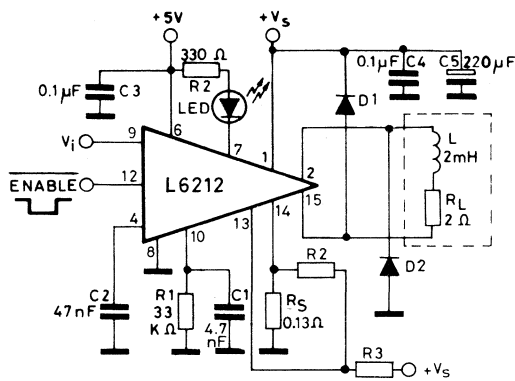
ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s = 37V$, $V_{ss} = 5V$, $T_{amb} = 25^\circ C$, unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s Power supply voltage (Pin 1)		12		46	V
I_d Quiescent drain current	$V_{EN} = H$		20	30	mA
	$V_i \geq 0.6V$ $V_{EN} = L$		70		mA
V_{ss} Logic supply voltage (Pin 6)		4.5		7	V
I_{ss} Quiescent logic supply current	$V_{DIAG} = L$		5	8	mA
	DIAG Output at high impedance		10	100	μA
V_i Input voltage (Pin 9)	Operating output	0.6			V
	Non-operative output			0.45	V
I_i Input current (Pin 9)	$V_i \geq 0.6V$			-2	μA
	$V_i \leq 0.45V$			-5	μA
V_{ENABLE} Enable input current (Pin 12)	Low level High level	-0.3 2.4		0.8	V
I_{ENABLE} Enable input current	$V_{EN} = L$ $V_i = 0.8V$ $V_{EN} = H$ $V_e = 2.4V$			-100 100	μA
$V_{sat H}$ Source output saturation volt.	$I_p = 5.5A$			2.5	V
$V_{sat L}$ Sink output saturation volt.	$I_{out} = 5.5A$			2.5	V
$V_{sat H} + V_{sat L}$ Total saturation voltage	$I_{out} = 5.5A$			4.5	V
$I_{leakage}$ Output leakage current source PNP	$V_s = 45V$ $V_i \leq 0.45V$			2	mA
$I_{leakage}$ Output leakage current sink NPN	$V_s = 45V$ $V_i \leq 0.45V$			2	mA
K On time limiter constant (*)	$V_{EN} = L$		120		
V_{DIAG} Diagnostic saturation voltage (Pin 7)	$I_{DIAG} = 10mA$			0.4	V
I_{DIAG} Diagnostic leakage current (Pin 7)	$V_{DIAG} = 40V$			10	μA
$\frac{V_{pin10}}{V_{pin13}}$ OP AMP DC voltage gain	$V_{pin13} = 100$ to $800mV$		5		
V_{pin10}	$I_{pin10} = 1mA$	4.5			V
I_{pin10}	$V_{pin10} = 4V$ $V_9 = V_{13} = 0$ $V_{pin10} = 2V$ $V_{13} = 0.9V$	1		10 1.5	μA mA
I_{sense} Input bias current (Pin 13)			-1		μA
V_{sense} Sensing voltage (Pin 14) (**)				0.9	V

(*) After a time interval $t_{max} = KC_2$, the output stages are disabled.

(**) Allowed range of V_{sense} without the intervention of the short circuit protection.

Fig. 2 - Test and typical application circuit



D2: 6A fast diode } $t_{rr} \leq 200ns$
D1: 2A fast diode }

Fig. 3 - Peak output current vs. input voltage

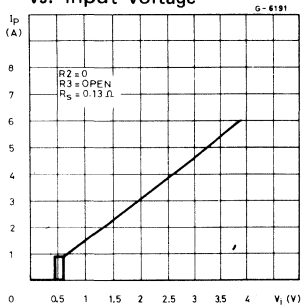


Fig. 4 - Peak output current vs. input voltage

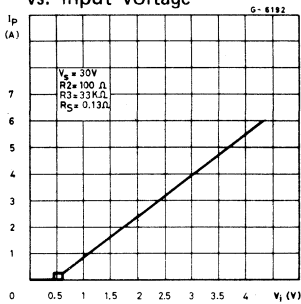
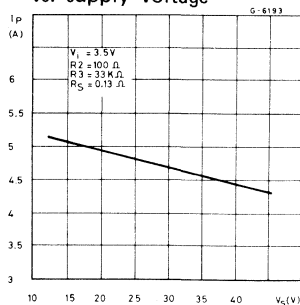


Fig. 5 - Peak output current vs. supply voltage





CIRCUIT OPERATION

The L6212 works as a transconductance amplifier: it can supply an output current directly proportional to an input voltage level (V_i). Furthermore, it allows complete switching control of the output current waveform (see Fig. 1).

The following explanation refers to the Block Diagram, to Fig. 1 and to the typical application circuit of Fig. 2.

The t_{on} time is fixed by the width of the Enable input signal (TTL compatible): it is active low and enables the output stages "source" and "sink". At the end of t_{on} , the load current I_{load} recirculates through D1 and D2, allowing fast current turn-off.

The rise time t_r depends on the load characteristics, on V_i and on the supply voltage value (V_s , pin 1).

During the t_{on} time, I_{load} is converted into a voltage signal by means of the external sensing resistance R_s connected to pin 13. This signal, amplified by the op amp charges the external RC network at pin 10 ($R1$, $C1$). The voltage at this pin is sensed by the inverting input of a comparator. The voltage on the non-inverting input of this one is fixed by the external voltage V_i (pin 9).

After, t_r , the comparator switches and the output stage "source" is switched off. The comparator output is confirmed by the voltage on the non-inverting input, which decreases of a constant fraction of V_i (1/10), allowing hysteresis operation. The current in the load now flows through D2.

Two cases are possible: the time constant of the recirculation phase is higher than $R1$, $C1$; the time constant is lower than $R1$, $C1$. In the first case, the voltage sensed on the non-inverting input of the comparator is just the value proportional to I_{load} . In the second case, when the current decreases too quickly, the comparator senses the voltage signal stored in the $R1$, $C1$ network.

In the first case t_1 depends on the load characteristics, while in the second case it depends only on the value of $R1$, $C1$.

In other words, $R1$, $C1$ fixed the minimum value of t_1 ($t_1 \geq 1/10 R1 \times C1$). Note that $C1$ should

be chosen in the range 2.7 to 10nF for stability reasons of the op amp).

After t_1 , the comparator switches again: the output is confirmed by the voltage on the non-inverting input, which reaches V_i again (hysteresis).

Now the cycle starts again: t_2 , t_4 and t_6 have the same characteristics as t_r , while t_3 and t_5 are similar to t_1 . The peak current I_p depends on V_i as shown in the typical transfer function of Fig. 3.

It can be seen that for V_i lower than 450mV the device is not operating.

For V_i included between 450 and 600mV, the operation is not guaranteed.

The other parts of the device have protection and diagnostic functions. At pin 4 is connected an external capacitor $C2$, charged at constant current when the Enable is low.

After a time interval equal to $K \cdot C1$ (K is defined in the table of Electrical Characteristics and has the dimensions of Ω) the output stages are switched off independently by the Input signal.

This avoids the load being driven in conduction for an excessive period of time (overdriving protection).

The action of this protection is shown in Fig. 1b. Note that the voltage ramp at pin 4 starts whenever the Enable signal becomes active (low state), regardless of the Input signal. To reset pin 4 and to restore the normal conditions, pin 12 must return high. This protection can be disabled by grounding pin 4.

In order to keep constant the energy delivered to the load, when the supply voltage changes, it's possible to modify the output maximum peak current (I_p) by means the external voltage divider $R2$ and $R3$ which "senses" the supply voltage.

I_p is given by:

$$I_p = \frac{V_i (R_s + R2 + R3) - 5 V_s (R2 + R_s)}{5 R3 R_s}$$

so the variation of I_p versus V_s is:

CIRCUIT OPERATION (continued)

$$\Delta I_P = - \frac{R_2 + R_s}{R_3 R_s}$$

The thermal protection included in the L6212 has a hysteresis.

It switches off the output stages whenever the junction temperature increases too much. After a fall of about 20°C, the circuit starts again.

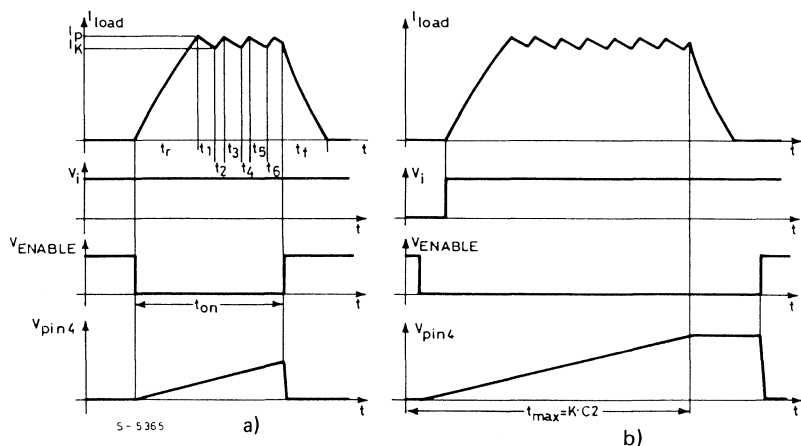
Finally, the device is protected against any type of short circuit at the outputs: to ground, to supply and across the load.

When the source stage current is higher than 7A and/or when the pin 13 voltage is higher

than 1V (i.e. for a sink current greater than $1V/R_s$) the output stages are switched off and the device is inhibited.

This condition is indicated at the open-collector output DIAG (pin 7); the internal flip-flop F/F changes and forces the output transistor into saturation. The F/F must be supplied independently through V_{ss} (pin 6). The DIAG signal is reset and the output stages made operative by switching off the supply voltage at pin 1 and then by switching the device on again. After that, two cases are possible: the reason for the "bad operation" is still present and the protection acts again; the reason has been removed and the device starts to work properly.

Fig. 1 - Output current waveforms





L6217

ADVANCE DATA

STEPPER MOTOR DRIVER

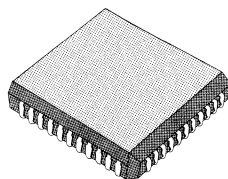
- MICROSTEPPING
- BIPOLAR OUTPUT CURRENT UP TO 400mA
- LOW SATURATION VOLTAGE
- BUILT-IN FAST RECOVERY DIODES
- OUTPUT CURRENT DIGITALLY PROGRAMMABLE
- 6 BIT D/A CONVERTERS SET OUTPUT CURRENT
- THERMAL SHUTDOWN

The L6217 is a monolithic IC that controls and drives both phases of a Bipolar Stepper Motor with PWM control of the phase current. The output current level of each phase is programmed by a 6 bit D/A converter so that the device may be used in full-step, half-step and micro-step applications. The inputs for the D/A converters and the phase inputs to select the direction of current flow are latched to minimize the interface to a microprocessor.

The power section of the device is a dual H-Bridge drive with internal clamp diodes for current recirculation. To maintain the degree of accuracy required for micro-stepping, the motor current is internally sensed and compared to the output of the D/A converter.

A monostable, programmed by an RC network sets the motor current decay time.

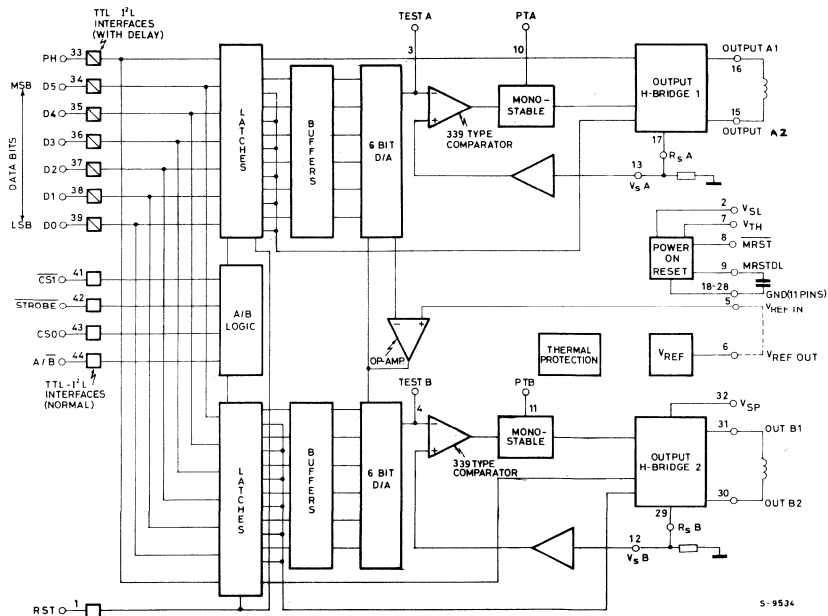
The L6217 is supplied in a 44 pin PLCC with 11 of the 44 pins used for heatsinking.



PLCC 44
(Plastic Chip-Carrier)

ORDERING NUMBER: L6217

BLOCK DIAGRAM



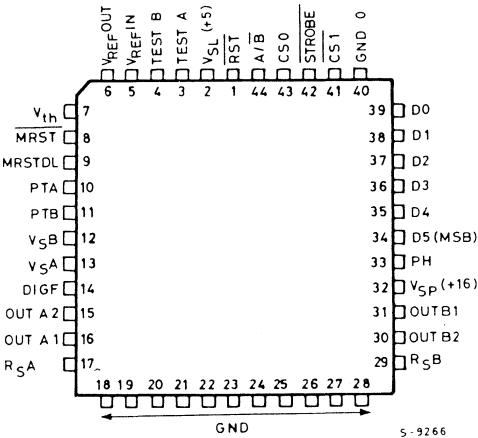
S-9534

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{si}	Logic supply voltage	7	V
V_{sp}	Motor supply voltage	18	V
V_i	Logic input voltage	6	V
V_{ref}	Reference input voltage	V_{si}	V
I_o	Output peak current	500	mA
T_j	Operating junction temperature	150	°C
T_{stg}	Storage temperature	-55 to +150	°C

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j-case}$	Thermal impedance junction-case	max	10	°C/W
$R_{th\ j-amb}$	Thermal impedance junction-ambient	max	80	°C/W

PIN FUNCTION DESCRIPTION

N°	NAME	FUNCTION
1	$\overline{R_{st}}$	Active low input resets the D/A latches to 0 and disables the output.
38, 39	D0 - D5	Data inputs for the D/A converter. (D0 = LSB) For a data input of 00, the corresponding outputs are held in the off state.
44	A/B	Channel select for input data. Pin $A/\overline{B}$ selects channel A when high.
33	PH	Logic input selects direction of current flow in output bridge from A1 (B1) to A2 (B2) for PH = 1.
42	$\overline{\text{Strobe}}$	Active low input latches input data (D0 - D5 and PH) into input latch.
9	MRST DL	The capacitor on this pin programs the power on reset delay according to the formula: $t_d = (0.35) (C) 10^6$
8	$\overline{\text{MRST}}$	Power-on reset circuit output. (Micro reset signal). This output remains low from power on until the delay capacitor has charged past the delay threshold.
10	P _t A	Pulse time A, an external parallel RC network tied to ground defines t _{off} time for channel A. (t _{off} = 0.69 R2C2).
11	P _t B	Pulse time B, an external parallel RC network tied to ground defines toll time for channel B. (t _{off} = 0.69 R3C3).
5	V _{ref in}	Voltage applied to this point sets the reference for the D/A converter and threfore sets the maximum output current. (See equation 1, next two pages).
18 to 28	Gnd	Ground connection and also conducts heat to the P.C. board.
40	Gnd 0	Pin must be connected to ground.
2	V _{sl}	Logic supply voltage
32	V _{sp}	Motor supply voltage

PIN FUNCTION DESCRIPTION (continued)

N°	NAME	FUNCTION
16, 15 31, 30	Out A1-A2 B1-B2	H-Bridge outputs.
43, 41	CS0, $\overline{\text{CS1}}$	Chip select inputs CS0 is active high, $\overline{\text{CS1}}$ is active low.
17, 29	R _s A - R _s B	Sense resistor from this pin to ground set the peak output current.
13, 12	V _s A - V _s B	Analog inputs for sensing motor current, Separate inputs are provides to allow filtering of the sense voltage if required.
3, 4	Test A & B	These pins are for testing of D/A outputs.
6	V _{ref out}	2.5V band gap reference.
7	V _{th}	Reset threshold voltage
14	DIGF	Can be used to modify the internal comparator lockout time. In the typical application this pin is left open.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_j = 25°C unless otherwise specified noted)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{sp} Motor supply voltage		8		16	V
V _{sl} Logic supply voltage		4.75		5.25	V

LOGIC INPUTS (D0 - D5, CS0, CS1, Reset and A/B)

V _{IL} Input low voltage				0.8	V
V _{IH} Input high voltage		2		V _{sl}	V
I _{IL} Input low current	V _I = 0.4V			-400	μA
I _{IH} Input high current	V _I = 2.4V			10	μA

CURRENT CONTROL AND D TO A SECTION

V _{ref} Reference voltage	V _{CC} = 5.0V	2.45	2.50	2.55	V
V _{rin} Reference input range		2.0		3.0	V
Monotonicity of D to A		-0.5		+0.5	LSB
Linearity of D to A		-1		+1	LSB
I _{op} Peak Output Current (Gain of current loop)	V _{ref} = 2.40V R _{sense} = 2Ω Data = 3F (Hex)	225	252	277	mA
I _o Output matching	V _{ref} = 2.40V			5	%

**L6217****ELECTRICAL CHARACTERISTICS** (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
MONOSTABLE					
t_{off} Cutoff time	$R_t = 56K\Omega$ $C_t = 820pF$	27		37	μs
t_d Turn-off delay				2	μs
I_{off} Output leakage current	Data = 00 (Hex)			100	μA

RESET CIRCUITRY

V_{th} Reset threshold voltage		3.9	4.1	4.3	V
Reset threshold hysteresis		70	100		mV
I_{so} Delay capacitor charging current	$V_C = 2.5V$	7	10	14	μA
I_{sj} Delay capacitor discharge current	$V_C = 2.5V$	10			mA
V_{dth} Delay threshold voltage		3.25	3.5	3.75	V
V_{dhys} Hysteresis voltage on delay threshold		70	100		mV
I_{ol} Output leakage current	$V_O = 5V$			200	μA
V_{sat} Output saturation of reset out	$I_O = 2mA$			0.4	V

SOURCE DIODE-TRANSISTOR PAIRS

V_{sat} Saturation voltage	$I_O = 400mA$		1.3	1.8	V
V_f Diode forward voltage	$I_O = 400mA$		0.8	1.2	V

SINK DIODE-TRANSISTOR PAIRS

V_{sat} Saturation voltage	$I_O = 400mA$		1.1	1.5	V
V_f Diode Forward voltage	$I_O = 400mA$		0.6	1.0	V

AC CHARACTERISTICS

t_s Set-up time				100	ns
t_h Hold time				500	ns
t_w Minimum input pulse width				600	ns

CIRCUIT OPERATION

The current control section of the L6217 is a pulse width modulated control that senses the motor current. When the motor current reaches the peak programmed current the comparator will trigger the monostable turning off the upper transistors. After the t_{off} time equal to 0.69 RC the upper drivers are enabled again.

The peak current is given by the equation :

$$I_{op} = \frac{V_{ref}}{4.69 \cdot R_{sense}} \cdot \frac{D}{64}$$

D = Input data (0 - 63)

When the input data is 00, the output stages are disabled by internal logic so that the output current decays rapidly to zero.

An internal generated lockout time avoids the use of an external RC network between the sensing resistor (R_sA , R_sB) and the corresponding input (V_sA , V_sB), by disabling the comparator sensing during the lockout time. This time is typically 2.5ms.

Timing diagram for the 9267 device. The diagram shows four signals: DATA, STROBE, CS1, and CS0. The DATA signal is a horizontal line with a central pulse. The STROBE signal is a horizontal line with a central pulse. The CS1 signal is a horizontal line with a central pulse. The CS0 signal is a horizontal line with a central pulse. The timing parameters are labeled: t_S (setup time), t_H (hold time), and t_W (write time).

Fig. 4 - Motor current (half step mode)

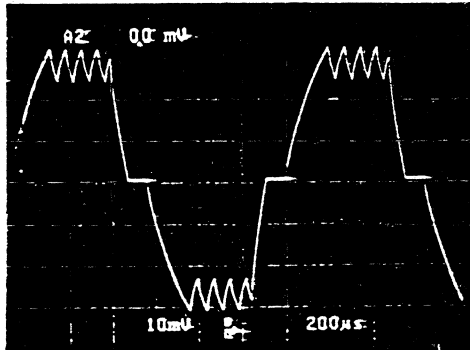


Fig. 5 - Monostable voltage and motor current repetitive steps.

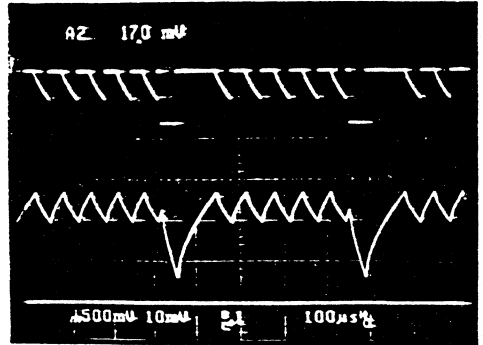
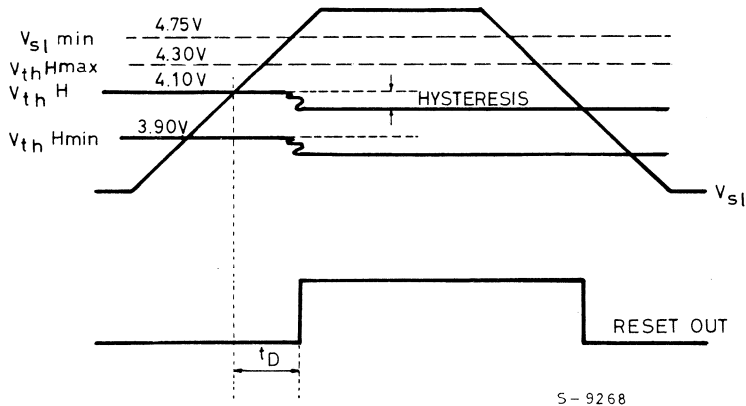


Fig. 6 - Reset waveforms





L6217A

ADVANCE DATA

STEPPER MOTOR DRIVER

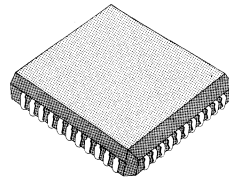
- MICROSTEPPING
- BIPOLAR OUTPUT CURRENT UP TO 400mA
- LOW SATURATION VOLTAGE
- BUILT-IN FAST RECOVERY DIODES
- OUTPUT CURRENT DIGITALLY PROGRAMMABLE
- 7 BIT D/A CONVERTERS SET OUTPUT CURRENT
- THERMAL SHUTDOWN

The L6217A is a monolithic IC that controls and drives both phases of a Bipolar Stepper Motor with PWM control of the phase current. The output current level of each phase is programmed by a 7 bit D/A converter so that the device may be used in full-step, half-step and micro-step applications. The inputs for the D/A converters and the phase inputs to select the direction of current flow are latched to minimize the interface to a microprocessor.

The power section of the device is a dual H-Bridge drive with internal clamp diodes for current recirculation. To maintain the degree of accuracy required for microstepping, the motor current is internally sensed and compared to the output of the D/A converter.

A monostable, programmed by an RC network sets the motor current decay time.

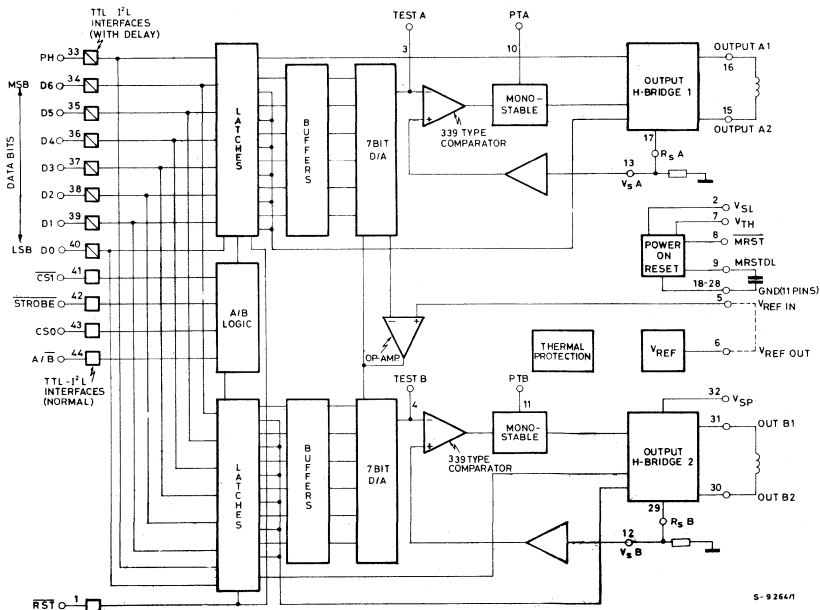
The L6217A is supplied in a 44 pin in PLCC with 11 of the 44 pins used for heatsinking.



PLCC 44
(Plastic Chip-Carrier)

ORDERING NUMBER: L6217A

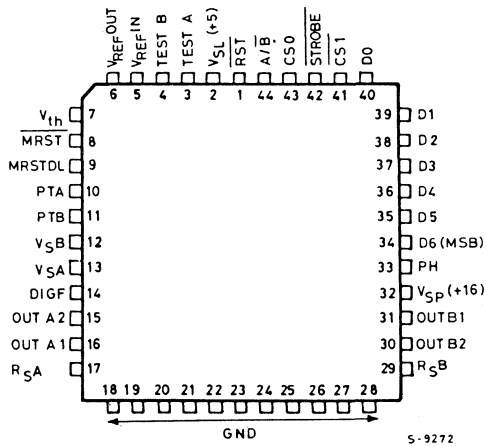
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{sl}	Logic supply voltage	7	V
V_{sp}	Motor supply voltage	18	V
V_i	Logic input voltage	6	V
V_{ref}	Reference input voltage	V_{sl}	V
I_o	Output peak current	500	mA
T_j	Operating junction temperature	150	°C
T_{stg}	Storage temperature	-55 to +150	°C

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j-case}$	Thermal impedance junction-case	max	10	°C/W
$R_{th\ j-amb}$	Thermal impedance junction-ambient	max	80	°C/W

PIN FUNCTION DESCRIPTION

N°	NAME	FUNCTION
1	$\overline{R_{st}}$	Active low input resets the D/A latches to 0 and disables the output.
40, 34	D0 - D6	Data inputs for the D/A converter. (D0 = LSB) For a data input of 00, the corresponding outputs are held in the off state.
44	$A/\overline{B}$	Channel select for input data. Pin $A/\overline{B}$ selects channel A when high.
33	PH	Logic input selects direction of current flow in output bridge from A1 (B1) to A2 (B2) for PH = 1.
42	$\overline{\text{Strobe}}$	Active low input latches input data (D0 - D5 and PH) into input latch.
9	MRST DL	The capacitor on this pin programs the power on reset delay according to the formula: $t_d = (0.35) (C) 10^6$
8	$\overline{\text{MRST}}$	Power-on reset circuit output. (Micro reset signal). This output remains low from power on until the delay capacitor has charged past the delay threshold.
10	P_tA	Pulse time A, an external parallel RC network tied to ground defines t_{off} time for channel A. ($t_{off} = 0.69 R2C2$).
11	P_tB	Pulse time B, an external parallel RC network tied to ground defines t_{off} time for channel B. ($t_{off} = 0.69 R2C2$)
5	$V_{ref\ in}$	Voltage applied to this point sets the reference for the D/A converter and therefore sets the maximum output current. (See equation 1, next two pages).
18 to 28	Gnd	Ground connection and also conduct heat to the P.C. board.
2	V_{sl}	Logic supply voltage
32	V_{sp}	Motor supply voltage
16, 15 31, 30	Out A1-A2 B1-B2	H-Bridge outputs.



L6217A

PIN FUNCTION DESCRIPTION (continued)

N°	NAME	FUNCTION
43, 41	CS0, $\overline{\text{CS1}}$	Chip select inputs CS0 is active high, $\overline{\text{CS1}}$ is active low.
17, 29	R _s A - R _s B	Sense resistor from this pin to ground set the peak output current.
13, 12	V _s A - V _s B	Analog inputs for sensing motor current, Separate inputs are provides to allow filtering of the sense voltage if required.
3, 4	Test A & B	These pins are for testing of D/A outputs.
6	V _{ref out}	2.5V band gap reference.
7	V _{th}	Reset threshold voltage
14	DIGF	Can be used to modify the internal comparator lockout time. In the typical application this pin is left open.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_j = 25°C unless otherwise specified noted)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{sp} Motor supply voltage		8		16	V
V _{sl} Logic supply voltage		4.75		5.25	V

LOGIC INPUTS (D0 - D6, CS0, $\overline{\text{CS1}}$, PH, $\overline{\text{RST}}$ and A/ $\overline{\text{B}}$)

V _{IL} Input low voltage				0.8	V
V _{IH} Input high voltage		2		V _{sl}	V
I _{IL} Input low current	V _i = 0.4V			-400	μA
I _{IH} Input high current	V _i = 2.4V			10	μA

CURRENT CONTROL AND D TO A SECTION

V _{ref} Reference voltage	V _{CC} = 5.0V	2.45	2.50	2.55	V
V _{rin} Reference input range		2.0		3.0	V
Monotonicity of D to A		-0.5		+0.5	LSB
Linearity of D to A		-1		+1	LSB
I _{op} Peak Output Current (Gain of current loop)	V _{ref} = 2.38V R _{sense} = 2Ω Data = 7F (Hex)	225	252	277	mA
I _o Output matching	V _{ref} = 2.38V			5	%

**L6217A****ELECTRICAL CHARACTERISTICS** (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
MONOSTABLE					
t_{off} Cutoff time	$R_t = 56K\Omega$ $C_t = 820pF$	27		37	μs
t_d Turn-off delay				2	μs
I_{off} Output leakage current	Data = 00 (Hex)			100	μA

RESET CIRCUITRY

V_{th} Reset threshold voltage		3.9	4.1	4.3	V
Reset threshold hysteresis		70	100		mV
I_{so} Delay capacitor charging current	$V_C = 2.5V$	7	10	14	μA
I_{si} Delay capacitor discharge current	$V_C = 2.5V$	10			mA
V_{dth} Delay threshold voltage		3.25	3.5	3.75	V
V_{dhys} Hysteresis voltage on delay threshold		70	100		mV
I_{ol} Output leakage current	$V_O = 5V$			200	μA
V_{sat} Output saturation of reset out	$I_O = 2mA$			0.4	V

SOURCE DIODE-TRANSISTOR PAIRS

V_{sat} Saturation voltage	$I_O = 400mA$		1.3	1.8	V
V_f Diode forward voltage	$I_O = 400mA$		0.8	1.2	V

SINK DIODE-TRANSISTOR PAIRS

V_{sat} Saturation voltage	$I_O = 400mA$		1.1	1.5	V
V_f Diode Forward voltage	$I_O = 400mA$		0.6	1.0	V

AC CHARACTERISTICS

t_s Set-up time				100	ns
t_h Hold time				500	ns
t_w Minimum input pulse width				600	ns

CIRCUIT OPERATION

The current control section of the L6217A is a pulse width modulated control that senses the motor current. When the motor current reaches the peak programmed current the comparator will trigger the monostable turning off the upper transistors. After the t_{off} time equal to 0.69 RC the upper drivers are enabled again.

The peak current is given by the equation :

$$I_{op} = \frac{V_{ref}}{4.69 \cdot R_{sense}} \cdot \frac{D}{128}$$

D = Input data (0 - 7F H)

When the input data is 00, the output stages are disabled by internal logic so that the output current decays rapidly to zero.

An internal generated lockout time avoids the use of an external RC network between the sensing resistor (R_sA , R_sB) and the corresponding input (V_sA , V_sB), by disabling the comparator sensing during the lockout time. This time is typically 2.5 μs .



L6217A

Fig. 1 - Typical application

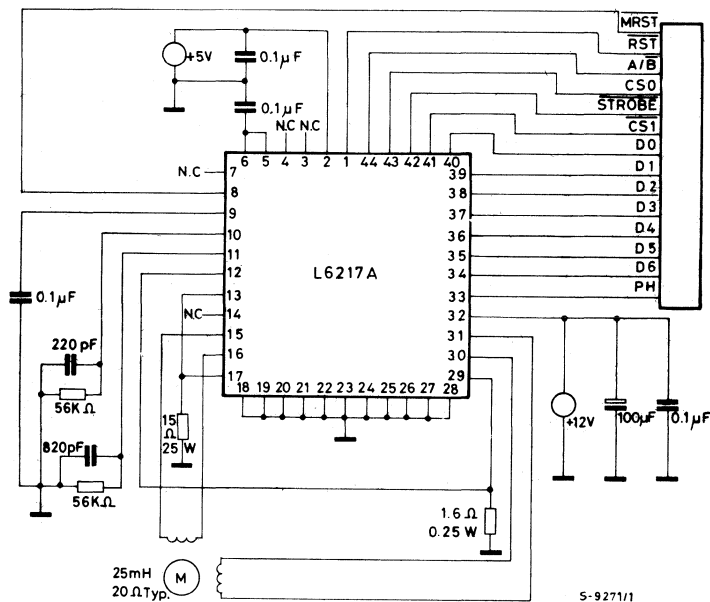


Fig. 2 - Microcomputer interface timing

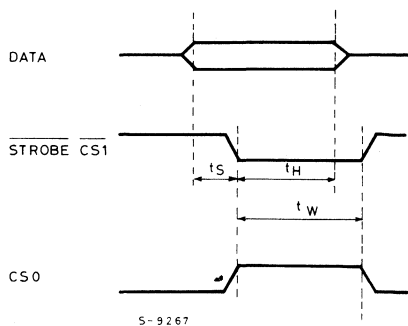


Fig. 3 - t_{off} DELAY

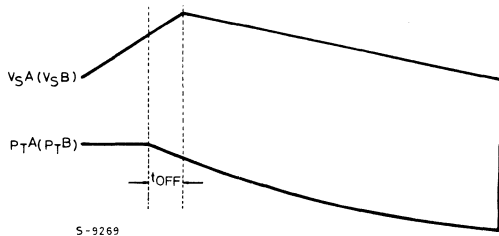


Fig. 4 - Motor current (half step mode)

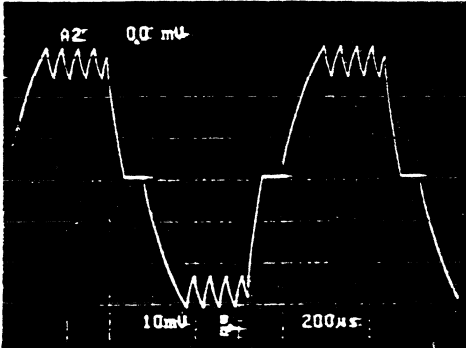


Fig. 5 - Monostable voltage and motor current for repetitive steps.

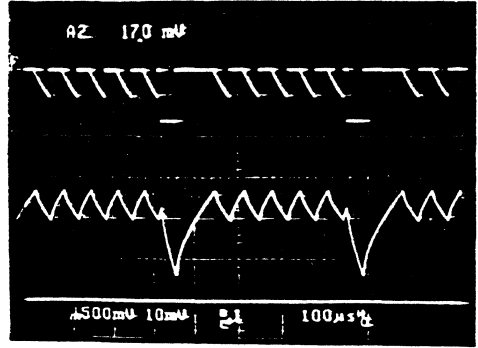
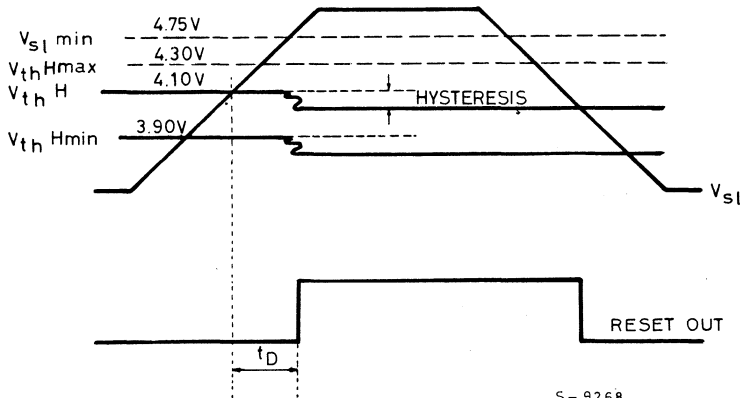


Fig. 6 - Reset waveforms





L6221A L6221N

ADVANCE DATA

QUAD DARLINGTON SWITCHES

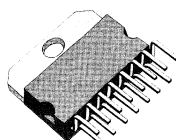
- OUTPUT VOLTAGE TO 50V
- OUTPUT CURRENT TO 1.8A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL FAST RECIRCULATION DIODES

The L6221 monolithic quad darlington switch is designed for high current, high voltage switching applications. Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL-compatible for direct connection to logic circuits.

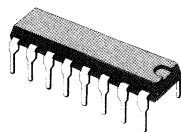
Each switch consists of an open-collector darlington transistor plus a fast diode for switching applications with inductive loads. The emitters

of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

Two versions are available: the L6221A mounted in a Powerdip 12+2+2 package and the L6221N mounted in a 15-lead Multiwatt package.



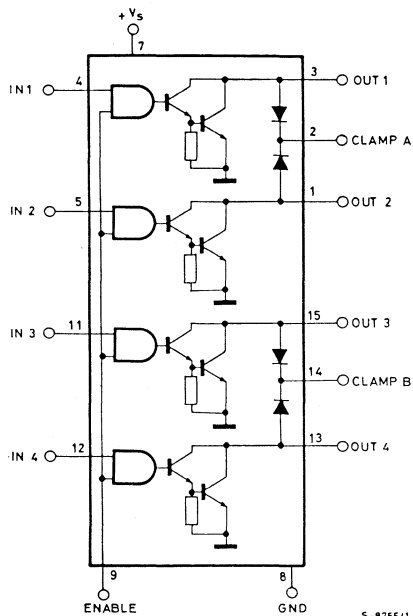
Multiwatt 15



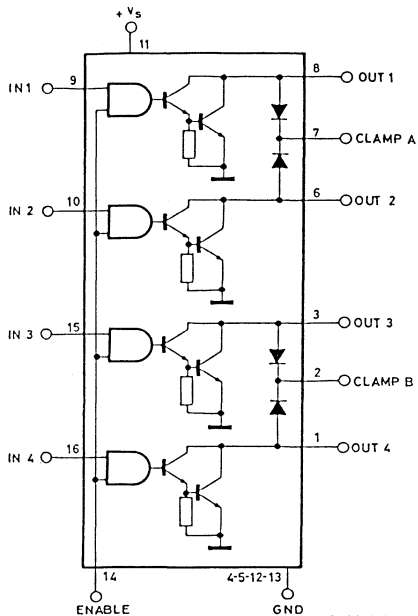
Powerdip 12 + 2 + 2
(V6P2)

ORDERING NUMBER :
L6221N L6221A

BLOCK DIAGRAMS



L6221N
Multiwatt



L6221A
Powerdip



L6221A
L6221N

ABSOLUTE MAXIMUM RATINGS

V_o	Output voltage	50	V
V_{SS}	Logic supply voltage	7	V
V_i	Input voltage	V_{SS}	
I_C	Collector current	1.8	A
I_C	Collector peak current (repetitive, duty cycle = 1% $t_{on} = 10ms$)	2.5	A
I_C	Collector peak current (non repetitive, $t = 10\mu s$)	3.2	A
T_{op}	Operating temperature range (junction)	-40 to +150	°C
T_{stg}	Storage temperature range	-55 to +150	°C
I_{sub}	Output substrate current	350	mA

THERMAL DATA

			Powerdip	Multiwatt
$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	80°C/W	35°C/W
$R_{th\ j-case}$	Thermal resistance junction-case	max	14°C/W	3°C/W

TRUTH TABLE

Enable	Input	Power out
H	H	ON
H	L	OFF
L	X	OFF

For each input: H = High level
L = Low level
X = Don't care



L6221A
L6221N

PIN FUNCTIONS

L6221N Multiwatt	L6221A Powerdip	Name	Function
4	9	IN 1	Input to driver 1
5	10	IN 2	Input to driver 2
3	8	OUT 1	Output of driver 1
1	6	OUT 2	Output of driver 2
2	7	CLAMP A	Diode clamp to driver 1 and driver 2
11	15	IN 3	Input to driver 3
12	16	IN 4	Input to driver 4
15	3	OUT 3	Output of driver 3
13	1	OUT 4	Output of driver 4
14	2	CLAMP B	Diode clamp to driver 3 and driver 4
9	14	ENABLE	Enable input to all drivers
7	11	V _{SS}	Logic supply voltage
8	4	GND	Ground
—	5	GND	Ground
—	12	GND	Ground
—	13	GND	Ground
6	—	NC	Not connected
10	—	NC	Not connected



L6221A
L6221N

ELECTRICAL CHARACTERISTICS ($V_{SS} = 5V$, $T_{amb} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SS} Logic supply voltage		4.5		7	V
$V_{CE(sus)}$ Output sustaining voltage	$V_{IN} = 0.8V$ $V_{EN} = 5V$ $I_C = 100mA$	46			V
I_{CEX} Output leakage current	$V_{CE} = 50V$ $V_{EN} = 5V$ $V_{IN} = 0.8V$			1	mA
$V_{CE(sat)}$ Collector emitter saturation voltage (One input on; all other inputs off.)	$I_C = 0.6A$	$V_{SS} = 4.5V$ $V_{IN} = 2V$ $V_{EN} = 4.5V$		1	V
	$I_C = 1A$			1.2	V
	$I_C = 1.8A$			1.8	V
V_{IL} Input low voltage				0.8	V
I_{IL} Input low current	$V_{IN} = 0.4V$			-100	μA
V_{IH} Input high voltage		2.0			V
I_{IH} Input high current	$V_{IN} = 2.0V$			± 10	μA
I_S Logic supply current	All outputs ON $I_C = 0.7A$			20	mA
	All outputs OFF			20	mA
I_R Clamp diode leakage current	$V_R = 50V$ $V_{EN} = 5V$ $V_{IN} = 0.8V$			100	μA
V_F Clamp diode forward voltage	$I_F = 1A$			1.6	V
	$I_F = 1.8A$			2.0	V
t_{on} Turn on time	$V_S = 5V$ $R_L = 10\Omega$			2	μs
t_{off} Turn off time	$V_S = 5V$ $R_L = 10\Omega$			5	μs
ΔI_S Logic supply current variation	$V_{IN} = 5V$, $V_{EN} = 5V$, $V_{SS} = 5V$ $I_{out} = -300mA$ for each channel			120	mA

QUAD TRANSISTOR SWITCH

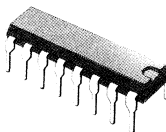
- OUTPUT VOLTAGE TO 50V
- OUTPUT CURRENT TO 1.2A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL SUPPRESSION DIODE

The L6222 monolithic quad transistor switch is designed for high current, high voltage switching applications.

Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL-compatible for direct connection to logic circuits. Each switch consists of an open-collector transistor plus a clamp diode for applications with inductive loads.

The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

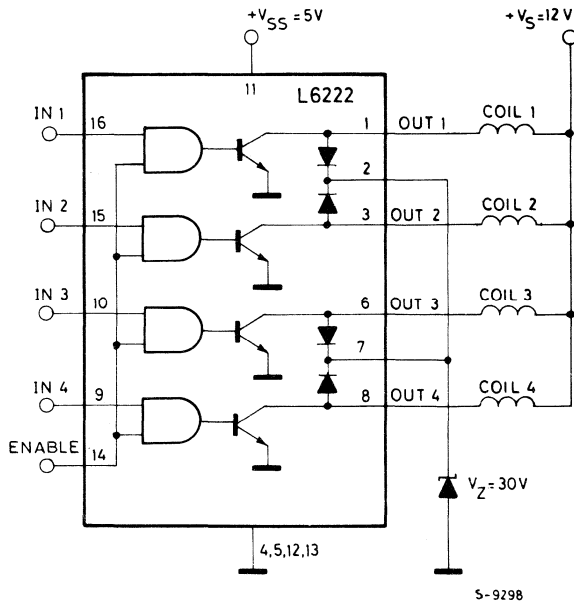
This device is intended to drive coils such as relays, solenoids, unipolar stepper motors, LED, etc.



Powerdip 12 + 2 + 2
(V6P2)

ORDERING NUMBER: L6222

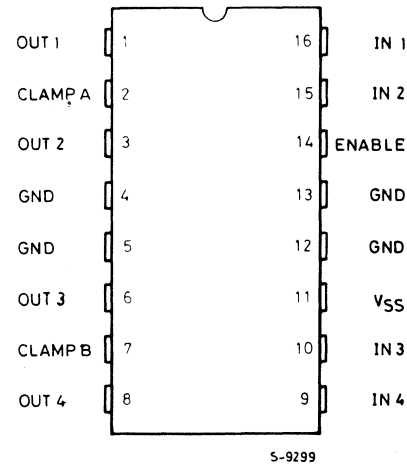
Fig. 1 - Unipolar stepper motor drive



ABSOLUTE MAXIMUM RATINGS

V_s	Output voltage	50	V
V_{ss}	Logic supply voltage	7	V
V_{IN}	Input voltage	15	V
I_C	Collector current (PEAK)	1.2	A
T_{op}	Operating temperature range (junction)	-40 to +150	°C
T_{stg}	Storage temperature range	-55 to +150	°C

CONNECTION DIAGRAM
(Top view)



TRUTH TABLE

Enable	Input	Power out
H	H	ON
H	L	OFF
L	X	OFF

For each input: H = High level
 L = Low level
 X = Don't care

THERMAL DATA

$R_{th\,j-amb}$	Thermal resistance junction-ambient	max	80	°C/W
$R_{th\,j-case}$	Thermal resistance junction-case	max	14	°C/W

**L6222****ELECTRICAL CHARACTERISTICS** ($T_{amb} = 25^{\circ}\text{C}$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{SS}	Logic supply voltage		4.50		7	V
$V_{CE(sus)}$	Output sustaining voltage	$V_{IN} = 0.8\text{V}$ $I_C = 100\text{mA}$	46			V
I_{CEX}	Output leakage current	$V_{CE} = 50\text{V}$ $V_{IN} = 0.8\text{V}$			1	mA
$V_{CE(sat)}$	Collector emitter saturation voltage	$V_{IN} \geq 2.0\text{V}$ $I_C = 0.1\text{A}$			0.2	V
		$I_C = 0.4\text{A}$			0.5	
		$I_C = 0.7\text{A}$			0.9	
V_{IL}	Input low voltage				0.8	V
I_{IL}	Input low current	$V_{IN} = 0.4\text{V}$			-100	μA
V_{IH}	Input high voltage		2.0			V
I_{IH}	Input high current	$V_{IN} \geq 2.0\text{V}$			± 10	μA
I_S	Logic supply current	$V_{SS} = 5\text{V}$ All outputs ON $I_C = 0.7\text{A}$		50	85	mA
		All outputs OFF		8		mA
I_R	Clamp diode leakage current	$V_R = 50\text{V}$			100	μA
V_F	Clamp diode forward voltage	$I_F = 0.7\text{A}$			1.6	V
		$I_F = 1.2\text{A}$			2.0	



BIDIRECTIONAL THREE-PHASE BRUSHLESS DC MOTOR DRIVER

- 3A OUTPUT CURRENT, CONTROLLED IN LINEAR MODE
- SUPPLY VOLTAGE UP TO 18V
- COMPATIBLE WITH ANI F-TO-V CONVERTER AND PLL SPEED CONTROL SYSTEM
- SLEW RATE LIMITING FOR EMI REDUCTION
- CONNECTS DIRECTLY TO HALL EFFECT CELLS
- THERMAL SHUTDOWN WITH HYSTERESIS
- THREE-STATE OPERATION ALLOWS NEGLIGIBLE POWER DISSIPATION DURING 1/3f CYCLE
- INTERNAL PROTECTION DIODES
- FEW EXTERNAL COMPONENTS

of the output stage. In addition the device is designed to limit power dissipation: during recirculation the output stage is switched to an off state, reducing dissipation to a very low value and minimizing torque ripple.

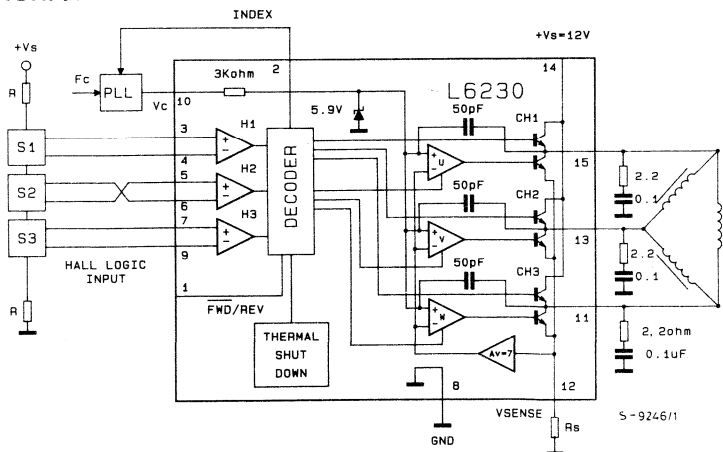
A speed control input controls the base current to the lower transistors to limit the motor current and hence control the speed. Any type of speed control system, including F to V and PLL systems, may be used with the L6230 by providing an analog signal at this input. The motor current may be sensed by an external resistor connected to a sensing pin on the device.

The power stage of the device is designed to eliminate the possibility of simultaneous conduction of the upper and lower power transistors of one output driver, when operating in the right loop.



ORDERING NUMBER: L6230H

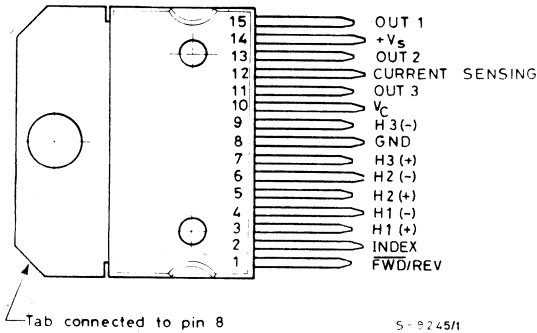
BLOCK DIAGRAM



633

12/86

CONNECTION DIAGRAM
 (Top view)



ABSOLUTE MAXIMUM RATINGS

V _s	Supply voltage	20	V
I _o	Peak output current each channel		
	— non repetitive (100μs)	4	A
	— repetitive (t = 10ms)	3.5	A
	— DC operation	3	A
V _i	Logic and analogic inputs	V _s	
P _{tot}	Total power dissipation T _{case} = 75°C	25	W
T _{op}	Operating temperature range	0 to 70	°C
T _j , T _{stg}	Storage and junction temperature	-40 to 150	°C

THERMAL DATA

R _{th j-case}	Thermal resistance junction-case	max	3	°C/W
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**L6230**

PIN FUNCTIONS

N°	NAME	I/O	FUNCTION
1	FWD/REV	I	Direction Control. When this pin is low, the motor will run in the forward direction. A high will drive the motor in the reverse direction. Direction is defined by the position of the sensors in the motor.
2	INDEX	O	Signal pulse proportional to the motor speed. In PLL speed control applications, this is the feedback to the PLL. One pulse per electrical rotation. This is an open collector output.
3	H1 (+)	I	Positive input of differential amplifier on channel 1. Interfaces with Hall Effect sensor, S1, from motor.
4	H1 (-)	I	Negative input of differential amplifier on channel 1. Interfaces with Hall Effect sensor, S1, from motor.
5	H2 (+)	I	Same as pin 3 for channel 2.
6	H2 (-)	I	Same as pin 4 for channel 2.
7	H3 (+)	I	Same as pin 3 for channel 3.
8	GND		Ground connection.
9	H3 (-)	I	Same as pin 4 for channel 3.
10	V _C	I	Speed control input. Connected to output of PLL in PLL speed control applications.
11	OUT3	O	Output motor drive for phase 3.
12	SENSE	I	Current Sensing. Input for load current sense voltage for output stage.
13	OUT2	O	Output motor drive for phase 2.
14	V _S		Motor supply voltage.
15	OUT1	O	Output motor drive for phase 1.



L6230

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$; $V_s = 12\text{V}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s Supply voltage		10	12	18	V
I_s Quiescent supply current			60	100	mA

HALL AMPLIFIERS

V_{CM} Common mode voltage range		0		10	V
V_{IO} Input offset voltage	$V_I = 6\text{V}$		2	10	mV
I_{IB} Input bias current	$V_I = 6\text{V}$		2	10	μA
I_{IO} Input offset current	$V_I = 6\text{V}$		0.1		μA

SPEED CONTROL INPUT (V_C)

V_I Input voltage range		0		5	V
I_{IB} Input bias current	$V_C < V_{sens}$		1	5	μA
V_{IC} Input clamping voltage			5.9		V

FWD/REVERSE INPUT

V_{IH} Input high voltage		2		V_s	V
V_{IL} Input low voltage		0		0.8	V
I_{IH} Input high current				10	μA
I_{IL} Input low current			-5	-50	μA

HALL LOGIC OUTPUT

V_{LO} Low output voltage	$I = 5\text{mA}$			0.8	V
I_L Leakage current	$V_{CE} = 12\text{V}$			10	μA

OUTPUT POWER STAGE

V_{sat} Total saturation voltage	$I_o = 1\text{A}$ $I_o = 2\text{A}$ $I_o = 3\text{A}$		2.7 3.6 4.2	3.7 4.5	V
V_{OSR} Output voltage slew-rate			100		V/ms
V_{sens} Sens voltage range		0		0.7	V

THERMAL SHUTDOWN

T_j Junction temperature		150			$^{\circ}\text{C}$
T_H Hysteresis				30	$^{\circ}\text{C}$



DESCRIPTION

The L6230 is a three-phase brushless motor driver IC containing all the power stages and commutation logic required for a three-phase bidirectional drive.

Logic signals from the motor's Hall effect sensors are decoded to generate the correct driving sequence according to the truth-table of Fig. 1.

The direction of rotation is controlled by the forward/reverse input (pin 1). When this pin is at a low level the motor rotates in the forward direction.

When one of the push-pull output drivers is activated the upper transistor is always in saturation while the lower transistor is controlled in linear mode to set the desired speed in steady state conditions.

In PLL speed control applications the device provides a signal proportional to the motor speed at pin 2 (it is the buffered H1 input). The output of the PLL is connected to the speed control input on the device at pin 10, V_C .

In addition, a 1V offset is added to the speed demand voltage to match the minimum output of the PLL.

An external resistor, R_s , senses the output stage current. The sensing voltage across this resistor is amplified in the device by a factor of 7 to allow a reduction in the voltage drop in the resistor.

The amplified sensing voltage is then compared with the speed demand signal from the PLL and the resulting error signal sets the amplifier output accordingly.

The output current is related to the speed control voltage by:

$$I_o = (V_C - 1) / 7 R_s$$

The value of the sensing resistor is given by:

$$R_s = (V_X - 1) / (7 I_{max})$$

where V_X is the full scale voltage of V_C (see fig. 2).

In this way the V_C/I_{out} characteristics can be modified as shown in Fig. 2. Note that V_X max is clamped at 5.9V.

The most important feature of the L6230 is slew rate control. With this device a typical value of 0.1V/ μ s is achieved, reducing EMI to a very low value.

In a delta configuration a key feature is three-state operation; when the current is recirculating the corresponding phase driver is switched off and power dissipation is negligible. Current recirculates through the integrated free-wheeling diodes in the acceleration phase and through the motor in steady-state conditions. Torque ripple is also minimized.

The L6230 can also operate with a brushless motor connected in a star configuration, leaving the center floating.

The Hall inputs are ground compatible comparators and can work with direct active digital Hall signals on three terminals (of the same polarity) and a TTL level on the other three terminals.

Fig. 1 - TRUTH TABLE FOR FORWARD ROTATION

HALL EFFECT DIFF. INPUT 1 = POSITIVE 0 = NEGATIVE			UPPER DRIVER STATUS 1 = ON 0 = OFF			LOWER DRIVER STATUS 1 = ON 0 = OFF		
H1	H2	H3	UD1	UD2	UD3	LD1	LD2	LD3
1	0	0	1	0	0	0	0	1
1	1	0	0	1	0	0	0	1
1	1	1	0	1	0	1	0	0
0	1	1	0	0	1	1	0	0
0	0	1	0	0	1	0	1	0
0	0	0	1	0	0	0	1	0

Fig. 2 – Output current vs. control voltage

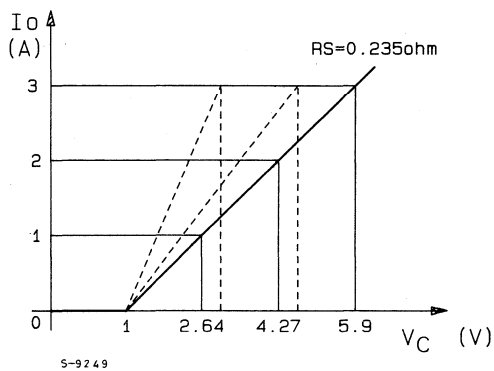
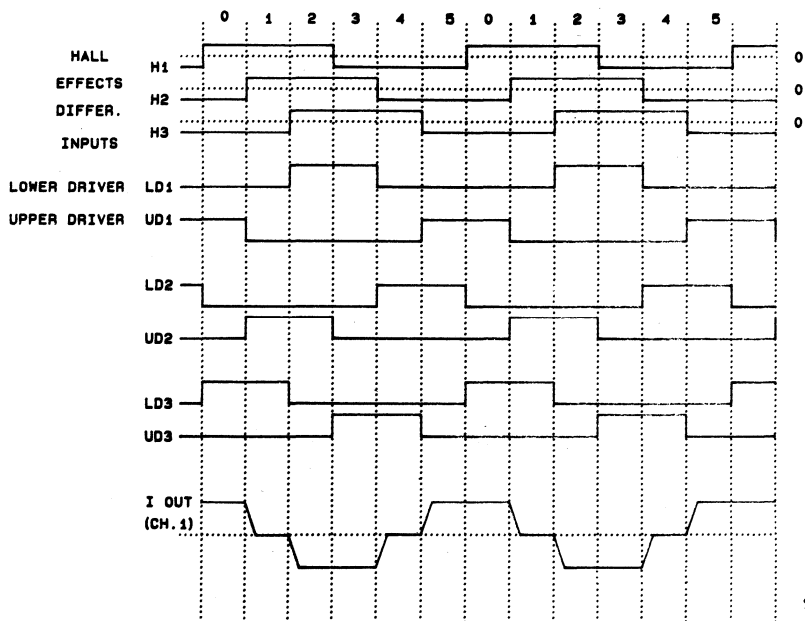


Fig. 3 – Timing diagram

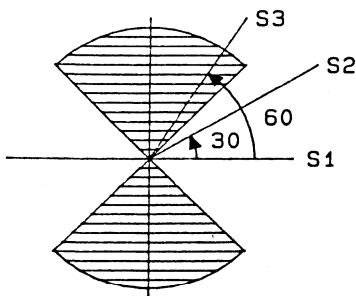


DETERMINING HALL EFFECT SENSOR CODING

The L6230 assumes that the positioning of the Hall Effect sensors in a three-phase brushless DC bipolar motor are at 30 intervals. One can imagine two "windows" on the rotor each of which is 90 wide and 180 apart, see fig. 4. As a window passes over a sensor, the sensor output goes high. The timing diagram, fig. 3, shows the waveforms produced. These waveforms must appear at the Hall Effect Inputs of the L6230. Note that the rotation in fig. 4 must be counter-clockwise for forward rotation of the motor in whatever manner that is defined for the motor.

Fig. 4 is a stylized concept for determining the Hall Effect code pattern and does not reflect the actual direction of rotation of the motor in a physical sense. If a motor is chosen whose sensor outputs do not match the L6230 desired input pattern, a signal set conversion must be determined. It is helpful to visualize this by developing a diagram similar to that of fig. 4.

Fig. 4



For example, let us examine the output pattern of a different type of motor (fig. 5). Assuming 90 windows at 180 intervals, then with respect to fig. 4, a similar diagram, fig. 6, results in sensors 60 apart with the windows rotating clockwise. This situation results in a "forward" rotation of the motor.

Since S3 is the first sensor encountered by the window in fig. 6, this should be used for the L6230 Hall Effect Input, H1. After 30 of rotation CW, the H2 input of the L6230 must go

high. The inverse of S1 from the motor would satisfy this. After an additional 30 of rotation, the H3 input must go high. The S2 sensor is encountered by the window. Thus, S2 is applied to this input, H3. By continuing around the diagram, one can develop a pattern which matches that for the L6230.

Fig. 5

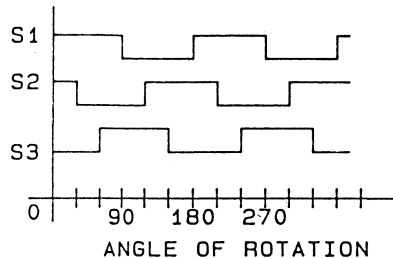
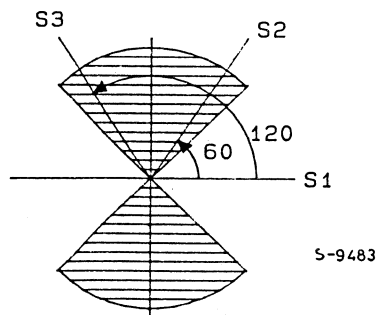


Fig. 6



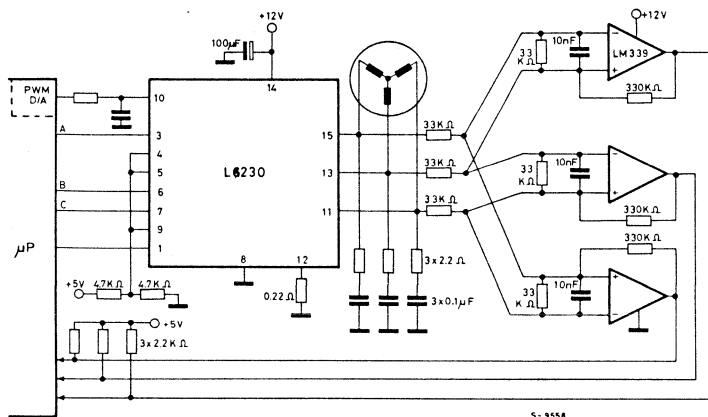
Thus, the conversion table for this particular motor is:

Motor Sensors	L6230 Inputs
S3	H1
S1	H2
S2	H3

Note, for the inverted signal from S1 an actual inverter gate is not necessary with the L6230. Since the L6230 has differential inputs, the negative input pin may be used. Therefore, with TTL compatible Hall Effect sensors, the positive input is connected to a reference point along with the other negative inputs.

APPLICATION INFORMATION

Fig. 7 – Brushless motor control without hall sensors



L6230 can be adapted to a brushless motor without Hall sensors.

The circuit detects after filtering the back EMF of the motor and use this signal for commutation. This application needs a μP to start up the motor with a rotating clock pulse on the outputs until the back EMF is present.

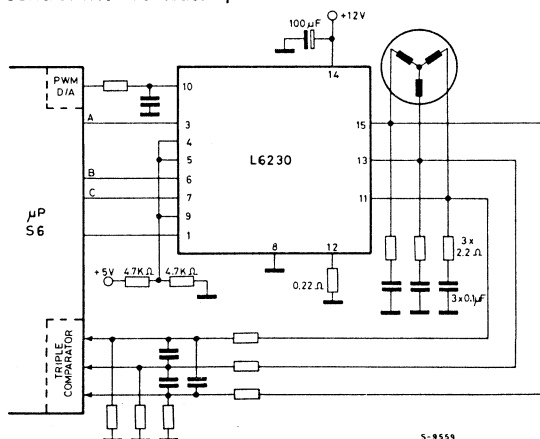
The μP can also provide the speed regulation loop by software. For a quick performance test

of application, it's possible to interconnect the comparator outputs directly to the L6230 inputs. In this case a manual start up is needed.

By using S6 μP with a dedicated ADC or comparator inputs, only passive external components are required.

A discussion with a motor producer give us the information, the cost of 3 phase hall sensors including assembly are in the range of 3 to 4 DM.

Fig. 8 – Brushless motor control with dedicated μP





L6231

ADVANCE DATA

THREE-PHASE BRUSHLESS DC MOTOR DRIVER

- 3A OUTPUT CURRENT, CONTROLLED IN LINEAR MODE
- SUPPLY VOLTAGE UP TO 18V
- COMPATIBLE WITH ANI F-TO-V CONVERTER AND PLL SPEED CONTROL SYSTEM
- INHIBIT FUNCTION
- SLEW RATE LIMITING FOR EMI REDUCTION
- CONNECTS DIRECTLY TO HALL EFFECT CELLS
- THERMAL SHUTDOWN WITH HYSTERESIS
- THREE-STATE OPERATION ALLOWS NEGLIGIBLE POWER DISSIPATION DURING 1/3f CYCLE
- INTERNAL PROTECTION DIODES
- FEW EXTERNAL COMPONENTS

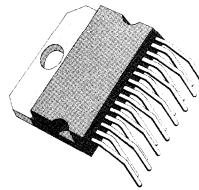
The L6231 is a single-chip driver for three-phase brushless DC motors capable of delivering 3A output current with supply voltages to 18V. Designed to accept differential input from the Hall effect sensors, the device drives the three phases of a brushless DC motor and includes all the commutation logic required for a three phase drive.

To limit EMI emission the L6231 controls the rise and fall times of the output stage. In ad-

dition the device is designed to limit power dissipation: during recirculation the output stage is switched to an off state, reducing dissipation to a very low value and minimizing torque ripple.

A speed control input controls the base current to the lower transistors to limit the motor current and hence control the speed. Any type of speed control system, including F to V and PLL systems, may be used with the L6231 by providing an analog signal at this input. The motor current may be sensed by an external resistor connected to a sensing pin on the device.

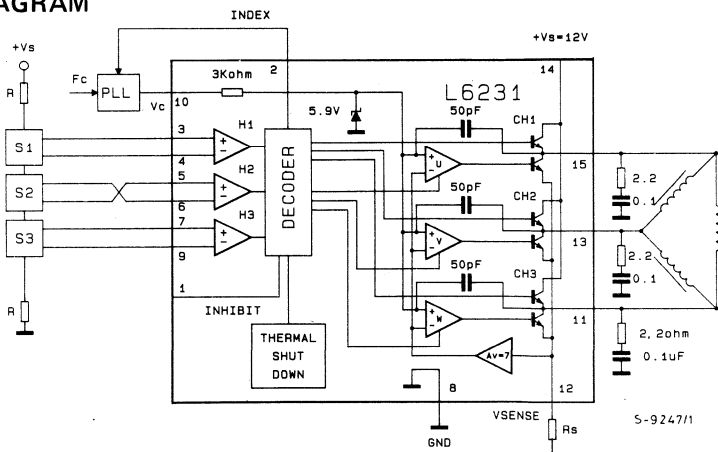
The power stage of the device is designed to eliminate the possibility of simultaneous conduction of the upper and lower power transistors of one output driver, when operating in the right loop.



**Multiwatt-15
(Horizontal)**

ORDERING NUMBER: L6231H

BLOCK DIAGRAM



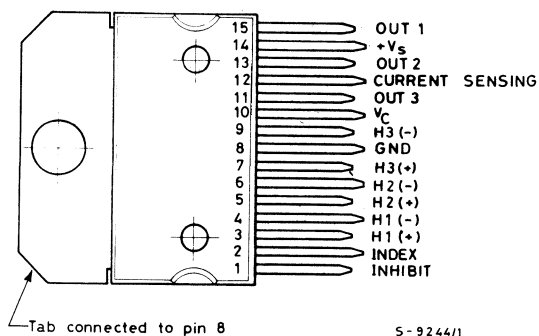


L6231

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
I_o	Peak output current each channel		
	– non repetitive (100 μ s)	4	A
	– repetitive (t = 10ms)	3.5	A
	– DC operation	3	A
V_I	Logic and analogic inputs	V_s	
P_{tot}	Total power dissipation $T_{case} = 75^\circ\text{C}$	25	W
T_{op}	Operating temperature range	0 to 70	$^\circ\text{C}$
T_j, T_{stg}	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

CONNECTION DIAGRAM (Top view)



THERMAL DATA

$R_{th j-case}$	Thermal resistance junction-case	max	3	$^\circ\text{C/W}$
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**L6231****PIN FUNCTIONS**

N°	NAME	I/O	FUNCTION
1	INHIBIT	I	Output stage inhibit. When this pin is high all three output stages are in a high impedance state!
2	INDEX	O	Signal pulse proportional to the motor speed. In PLL speed control applications, this is the feedback to the PLL. One pulse per electrical rotation. This is an open collector output.
3	H1 (+)	I	Positive input of differential amplifier on channel 1. Interfaces with Hall Effect sensor, S1, from motor.
4	H1 (-)	I	Negative input of differential amplifier on channel 1. Interfaces with Hall Effect sensor, S1, from motor.
5	H2 (+)	I	Same as pin 3 for channel 2.
6	H2 (-)	I	Same as pin 4 for channel 2.
7	H3 (+)	I	Same as pin 3 for channel 3.
8	GND		Ground connection.
9	H3 (-)	I	Same as pin 4 for channel 3.
10	V _c	I	Speed control input. Connected to output of PLL in PLL speed control applications.
11	Out 3	O	Output motor drive for phase 3.
12	Sense	I	Current Sensing. Input for load current sense voltage for output stage.
13	Out 2	O	Output motor drive for phase 2.
14	V _s		Motor supply voltage.
15	Out 1	O	Output motor drive for phase 1.

**L6231****ELECTRICAL CHARACTERISTICS** ($T_{amb} = 25^{\circ}\text{C}$; $V_s = 12\text{V}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s Supply voltage		10	12	18	V
I_s Quiescent supply current			60	100	mA

HALL AMPLIFIERS

V_{CM} Common mode voltage range		0		10	V
V_{IO} Input offset voltage	$V_I = 6\text{V}$		2	10	mV
I_{IB} Input bias current	$V_I = 6\text{V}$		2	10	μA
I_{IO} Input offset current	$V_I = 6\text{V}$		0.1		μA

SPEED CONTROL INPUT (V_C)

V_I Input voltage range		0		5	V
I_{IB} Input bias current	$V_C < V_{sens}$		1	5	μA
V_{IC} Input clamping voltage			5.9		V

INHIBIT INPUT

V_{IH} Input high voltage		2		V_s	V
V_{IL} Input low voltage		0		0.8	V
I_{IH} Input high current				10	μA
I_{IL} Input low current			-5	-50	μA

HALL LOGIC OUTPUT

V_{LO} Low output voltage	$I = 5\text{mA}$			0.8	V
I_L Leakage current	$V_{CE} = 12\text{V}$			10	μA

OUTPUT POWER STAGE

V_{sat} Total saturation voltage	$I_o = 1\text{A}$ $I_o = 2\text{A}$ $I_o = 3\text{A}$		2.7 3.6 4.2	3.7 4.5	V
V_{OSR} Output voltage slew-rate			100		V/ms
V_{sens} Sens voltage range		0		0.7	V

THERMAL SHUTDOWN

T_j Junction temperature		150			$^{\circ}\text{C}$
T_H Hysteresis				30	$^{\circ}\text{C}$



DESCRIPTION

The L6231 is a three-phase brushless motor driver IC containing all the power stages and commutation logic required for a three-phase drive. When the INHIBIT INPUT is high all three OUTPUTS ARE PLACED in a high - IMPEDANCE STATE.

Logic signals from the motor's Hall effect sensors are decoded to generate the correct driving sequence according to the truth-table of Fig. 1.

When one of the push-pull output drivers is activated the upper transistor is always in saturation while the lower transistor is controlled in linear mode to set the desired speed in steady state conditions.

In PLL speed control applications the device provides a signal proportional to the motor speed at pin 2 (it is the buffered H1 input). The output of the PLL is connected to the speed control input of the device at pin 10, V_C .

In addition, a 1V offset is added to the speed demand voltage to match the minimum output of the PLL.

An external resistor, R_s , senses the output stage current. The sensing voltage across this resistor is amplified in the device by a factor of 7 to allow a reduction in the voltage drop the resistor.

The amplified sensing voltage is then compared with the speed demand signal from the PLL and the resulting error signal sets the amplifier output accordingly.

The output current is related to the speed control voltage by:

$$I_o = \frac{(V_C - 1)}{7 R_s}$$

The value of the sensing resistor is given by:

$$R_s = (V_X - 1)/(7 I_{\max})$$

where V_X is the full scale voltage of V_C (see fig. 2).

In this way the V_C/I_{out} characteristics can be modified as shown in Fig. 2. Note that V_X max is clamped at 5.9V.

The most important feature of the L6231 is slew rate control. With this device a typical value of $0.1V/\mu s$ is achieved, reducing EMI to a very low value.

Another key feature is three-state operation; when the current is recirculating the corresponding phase driver is switched off and power dissipation is negligible. Current recirculates through the free-wheeling diodes in the acceleration phase and through the motor in steady-state conditions. Torque ripple is also minimized.

The L6231 can also operate with a brushless motor connected in a star configuration, leaving the center floating.

The Hall inputs are ground compatible comparators and can work with direct active digital Hall signals on three terminals (of the same polarity) and a TTL level on the other three terminals.

Fig. 1 - TRUTH TABLE

HALL EFFECT DIFF. INPUT 1 = POSITIVE 0 = NEGATIVE			UPPER DRIVER STATUS 1 = ON 0 = OFF			LOWER DRIVER STATUS 1 = ON 0 = OFF		
H1	H2	H3	UD1	UD2	UD3	LD1	LD2	LD3
1	0	0	0	0	1	1	0	0
1	1	0	0	0	1	0	1	0
1	1	1	1	0	0	0	1	0
0	1	1	1	0	0	0	0	1
0	0	1	0	1	0	0	0	1
0	0	0	0	1	0	1	0	0

Fig. 2 - Output current vs. input voltage

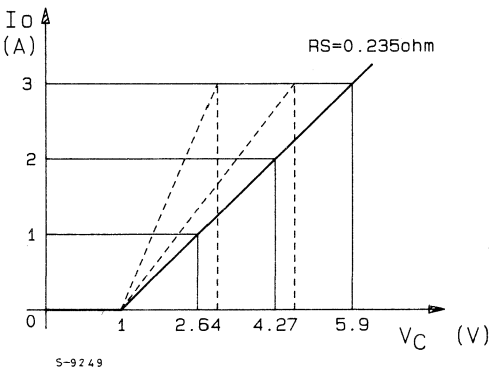
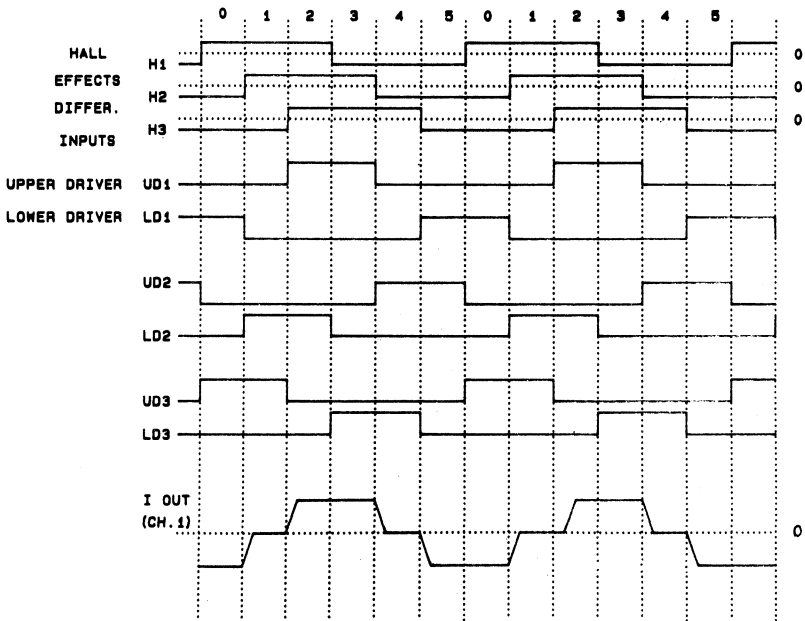


Fig. 3 - Timing diagram

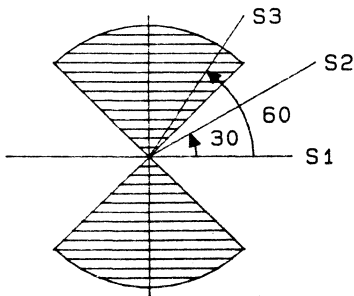


DETERMINING HALL EFFECT SENSOR CODING

The L6231 assumes that the positioning of the Hall Effect sensors in a three-phase brushless DC bipolar motor are at 30 intervals. One can imagine two "windows" on the rotor each of which is 90 wide and 180 apart, see fig. 4. As a window passes over a sensor, the sensor output goes high. The timing diagram, fig. 3, shows the waveforms produced. These waveforms must appear at the Hall Effect Inputs of the L6231. Note that the rotation in fig. 4 must be counter-clockwise for forward rotation of the motor in whatever manner that is defined for the motor.

Fig. 4 is a stylized concept for determining the Hall Effect code pattern and does not reflect the actual direction of rotation of the motor in a physical sense. If a motor is chosen whose sensor outputs do not match the L6231 desired input pattern, a signal set conversion must be determined. It is helpful to visualize this by developing a diagram similar to that of fig. 4.

Fig. 4



For example, let us examine the output pattern of a different type of motor (fig. 5). Assuming 90 windows at 180 intervals, then with respect to fig. 4, a similar diagram, fig. 6, results in sensors 60 apart with the windows rotating clockwise. This situation results in a "forward" rotation of the motor.

Since S3 is the first sensor encountered by the window in fig. 6, this should be used for the L6231 Hall Effect Input, H1. After 30 of rotation CW, the H2 input of the L6231 must go

high. The inverse of S1 from the motor would satisfy this. After an additional 30 of rotation, the H3 input must go high. The S2 sensor is encountered by the window. Thus, S2 is applied to this input, H3. By continuing around the diagram, one can develop a pattern which matches that for the L6231.

Fig. 5

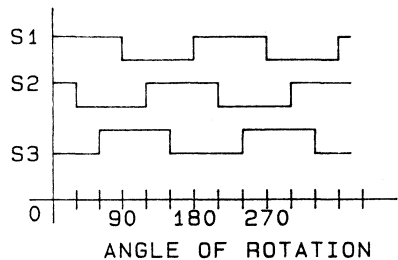
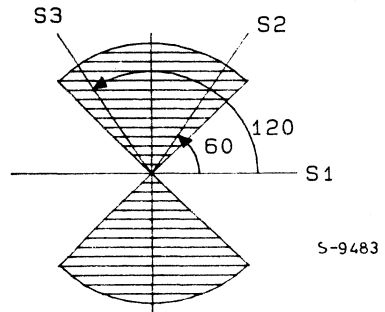


Fig. 6



Thus, the conversion table for this particular motor is:

Motor Sensors	L6231 Inputs
S3	H1
S1	H2
S2	H3

Note, for the inverted signal from S1 an actual inverter gate is not necessary with the L6231. Since the L6231 has differential inputs, the negative input pin may be used. Therefore, with TTL compatible Hall Effect sensors, the positive input is connected to a reference point along with the other negative inputs.



L6233

ADVANCE DATA

PHASE LOCKED FREQUENCY CONTROLLER

- PRECISION PHASE LOCKED FREQUENCY CONTROL SYSTEM
- XTAL OSCILLATOR
- PROGRAMMABLE REFERENCE FREQUENCY DIVIDERS
- PHASE DETECTOR WITH ABSOLUTE FREQUENCY STEERING
- DIGITAL LOCK INDICATOR
- DOUBLE EDGE OPTION ON THE FREQUENCY FEEDBACK SENSE AMPLIFIER
- TWO HIGH CURRENT OP-AMPS
- 5V REFERENCE OUTPUT

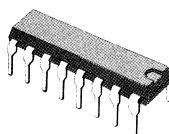
The L6233 is designed for use in phase locked frequency control loops. While optimized for precision speed control of DC motors, these device is universal enough for most applications that require phase locked control. A precise reference frequency can be generated using the device's high frequency oscillator and programmable frequency dividers. The oscillator operates using a broad range of crystals, or, can function as a buffer stage to an external frequency source.

The phase detector on these integrated circuit compares the reference frequency with a frequency/phase feedback signal. In the case of a motor, feedback is obtained at a hall output or other speed detection device. This signal is buffered by a sense amplifier that squares up the

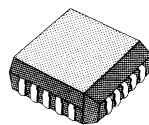
signal as it goes into the digital phase detector. The phase detector responds proportionally to the phase error between the reference and the sense amplifier output. This phase detector includes absolute frequency steering to provide maximum drive signals when any frequency error exists. This feature allows optimum start-up and lock times to be realized.

Two op-amps are included that can be configured to provide necessary loop filtering. The outputs of these op-amps will source or sink in excess of 16mA, so they can provide a low impedance control signal to driving circuits.

Additional features include a double edge option on the sense amplifier that can be used to double the loop reference frequency for increased loop bandwidths. A digital lock signal is provided that indicates when there is zero frequency error and a 5V reference output allows DC operating levels to be accurately set.



DIP-16 Plastic (0.25)

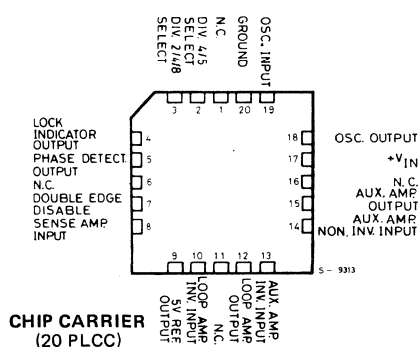
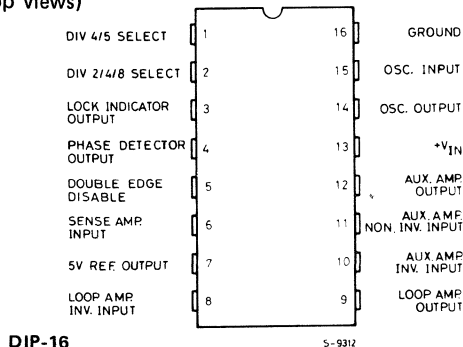


20 PLCC

ORDERING NUMBERS: L6233 (DIP-16)
L6233P (20 PLCC)

CONNECTION DIAGRAMS

(Top views)



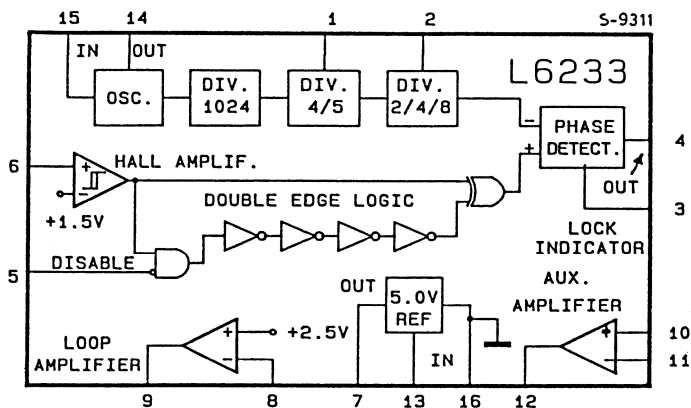


L6233

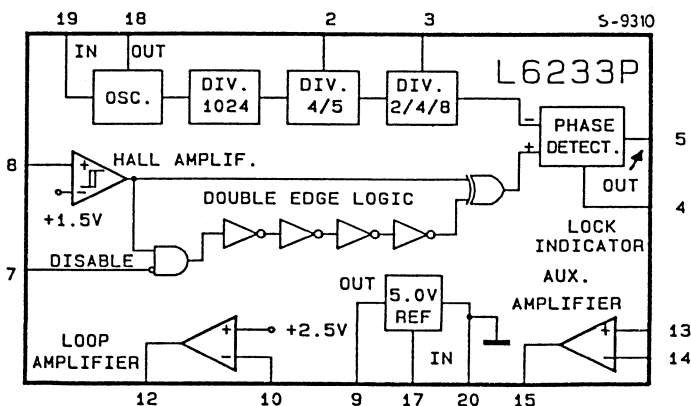
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	14	V
P_{tot}	Power dissipation ($T_{amb} \leq 70^\circ\text{C}$)	1	W
T_{op}	Operating temperature range	0 to 70	$^\circ\text{C}$
T_{stg}	Storage temperature	-65 to 150	$^\circ\text{C}$

BLOCK DIAGRAMS (DIP-16)



(PLCC PACKAGE)



**L6233**

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, specifications hold for $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$; $V_{IN} = 12\text{V}$)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_S Supply current			20		mA

REFERENCE

V_{REF} Output voltage		4.75	5.0	5.25	V
ΔV_{REF} Load Regulation	$I_{OUT} = 0$ to 7mA		5.0	20	mV
ΔV_{REF} Line regulation	$+V_{IN} = 8$ to 12V		2.0	20	mV
I_{SC} Short circuit current	$V_{OUT} = 0\text{V}$		35		mA

OSCILLATOR

G_V DC voltage gain	Oscillator input to oscillator output		16		dB
V_{IB} Input DC level	Oscillator input pin open, $T_J = 25^{\circ}\text{C}$		1.3		V
Z_{IN}^* Input impedance	$V_{IN} = V_{IB} \pm 0.5\text{V}$, $T_J = 25^{\circ}\text{C}$		1.6		$\text{K}\Omega$
V_O Output DC level	Oscillator input pin open $T_J = 25^{\circ}\text{C}$		1.4		V
f_{oMAX} Maximum operating frequency		10			MHz

DIVIDERS

f_{oMAX} Maximum input frequency	Input = $1V_{pp}$ at oscillator input	10			MHz
Div. 4/5 input current	Input = 5V (Div. by 4)		150	500	μA
	Input = 0V (Div. by 5)	-5.0	0.0	5.0	μA
V_{TH} Div. 4/5 threshold		0.5	1.6	2.2	V
Div. 2/4/8 input current	Input = 5V (Div. by 8)		150	500	μA
	Input = 0V (Div. by 2)	-500	-150		μA
Div. 2/4/8 open circuit voltage	Input current = $0\mu\text{A}$ (Div. by 4)	1.5	2.5	3.5	V
Div. by 2 threshold		0.35	0.8		V
Div. by 4 threshold		1.5		3.5	V
Div. by 8 threshold	Volts below V_{REF}	0.35	0.8		V

SENSE AMPLIFIER

V_T Threshold voltage	Percent of V_{REF}		30		%
H_T Threshold hysteresis			10		mV
I_B Input bias current	Input = 1.5V		-0.2		μA

DOUBLE EDGE DISABLE INPUT

V_I Input current	Input = 5V (Disabled)		150	500	μA
	Input = 0V (Enabled)	-5.0	0.0	5.0	μA
V_T Threshold voltage		0.5	1.6	2.2	V

**L6233****ELECTRICAL CHARACTERISTICS** (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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PHASE DETECTOR

V _{OH}	High output level	Positive Phase/Freq. Error, Volts Below V _{REF}		0.2	0.5	V
V _{OL}	Low output level	Negative Phase/Freq. Error		0.2	0.5	V
V _{OM}	Mid output level	Zero Phase/Freq. Error, Percent of V _{REF}	47	50	53	%
	High level maximum source current	V _{OUT} = 4.3V	2.0	8.0		mA
	Low level maximum sink curr.	V _{OUT} = 0.7V	2.0	5.0		mA
	Mid level output impedance (Note 2)	I _{OUT} = -200 to +200μA T _j = 25°C		6.0		KΩ

LOCK INDICATOR OUTPUT

V _{sat}	Saturation voltage	Freq. Error, I _{OUT} = 5mA		0.3	0.45	V
	Leakage current	Zero Freq. Error V _{OUT} = 12V		0.1	1.0	μA

LOOP AMPLIFIER

	NON INV. reference voltage	Percent of V _{REF}	47	50	53	%
I _b	Input bias current	Input = 2.5V	-0.8	-0.2		μA
G _v	Open loop gain		60	75		dB
SVR	Supply voltage rejection	+V _{IN} = 8 to 12V	70	100		dB
I _{SH}	Short circuit current	Source, V _{OUT} = 0V	16	35		mA
		Sink, V _{OUT} = 5V	16	30		mA

AUXILIARY OP-AMP

V _{OS}	Input offset voltage	V _{CM} = 2.5V			8	mV
I _b	Input bias current	V _{CM} = 2.5V		200		mA
I _{os}	Input offset current	V _{CM} = 2.5V		10		mA
G _v	Open loop gain		70	120		dB
SVR	Supply voltage rejection	+V _{IN} = 8 to 12V	70	100		dB
CMR	Common mode rejection	V _{CM} = 0 to 10V	70	100		dB
I _{SH}	Short circuit current	Source, V _{OUT} = 0V		35		mA
		Sink, V _{OUT} = 5V		30		mA

* These impedance levels will vary with T_j at about 1700ppm/°C**THERMAL DATA**

R _{thj-amb}	Thermal resistance junction-ambient	max	100	°C/W
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APPLICATION INFORMATION

Determining the Oscillator Frequency

The frequency at the oscillator is determined by: the desired RPM of the motor, the divide ratio selected, the number of poles in the motor, and the state of the double edge select pin.

$$f_{osc} \text{ (Hz)} = (\text{Divide Ratio}) \cdot (\text{Motor RPM}) \cdot (1/60 \text{ SEC/MIN}) \cdot (\text{No. of Rotor Poles}/2) \cdot (\times 2 \text{ if Pin 5 Low})$$

The resulting reference frequency appearing at the phase detector inputs is equal to the oscillator frequency divided by the selected divide ratio. If the double edge option is used, (Pin 5 low), the frequency of the sense amplifier input signal is doubled by responding to both the rising and falling edges of the input signal. Using this option the loop reference frequency can be doubled for a given motor RPM.

Fig. 1 - Recommended Oscillator Configuration Using AT Cut Quartz XTAL

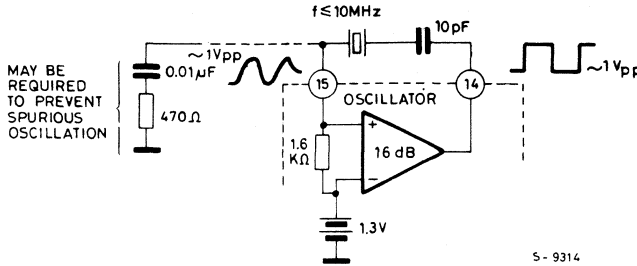


Fig. 2 - External Reference Frequency Input

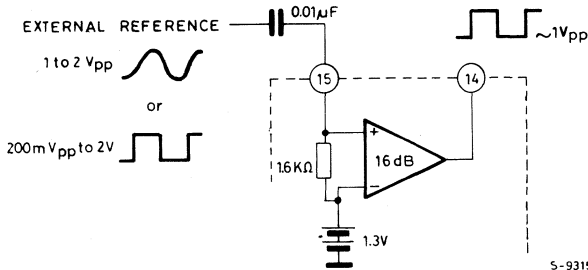
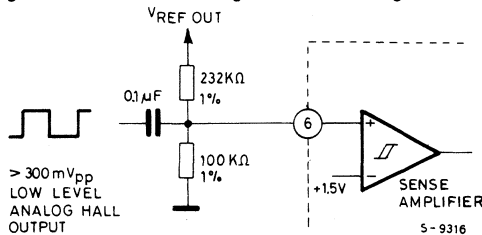


Fig. 3 - Method for Deriving Rotation Feedback Signal From Analog Hall Effect Device



* This signal may require filtering if chopped mode drive scheme is used.

APPLICATION INFORMATION (continued)

Phase detector operation

The phase detector on these devices is a digital circuit that responds to the rising edges of the detector's two inputs. The phase detector output has three states: a high, 5V state, a low, 0V state, and a middle, 2.5V state. In the high and low states the output impedance of the detector is low, the middle state output impedance is high, typically 6.0K Ω . When there is any static frequency difference between the inputs the detector output is fixed at its high level if the +input (the sense amplifier signal) is greater in frequency, and fixed at its low level if the -input (the reference frequency signal) is greater in frequency.

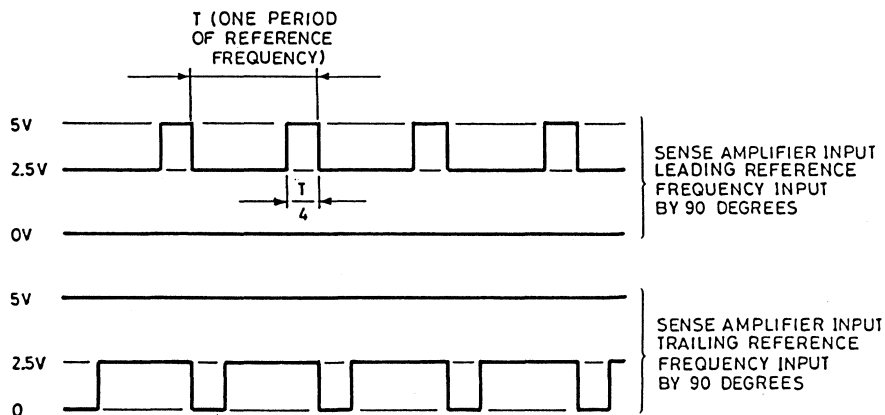
When the frequencies of the two inputs to the detector are equal the phase detector switches between its middle state and either the high or low states, depending on the relative phase of the two signals. If the +input is leading in phase then, during each period of the input frequency, the detector output will be high for a time equal to the time difference between the rising edges of the inputs, and will be at its middle level the remainder of the period. If the phase relationship is reversed then the detector will go low for a time proportional to the phase difference of the inputs. The resulting gain of the

phase detector, $K\phi$, is $5V/4\pi$, radians, or about 0.4V/radian. The dynamic range of the detector is $\pm 2\pi$ radians.

The operation of the phase detector is illustrated in the figures below. The upper figure shows typical voltage waveforms seen at the detector output for leading and lagging phase conditions. The lower figure is a state diagram of the phase detector logic. In this figure, the circles represent the 10 possible states of the logic and the connecting arrows the transition events/paths to and from these states. Transition arrows that have a clockwise rotation are the result of a rising edge on the +input, and conversely, those with counter-clockwise rotation are tied to the rising edge on the -input signal.

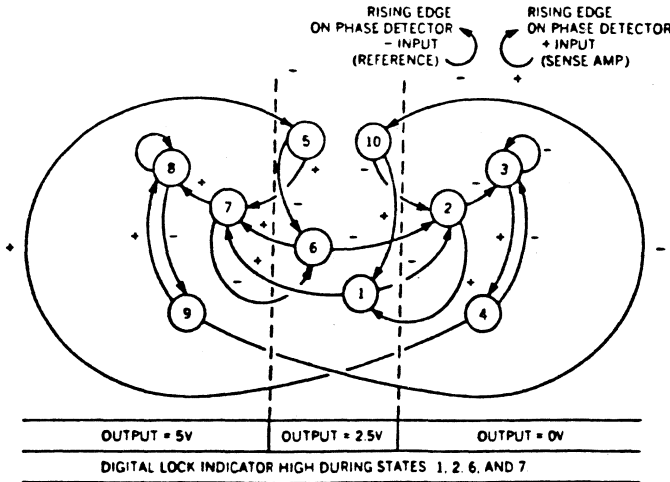
The normal operational states of the logic are 6 and 7 for positive phase error, 1 and 2 for a negative phase error. States 8 and 9 occur during positive frequency error, 3 and 4 during negative frequency error. States 5 and 10 occur only as the inputs cross over from a frequency error to a normal phase error only condition. The level of the phase detector output is determined by the logic state as defined in the state diagram figure. The lock indicator output is high, off, when the detector is in states 1, 2, 6 or 7.

Fig. 4 - Typical Phase Detector Output Waveforms



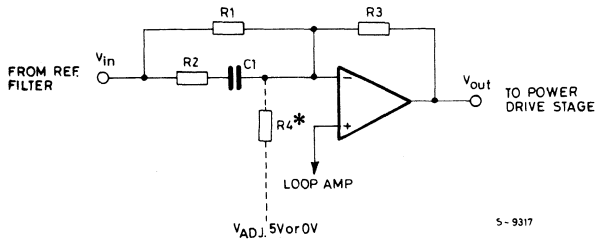
S-9319

Fig. 5 - Phase Detector State Diagram



S-9421

Fig. 6 - Suggested Loop Filter Configuration



S-9317

$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{R_3}{R_1} \cdot \frac{1 + S/\omega P}{1 + S/\omega Z}$$

$$\omega P = \frac{1}{R_2 C_1}$$

$$\omega Z = \frac{1}{(R_1 + R_2) C_1}$$

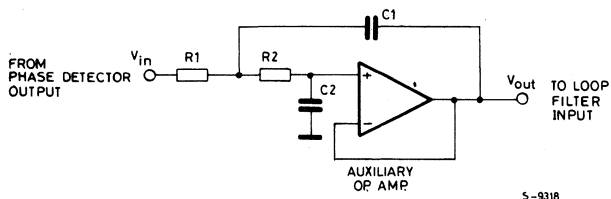
Where: $|\Delta V_{OUT}| = |V_{OUT} - 2.5V|$
and V_{OUT} = DC Operating Voltage At Loop Amplifier Output During Phase Lock

* The statistic phase error of the loop is easily adjusted by adding resistor, R_4 , as shown. To lock at zero phase error R_4 is determined by:

$$R_4 = \frac{2.5V \cdot R_3}{|\Delta V_{OUT}|}$$

$(V_{OUT} - 2.5) > 0$ R_4 Goes to 0V
 $(V_{OUT} - 2.5) < 0$ R_4 Goes to 5.0V

Fig. 7 - Reference Filter Configuration



S-9318

$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{1}{1 + \frac{S^2}{\omega_N} + \frac{S^2}{\omega_N^2}}$$

$$\omega_N = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$\delta = \frac{1}{2Q} = \frac{1}{2} \sqrt{\frac{C_2}{C_1}} \sqrt{\frac{R_1 + R_2}{R_1 R_2}}$$

Note: with $R_1 = R_2$ $\delta = \sqrt{\frac{C_2}{C_1}}$

Fig. 8 - Reference Filter Design Aid - Gain Response

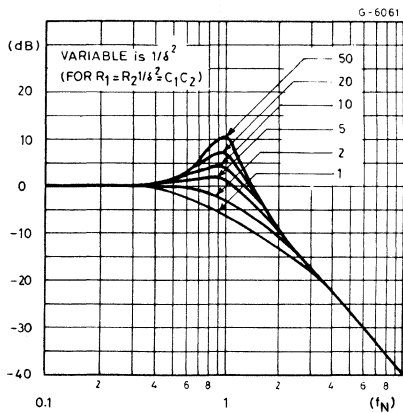
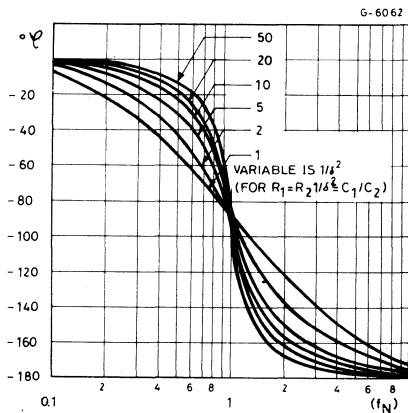


Fig. 9 - Reference Filter Design Aid - Phase Response





L6503

ADVANCE DATA

HAMMER SOLENOID CONTROLLER

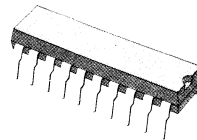
- DRIVES FOUR DARLINGTONS WITH UP TO 2.5mA DRIVE CURRENT
- FEEDBACK LOOP CONTROLS DARLINGTON CURRENT
- PRESETTABLE CONDUCTION TIME
- LATCHED μ C-COMPATIBLE INPUTS
- DIAGNOSTIC CIRCUITRY

Designed primarily for solenoid driving applications, the L6503 Hammer Solenoid Controller includes all the circuitry needed to control four darlington power devices or a quad darlington array such as the SGS L7180.

The device is controlled by four latched logic inputs, which may be connected directly to a microcomputer chip, plus an analog input which sets the load current. Additionally, the conduction time of the outputs is controlled by a clock input which drives internal timers.

Fault conditions may be detected thanks to diagnostic circuitry which allows the control micro to read (serially) the load current status of the external darlington.

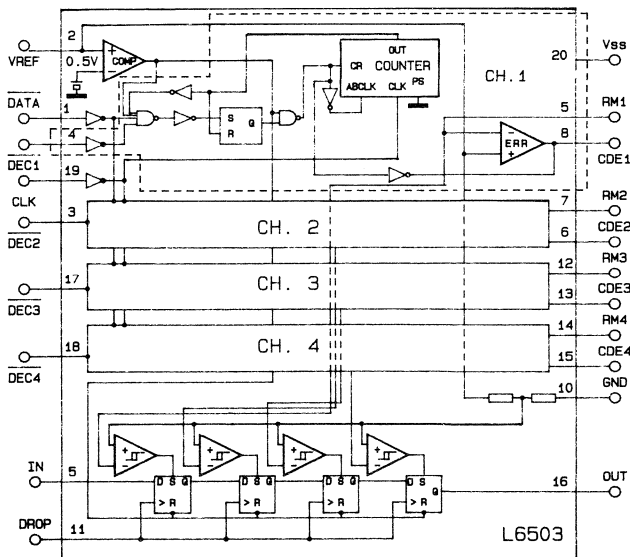
Assembled in a 20-pin DIP package, the L6503 operates on a single 5V supply and is suitable for computer printers, solenoid valves and similar applications.



DIP-20 Plastic
(X3P2)

ORDERING NUMBER: L6503

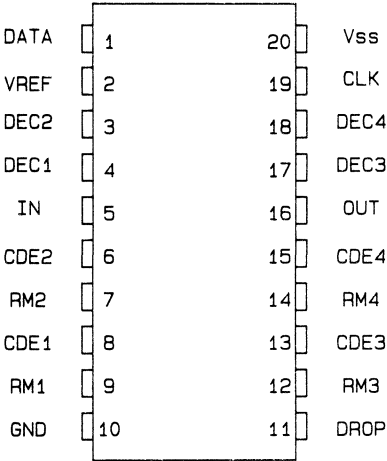
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{ss}	Supply voltage	7	V
I_{CDE}	Output current	10	mA
V_i	Input voltage (for analog and logic inputs)	0 to $V_{ss} - 0.5$	V
T_{op}	Operating temperature	0 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM
(Top view)



S-9273

THERMAL DATA

$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	80	°C/W
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**PIN FUNCTION DESCRIPTION**

N°	NAME	FUNCTION
1	$\overline{\text{DATA}}$	Latches control command into the four inputs DEC1-DEC4 on the high-low transition.
2	V_{ref}	Analog reference input which sets the load current for all four channels; when lower than 0.5V resets the logic circuitry.
3	$\overline{\text{DEC2}}$	Data input for channel 2. Data is latched on the high-low transition of the DATA input.
4	$\overline{\text{DEC1}}$	Data input for channel 1.
5	IN	Input for diagnostic shift register used to cascade several device.
6	CDE2	Channel 2 output (connect to base of darlington). Up to 2.5mA drive.
7	RM2	Feedback input from sensing resistor of channel 2 darlington.
8	CDE1	Channel 1 output.
9	RM1	Feedback input for channel 1 sense resistor.
10	GND	Ground.
11	DROP	Clock input for diagnostic register.
12	RM3	Feedback input for channel 3 sense resistor.
13	CDE3	Channel 3 output.
14	RM4	Feedback input for channel 4 sense resistor.
15	CDE4	Channel 4 output.
16	OUT	Output of diagnostic register.
17	$\overline{\text{DEC3}}$	Input for channel 3.
18	$\overline{\text{DEC4}}$	Input for channel 4.
19	CLK	Input for clock signal which sets conduction time for all four channels. $T_{\text{on}} = 128/f_{\text{CLK}}$.
20	V_{ss}	5V supply input voltage.

ELECTRICAL CHARACTERISTICS ($V_{SS} = 5V$, $T_{amb} = 25^{\circ}C$, unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SS} Supply voltage	$T_j = 0 \text{ to } 70^{\circ}C$	4.75	5	5.25	V
I_{SS} Total supply current	$I_{CDE} = 2mA$ all channels on		75	90	mA
V_{REF} Input voltage reference		1		2.4	V
V_{REF} Reset logic function		0.3		0.65	V
I_{REF} Input BIAS reference current	$V_{REF} = 0 \text{ to } 2.4V$			-5	μA
V_i Input voltage (pin 1, 3, 4, 5, 11, 17, 18, 19)	V_{iL}			0.4	V
	V_{iH}	2.7			
V_{out} Output logic voltage (pin 16)	V_{OL} $I_{OUT} = +1.6mA$			0.4	V
	V_{OH} $I_{OUT} = -100\mu A$	2.7			
I_b Input bias current (pin 1, 3, 4, 5, 11, 17, 18, 19)	V_{iL}			-100	μA
	V_{iH}			± 10	
I_b Input bias current (pin 7, 9, 12, 14)	$1 \leq V_{RM} \leq 2.4V$			-100	μA
I_{CDE} Output current (pin 6, 8, 13, 15)	$V_{OUT} = V_{SS} - 0.5V$	2.5			mA
Output voltage range (pin 6, 8, 13, 15)	V_{OL}			0.2	V
	V_{OH}	$V_{SS} - 0.5$			
Error amplifier input offset voltage	$1V \leq V_{REF} \leq 2.4V$			± 10	mV

TIMING SECTION

Data ability time t		160			ns
Data to CDE delay time t1 (1)	$V_{RM} = 0V$		0.8	1.5	μs
Clock to CDE delay time t2 (1)	$V_{RM} = 0V$		7	10	μs
Reset time t3		1.9			μs
Reset to CDE delay time t4 (1)				1.3	μs
Clock frequency				100	KHz
Low level clock state t5 (1)		500			ns
RM to OUT delay time t6 (1)				3	μs
Drop frequency				500	KHz
Low level drop state t7		500			ns
Reset to output delay time t8 (1)				1.3	μs
Drop to in delay time t9 (1)				1.0	μs

(1) 100% Tested

FUNCTIONAL DESCRIPTION

The L6503 Hammer Solenoid Controller is designed to control a quad darlington array, such as the SGS L7180, in solenoid driving applications.

Compatible with 5V microcomputer and peripheral chips, the L6503 is controlled by four logic inputs - one per channel (DEC1-DEC4) - which are latched by a high-low transition on the DATA input.

When one of the channels is activated the corresponding darlington is driven, with up to 2.5mA drive current. The conduction period is determined by the frequency applied to the CLK input which clocks the 7-bit timer in each channel. The conduction time is therefore $128/fCLK$. Typically the CLK frequency will be of the order of 100KHz but the L6503's internal logic will operate at any clock rate within the range of practical conduction times.

During the conduction period the load current is controlled by feedback from a sense resistor in the darlington's emitter and set by the voltage applied to the V_{ref} input. The current depends on both the values of V_{ref} and the sensing resistor: $I = V_{ref}/R_{sense}$.

The control microcomputer may verify correct operation of the complete drive subsystem thanks to a diagnostic circuit in the L6503. A four bit PISO shift register in the device monitors the feedback signals from the four output darlington's and may be read serially after each command to check that the loads were driven.

Typically, this register, clocked by the DROP input, will be read a short time after each drive command has been latched into the device.

The input of this register (IN) is available externally so that multiple devices may be cascaded.

Fig. 1 - Application diagram

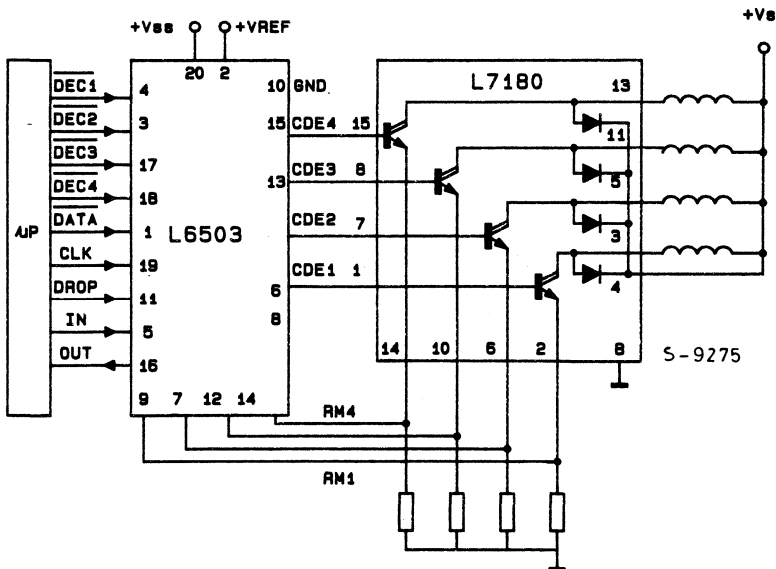
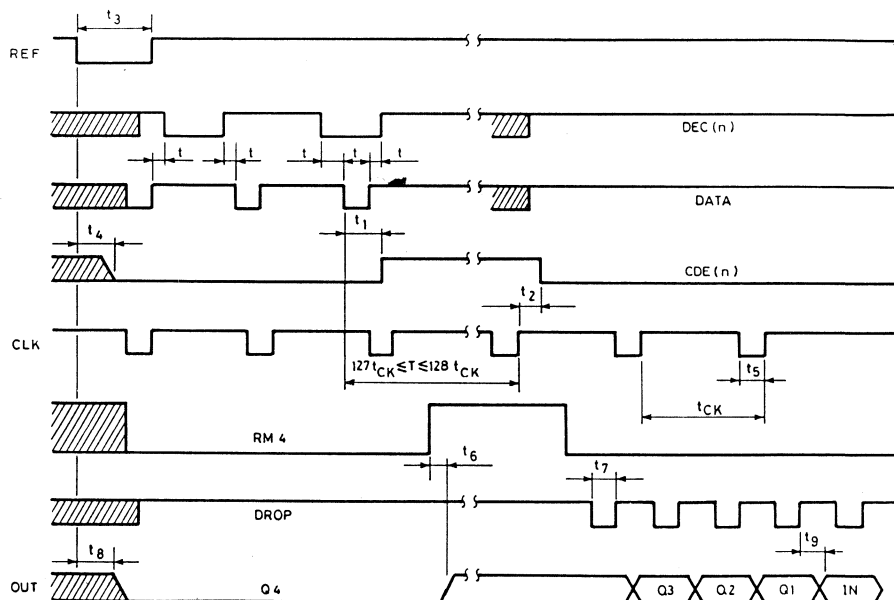


Fig. 2 - Timing diagram



S-9276/1



Technology
and Service

L6504

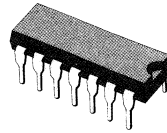
ADVANCE DATA

SOLENOID CONTROLLER

- SWITCH MODE CURRENT REGULATION
- TTL COMPATIBLE LOGIC INPUTS
- DRIVES ONE OR TWO EXTERNAL POWER TRANSISTORS
- VERY PRECISE ON-CHIP REFERENCE
- ANALOG CURRENT CONTROL INPUT
- ADJUSTABLE CURRENT RISE AND FALL TIME CONTROL INDEPENDENT OF SOLENOID SUPPLY VOLTAGE
- UNDERVOLTAGE LOCKOUT

Designed for use with one external power transistor, the L6504 drives the hammer solenoid in daisywheel printers and typewrites. The device

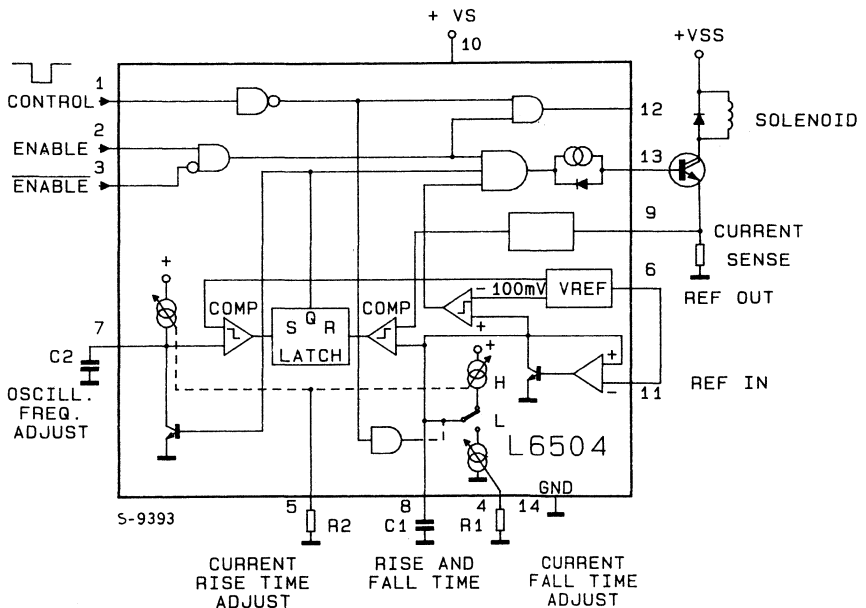
is controlled by three logic inputs and features switchmode regulation of the load current. A key feature of the device is that the rise and fall time of the load current can be set by external components. Additionally an analog input allows the load current to be set by an external DC voltage. An undervoltage lockout circuit guarantees the output off state for switch on phase.



DIP-14 Plastic
(0.25)

ORDERING NUMBER: L6504

BLOCK DIAGRAM





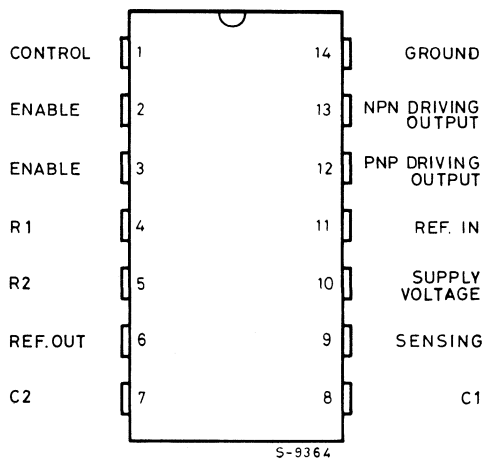
L6504

ABSOLUTE MAXIMUM RATINGS

V_s	DC supply voltage	10	V
$V_{2,3}$	Enable input voltage range	-0.3 to 7	V
V_1	Control input voltage range	-0.3 to 7	V
V_9	Sense voltage	-0.3 to 2	V
I_6	Reference output current	2	mA
V_{11}	External reference voltage	2	V
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Junction temperature	-55 to 150	°C
T_{op}	Operating temperature	0 to 85	°C

CONNECTION DIAGRAM

(Top view)



THERMAL DATA

$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	100	°C/W
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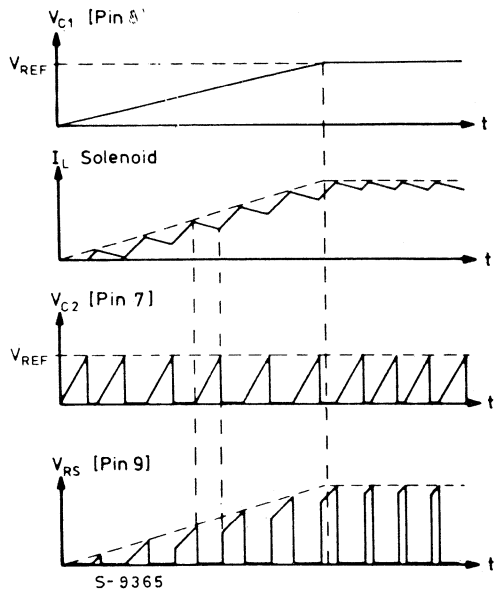
PIN FUNCTION

N°	NAME	FUNCTION
1	CONTROL	TTL compatible control input. A low level activates the output, driving the load. Internal pull-up resistor.
2	ENABLE	TTL compatible enable input. A low level disables the output stage.
3	<u>ENABLE</u>	TTL compatible enable input. A high level disables the output stage.
4	R1	The value of this resistor sets slope of trailing edge of load current.
5	R2	The value of this resistor sets slope of leading edge of load current.
6	REFERENCE OUT	Output for internal reference voltage.
7	C2	The value of this capacitor set the duration of power transistor switch off time.
8	C1	The value of this capacitor sets slope of leading and trailing edge of load current.
9	SENSING	Connection for load current sense resistor. Value sets the maximum load current : $I = V_{ref}/R_s$.
10	SUPPLY VOLTAGE	Supply voltage input.
11	REFERENCE IN	Input for external reference voltage to control load current by DC-level.
12	PNP DRIVING OUTPUT	Output to control external PNP-transistor for fast current discharge.
13	NPN DRIVING OUTPUT	Output for basecharge and discharge of external power transistor.
14	GROUND	Ground.

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $V_s = 5.0\text{V}$)

Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
V_s Operating supply voltage	10		4.5		10	V
$V_{s\ th}$ Supply voltage threshold for output switch-OFF	10	$V_{CH} = \text{Low}$ $V_E = \text{High}$		3.7		V
I_s Quiescent current	10	Pin 1 High state		7	12	mA
V_{CL} Control voltage	1	Low state			1.5	V
V_{CH} Control voltage	1	High state	2.3			V
V_{EL} Enable voltage	2/3	Low state			1.5	V
V_{EH} Enable voltage	2/3	High state	2.3			V
I_D Driving current	13	$V_{13} = 2\text{V}$	6.5	10	16	mA
V_{SE} Sense voltage	9		0		2	V
V_{REF} Reference voltage	6	$I_6 = 0 \dots 2\text{mA}$	1.28	1.33	1.38	V
I_{REF} Reference current	6				2	mA
V_{RIN} Reference input	11		0.3		2	V
I_{C8} Charge current	8	R_2 (Pin 5) = $20\text{K}\Omega$ Pin 1	58	65	72	μA
I_{D8} Discharge current	8	R_1 (Pin 4) = $20\text{K}\Omega$ Pin 1	28	32.5	37	μA
t_r Recirculation time of load current	7	$C_2 = 1.5\text{ns}$ $R_2 = 20\text{K}\Omega$	27	30	33	μs
I_{SD} Source current	12	$V_{12} = 2\text{V}$	0.5	1	1.6	mA
$V_{sat}(\text{SOURCE})$ Source saturation voltage	12	$I_{SOURCE} = 0.5\text{mA}$			4.5	V
$V_{sat}(\text{SINK})$ Sink saturation voltage	12	$I_{SINK} = 2\text{mA}$			0.4	V
V_{VI} VI-Converter voltage	4/5	$10\text{K}\Omega < R_{1/2} < 200\text{K}\Omega$ $R_1 = R_2$	1.26	1.32	1.4	V
I_{IN} Input current	2/3	$V_{2,3}$ Low state	-10			μA
t_D Current sense delay time	9			1	2.5	μs
I_{CH} Control input current	1	V_1 Low state	-1			mA

Fig. 1 – Timing diagram start phase



APPLICATION INFORMATION

Fig. 2 – Free running load current leading and trailing edge

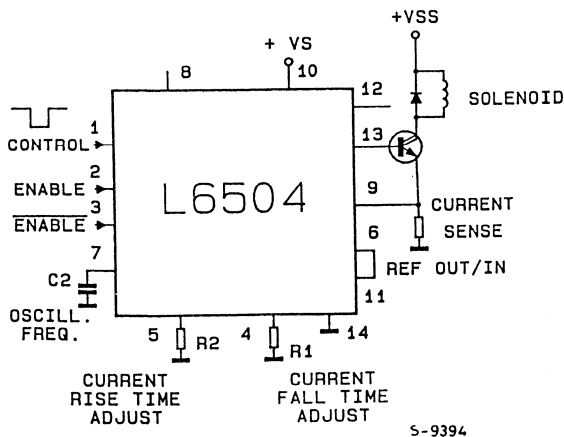
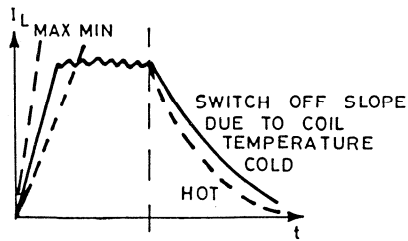


Fig. 3

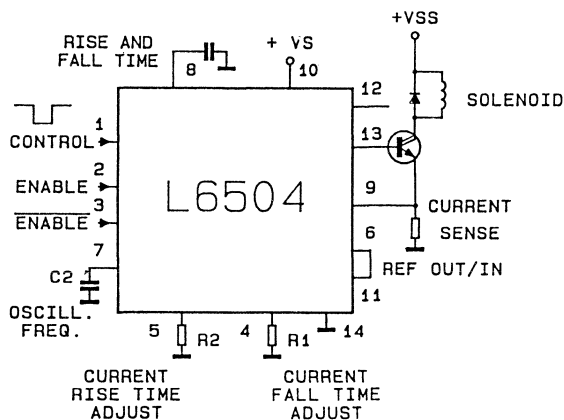




L6504

APPLICATION INFORMATION (continued)

Fig. 4 - Slew rate of leading edge controlled



S-9395

Fig. 5

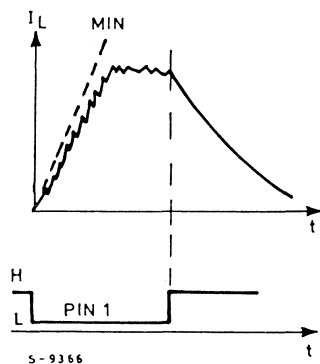
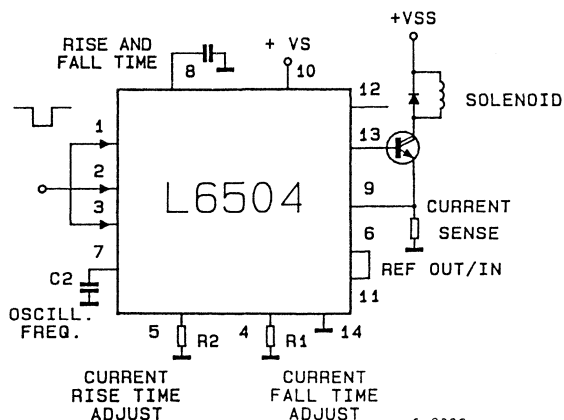
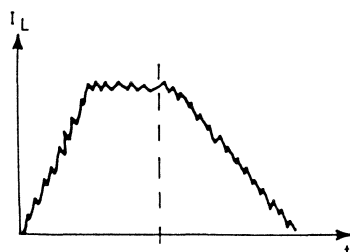


Fig. 6 - Slew rate leading and trailing edge controlled



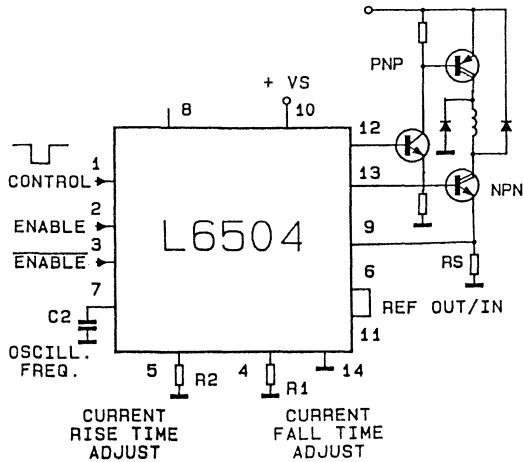
S-9396

Fig. 7



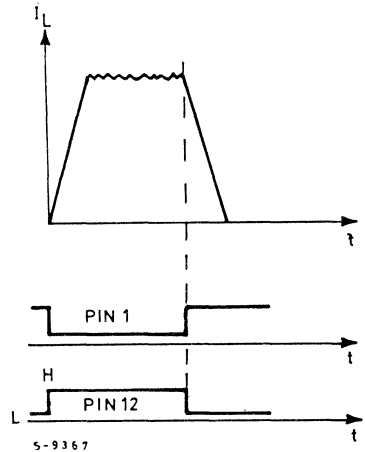
APPLICATION INFORMATION (continued)

Fig. 8 - Free running leading edge fast current slope at trailing edge



S-9397

Fig. 9



S-9367



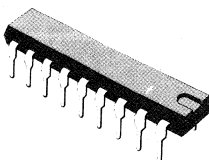
L6506

ADVANCE DATA

CURRENT CONTROLLER FOR STEPPING MOTORS

The L6506 is a linear integrated circuit designed to sense and control the current in stepping motors and similar devices. When used in conjunction with the L293, L298, L7150, or L7180, the chip set forms a constant current drive for an inductive load and performs all the interface function from the control logic thru the power stage.

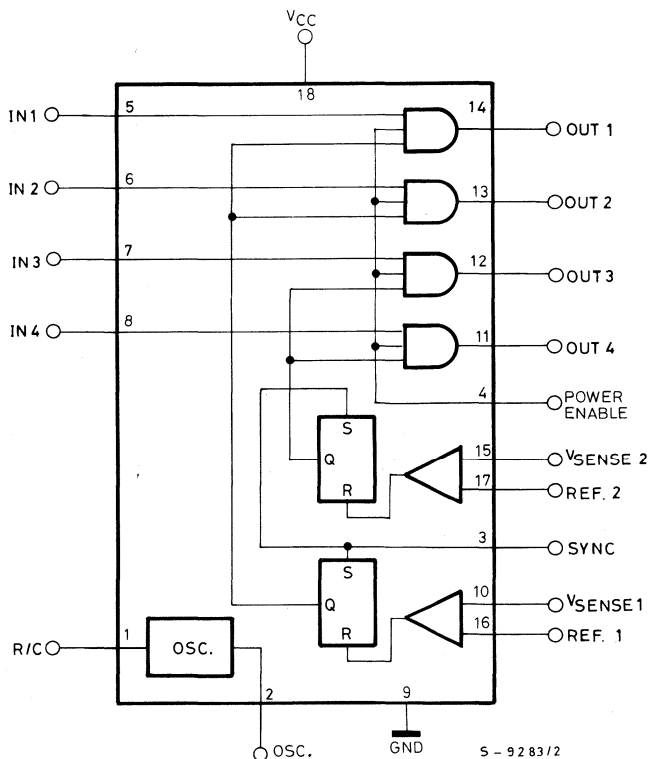
Two or more devices may be synchronized using the sync pin. In this mode of operation the oscillator in the master chip sets the operating frequency in all chips.



**DIP-18 Plastic
(U7P2)**

ORDERING NUMBER: L6506

BLOCK DIAGRAM



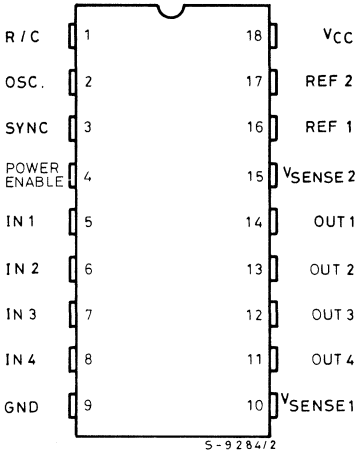


L6506

ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	10	V
V_I	Input signals	7	V
P_{tot}	Total power dissipation ($T_{amb} = 70^{\circ}C$)	1	W
T_j	Junction temperature	150	$^{\circ}C$
T_{stg}	Storage temperature	-40 to 150	$^{\circ}C$

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	80	$^{\circ}C/W$
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**L6506****ELECTRICAL CHARACTERISTICS** ($V_{CC} = 5.0V$, $T_{amb} = 25^{\circ}C$ unless otherwise noted)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC} Supply voltage		4.5		7	V
I_{CC} Quiescent supply current	$V_{CC} = 7V$			25	mA

COMPARATOR SECTION

V_{IN} Input voltage range	V_{sense} inputs	-0.3		3	V
V_{IO} Input offset voltage	$V_{IN} = 1.4V$			± 5.0	mV
I_{IO} Input Offset Current				± 200	nA
I_{IB} Input bias current				1	μA
Response time	$V_{REF} = 1.4V$ $V_{SENS} = 0$ to $5V$		0.8	1.5	μs

COMPARATOR SECTION PERFORMANCE (over operating temperature range)

V_{IO} Input offset voltage	$V_{IN} = 1.4V$			± 20	mV
I_{IO} Input offset current				± 500	nA

LOGiC SECTION (over operating temperature range) - (TTL compatible inputs & outputs)

V_{IH} Input high voltage		2.0		V_s	V
V_{IL} Input low voltage				0.8	V
V_{OH} Output high voltage	$V_{CC} = 4.75V$ $I_{OH} = 400\mu A$	2.5	3.5		V
V_{OL} Output low voltage	$V_{CC} = 4.75V$ $I_{OL} = 4.0mA$		0.25	0.4	V
I_{OH} Output source current Outputs 1 - 4	$V_{CC} = 4.75V$	2.75			mA

OSCILLATOR

f_{osc} Frequency Range		5		70	KHz
$V_{th L}$ Lower threshold voltage			$0.33V_{CC}$		V
$V_{th H}$ Higher threshold voltage			$0.66V_{CC}$		V
R_i Internal discharge resistor		0.7	1	1.3	K Ω

CIRCUIT OPERATION

The L6506 is intended for use with dual bridge drivers, such as the L298, quad darlington arrays, such as the L7180, or discrete power transistors to drive stepper motors and other similar loads. The main function of the device is to sense and control the current in each of the load windings.

A common on-chip oscillator drives the dual chopper and sets the operating frequency for the pulse width modulated drive. The RC network on pin 1 sets the operating frequency which is given by the equation:

$$f = \frac{1}{0.69 RC} \text{ for } R > 10K$$

The oscillator provides pulses to set the two flip-flops which in turn cause the outputs to activate the drive. When the current in the load winding reaches the programmed peak value, the voltage across the sense resistor (R_{sense}) is equal to V_{ref} and the corresponding comparator resets its flip-flop interrupting the drive current until the next oscillator pulse occurs. The peak current in each winding is programmed by selecting the value of the sense resistor and V_{ref} . Since separate inputs are provided for each chopper, each of the loads may be programmed independently allowing the device to be used to implement microstepping of the motor. Lower threshold of L6506's oscillator is $1/3 V_{CC}$. Upper threshold is $2/3 V_{CC}$ and internal discharge resistor is $1K\Omega \pm 30\%$.

Ground noise problems in multiple configurations can be avoided by synchronizing the

oscillators. This may be done by connecting the sync pins of each of the devices with the oscillator output of the master device and connecting the R/C pin of the unused oscillators to ground.

The equations for the active time of the sync pulse (T_2), the inactive time of the sync signal (T_1) and the duty cycle can be found by looking at the figure 1 and are:

$$T_2 = 0.69 C_1 \frac{R_1 R_{IN}}{R_1 + R_{IN}} \quad (1)$$

$$T_1 = 0.69 R_1 C_1 \quad (2)$$

$$DC = \frac{T_2}{T_1 + T_2} \quad (3)$$

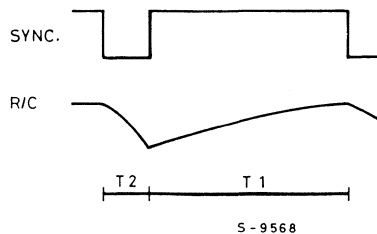
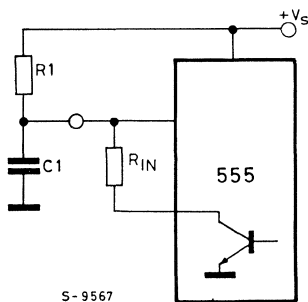
By substituting equations 1 and 2 into equation 3 and solving for the value of R_1 the following equations for the external components can be derived:

$$R_1 = \left(\frac{1}{DC} - 2 \right) R_{IN} \quad (4)$$

$$C_1 = \frac{T_1}{0.69 R_1} \quad (5)$$

Looking at equation 1 it can easily be seen that the minimum pulse width of T_2 will occur when the value of R_1 is at its minimum and the value of R_1 at its maximum. Therefore, when evaluating equation 4 the minimum value for R_1 of 700Ω ($1K\Omega - 30\%$) should be used to guarantee the required pulse width.

Fig. 1 - Oscillator circuit and waveforms



APPLICATIONS INFORMATION

The circuits shown in figures 2 and 3 use the L6506 to implement constant current drives for stepper motors. Figure 2 shows the L6506 used with the L298 to drive a 2 phase bipolar motor. Figure 3 shows the L6506 used with the L7180 to drive a 4 phase unipolar motor. The peak current can be calculated using the equation:

$$I_{\text{peak}} = \frac{V_{\text{ref}}}{R_{\text{sense}}}$$

The circuit of Fig. 2 can be used in applications requiring different peak and hold current values by modifying the reference voltage.

The L6506 may be used to implement either full step or half step drives. In the case of 2 phase bipolar stepper motor applications, if a half step drive is used, the bridge requires an additional input to disable the power stage during the half step. If used in conjunction with the L298 the enable inputs may be used for this purpose.

For quad darlington array in 4 phase unipolar motor applications half step may be implemented using the 4 phase inputs.

The L6506 may also be used to implement microstepping of either bipolar or unipolar motors.

Fig. 2 – Application circuit bipolar stepper motor driver

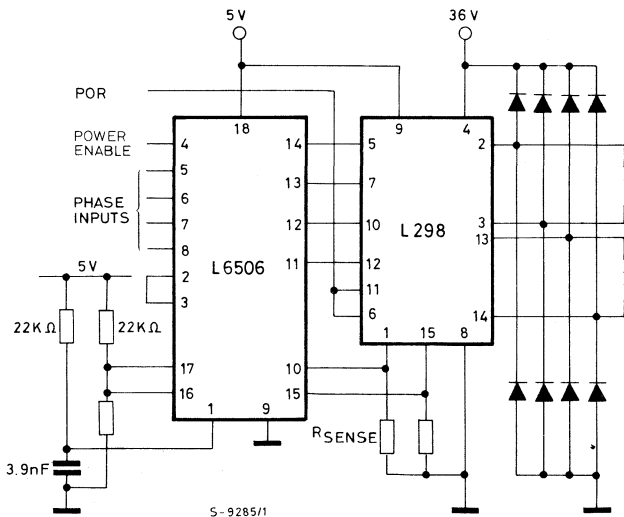
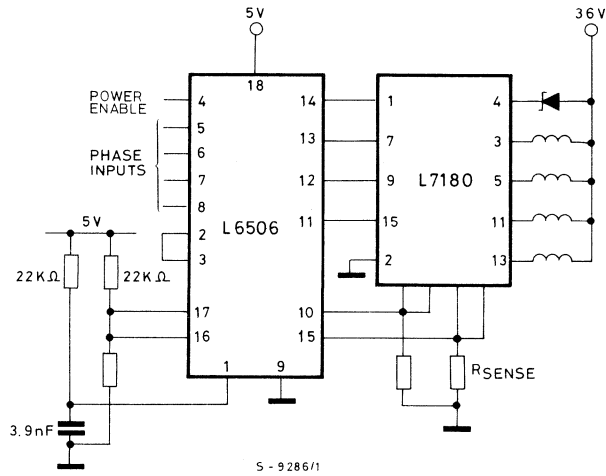


Fig. 3 - Application circuit unipolar stepper motor





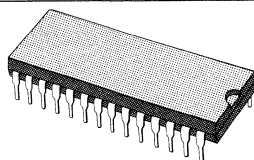
L6570A L6570B

ADVANCE DATA

2-CHANNEL FLOPPY DISK READ/WRITE CIRCUITS

- TWO GAIN VERSIONS (A AND B)
- COMPATIBLE WITH 8", 5.25" AND 3.5" DRIVES.
- INTERNAL WRITE AND ERASE CURRENT SOURCES, EXTERNALLY SET
- INTERNAL CENTER TAP VOLTAGE SOURCE
- CONTROL SIGNALS ARE TTL COMPATIBLE
- TTL SELECTABLE WRITE CURRENT BOOST
- OPERATES ON +12 AND +5V POWER SUPPLIES

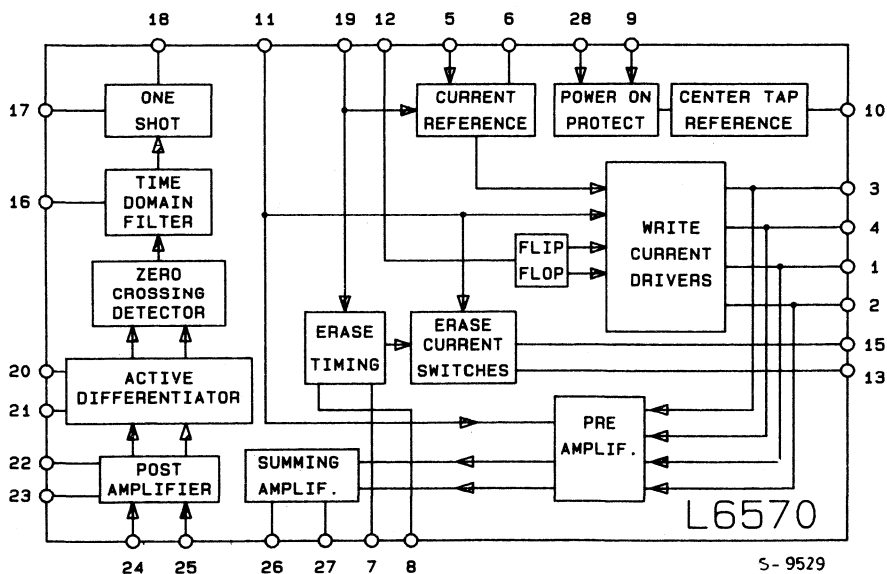
The L6570A/B are integrated circuits which perform the functions of generating write signals and amplifying and processing read signals required for a double sided floppy disk drive. The L6570A features a gain of 85 min and the L6570B of 300 min. All logic inputs and outputs are TTL compatible and all timing is externally programmable for maximum design flexibility.



DIP-28 Plastic

ORDERING NUMBER: L6570A
L6570B

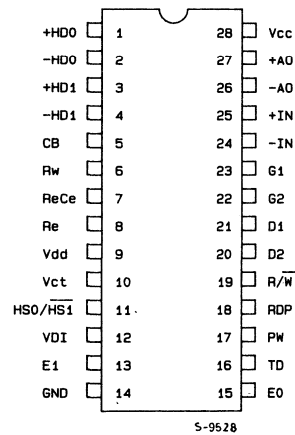
BLOCK DIAGRAM



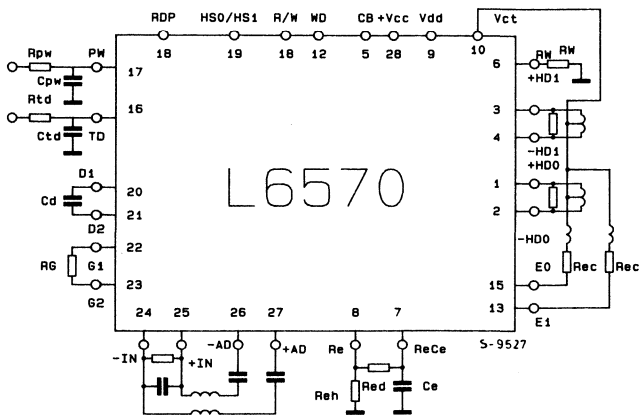
ABSOLUTE MAXIMUM RATINGS

V _{CC}	5V supply voltage	7	V
V _{DD}	12V supply voltage	14	V
T _{stg}	Storage temperature	-65 to 150	°C
T _{amb}	Ambient operating temperature	0 to +70	°C
T _j	Junction operating temperature	0 to +130	°C
V _I	Logic input voltage	-0.5 to 7.0	V
P _{tot}	Power dissipation	500	mW

CONNECTION DIAGRAM
(Top view)



TEST CIRCUIT



THERMAL DATA

R _{thJ-amb}	Thermal resistance junction-ambient	max	100	°C/W
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ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $4.75V \leq V_{CC} \leq 5.25V$; $11.4V \leq V_{DD} \leq 12.6V$; $0^{\circ}C \leq T_{amb} \leq 70^{\circ}C$; $R_W = 430\Omega$; $R_{ED} = 62K\Omega$; $C_E = 0.012\mu F$; $R_{EH} = 62K\Omega$; $R_{EC} = 220\Omega$)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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POWER SUPPLY CURRENTS

I_{CC}	5V supply current	Read Mode		35	mA
		Write Mode		38	mA
I_{DD}	12V supply current	Read Mode	L6570A L6570B	26 35	mA mA
		Write Mode (exclude Write and Erase currents)	L6570A L6570B	24 35	mA mA

LOGIC SIGNALS — READ/WRITE (R/W), CURRENT BOOST (CB)

V_{IL}	Input Low voltage			0.8	V
I_{IL}	Input Low current	$V_{IL} = 0.4V$		-0.4	mA
V_{IH}	Input High voltage		2.0		V
I_{IH}	Input High current	$V_{IH} = 2.4V$		20	μA

LOGIC SIGNALS — WRITE DATA INPUT (WDI), HEAD SELECT (HS0/HS1)

V_{T+}	Threshold voltage, Positive - going		1.4	1.9	V
V_{T-}	Threshold voltage, Negative - going		0.6	1.1	V
V_{T+}, V_{T-}	Hysteresis		0.4		V
I_{IH}	Input High current	$V_{IH} = 2.4V$		20	μA
I_{IL}	Input Low current	$V_{IL} = 0.4V$		-0.4	mA

CENTER TAP VOLTAGE REFERENCE

V_{CT}	Output voltage	$I_{WC} + I_E = 3mA$ to 60mA	$V_{DD}-1.5$	$V_{DD}-0.5$	V
V_{CC}	Turn-Off threshold		4.0		V
V_{DD}	Turn-Off threshold		9.6		V
V_{CT}	Disabled voltage			1.0	V

ERASE OUTPUTS (E1, E0)

	Unselected head leakage	$V_{E0}, V_{E1} = 12.6V$		100	μA
V_{E1}, V_{E0}	Output on voltage	$I_E = 50mA$		0.5	V

WRITE CURRENT

	Unselected head leakage	$V_{E1}, V_{E0} = 12.6V$		25	μA
	Write current range	$R_W = 820\Omega$ to 180Ω	3	10	mA
	Current reference accuracy	$I_{WC} = 2.3/R_W$ V_{CB} (current boost) = 0.5V	-5	+5	%



L6570A L6570B

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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WRITE CURRENT (continued)

Write current unbalanced	$I_{WC} = 3\text{mA to } 10\text{mA}$			1.0	%
Differential head voltage swing	$\Delta I_{WC} \leq 5\%$	12.8			V_{pk}
Current boost	$V_{CB} = 2.4\text{V}$	$1.25 I_{WC}$		$1.35 I_{WC}$	

ERASE TIMING

Erase delay range	$R_{ED} = 39\text{K}\Omega \text{ to } 82\text{K}\Omega$ $C_E = 0.0015\mu\text{F to } 0.043\mu\text{F}$	0.1		1.0	ms
Erase delay accuracy $\frac{\Delta T_{ED}}{T_{ED}} \times 100\%$	$T_{ED} = 0.69 R_{ED} C_E$ $R_{ED} = 39\text{K}\Omega \text{ to } 82\text{K}\Omega$ $C_E = 0.0015\mu\text{F to } 0.043\mu\text{F}$	-15		+15	%
Erase hold range	$R_{EH} + R_{ED} = 78\text{K}\Omega \text{ to } 164\text{K}\Omega$ $C_E = 0.0015\mu\text{F to } 0.043\mu\text{F}$	0.2		2.0	ms
Erase hold accuracy $\frac{\Delta T_{ED}}{T_{ED}} \times 100\%$	$T_{EH} = 0.69 (R_{ED} + R_{ED}) C_E$ $R_{EH} + R_{ED} = 78\text{K}\Omega \text{ to } 164\text{K}\Omega$ $C_E = 0.0015\mu\text{F to } 0.043\mu\text{F}$	-15		+15	%

ELECTRICAL CHARACTERISTICS (Unless otherwise specified: V_{IN} (Preamplifier) = 10mV_{pp} sine wave, DC coupled to center tap. Summing amplifier load = $2\text{K}\Omega$ line-line, AC coupled. V_{IN} (Post-amplifier) = 0.2V_{pp} sine wave, AC coupled; R_G = open; Data pulse load = $1\text{K}\Omega$ to V_{CC} ; $C_D = 240\text{pF}$; $C_{TD} = 100\text{pF}$; $R_{TD} = 7.5\text{K}\Omega$; $C_{PW} = 47\text{pF}$; $R_{PW} = 7.5\text{K}\Omega$).

READ MODE

Parameter	Test Condition	Min.	Typ.	Max.	Unit
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PREAMPLIFIER – SUMMING AMPLIFIER

Diff voltage gain	Freq. = 250KHz	L6570A L6570B	85 300		115 400	V/V
Bandwidth (-3dB)			3			MHz
Gain flatness	Freq. = DC to 1.5MHz				± 1.0	dB
Diff. input impedance	Freq. = 250KHz		20			$\text{K}\Omega$
Max. diff. output voltage swing	$V_{IN} = 250\text{KHz}$ sine wave THD $\leq 5\%$	L6570A L6570B	2.5 4.0			V_{pp}
Small signal difference output resistance	$I_O \leq 1.0\text{mA}_{pp}$				75	Ω
Common mode rejection ratio	$V_{IN} = 300\text{V}_{pp}$ @ 500KHz Inputs shorted	L6570A L6570B	50 40			dB



L6570A
L6570B

ELECTRICAL CHARACTERISTICS (continued);

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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PREAMPLIFIER — SUMMING AMPLIFIER

Power supply rejection ratio	$\Delta V_{DD} = 300mV_{pp}$ @ 500KHz Inputs shorted to V_{CT}	50			dB
Channel isolation	Unselected channel $V_{IN} = 100mV_{pp}$ @ 500KHz. Selected channel input connected to V_{CT}	40			dB
Equivalent input noise	Power BW = 10KHz to 1MHz Inputs shorted to V_{CT}			10	μV_{rms}
V_{CT} Center tap voltage			1.5		V

POSTAMPLIFIER — ACTIVE DIFFERENTIATOR

A0, diff. voltage gain +IN, -IN to D1, D2	Freq. = 250KHz	8.5		11.5	V/V
Bandwidth (-3dB) +IN, -IN to D1, D2	$C_D = 0.1\mu F$, $R_D = 2.5K\Omega$	3			MHz
Gain flatness +IN, -IN to D1, D2	Freq. = DC to 1.5MHz $C_D = 0.1\mu F$, $R_D = 2.5K\Omega$			± 1.0	dB
Max. diff. output voltage swing	$V_{IN} = 250KHz$ sine wave, AC coupled. $\leq 5\%$ THD in voltage across C_D	5.0			V_{pp}
Max. diff. input voltage	$V_{IN} = 250KHz$ sine wave, AC coupled. $\leq 5\%$ THD in voltage across C_D , $R_G = 1.5K\Omega$	2.5			V_{pp}
Diff. input impedance		10			$K\Omega$
Gain control accuracy $\frac{\Delta A_R}{A_R} \times 100\%$	$A_R = A_0 R_G / (8 \times 10^3 + R_G)$ $R_G = 2K\Omega$	-25		+25	%
Threshold differential input voltage	Min. diff. input voltage at post amp. that results in a change of state at RDP $V_{IN} = 250KHz$ square wave, $C_D = 0.1\mu F$, $R_D = 500\Omega$, $T_R, T_F \leq 0.2\mu s$. No overshoot; Data pulse from each V_{IN} transition			3.7	mV_{pp}
Peak differential Network current		1.0			mA

TIME DOMAIN FILTER

Delay accuracy $\frac{\Delta T_{TD}}{T_{TD}} \times 100\%$	$T_{TD} = 0.58 R_{TD} \cdot (C_{TD} + 10^{-11}) + 150ns$, $R_{TD} = 5K\Omega$ to $10K\Omega$ $C_{TD} = 56pF$ $V_{IN} = 50mV_{pp}$ @ 250KHz sq. wave $T_R, T_F \leq 20ns$, AC coupled. Delay measured from 50% input amplitude to 1.5V data pulse	-15		+15	%
Delay range	$T_{TD} = 0.58 R_{TD} \cdot (C_{TD} + 10^{-11}) + 150ns$, $R_{TD} = 5K\Omega$ to $10K\Omega$ $C_{TD} = 56pF$ to $240pF$ $R_D = 500\Omega$ $C_D = 0.1\mu F$.	240		2370	ns

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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DATA PULSE

Width accuracy $\frac{\Delta T_{PW}}{T_{PW}} \times 100\%$	$T_{PW} = 0.58 R_{PW} \times (C_{PW} + 8 \times 10^{-12}) + 20ns$ $R_{PW} = 5K\Omega \text{ to } 10K\Omega$ $C_{PW} \geq 36pF$ with measured at 1.5V amplitudes	-20		+20	%
Active level output voltage	$I_{OH} = 400\mu A$	2.7			V
Inactive level output leakage	$I_{OL} = 4mA$			0.5	V
Pulse width	$T_{PW} = 0.58 R_{PW} \times (C_{PW} + 8 \times 10^{-12}) + 20ns$ $R_{PW} = 5K\Omega \text{ to } 10K\Omega$ $C_{PW} = 36pF \text{ to } 200pF$	145		1225	ns

TEST SCHEMATICS

Fig. 1 – Preamplifier characteristics

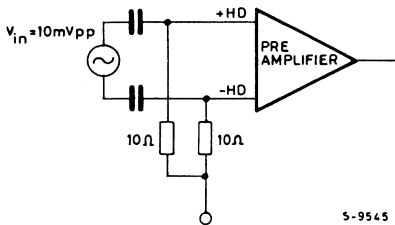


Fig. 2 – Postamplifier differential output voltage swing and voltage gain

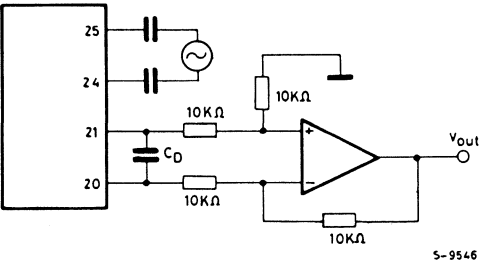
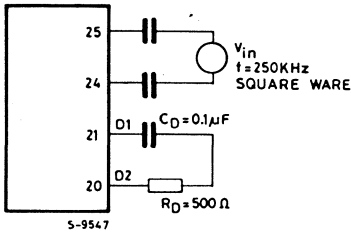


Fig. 3 – Postamplifier threshold differential input voltage





L7150 L7152

PRELIMINARY DATA

50V QUAD DARLINGTON SWITCHES

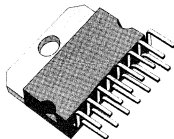
- FOUR NPN DARLINGTONS WITH ISOLATED CONNECTIONS
- OUTPUT CURRENT TO 1.5A EACH DARLINGTON
- MINIMUM BREAKDOWN 50V
- SUSTAINING VOLTAGE AT LEAST 35V
- MULTIWATT PACKAGE ALLOWS OPERATION AT 1.5A, 50V, 100% DUTY CYCLE, ALL FOUR DEVICES ON
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR 5V AND 6-15V LOGIC FAMILIES

The L7150 and L7152 are 1.5A quad darlington arrays mounted in the 15-lead Multiwatt[®] plastic package. Each darlington is equipped with a suppression diode for inductive loads and all three terminals are isolated.

down of 50V is specified and the minimum sustaining voltage is 35V, measured at 100mA.

The L7150 has 350 Ω input resistors and is compatible with TTL, DTL, LSTTL and 5V CMOS logic. The L7152 has 3K Ω input resistors for use with 6-15V CMOS and PMOS logic.

These devices are suitable for driving a wide range of inductive and non-inductive loads including DC motors, stepper motors, solenoids, relays, lamps, multiplexed LEDs and heaters.



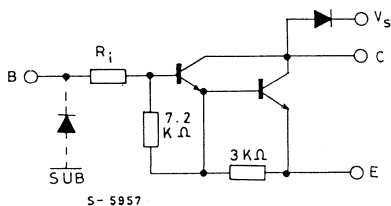
Multiwatt 15

ORDERING NUMBER: L7150
L7152

ABSOLUTE MAXIMUM RATINGS

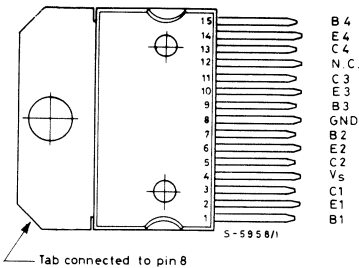
V_{CEX}	Output voltage	50	V
$V_{CE(sus)}$	Output sustaining voltage	35	V
I_o	Output current	1.75	A
V_i	Input voltage	30	V
I_B	Input current	25	mA
P_{tot}	Power dissipation ($T_{case} = 75^{\circ}C$)	25	W
T_{amb}	Operating ambient temperature range	0 to 70	$^{\circ}C$
T_{stg}	Storage temperature	-55 to 150	$^{\circ}C$

SCHEMATIC DIAGRAM



L7150 : $R_{IN} = 350\Omega$
L7152 : $R_{IN} = 3K\Omega$

CONNECTION DIAGRAM
(top view)



THERMAL DATA

R _{th j-case}	Thermal resistance junction-case	max.	3	°C/W
R _{th j-amb}	Thermal resistance junction-ambient	max.	35	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit	Fig.
I _{CEX} Output leakage current	V _{CE} = 50V V _{CE} = 50V T _{amb} = 70°C			100 500	μA μA	1
V _{CE(sus)} Collector-emitter sustaining voltage	I _C = 100mA V _i = 0.4V	35			V	2
V _{CE(sat)} Collector-emitter saturation voltage	I _C = 500mA I _B = 625μA I _C = 750mA I _B = 935μA I _C = 1A I _B = 1.25mA I _C = 1.25A I _B = 2 mA			1.15 1.3 1.4 1.5	V V V V	3
I _{i(on)} Input current	for L7150 V _i = 2.4V for L7150 V _i = 3.75V for L7152 V _i = 5V for L7152 V _i = 12V	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
V _{i(on)} Input voltage	for L7150 V _{CE} = 2V I _C = 1A V _{CE} = 2V I _C = 1.5A for L7152 V _{CE} = 2V I _C = 1A V _{CE} = 2V I _C = 1.5A			2 2.5 6.5 10	V V V V	5
t _{PLH} Turn-on delay time	0.5V _i to 0.5V _o			1	μs	
t _{PHL} Turn-off delay time	0.5V _i to 0.5V _o			1.5	μs	

TEST CIRCUITS

Fig. 1

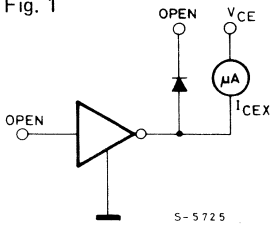


Fig. 2

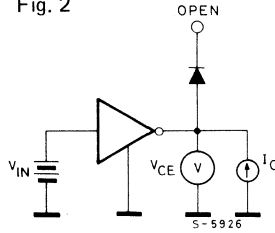


Fig. 3

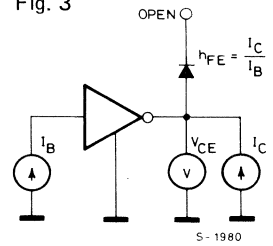


Fig. 4

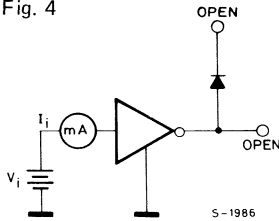
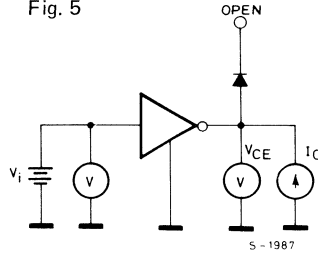


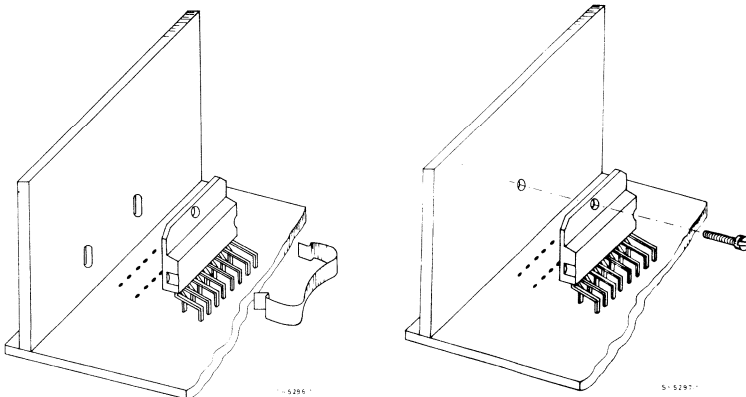
Fig. 5



MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink. Thanks to the Multiwatt® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 6 - Mounting example





L7180 L7182

80V QUAD DARLINGTON SWITCHES

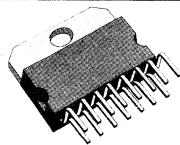
- FOUR NPN DARLINGTONS WITH ISO-LATED CONNECTIONS
- OUTPUT CURRENT TO 1.5A EACH DAR-LINGTON
- MINIMUM BREAKDOWN 80V
- SUSTAINING VOLTAGE AT LEAST 50V
- MULTIWATT PACKAGE ALLOWS OPERA-TION AT 1.5A, 80V, 100% DUTY CYCLE, ALL FOUR DEVICES ON
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR 5V AND 6-15V LOGIC FAMILIES

The L7180 and L7182 are 1.5A quad darlington arrays mounted in the 15-lead Multiwatt[®] plastic package. Each darlington is equipped with a sup-pression diode for inductive loads, and all three terminals are isolated. A minimum breakdown

of 80V is specified and the minimum sustaining voltage is 50V.

The L7180 has 350Ω input resistors and is com-patible with TTL, DTL, LSTTL and 5V CMOS logic. The L7182 has 3KΩ input resistors for use with 6-15V CMOS and PMOS logic.

These devices are suitable for driving a wide range of inductive and non-inductive loads including DC motors, stepper motors, solenoids, relays, lamps, multiplexed LEDs and heaters.



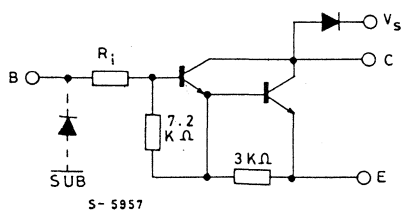
Multiwatt 15

ORDERING NUMBER: L7180
L7182

ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Output voltage	80	V
$V_{CE(sus)}$	Output sustaining voltage	50	V
I_o	Output current	1.75	A
V_i	Input voltage	60	V
I_B	Input current	25	mA
P_{tot}	Power dissipation ($T_{case} = 75^{\circ}C$)	25	W
T_{amb}	Operating ambient temperature range	0 to 70	$^{\circ}C$
T_{stg}	Storage temperature	-55 to 150	$^{\circ}C$

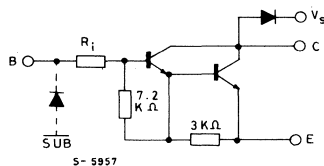
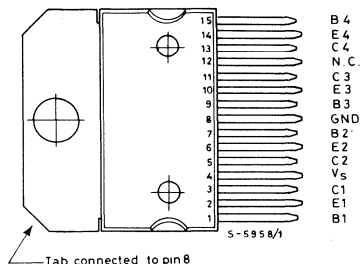
SCHEMATIC DIAGRAM



L7180 : $R_{IN} = 350 \Omega$
L7182 : $R_{IN} = 3 K\Omega$

CONNECTION AND SCHEMATIC DIAGRAMS

(top view)



L7180 : $R_{IN} = 350 \Omega$
L7182 : $R_{IN} = 3 K\Omega$

THERMAL DATA

$R_{thj-case}$	Thermal resistance junction-case	max.	3	$^{\circ}C/W$
$R_{thj-amb}$	Thermal resistance junction-ambient	max.	35	$^{\circ}C/W$

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX} Output leakage current	$V_{CE} = 80V$ $V_{CE} = 80V$ $T_{amb} = 70^{\circ}C$			100 500	μA μA	1
$V_{CE(sus)}$ Collector-emitter sustaining voltage	$I_C = 100mA$ $V_i = 0.4V$	50			V	2
$V_{CE(sat)}$ Collector-emitter saturation voltage	$I_C = 500mA$ $I_B = 625\mu A$ $I_C = 750mA$ $I_B = 935\mu A$ $I_C = 1A$ $I_B = 1.25mA$ $I_C = 1.5A$ $I_B = 2.25mA$			1.15 1.3 1.4 1.6	V V V V	3
$I_{i(on)}$ Input current	for L7180 $V_i = 2.4V$ for L7180 $V_i = 3.75V$ for L7182 $V_i = 5V$ for L7182 $V_i = 12V$	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$ Input voltage	for L7180 $V_{CE} = 2V$ $I_C = 1A$ for L7180 $V_{CE} = 2V$ $I_C = 1.5A$ for L7182 $V_{CE} = 2V$ $I_C = 1A$ for L7182 $V_{CE} = 2V$ $I_C = 1.5A$			2 2.5 6.5 10	V V V V	5
t_{PLH} Turn-on delay time	$0.5V_i$ to $0.5V_o$			1	μs	
t_{PHL} Turn-off delay time	$0.5V_i$ to $0.5V_o$			1.5	μs	

TEST CIRCUITS

Fig. 1

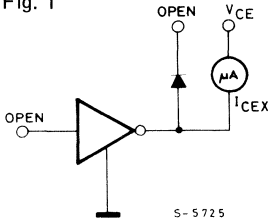


Fig. 2

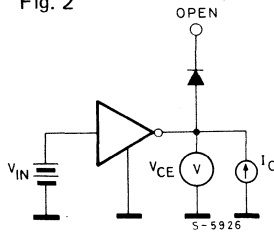


Fig. 3

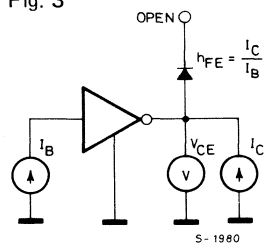


Fig. 4

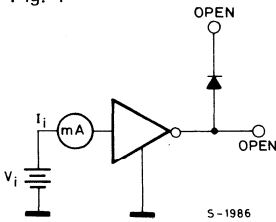
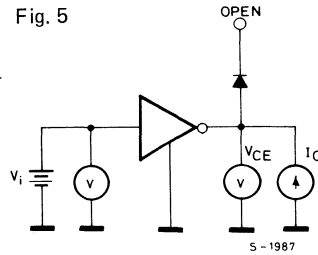


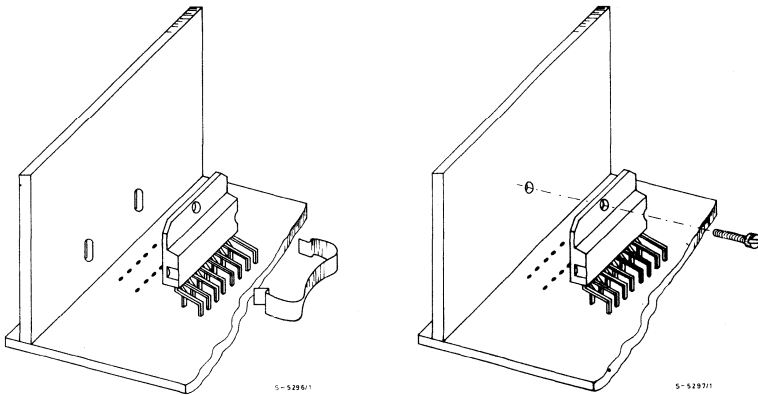
Fig. 5



MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink. Thanks to the Multiwatt[®] package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 6 - Mounting example





L9222

ADVANCE DATA

QUAD INVERTING TRANSISTOR SWITCHES

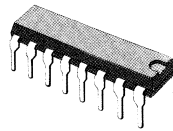
- OUTPUT VOLTAGE TO 50V
- OUTPUT CURRENT TO 1.2A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL SUPPRESSION DIODE

The L9222 monolithic quad transistor switch is designed for high current, high voltage switching applications.

Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL-compatible for direct connection to logic circuits.

Each switch consists of an open-collector transistor plus a clamp diode for applications with inductive loads. The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

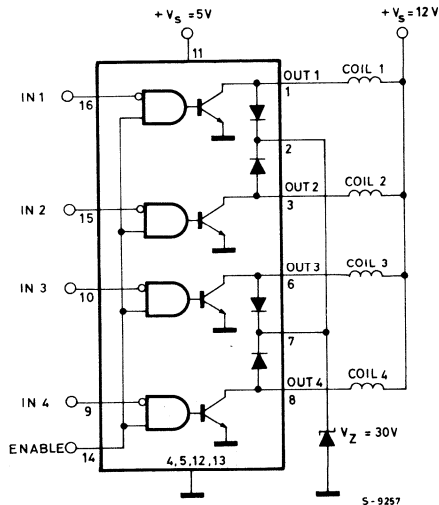
The device is intended to drive coils such as relays, solenoids, unipolar stepper motors, LED etc.



**Powerdip 12 + 2 + 2
(V6P2)**

ORDERING NUMBER: L9222

BLOCK DIAGRAM

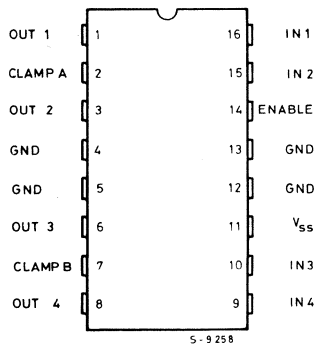


**L9222****ABSOLUTE MAXIMUM RATINGS**

V_s	Output voltage	50	V
V_{ss}	Logic supply voltage	7	V
V_i	Input voltage	15	V
I_c	Collector current	1.2	A
T_{op}	Operating temperature range (junction)	-40 to +150	°C
T_{stg}	Storage temperature range	-55 to +150	°C

CONNECTION DIAGRAM

(Top view)

**TRUTH TABLE**

Enable	Input	Power Out
H	L	ON
H	H	OFF
L	X	OFF

For each input: H = High level
L = Low level
X = Don't care

THERMAL DATA

$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	80	°C/W
$R_{th\ j-case}$	Thermal resistance junction-case	max	14	°C/W

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{CE(sus)}$ Output sustaining voltage	$V_{IN} = 2V$ $V_{EN} = 2V$ $I_C = 100\text{mA}$	46			V
I_{CEX} Output leakage current	$V_{CE} = 50V$ $V_{IN} = 2V$			1	mA
$V_{CE(sat)}$ Collector emitter saturation voltage	$V_{IN} \leq 0.8V$	$I_C = 0.1A$		0.2	V
		$I_C = 0.4A$		0.5	
		$I_C = 0.7A$		0.7	
V_{IL} Input low voltage				0.8	V
I_{IL} Input low current	$V_{IN} = 0.4V$			-100	μA
V_{IH} Input high voltage		2.0			V
I_{IH} Input high current	$V_{IN} \geq 2.0V$			± 10	μA
I_s Logic supply current	$V_{ss} = 5V$ All outputs ON $I_C = 0.7A$		50	85	mA
		All outputs OFF	8		mA
I_R Clamp diode leakage current	$V_R = 50V$			100	μA
V_F Clamp diode forward voltage	$I_F = 1A$			1.6	V
	$I_F = 1.2A$			2.0	
V_{ss} Logic supply voltage		4.50		7	V



L9305A L9305C

ADVANCE DATA

DUAL HIGH CURRENT RELAY DRIVER

- HIGH OUTPUT CURRENT
- HYSTERESIS INPUT COMPARATOR WITH WIDE RANGE COMMON MODE OPERATION AND GROUND COMPATIBLE INPUTS
- SHORT CIRCUIT PROTECTION OF OUTPUT TO 18V (FOR L9305A) AND 12V (FOR L9305C)
- INTERNAL THERMAL PROTECTION WITH HYSTERESIS
- OVERVOLTAGE CLAMP OF THE OUTPUT
- SINGLE SUPPLY VOLTAGE FROM 18V DOWN TO 3.5V

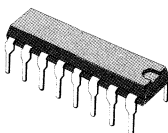
The L9305A and L9305C are a monolithic interface circuit with differential input comparator and open collector output able to sink high current specially to drive relays, lamps, d.c. motors.

Particular care has been taken to protect the

device against destructive failures – short circuit of outputs to V_S , output overvoltages, supply overvoltage.

A built in thermal shut-down switches off the device when the IC's internal dissipation becomes too great and the chip temperature exceeds a setted security threshold.

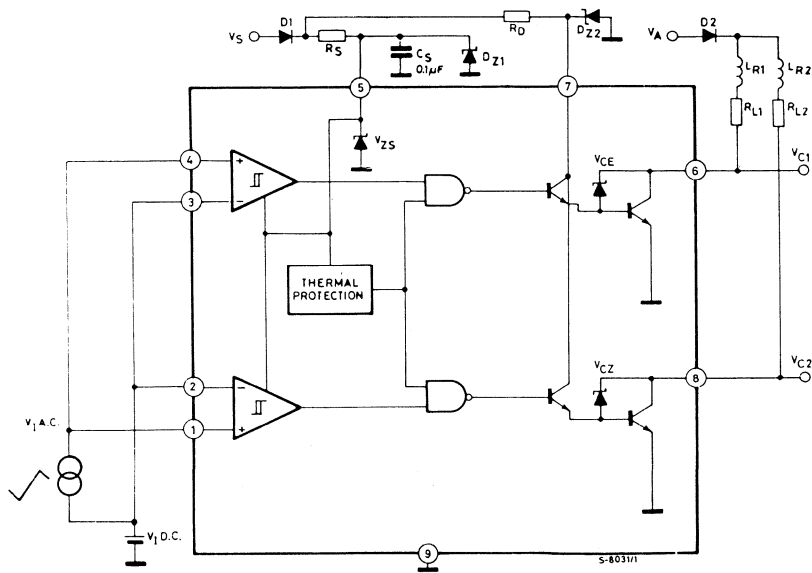
A hysteresis input comparator increases the interface's noise immunity, allowing the correct use also in critical environments as automotive or industrial applications.



**Powerdip
(8 + 8)**

**ORDERING NUMBER: L9305A
L9305C**

TEST AND APPLICATION CIRCUIT





L9305A
L9305C

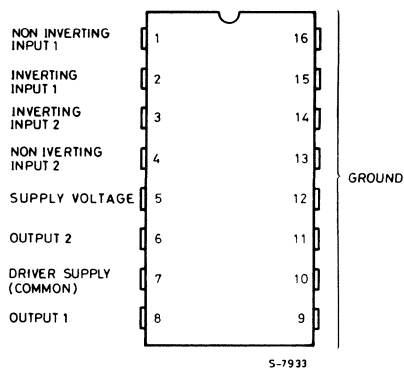
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	(*) 20	V
I_c	Output current	2.3	A
I_{cz}	Zener clamp current (DC)	30	mA
	(PULSED) (**)	80	mA
V_i	Input voltage range	-0.2 to 24	V
V_i	Differential input voltage	24	V
T_{stg}	Storage temperature	-55 to 150	°C
T_{op}	Operating ambient temperature	-40 to + 85	°C
	Output short circuit protection (L9305A)	up to 18	V
	Output short circuit protection (L9305C)	up to 12	V
T_j	Maximum junction temperature	150	°C

(*) The maximum allowed supply voltage without series resistors is limited by the built-in zener protection diodes.

(**) $T_{on} \leq 2.5ms$; Repetition time $\geq 30ms$

CONNECTION DIAGRAM (top view)



THERMAL DATA

$R_{thj-pins}$	Thermal resistance junction-pins	max	15	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	max	70	°C/W



L9305A
L9305C

ELECTRICAL CHARACTERISTICS ($V_{ST} = 14.4V$, $T_{amb} = 25^{\circ}C$; refer to block diagram unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S Supply voltage		3.5		18 (**)	V
I_S "st. by" Supply current	$V_i^+ - V_i^- \geq 70mV$ for L9305A for L9305C		5 5	8 12	mA mA
I_{SON} Supply current	$V_i^+ - V_i^- > 70mV$		18	30	mA
V_{CZ} Voltage clamp at the output of each channel	$I_{CZ} = 1A$	20		27	V
V_{ZS} Voltage clamp supply protection	$I_Z = 10mA$	20		27	V
V_{IH} Hysteresis of the input comparator	$V_{IN} = 20mV_{pp}$ $f = 1KHz$	20		70	mV
I_B Input bias current	$V^+ = V^- = 0V$		0.2	1	μA
I_{OS} Input offset current	$V^+ = V^- = 0V$		± 20	± 200	nA
CMR Input common mode range	$V_{ST} = 3.5V$ to $18V$	0		$V_{ST} - 1.6$	V
I_{SC} Output short circuit	$V_i^- - V_i^+ \geq 70mV$; $V_S = 6V$; for L9305A $V_S = 16V$; for L9305A	1.2 0.25		2.6 0.7	A A
	$V_S = 6$ to $12V$; for L9305C	1		2.3	A
I_{CD} Driver transistor curr.	$V_i^- - V_i^+ \geq 70mV$ DC			300	mA
	Pulsed (*)			600	
T_j Thermal shut-down threshold			145		$^{\circ}C$
T_j Thermal shut-down hysteresis			15		$^{\circ}C$
V_C (sat) On status saturation voltage	$V_i^+ - V_i^- \geq 70mV$ $I_{CD} = 100mA$ $I_{COUT} = 1.2A$ for L9305A $I_{COUT} = 1A$ for L9305C			1	V
I_{OL} Output leakage current	$V_i^- - V_i^+ \geq 70mV$ for L9305A for L9305C			250 500	μA μA

(*) $T_{ON} \leq 2.5ms$; repetition time $\geq 30ms$

(**) The maximum allowed supply voltage without limiting resistors is limited by the built-in protection zener diodes see V_{CZ} , V_{ZS} Spec. values

(1) The L9305 has a SOA short circuit protection - (See Fig. 1).



L9305A
L9305C

APPLICATION INFORMATION (Refer to application circuit)

D1 and D2 diodes are required only for reverse polarity protection.

If V_S may be higher than V_{ZS} a resistor R_S is necessary to limit the zener current I_{ZS} . In order to determine R_S value the following equations can be used:

- 1)
$$\frac{V_{S\text{MAX}} - V_{D1} - V_{ZS\text{min}}}{R_S} < I_{ZS\text{MAX}}$$
- 2)
$$V_{S\text{min}} - V_{D1} - R_S - I_{SON\text{MAX}} > V_{ST\text{min}}$$

where from $T_{\text{amb}} = 25^\circ\text{C}$:

- $V_{S\text{MAX}}$ and $V_{S\text{min}}$ are the maximum and minimum values of power supply voltage
- V_{D1} is the forward diode D1 voltage drop
- $V_{ZS\text{min}} = 20\text{V}$
- $I_{ZS\text{MAX}} = 30\text{mA}$ for d.c. mode and $I_{ZS\text{MAX}} = 80\text{mA}$ for pulsed mode (see Absolute maximum ratings)
- $I_{SON\text{MAX}} = 30\text{mA}$
- $V_{ST\text{min}} = 3.5\text{V}$

If no R_S value can satisfy the system 1), 2) a more powerfull external zener $D_Z = 18\text{V}$ is required.

Then 1) becomes:

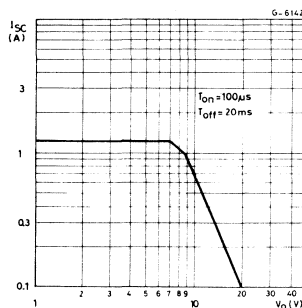
$$\frac{V_{S\text{MAX}} - V_{D1} - 18}{R_S} < I_{DZ\text{MAX}}$$

where $I_{DZ\text{MAX}}$ is the maximum allowed Dz current.

V_A voltage cannot be higher than 20V otherwise output overvoltage protection may be activated. Moreover V_A must be less than 18V (for L9305A) or 12V (for L9305C) if short circuit protection is required.

$D_{Z2} = 22$ to 24V is a mandatory for output 7 protection if V_S may be higher than 26V.

Fig. 1 – SOA protection (L9305A)





L9306 L9306C

ADVANCE DATA

DUAL RELAY DRIVER

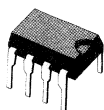
- HIGH OUTPUT CURRENT
- HYSTERESIS INPUT COMPARATOR WITH WIDE RANGE COMMON MODE OPERATION AND GROUND COMPATIBLE INPUTS
- SHORT CIRCUIT PROTECTION OF OUTPUT TO V_S (16V MAX. FOR L9306) AND (12V MAX. FOR L9306C)
- INTERNAL THERMAL PROTECTION WITH HYSTERESIS
- OVERVOLTAGE CLAMPING OF THE OUTPUT
- SINGLE SUPPLY VOLTAGE FROM 3.5V UP TO 18V

The L9306 and L9306C are a monolithic interface circuit with differential input comparator and open collector output able to sink current specifically to drive high inductive loads, relays, d.c. motors, electro valves etc.

Particular care has been taken to protect the device against destructive failures – short circuit of outputs to V_S , output overvoltages, supply overvoltage.

A built in thermal shut-down switches off the device when the IC's internal dissipation becomes too great and the chip temperature exceeds a setted security threshold.

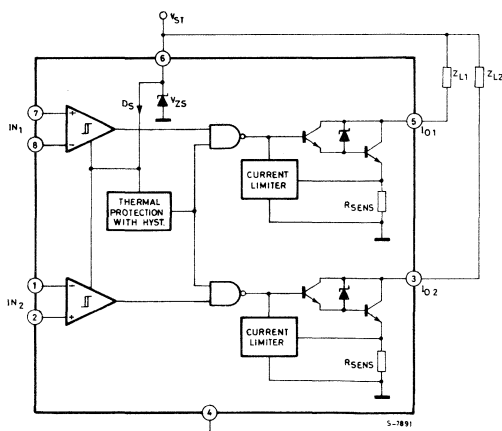
A hysteresis input comparator increases the interface's noise immunity, allowing the correct use also in critical environments as automotive or industrial applications.



Minidip Plastic

ORDERING NUMBER: L9306
L9306C

BLOCK DIAGRAM





L9306 L9306C

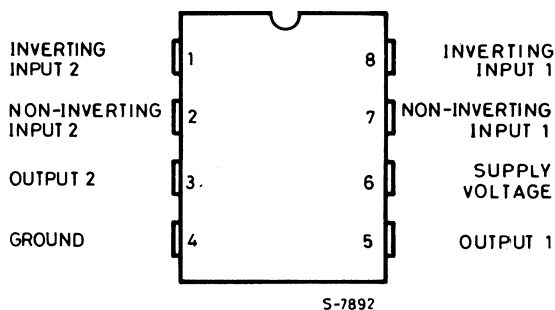
ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	(*) 20	V
I_C	Output current	1.2	A
V_I	Input voltage range	-0.2 to 24	V
V_I	Differential input voltage	24	V
T_{stg}	Storage temperature	-65 to + 150	°C
T_{OP}	Operating room temperature - free air	-45 to + 85	°C
I_{zs}	Zener clamp current (DC)	30	mA
	(PULSED) (**) 80		mA
P_{tot}	Power dissipation at $T_{amb} = 85^{\circ}\text{C}$	(intern. lim.) 650	mW
	Output short circuit protection: L9306	up to 16V	V
	L9306C	up to 12V	V
T_{JMAX}	Maximum junction temperature	150	°C

(*) The maximum allowed supply voltage without series resistors is limited by the built-in protection zener diodes.

(**) $T_{on} \leq 2.5\text{ms}$; Repetition time $\geq 30\text{ms}$

CONNECTION DIAGRAM (top view)



THERMAL DATA

$R_{thj-amb}$	Thermal resistance junction-ambient	max	100	°C/W
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ELECTRICAL CHARACTERISTICS ($V_{ST} = 14.4V$, $T_{amb} = 25^{\circ}C$ refer to block diagram unless otherwise specified)

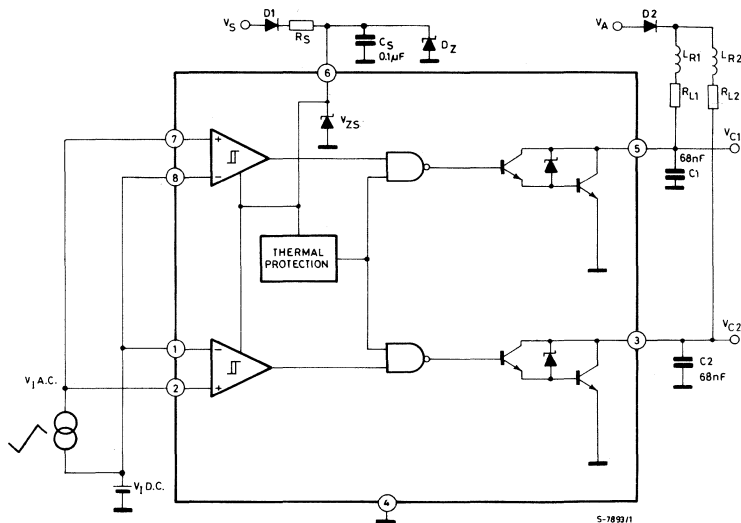
Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ST} Supply voltage		3.5		18 (*)	V
I_S "st. by" Supply current I_S "ON" Supply current	$V_I^+ - V_I^- \geq 70mV$ $V_I^- - V_I^+ \geq 70mV$		5 18	8 30	mA mA
V_{ZS} Voltage clamp - supply protection -	$I_{ZS} = 10mA$	20	23	27	V
V_{CSAT} On status saturation voltage voltage	$V_I^- - V_I^+ \geq 70mV$ for L9306 for L9306C $I_{COUT} = 300mA$ $I_{COUT} = 250mA$		0.8	1.4	V
I_{SC} Output short circuit current for each channel	$V_I^- - V_I^+ \geq 70mV$ for L9306 for L9306C	300 250	550 550	700 1200	mA mA
V_{CZ} Voltage clamp at the output - each channel	$I_{CZ} = 300mA$	20	24	27	V
I_{OL} Output leakage current	$V_I^+ - V_I^- \geq 70mV$ $T_{amb} = 25^{\circ}C$			500	μA
I_B Input bias current	$V_I^+ = V_I^- = 0$		0.2	1	μA
I_{OS} Input offset current	$V_I^+ = V_I^- = 0$		± 20	± 200	nA
V_{IH} Hysteresis of the input comparator	$V_{IN} = 200mV_{pp}$ $f = 1kHz$	20		70	mV
CMR Input common mode range	$V_{ST} = 3.5$ to $18V$	0	$V_{ST}-1.6V$		V

(*) The maximum allowed supply voltage without limiting resistors is limited by the built-in protection zener diodes: see V_{CZ} , V_{ZS} spec. values



L9306
L9306C

TEST AND APPLICATION CIRCUIT



APPLICATION INFORMATIONS (Refer to application circuit)

Capacitors C1 and C2 are necessary to cut high frequency gain during current limiting and D1 and D2 diodes are required only for reverse polarity protection.

If V_S may be higher than V_{ZS} a resistor R_S is necessary to limit the zener current I_{ZS} . In order to determine R_S value the following equations can be used:

$$1) \frac{V_{S\text{MAX}} - V_{D1} - V_{ZS\text{min}}}{R_S} < I_{ZS\text{MAX}}$$

$$2) V_{S\text{min}} - V_{D1} - R_S - I_{SON\text{MAX}} > V_{ST\text{min}}$$

where from $T_{\text{amb}} = 25^\circ\text{C}$:

- $V_{S\text{MAX}}$ and $V_{S\text{min}}$ are the maximum and minimum values of power supply voltage
- V_{D1} is the forward diode D1 voltage drop
- $V_{ZS\text{min}} = 20\text{V}$

– $I_{ZS\text{MAX}} = 30\text{mA}$ for d.c. mode and $I_{ZS\text{MAX}} = 80\text{mA}$ for pulsed mode (see Absolute maximum ratings)

– $I_{SOM\text{MAX}} = 30\text{mA}$

– $V_{ST\text{min}} = 3.5\text{V}$

If no R_S value can satisfy the system 1), 2) a more powerfull external zener $D_Z = 18\text{V}$ is required.

Then 1) becomes:

$$\frac{V_{S\text{MAX}} - V_{D1} - 18}{R_S} < I_{DZ\text{MAX}}$$

where $I_{DZ\text{MAX}}$ is the maximum allowed D_Z current.

V_A voltage cannot be higher than 20V otherwise output overvoltage protection may be activated. Moreover V_A must be less than 16V (for L9306) or 12V (for L9306C) if short circuit protection is required.



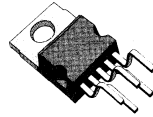
L9335 L9336

ADVANCE DATA

SOLENOID DRIVERS

- WIDE SUPPLY VOLTAGE RANGE 6 TO 24V
- INTERNAL CURRENT SENSING
- PRECISION OUTPUT CURRENT LEVELS 2.4A/0.6A (L9335) AND 4A/1A (L9336)
- LOW OUTPUT SATURATION VOLTAGE 2.5V AT $I_O = 1.5A$ (L9335) AND 3V AT $I_O = 3A$ (L9336)
- WIDE OPERATION JUNCTION TEMPERATURE RANGE $-40^{\circ}C$ TO $150^{\circ}C$
- MICROPROCESSOR COMPATIBLE INPUT
- DISABLE INPUT APPLICABLE FOR SWITCHING OFF DURING LOAD DUMP
- INTERNAL COMPENSATION
- INTERNAL SUPPLY STABILIZING ZENER DIODE

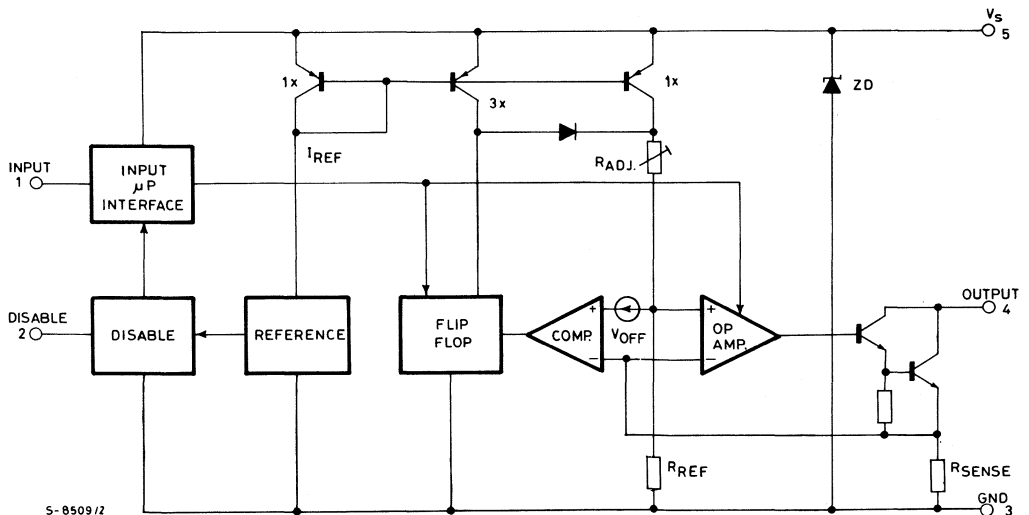
The L9335 and L9336 are monolithic integrated constant current sink drivers with internal current sensing and precision stable output current. The output current waveform for inductive load with switching to the holding current level after the peak current level has been reached is fitted for driving fuel injectors.



Pentawatt

ORDERING NUMBER: L9335
L9336

BLOCK DIAGRAM





L9335
L9336

ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	-1 to 24	V
V_{SD}	Supply voltage dump transient (*)	60	V
V_i	Input voltage	-6 to 24	V
I_S	Supply current	50	mA
I_{SD}	Supply current dump transient	150	mA
T_{OP}	Operating junction temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

(*) Test circuit of Fig. 1

CONNECTION DIAGRAM

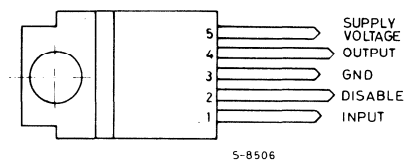
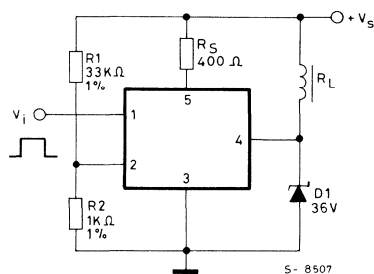


Fig. 1 - Test circuit





L9335
L9336

PIN FUNCTION

N°	NAME	FUNCTIONS
1	INPUT	Logical input. If high, output current sink stage is activated.
2	DISABLE	Voltage at this pin higher than the disable threshold disables the output stage and reset the reference to the I_{OP} value.
3	GRUOND	Common ground terminal.
4	OUTPUT	Open collector output of the current sink darlington transistor.
5	SUPPLY	Internal zener diode between pin 5 and 3 stabilizes the supply voltage for the signal processing circuitry.

THERMAL DATA

$R_{thj-case}$	Thermal resistance junction case	max	4	$^{\circ}C/W$
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ELECTRICAL CHARACTERISTICS ($V_S = 14.4V$; $T_j = 25^{\circ}C$, unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
I_{OP}	Output peak current (L9335) (L9336)	$V_1 = 5V$	$V_2 = 0$	1.74 3.4	2.3 4.2	2.8 5.1	A
I_{OH}	Output hold current (L9335) (L9336)	$V_1 = 5V$	$V_2 = 0$	0.51 0.95	0.6 1.1	0.69 1.25	A
V_{OS}	Output saturation voltage (L9335) (L9336)	$I_O = 1.5A$ $I_O = 3A$	$V_1 = 5V$ $V_2 = 0$		1 1.5	2.5 3	V
I_{OL}	Output leakage current	$V_1 = 0$	$V_2 = 0$			1	mA
BV_O	Output sustaining voltage	$I_O = 2mA$; $V_1 = 0$; $V_2 = 0$		42			V
V_{IL}	Input low voltage					0.8	V
V_{IH}	Input high voltage			2			V
I_i	Input current	$V_1 = 5V$				450	μA
V_{2T}	Disable input threshold voltage			1.25	1.5	1.75	V
V_{2H}	Disable input hysteresis				50		mV
I_{DB}	Disable input bias current					450	μA
V_{ZD}	Supply stabilizing zener	$I_S = 20mA$		6	7.5	9	V
I_Q	Quiescent current	$V_S = 5.5V$			2.5	10	mA



L9342

ADVANCE DATA

SIX-SOLENOID DRIVER

- DRIVES SIX INJECTOR SOLENOIDS
- CUTOFF FUNCTION
- ADJUSTABLE PEAK CURRENT
- INJECTOR STATUS OUTPUT
- TTL-COMPATIBLE INPUTS
- LOW POWER CONSUMPTION
- WIDE TEMPERATURE RANGE
- HIGH DENSITY I²L/LINEAR TECHNOLOGY

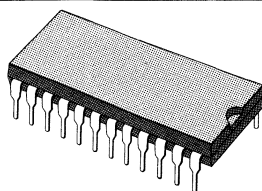
Designed for multipoint fuel injection systems, the L9342 Multipoint Injector Driver includes six drivers for external darlingtons with TTL-compatible inputs and circuitry which controls the peak current.

A separate logic input controls each driver. In addition a common logic input enables all six

and a single reference input sets the peak current level. A status feedback output allows the control processor to monitor correct operation.

The L9342 is realized with a high density mixed I²L/analog technology.

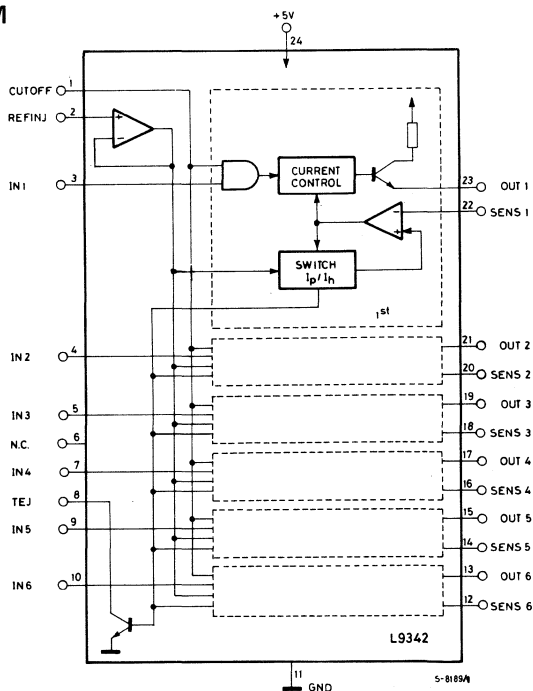
Features include low power consumption and a wide operating temperature range.



DIP-24 Plastic

ORDERING NUMBER: L9342

BLOCK DIAGRAM



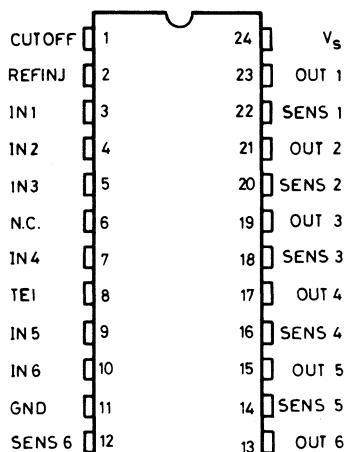


L9342

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	5.25	V
V_i	Input voltage	5.25	V
T_j	Operating junction temperature	-40 to 125	°C
T_{stg}	Storage temperature	-65 to 150	°C
I_{te}	Test pin output current	300	μ A

CONNECTION DIAGRAM



S-8188

THERMAL DATA

$R_{th j-amb}$	Thermal resistance junction-ambient	max	100	°C/W
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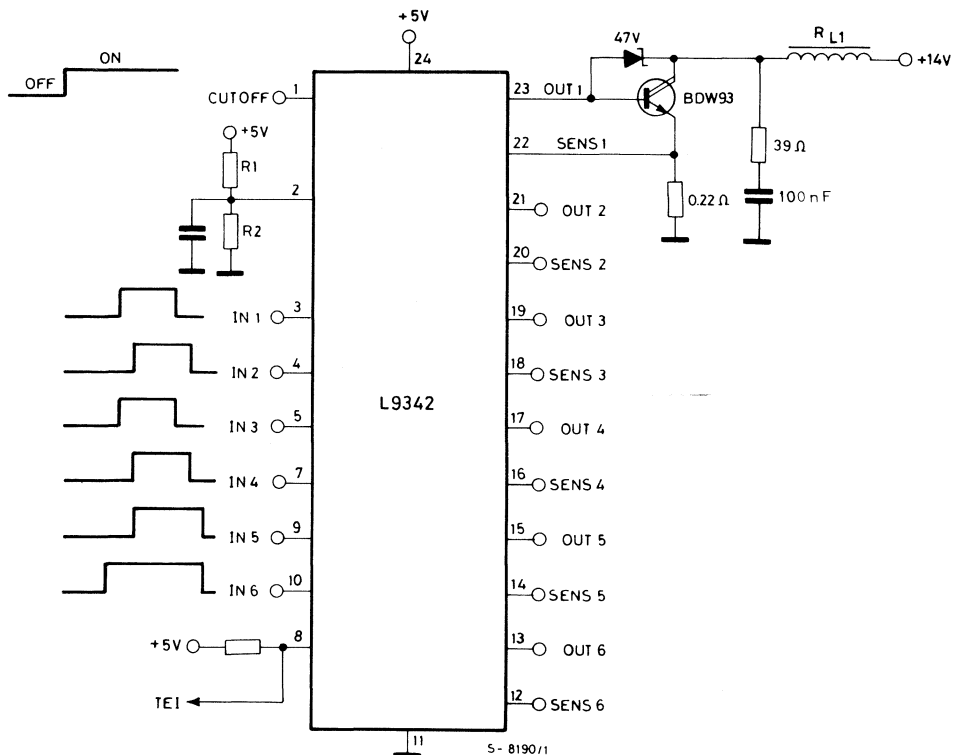
**L9342****PIN FUNCTIONS**

N°	NAME	FUNCTION
1	CUTOFF	Enable input. When this pin is high the six drivers are enabled. When this input is low all six outputs are OFF, irrespective of the inputs.
2	REFINJ	Injector reference. A voltage applied to this pin sets the peak current $I_p = V_{REFINJ}/R_S$. The hold current is $I_h = \frac{I_p}{6}$
3, 4, 5 7, 9, 10	IN1 - IN6	Injector logic inputs. The output at each driver is active when its input is high.
8	TEI	Injector test output; an open-collector output used to monitor injector operation. This output is inactive until the injector current reaches the peak value. It remains active during the hold phase.
12, 14, 16 18, 20, 22	SENS1 - SENS2	Current sensing feedback inputs for the six drivers.
13, 15, 17 19, 21, 23	OUT1 - OUT6	Outputs for power darlington driving.

ELECTRICAL CHARACTERISTICS ($V_S = 5V$; $T_j = 25^\circ C$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		4.75	5	5.25	V
I_S	Supply Current			15		mA
V_{IH}	Input High Voltage		2.5		V_S	V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	$V_{IH} = 2.5V$		120		μA
I_{IL}	Input Low Current	$V_{IL} = 0.4V$		18		μA
I_O	Output Current	$V_O = 1.4V$		36	50	mA
I_i	Input Current at pin 2			100	150	nA
BV_{CEO}	Collector emitter output voltage	$I_C = 10\mu A$	10			V
R_i	Input Resistance (pin 1, 3, 4, 5, 7, 9, 10)			22		K Ω
$\frac{I_p}{I_h}$	Peak to holding current ratio		5.7	6	6.3	

Fig. 1 – Application circuit



CIRCUIT OPERATION

The L9342 is enabled when the CUTOFF input is high and the desired peak current has been set by a voltage applied to the REFINJ input.

In this condition when one of the input pins (IN1, IN2...) goes high the corresponding output will be activated and the current in the injector solenoid will rise.

When this current reaches the peak level I_p , where the voltage across R_S is equal to REFINJ, the output current is reduced to the holding level I_h ($I_p/6$).

The output remains active as long as the input is high.

The TE1 output goes low when the load current has reached the peak value.

In a typical system this output is tested by the controlling microprocessor to monitor injector operation. If it goes low in a shorter time than the injector's fastest opening time, there must be a short circuit in the injector coil or cable. If it remains high ever when sufficient time has elapsed for the injector to open the injector solenoid or cable must be open circuit.

The values of the RC dumping network components must be tuned depending on the load and can be chosen between $39\Omega/100nF$ and $1K\Omega/6.8nF$.

CIRCUIT OPERATION (continued)

Fig. 2 - Timing

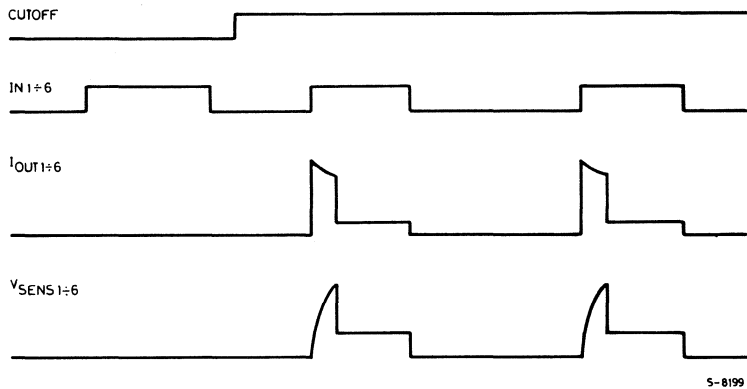
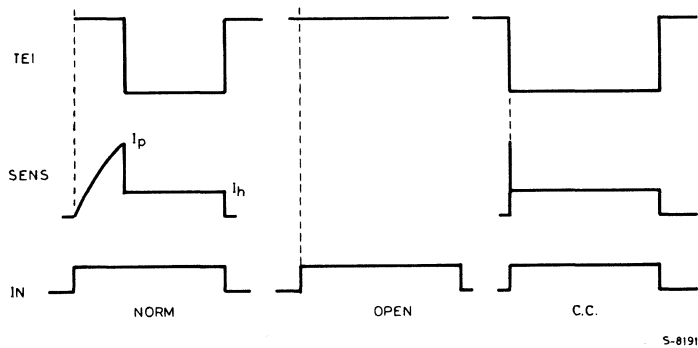


Fig. 3 - Injector test timing





L9350

ADVANCE DATA

LOW SATURATION DRIVER

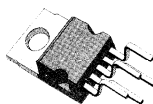
- LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUT
- WIDE SUPPLY VOLTAGE
- NO EXTERNAL COMPONENTS
- INTERNAL RECIRCULATION PATH FOR FAST DECAY OF INDUCTIVE LOAD CURRENT
- SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN
- LOAD DUMP AND REVERSE BATTERY PROTECTION
- FAILSAFE OPERATION: OUTPUT IS OFF IF THE LOGIC INPUT IS LEFT OPEN

The L9350 is a monolithic integrated circuit designed to drive grounded resistive, inductive or mixed loads from the power supply positive side. Very low stand-by current ($100\mu\text{A}$ typ.) and internally implemented protections against load dump and reverse voltages make the device very useful in automotive applications.

No external components are required because the output recirculation clamping zener is included in the chip. This zener can withstand an initial current of 550mA going down through an 80mH and 25Ω load.

Other safety features of the device include thermal shutdown, short circuit protection, a supply voltage range of $4.5 - 24\text{V}$ and a shut off condition of the output if the logic input (pin 5) is left open.

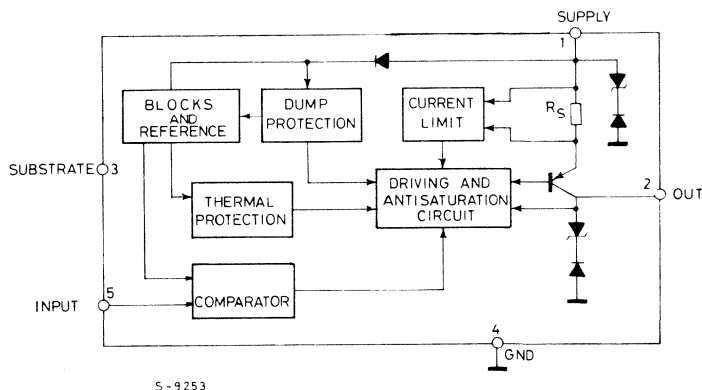
ON and OFF delay times of $25\mu\text{s}$ max in any output status, including recirculating situation, allows PWM use of L9350.



Pentawatt

ORDERING NUMBER: L9350

BLOCK DIAGRAM



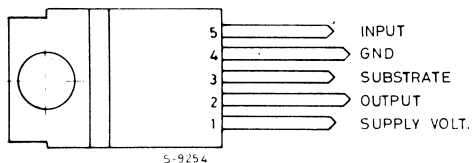


L9350

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	24	V
V_i	Input voltage	-0.85 to V_s	
I_o	Output current	internally limited	
V_D	Positive transient peak voltage (time constant $< 100\text{ms}$)	60	V
V_d	Transient peak voltage (time constant $< 1\text{ms}$ $R_s > 10\Omega$)	± 120	V
V_R	Reverse voltage	-13	V
P_{tot}	Total power dissipation at $T_{\text{case}} = 90^\circ\text{C}$	17	W
T_{op}	Operating junction temperature	-40 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature	-65 to 150	$^\circ\text{C}$

CONNECTION DIAGRAM



Note: pin 3 must be left open or connected to ground

THERMAL DATA

$R_{\text{th j-amb}}$	Thermal resistance junction-ambient	max	60	$^\circ\text{C/W}$
$R_{\text{th j-case}}$	Thermal resistance junction-case	max	3.5	$^\circ\text{C/W}$

**L9350****ELECTRICAL CHARACTERISTICS** ($V_s = 14.4V$, $T_j = +25^{\circ}C$, unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s Operating supply voltage		4.5		24	V
V_{AH} Input voltage High	$4.5 < V_s < 24V$	2			V
V_{AL} Input voltage Low				0.8	
I_I Input current	$0.8 < V_I < 5.5V$		20	50	μA
I_I Output leakage current	$V_O = 0V$ $V_s = 24V$ $V_I < 0.8V$			1	mA
V_{sat} Output saturation voltage	$I_O = 150mA$ $V_s = 4.5V$		0.3	0.6	V
	$I_O = 400mA$ $V_s = 14.4V$		0.5	0.7	V
	$I_O = 550mA$ $V_s = 14.4V$		0.7	1	V
I_{sc} Output short circuit current			1.5		A
I_Q Quiescent current	$V_I > 2V$		50	80	mA
	$V_I < 0.8V$ stand-by condition		100	200	μA
V_{zo} Negative output zener voltage	$R_L = 25\Omega$ $L = 80mH$ on V_I transition from "1" to "0"	-36	-30	-24	V
t_{on} Turn ON delay	Only resistive load $R_L = 25\Omega$ (Fig. 2)			20	μs
t_{off} Turn OFF delay				25	μs
t_{dc} Turn ON delay while output is clamped	$R_L = 25$ $L = 80mH$ any time during clamping interval (Fig. 3)			20	μs

For $V_s > 26$ the device is not operating.

Fig. 1 – Automotive application circuit

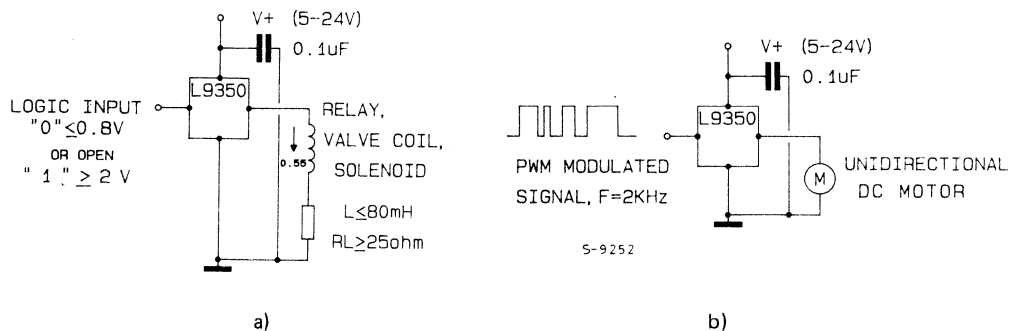


Fig. 2 – Resistive load

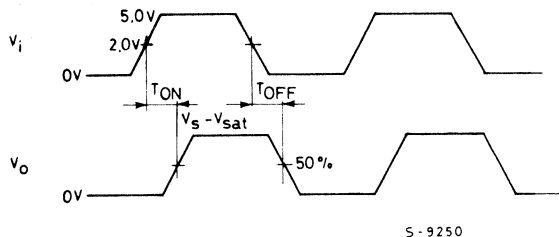


Fig. 3 – Inductive load

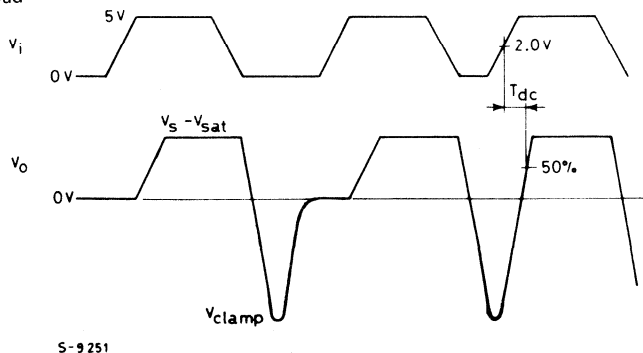


Fig. 4 - 5V self-oscillating SMPS

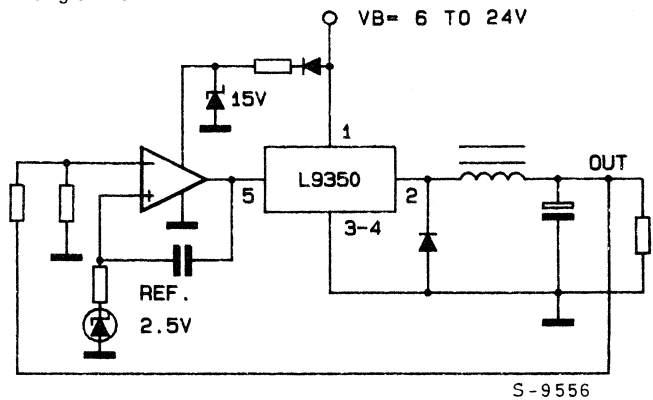
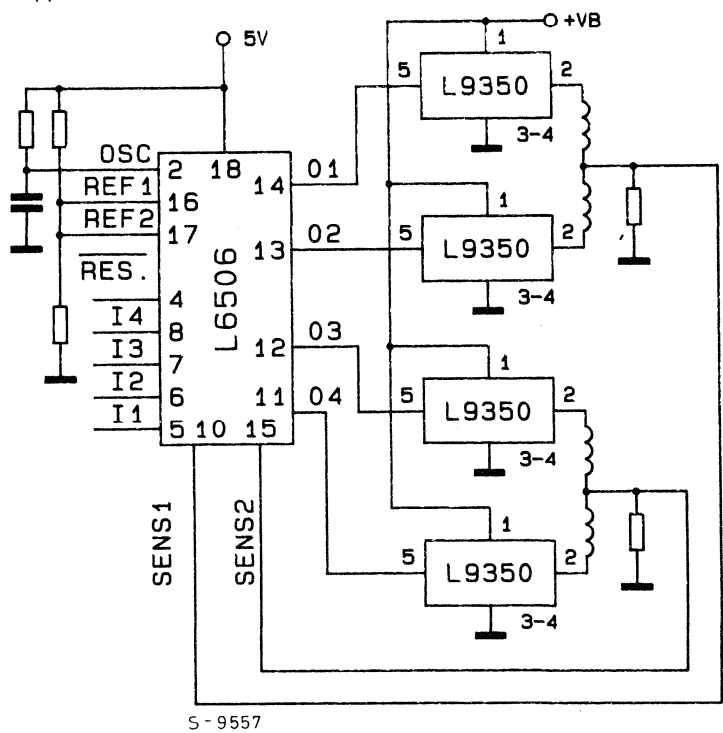


Fig. 5 - DC stepper motor driver





M5450 M5451

PRELIMINARY DATA

LED DISPLAY DRIVERS

- M5450 34 OUTPUTS/15mA SINK
- M5451 35 OUTPUTS/15mA SINK
- CURRENT GENERATOR OUTPUTS (NO EXTERNAL RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- ENABLE (ON M5450)
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples:

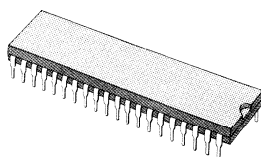
- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5450 and M5451 are monolithic MOS integrated circuits produced with an N-channel

silicon gate technology. They are available in 40-pin dual in-line plastic packages.

A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD} or to a separate supply of 13.2V maximum.

The M5450 and M5451 are improved pin-to-pin replacements of the NS MM 5450 and MM 5451.



DIP-40 Plastic

ORDERING NUMBERS: M5450 B7
M5451 B7

ABSOLUTE MAXIMUM RATINGS

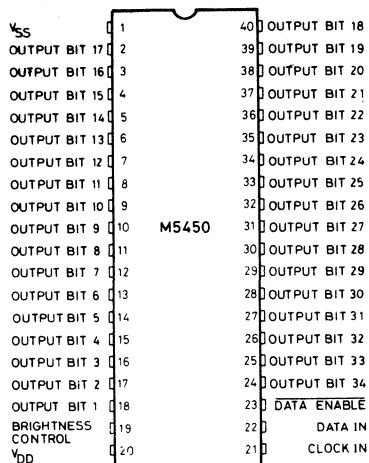
V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	1W
		at 85°C	560 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

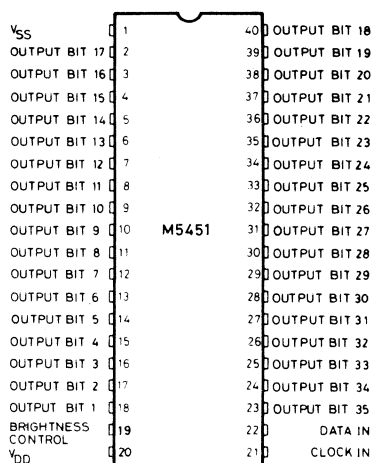


M5450
M5451

CONNECTION DIAGRAMS



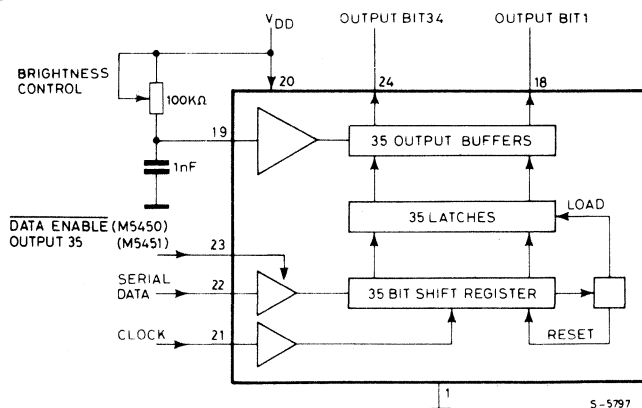
S-5795



S-5796

BLOCK DIAGRAM

Fig. 1



S-5797



M5450
M5451

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, $V_{DD} = 4.75V$ to $13.2V$, $V_{SS} = 0V$, unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD} Supply Voltage		4.75		13.2	V
I_{DD} Supply Current	$V_{DD} = 13.2V$			7	mA
V_I Input Voltage Logical "0" Level Logical "1" Level	$\pm 10 \mu A$ input bias $4.75 \leq V_{DD} \leq 5.25$ $V_{DD} > 5.25$	-0.3 2.2 $V_{DD}-2$		0.8 V_{DD} V_{DD}	V V V
I_B Brightness Input Current (note 2)		0		0.75	mA
V_B Brightness Input Voltage (pin 19)	Input current = $750 \mu A$	3		4.3	V
$V_{O(off)}$ Off State Out. Voltage				13.2	V
I_O Out. Sink Current (note 3) Segment OFF Segment ON	$V_O = 3V$ $V_O = 1V$ (note 4) Brightness In. = $0 \mu A$ Brightness In. = $100 \mu A$ Brightness In. = $750 \mu A$	0 2 12	2.7 15	10 10 4 25	μA μA mA mA
f_{clock} Input Clock Frequency		0		0.5	MHz
I_O Output Matching (note 1)				± 20	%

- Notes :**
1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.
 2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
 3. Absolute maximum for each output should be limited to 40 mA.
 4. The V_O voltage should be regulated by the user. See figures 5 and 6 for allowable V_O versus I_O operation.

FUNCTIONAL DESCRIPTION

Both the M5450 and the M5451 are specifically designed to operate 4 or 5-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time.

Display brightness is determined by control of the output current LED displays.

A 1nF capacitor should be connected to brightness control, pin 19, to prevent possible oscillations.

A block diagram is shown in figure 1. For the M5450 a DATA ENABLE is used instead of the 35th output. The DATA ENABLE input is a metal option for the M5450.



FUNCTIONAL DESCRIPTION (continued)

The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400 Ω nominal value.

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.

At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Bit 1 is the first bit following the start bit and it will appear on pin 18. A logical "1" at the input will turn on the appropriate LED.

Figure 3 shows the timing relationship between Data, Clock and DATA ENABLE.

A max clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT} .

The following equation can be used for calculations.

$$T_j = [(V_{OUT}) (I_{LED}) (\text{No. of segments}) + (V_{DD} \cdot 7 \text{ mA})] (124^\circ\text{C/W}) + T_{amb}$$

where:

T_j = junction temperature (150°C max)

V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

124°C/W = thermal coefficient of the package

T_{amb} = ambient temperature

The above equation was used to plot figure 4, 5 and 6.

Fig. 2 - Input Data Format

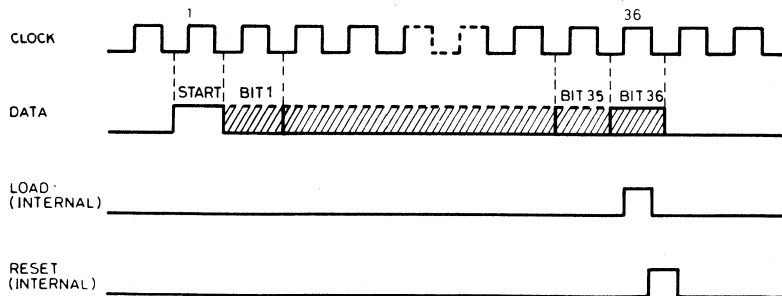
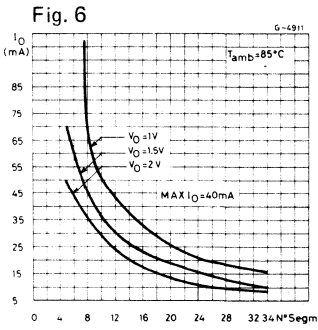
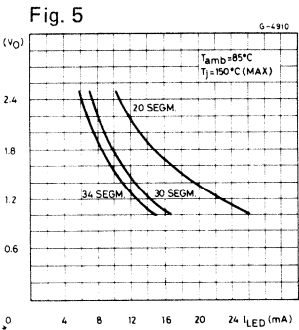
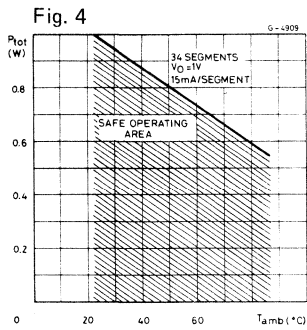
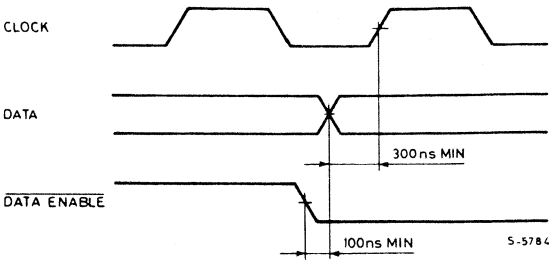
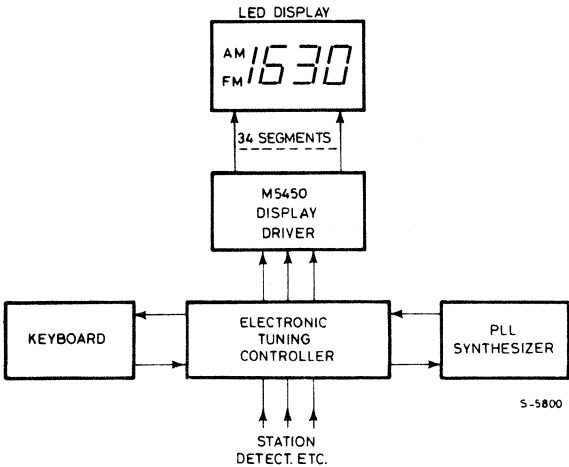


Fig. 3



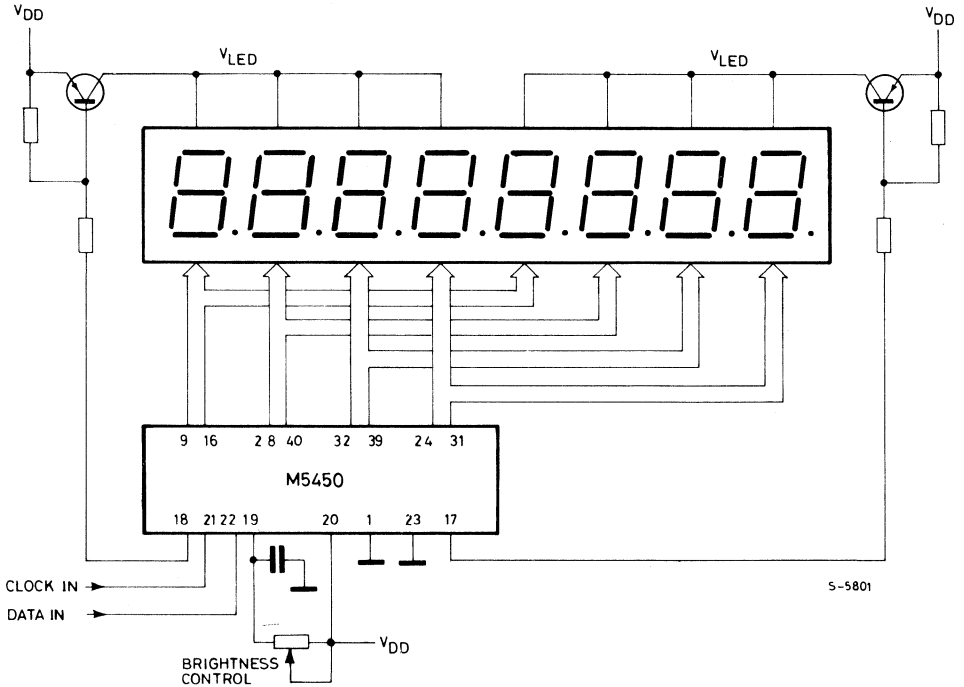
TYPICAL APPLICATIONS

Basic electronically tuned Radio or TV system



TYPICAL APPLICATIONS (continued)

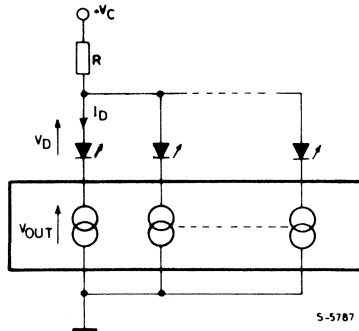
Duplexing 8 Digits with One M5450



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)



In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated

$$R = \frac{V_C - V_{D\ MAX} - V_{O\ MIN}}{N_{MAX} \cdot I_D}$$

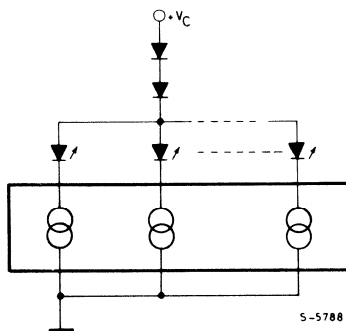
The worst case condition for the device is when roughly half of the maximum number of segments are activated.

It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.

In critical cases more resistors can be used in conjunction with groups of segments.

In this case the current variation in the single resistor is reduced and P_{tot} limited.

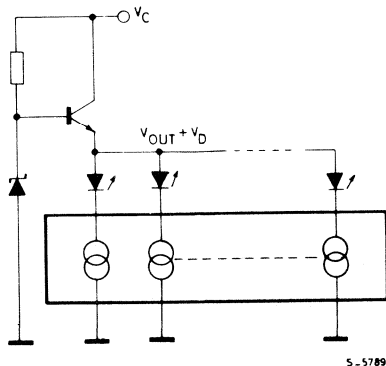
b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.

The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.

c)



In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.



M5480

LED DISPLAY DRIVER

- 3 DIGIT LED DRIVER (23 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- NO LOAD SIGNAL REQUIRED
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

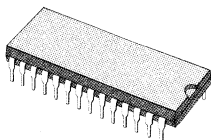
Applications examples:

- MICROPROCESSOR DISPALYS
- INDUSTRIAL CONTROL INDICATION
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5480 is a monolithic MOS integrated circuit produced with a N-channel silicon gate

technology. It utilizes the M5451 die packaged in a 28-pin plastic package making it ideal for a 3½ digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.

The M5480 is an improved pin-to-pin replacement of the NS MM 5480.



DIP-28 Plastic

ORDERING NUMBER : M5480 B7

ABSOLUTE MAXIMUM RATINGS

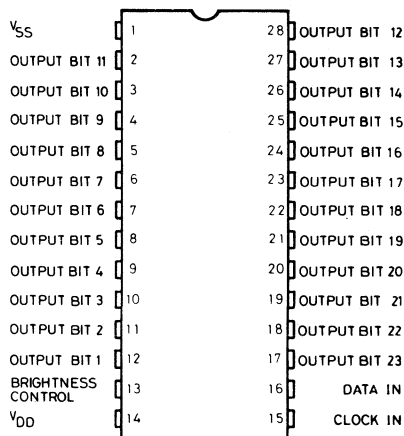
V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C 940 mW	
		at 85°C 490 mW	
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



M5480

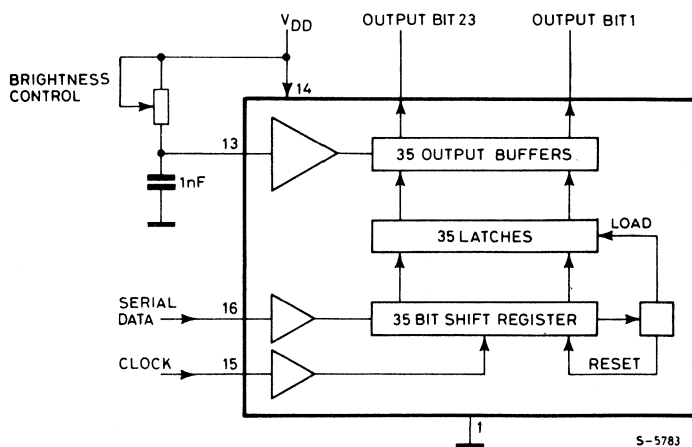
CONNECTION DIAGRAM



S-5782

BLOCK DIAGRAM

Fig. 1



**M5480****STATIC ELECTRICAL CHARACTERISTICS** (T_{amb} within operating range, $V_{DD} = 4.75V$ to $13.2V$, $V_{SS} = 0V$, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	$V_{DD} = 13.2V$			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	$\pm 10 \mu A$ Input Bias $4.75 \leq V_{DD} \leq 5.25$ $V_{DD} > 5.25$	-0.3 2.2 $V_{DD}-2$		0.8 V_{DD} V_{DD}	V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 13)	Input Current = $750 \mu A$	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	$V_O = 3V$ $V_O = 1V$ (note 4) Brightness In. = $0 \mu A$ Brightness In. = $100 \mu A$ Brightness In. = $750 \mu A$	0 2 12	2.7 15	10 4 25	μA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

- Notes:**
1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.
 2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
 3. Absolute maximum for each output should be limited to 40 mA.
 4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5480 is specifically designed to operate $3\frac{1}{2}$ digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.

Outputs change only if the serial data bits differ from the previous time.

Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 13, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 13, which is set by an external variable resistor.

There is an internal limiting resistor of 400Ω nominal value.

FUNCTIONAL DESCRIPTION (continued)

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.

At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data, and Clock. A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the 5480. Because it uses only 23 of the possible 35 outputs, 12 of the bits are "Don't Care".

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT} .

The following equation can be used for calculations.

$$T_j = [(V_{OUT}) (I_{LED}) (\text{No. of segments}) + V_{DD} \cdot 7 \text{ mA}] (132^\circ\text{C/W}) + T_{amb}$$

where:

T_j = junction temperature (150°C max)

V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

132°C/W = thermal coefficient of the package

T_{amb} = ambient temperature

Fig. 2 - Input Data Format

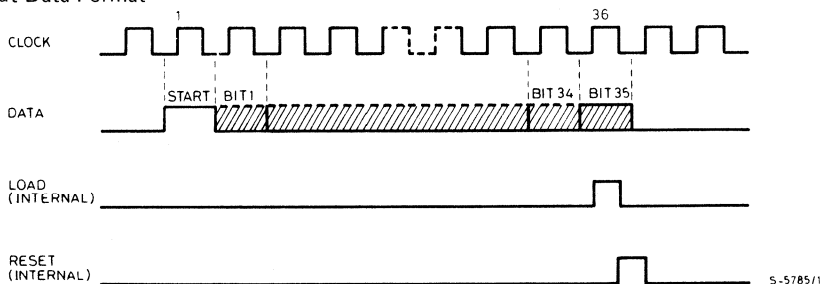


Fig. 3

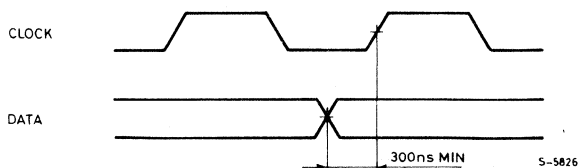
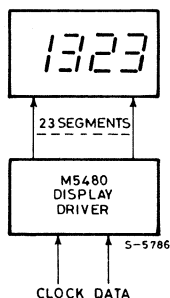


Fig. 4 - Serial Data Bus/Outputs Correspondence

5451	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5480	X	X	23	22	21	20	19	X	X	18	X	17	16	15	14	13	12	X	X	X	11	10	9	8	X	X	X	7	6	5	4	3	2	1	X	START

TYPICAL APPLICATION

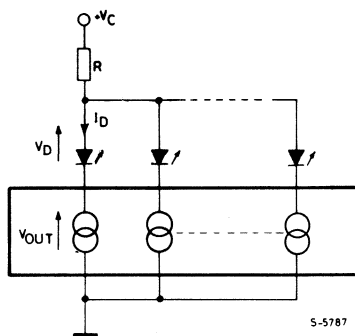
BASIC 3½ Digit interface.



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)



In this application R must be chosen taking into account the worst operating conditions. R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D \text{ MAX}} - V_{OUT \text{ MIN}}}{N_{MAX} \cdot I_D}$$

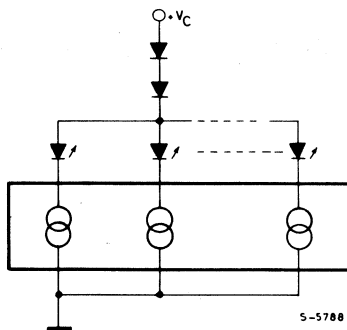
The worst case condition for the device is when roughly half of the maximum number of segments are activated.

It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.

In critical cases more resistors can be used in conjunction with groups of segments.

In this case the current variation in the single resistor is reduced and P_{tot} limited.

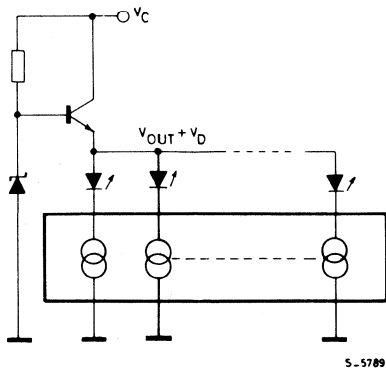
b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.

The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.

c)



In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.



M5481

LED DISPLAY DRIVER

- 2 DIGIT LED DRIVER (14 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTOR REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- DATA ENABLE
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

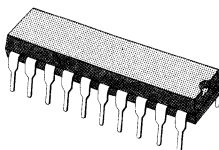
Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5481 is a monolithic MOS integrated circuit produced with a N-channel silicon gate

technology. It utilizes the M5450 die packaged in a 20-pin plastic package copper frame, making it ideal for a 2-digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.

The M5481 is an improved pin-to-pin replacement of the NS MM 5481.



**DIP-20 Plastic
(0.25)**

ORDERING NUMBER: M5481 B7

ABSOLUTE MAXIMUM RATINGS

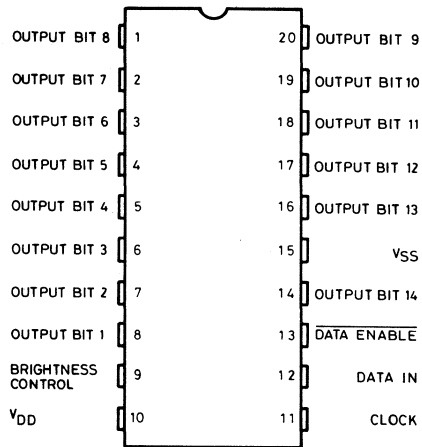
V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C 1.5W	
		at 85°C 800 mW	
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



M5481

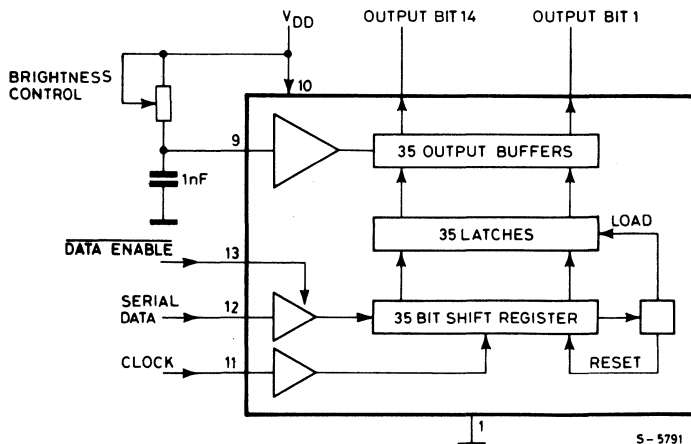
CONNECTION DIAGRAM



S-5790

BLOCK DIAGRAM

Fig. 1



S-5791

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, $V_{DD}= 4.75V$ to $13.2V$, $V_{SS}= 0V$, unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD} Supply Voltage		4.75		13.2	V
I_{DD} Supply Current	$V_{DD}= 13.2V$			7	mA
V_I Input Voltages Logical "0" Level Logical "1" Level	$\pm 10 \mu A$ Input Bias $4.75 \leq V_{DD} \leq 5.25$ $V_{DD} > 5.25$	-0.3 2.2 $V_{DD}-2$		0.8 V_{DD} V_{DD}	V V V
I_B Brightness Input Current (note 2)		0		0.75	mA
V_B Brightness Input Voltage (pin 9)	Input Current = $750 \mu A$	3		4.3	V
$V_{O(off)}$ Off State Output Voltage				13.2	V
I_O Output Sink Current (note 3) Segment OFF Segment ON	$V_O = 3V$ $V_O = 1V$ (note 4) Brightness In. = $0 \mu A$ Brightness In. = $100 \mu A$ Brightness In. = $750 \mu A$	0 2 12	2.7 15	10 10 4 25	μA μA mA mA
f_{clock} Input Clock Frequency		0		0.5	MHz
I_O Output Matching (note 1)				± 20	%

- Notes:**
1. Output matching is calculates as the percent variation from $I_{MAX} + I_{MIN}/2$.
 2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
 3. Absolute maximum for each output should be limited to 40 mA.
 4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5481 uses the M5450 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal.

The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.

These is an internal limiting resistor of 400Ω nominal value.

FUNCTIONAL DESCRIPTION (continued)

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.

At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data, Clock and $\overline{\text{DATA ENABLE}}$. A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the M5481. Because it uses only 14 of the possible 35 outputs, 21 of the bits are "Don't Cares".

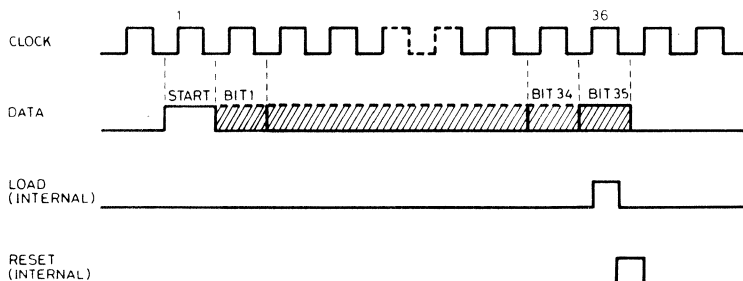
For applications where a lesser number of outputs are used it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT} . The following equation can be used for calculations.

$$T_j \equiv [(V_{\text{OUT}}) (I_{\text{LED}}) (\text{No. of segments}) + V_{\text{DD}} \cdot 7 \text{ mA}] (80^\circ\text{C/W}) + T_{\text{amb}}$$

where:

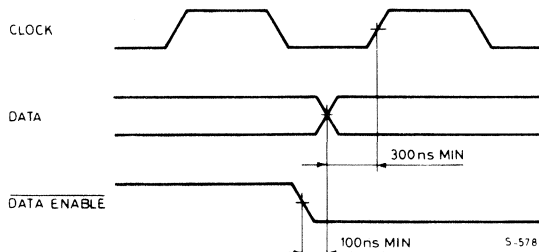
- T_j = junction temperature (150°C max)
- V_{OUT} = the voltage at the LED driver outputs
- I_{LED} = the LED current
- 80°C/W = thermal coefficient of the package
- T_{amb} = ambient temperature

Fig. 2 - Input Data Format



S-5785/1

Fig. 3



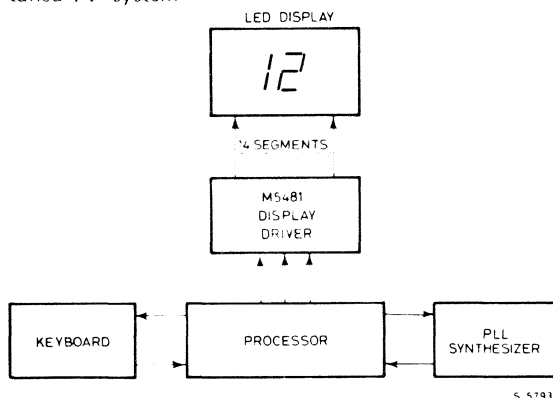
S-5784

Fig. 4 – Serial Data Bus/Outputs Correspondence

5450	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5481	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	START	

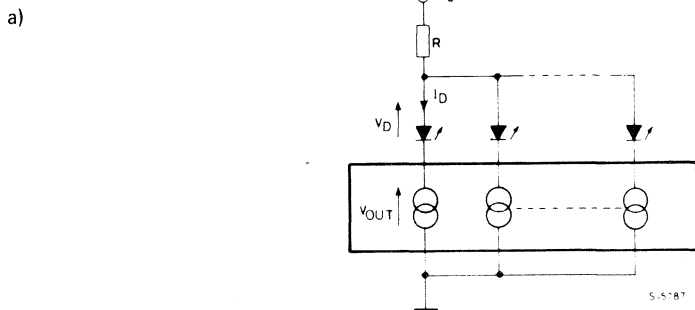
TYPICAL APPLICATION

BASIC electronically tuned TV system



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

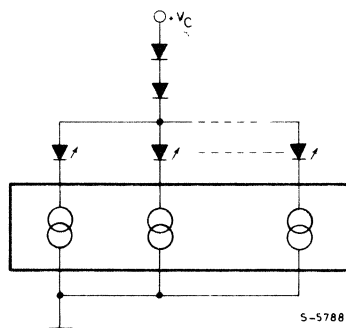


In this application R must be chosen taking into account the worst operating conditions. R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_D \text{ MAX} - V_O \text{ MIN}}{N_{\text{MAX}} \cdot I_D}$$

The worst case condition for the device is when roughly half of the maximum number of segments are activated. It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device. In critical cases more resistors can be used in conjunction with groups of segments. In this case the current variation in the single resistor is reduced and P_{Tot} limited.

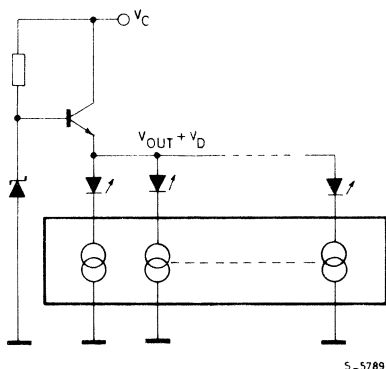
b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.

The total power dissipation of the IC is, in first approximation, depending only on the number of segments activated.

c)



In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.



M5482

LED DISPLAY DRIVER

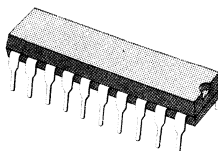
- 2 DIGIT LED DRIVER (15 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTOR REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5482 is a monolithic MOS integrated circuit produced with an N-channel silicon gate

technology. It utilizes the M5450 die packaged in a 20-pin plastic package copper frame, making it ideal for a 2-digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.



DIP-20 Plastic
(0.25)

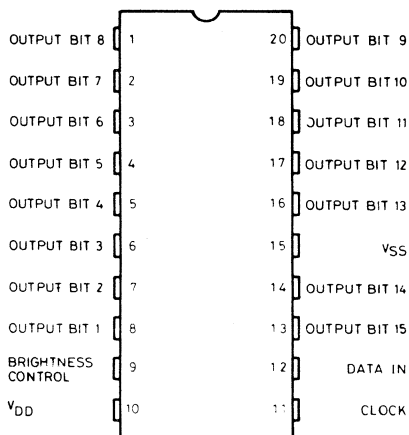
ORDERING NUMBER: M5482 B7

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C 1.5W at 85°C 800 mW	
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

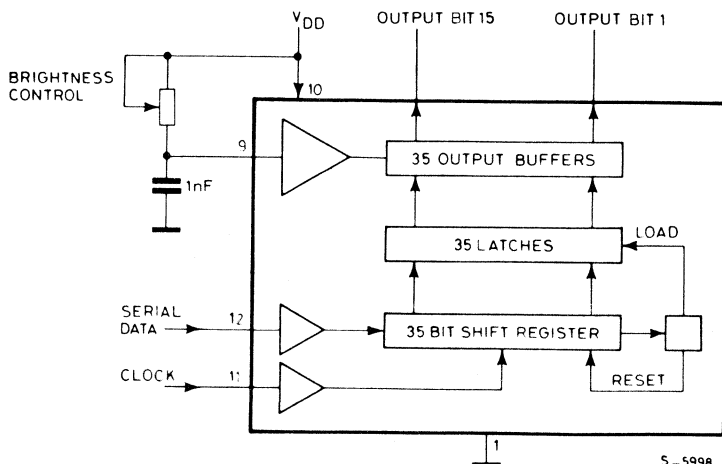
CONNECTION DIAGRAM



S-5997

BLOCK DIAGRAM

Fig. 1



S-5998

**M5482**

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, $V_{DD} = 4.75V$ to $13.2V$, $V_{SS} = 0V$, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	$V_{DD} = 13.2V$			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	$\pm 10 \mu A$ Input Bias	-0.3		0.8	V
		$4.75 \leq V_{DD} \leq 5.25$	2.2		V_{DD}	V
		$V_{DD} > 5.25$	$V_{DD}-2$		V_{DD}	V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 9)	Input Current = $750 \mu A$	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	$V_O = 3V$			10	μA
		$V_O = 1V$ (note 4)				
		Brightness In. = $0 \mu A$	0		10	μA
		Brightness In. = $100 \mu A$	2	2.7	4	mA
		Brightness In. = $750 \mu A$	12	15	25	mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

- Notes:**
1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.
 2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
 3. Absolute maximum for each output should be limited to 40 mA.
 4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5482 uses the M5451 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal.

The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.

There is an internal limiting resistor of 400Ω nominal value.

FUNCTIONAL DESCRIPTION (continued)

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.

At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data and Clock.

A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the M5482. Because it uses only 15 of the possible 35 outputs, 20 of the bits are "Don't Cares".

For applications where a lesser number of outputs are used it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT} .

The following equation can be used for calculations.

$$T_j \equiv [(V_{OUT}) (I_{LED}) (\text{No. of segments}) + V_{DD} \cdot 7 \text{ mA}] (80^\circ\text{C/W}) + T_{amb}$$

where:

T_j = junction temperature (150°C max)

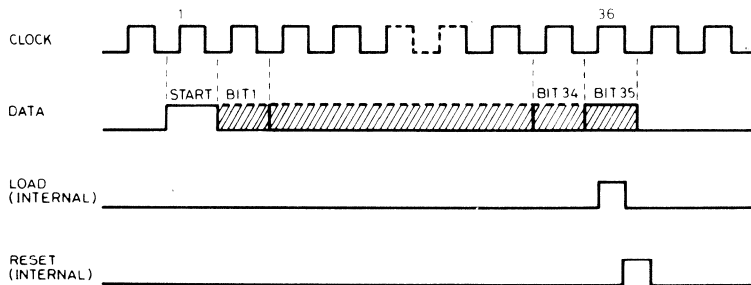
V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

80°C/W = thermal coefficient of the package

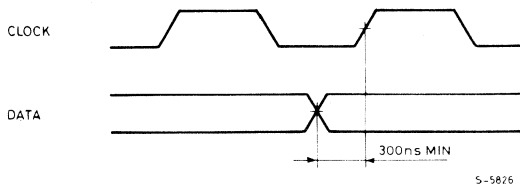
T_{amb} = ambient temperature

Fig. 2 - Input Data Format



S-5785/1

Fig. 3



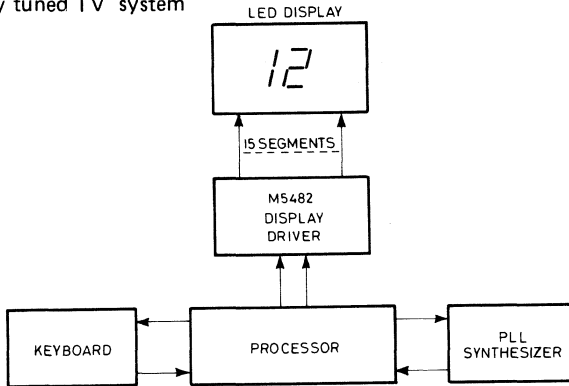
S-5826

Fig. 4 - Serial Data Bus/Outputs Correspondence

5451	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5482	15	X	X	X	X	14	13	X	X	X	X	12	11	10	9	X	X	X	X	8	7	6	5	X	X	X	X	4	3	2	1	X	X	X	X	START

TYPICAL APPLICATION

BASIC electronically tuned TV system

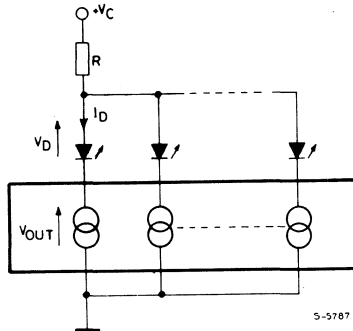


S-5999

POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)



S-5787

In this application R must be chosen taking into account the worst operating conditions.

R is determined by the maximum number of segments activated.

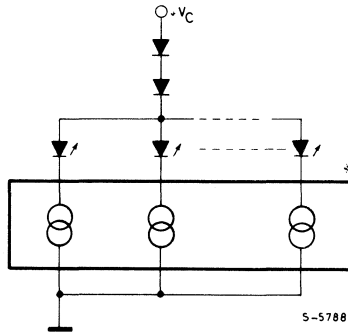
$$R = \frac{V_C - V_{D \text{ MAX}} - V_{O \text{ MIN}}}{N_{\text{MAX}} \cdot I_D}$$

The worst case condition for the device is when roughly half of the maximum number of segments are activated.

It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.

In critical cases more resistors can be used in conjunction with groups of segments. In this case the current variation in the single resistor is reduced and P_{tot} limited.

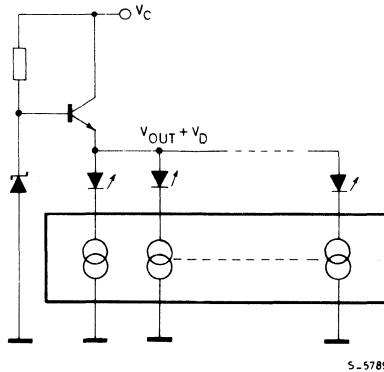
b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.

The total power dissipation of the IC is, in first approximation, depending only on the number of segments activated.

c)



In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.



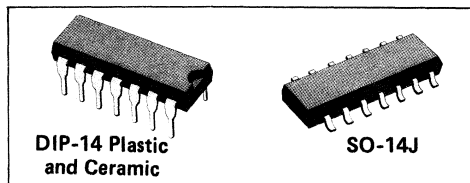
MC1488

RS232C QUAD LINE DRIVER

- CURRENT LIMITED OUTPUT $\pm 10\text{mA}$ TYP.
- POWER-OFF SOURCE IMPEDANCE 300Ω MIN.
- SIMPLE SLEW RATE CONTROL WITH EXTERNAL CAPACITOR
- FLEXIBLE OPERATING SUPPLY RANGE
- INPUTS ARE TTL AND μP COMPATIBLE

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in con-

formance with the specifications of EIA Standard No. RS232C.

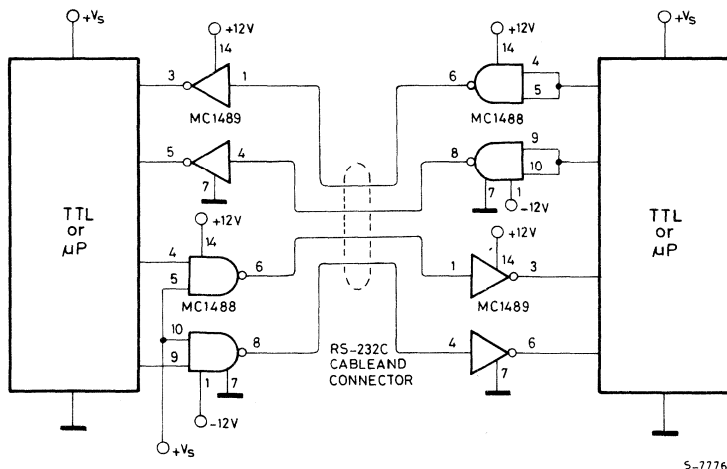


ORDERING NUMBER: MC1488P (Plastic DIP)
MC1488L (Ceramic DIP)
MC1488D (SO-14)

ABSOLUTE MAXIMUM RATINGS

V_S	Power supply voltage	15	V
V_{EE}	Power supply voltage	-15	V
V_{IR}	Input voltage range	$-15 \leq V_{IR} \leq 7$	V
V_O	Output signal voltage	± 15	V
T_{amb}	Operating ambient temperature	0 to 75	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-65 to 150	$^{\circ}\text{C}$

Typical Application: RS232C data transmission

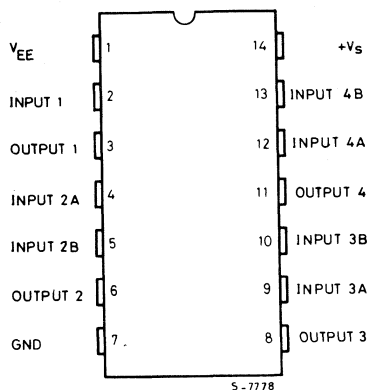


S-7776

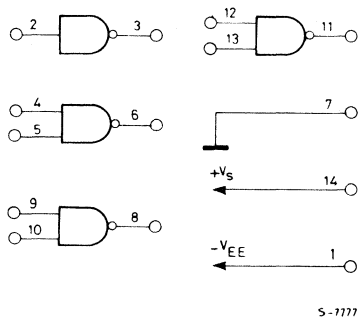


MC1488

CONNECTION DIAGRAM (top view)



LOGIC DIAGRAM



THERMAL DATA

			Plastic DIP-14	Ceramic DIP-14	SO-14
$R_{thj-amb}$	Thermal resistance junction-ambient	max	200°C/W	165°C/W	165°C/W

ELECTRICAL CHARACTERISTICS ($V_S = 9 \pm 10\% V$, $V_{EE} = -9 \pm 10\% V$, $T_{amb} = 0$ to $75^\circ C$ unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{IL} Input current	Low logic state ($V_{IL} = 0$)		1	1.6	mA	1
I_{IH} Input current	High logic state ($V_{IH} = 5V$)			10	μA	1
V_{OH} Output voltage	High logic state $R_L = 3K\Omega$ $V_{IL} = 0.8V$, $V_S = 9V$, $V_{EE} = -9V$ $V_{IL} = 0.8V$, $V_S = 13.2V$, $V_{EE} = -13.2V$	6 9	7 10.5		V V	2 2
V_{OL} Output voltage	Low logic state $R_L = 3K\Omega$ $V_{IH} = 1.9V$, $V_{EE} = -9V$, $V_S = 9V$ $V_{IH} = 1.9V$, $V_{EE} = -13.2V$, $V_S = 13.2V$	-6 -9	-7 -10.5		V V	2 2
I_{OS+} * Positive output short-circuit current		6	10	12	mA	3
I_{OS-} * Negative output short-circuit current		-6	-10	-12	mA	3
R_o Output resistance	$V_S = V_{EE} = 0$ $V_o = \pm 2V$	300			Ω	4

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_S Positive supply current ($R_I = \infty$)	$V_{IH} = 1.9V$ $V_S = 9V$ $V_{IL} = 0.8V$ $V_S = 9V$ $V_{IH} = 1.9V$ $V_S = 12V$ $V_{IL} = 0.8V$ $V_S = 12V$ $V_{IH} = 1.9V$ $V_S = 15V$ $V_{IL} = 0.8V$ $V_S = 15V$		15 4.5 19 5.5	20 6 25 7 34 12	mA	5
I_{EE} Negative supply current ($R_L = \infty$)	$V_{IH} = 1.9V$ $V_{EE} = -9V$ $V_{IL} = 0.8V$ $V_{EE} = -9V$ $V_{IH} = 1.9V$ $V_{EE} = -12V$ $V_{IL} = 0.8V$ $V_{EE} = -12V$ $V_{IH} = 1.9V$ $V_{EE} = -15V$ $V_{IL} = 0.8V$ $V_{EE} = -15V$		-13 -18	-17 -15 -23 -15 -34 -2.5	mA μ A mA μ A mA mA	5
P_C Power consumption	$V_S = 9V$ $V_{EE} = -9V$ $V_S = 12V$ $V_{EE} = -12V$			333 576	mW	

SWITCHING CHARACTERISTICS ($V_S = \pm 9 \pm 1\%$ V, $V_{EE} = -9 \pm 1\%$ V, $T_{amb} = 25^\circ\text{C}$)

t_{PLH} Propagation delay time	$Z_I = 3K\Omega$ and 15pF		275	350	ns	6
t_{THL} Fall time	$Z_I = 3K\Omega$ and 15pF		45	75	ns	6
t_{PHL} Propagation delay time	$Z_I = 3K\Omega$ and 15pF		110	175	ns	6
t_{TLH} Rise time	$Z_I = 3K\Omega$ and 15pF		55	100	ns	6

* Maximum package power dissipation may be exceeded if all outputs are shorted simultaneously

TEST CIRCUITS

Fig. 1 - Input current

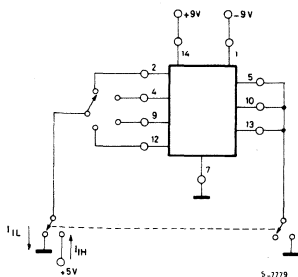


Fig. 2 - Output voltage

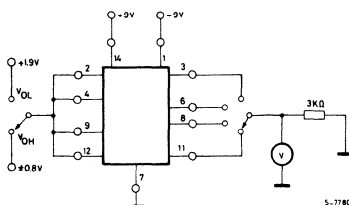
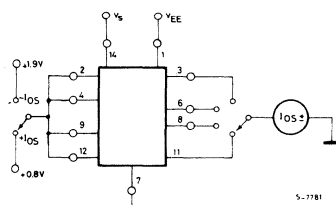


Fig. 3 - Output short-circuit current



TEST CIRCUITS

Fig. 4 - Output resistance (power off)

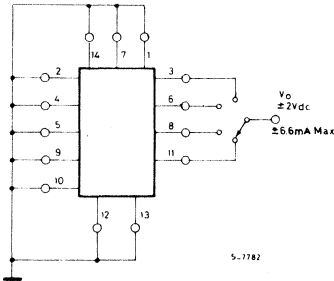


Fig. 5 - Power supply currents

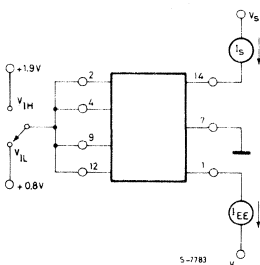


Fig. 6 - Switching response

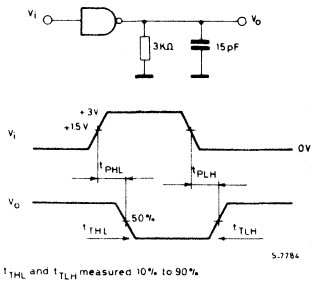


Fig. 7 - Transfer characteristics vs. power supply voltage

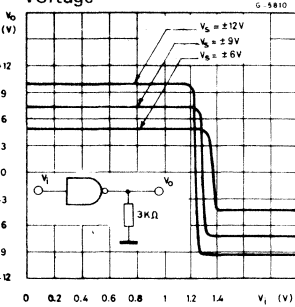


Fig. 8 - Short-circuit output current vs. temperature

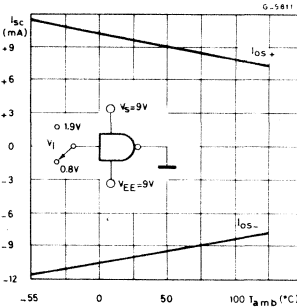


Fig. 9 - Output slew-rate load capacitance

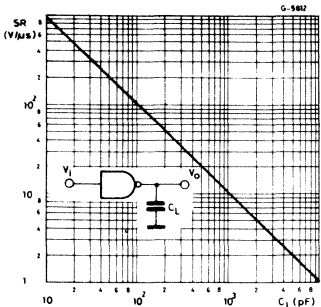


Fig. 10 - Output voltage and current-limiting characteristics

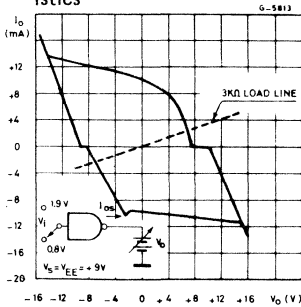
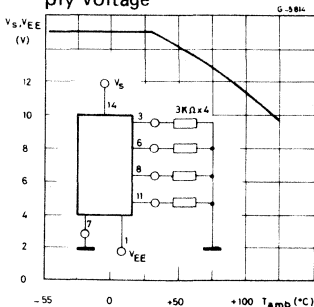


Fig. 11 - Maximum operating temperature vs. power-supply voltage



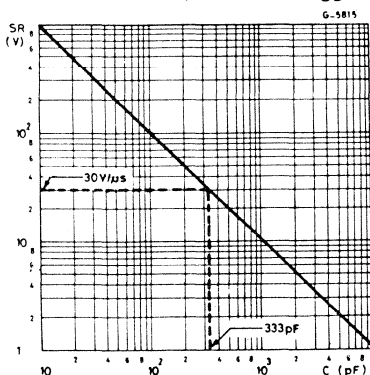
APPLICATIONS INFORMATION

The Electronic Industries Association (EIA) has released the RS232C specification detailing the requirements for the interface between data processing equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15V in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000 Ω resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30V per μ s. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T / \Delta V$ from which Figure 12 is derived. Accordingly, a 330pF capacitor on each output will guarantee a worst case slew rate of 30V per μ s.

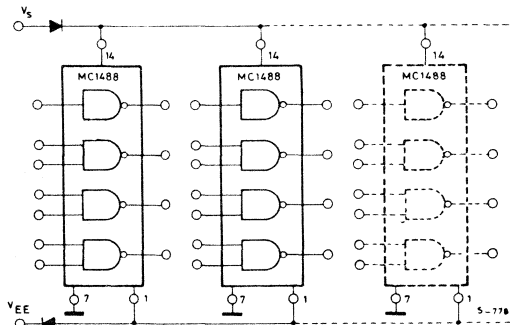
Fig. 12 - Slew rate vs. capacitance for $I_{SC} = 10$ mA



The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15V, 500mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0V (i.e., $V_S \geq 9.0V$; $V_{EE} \leq -9.0V$). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300 Ω output resistor to ground. If **all four outputs** were then shorted to plus or minus 15V, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent over-heating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ± 15 V limits specified in the earlier Standard RS232B). The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0V stated above.

The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10mA output current limiting.

Fig. 13 - Power supply protection to meet power-off fault conditions





Other Applications

The MC1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. **Output Current Limiting** — this enables the circuit designer to define the output voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins.
2. **Power-Supply Range** — as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not

require matching power-supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15V. The negative supply can vary from approximately -2.5V to the minimum specified -15V. The MC1488 will drive the output to within 2V of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package.



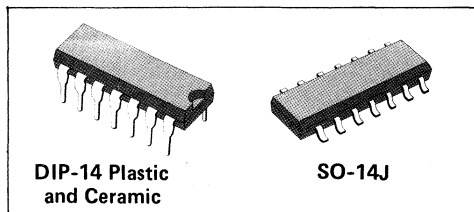
MC1489 MC1489A

QUAD LINE RECEIVERS

- INPUT RESISTANCE – 3.0K to 7.0K Ω
- INPUT SIGNAL RANGE – $\pm 30V$
- INPUT THRESHOLD HYSTERESIS BUILT-IN
- RESPONSE CONTROL:
 - a) LOGIC THRESHOLD SHIFTING
 - b) INPUT NOISE FILTERING

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment

with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

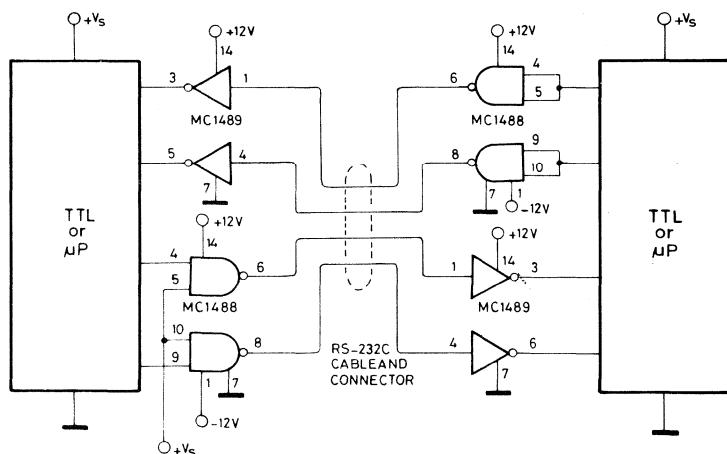


ABSOLUTE MAXIMUM RATINGS

V_S	Power supply voltage	10	V
V_i	Input voltage range	± 30	V
I_{OL}	Output load current	20	mA
P_{tot}	Power dissipation	1	W
T_{amb}	Operating ambient temperature	0 to 75	$^{\circ}C$
T_{stg}	Storage temperature range	-65 to 150	$^{\circ}C$

ORDERING NUMBER: MC1489L, MC1489AL (DIP-14 Ceramic)
 MC1489P, MC1489AP (DIP-14 Plastic)
 MC1489D, MC1489AD (SO-14)

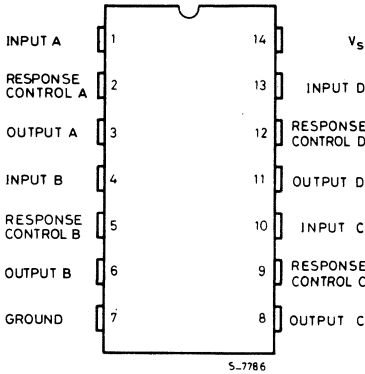
Typical Application: RS232C data transmission



S-7776

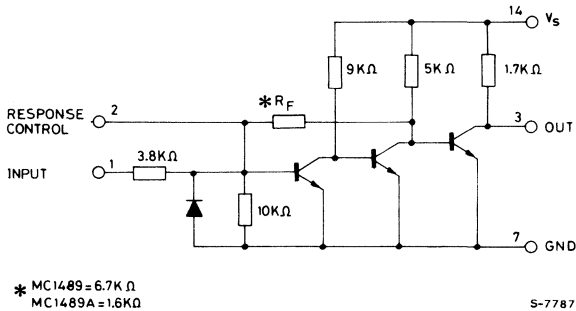
CONNECTION DIAGRAM

(Top view)



SCHEMATIC DIAGRAM

(1/4 of circuit shown)



ELECTRICAL CHARACTERISTICS

(Response control pin is open; $V_S = 5V$, $T_{amb} = 0$ to $75^{\circ}C$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{IH}	Positive input current $V_{IH} = 25V$ $V_{IH} = 3V$	3.6 0.43		8.3	mA
I_{IL}	Negative input current $V_{IL} = -25V$ $V_{IL} = -3V$	-3.6 -0.43		-8.3	mA
V_{IH}	Input Turn-on threshold voltage $T_{amb} = 25^{\circ}C$ $I_L = 10mA$ $V_{OL} \leq 0.45$ for MC1489 for MC1489A	1 1.75	1.95	1.5 2.25	V
V_{IL}	Input Turn-off threshold voltage $T_{amb} = 25^{\circ}C$ $I_L = -0.5mA$ $V_{OH} \geq 2.5V$	0.75		1.25	V
V_{OH}	Output voltage high $V_{IH} = 0.75V$ $I_L = -0.5mA$ $I_L = 0.5mA$ input open circuit	2.5 2.5	4 4	5 5	V V
V_{OL}	Output voltage low $V_{IL} = 3V$ $I_L = 10mA$		0.2	0.45	V
I_{OS}	Output short circuit current		-3	-4	mA
I_S	Power supply current All gates "on" $V_{IH} = 5V$ $I_O = 0mA$		16	26	mA
P_C	Power consumption $V_{IH} = 5V$		80	130	mW

SWITCHING CHARACTERISTICS

($V_S = 5V$, $T_{amb} = 25^{\circ}C$, see Fig. 1)

t_{PLH}	Propagation Delay time	$R_L = 3.9K\Omega$	25	85	ns
t_{TLH}	Rise time	$R_L = 3.9K\Omega$	120	175	ns
t_{PHL}	Propagation Delay time	$R_L = 390\Omega$	25	50	ns
t_{THL}	Fall time	$R_L = 390\Omega$	10	20	ns



MC1489
MC1489A

TEST CIRCUITS

Fig. 1 - Switching response

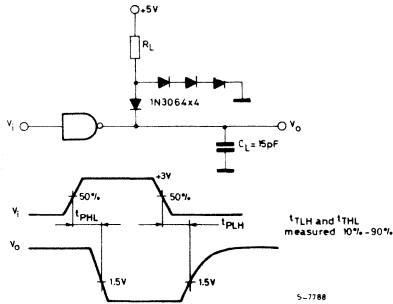
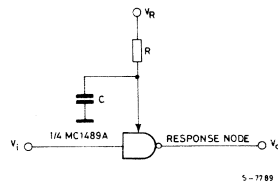


Fig. 2 - Response control node



C, capacitor is for noise filtering
R, resistor is for threshold shifting

Fig. 3 - Input current

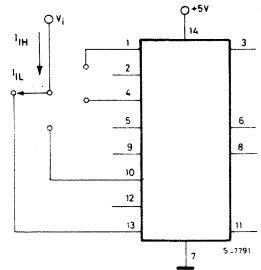


Fig. 4 - Output short-circuit current

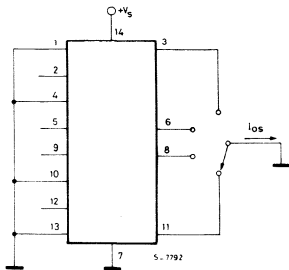


Fig. 5 - Output voltage and input threshold voltage

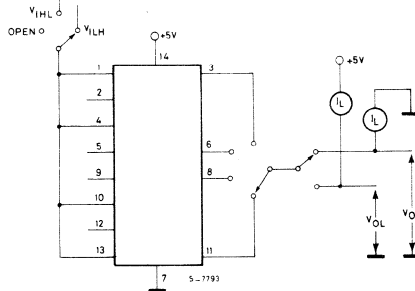
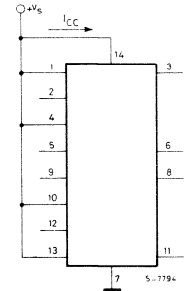


Fig. 6 - Power supply current



TYPICAL CHARACTERISTICS ($V_S = 5\text{V}$, $T_{\text{amb}} = 25^\circ\text{C}$ unless otherwise specified)

Fig. 7 - Input current

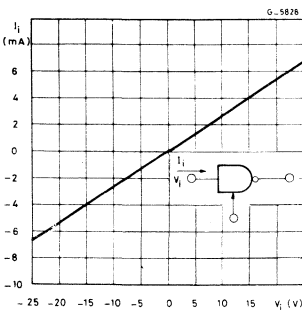


Fig. 8 - MC1489 input threshold voltage adjustment

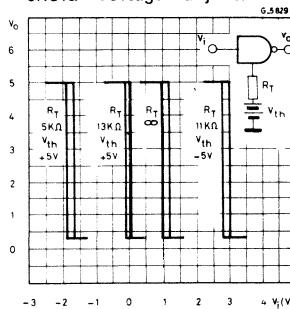
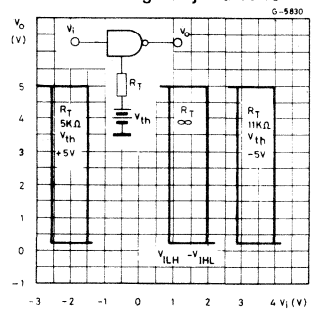


Fig. 9 - MC1489A input threshold voltage adjustment





MC1489 MC1489A

Fig. 10 - Input threshold voltage vs. temperature

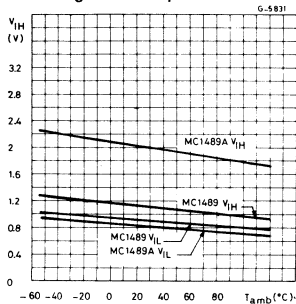
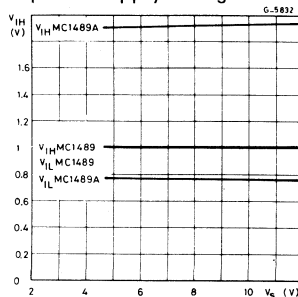


Fig. 11 - Input threshold vs. power-supply voltage



APPLICATION INFORMATION

General Information

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 Ω and 7000 Ω for input voltages between 3.0 and 25V in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0V in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE} .

The receiver shall detect a voltage between -3.0 and -25V as a Logic "1" and inputs between +3.0 and +2.5V as a Logic "0". On some interchange leads, an open circuit of power "OFF" condition (300 Ω or more to ground) shall be decoded as an "OFF" condition or Logic "1". For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25V and turn-off of 1.0V for a typical hysteresis of 250mV. The MC1489A has typical turn-on of 1.95V and turn-off of 0.8V for typically 1.15V of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power supply. Figure 2, 4 and 5 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high-frequency, high-energy noise pulses. Figures 8 and 9 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted. (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 10).



MC1489
MC1489A

APPLICATION INFORMATION (continued)

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above

ground or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

Fig. 12 - Typical Turn-on threshold vs. capacitance from response control pin to GND

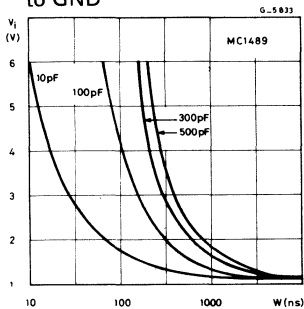


Fig. 13 - Typical Turn-on threshold vs. capacitance from response control pin to GND

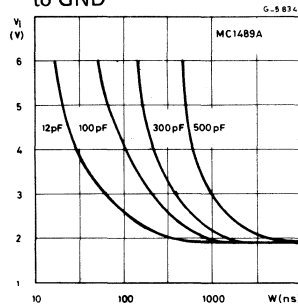
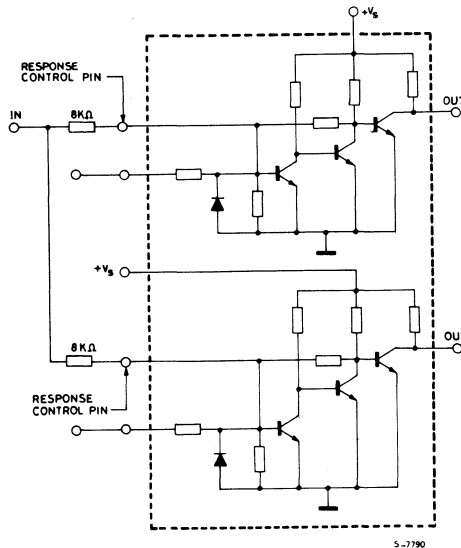


Fig. 14 - Typical paralleling of two MC1489/A receivers to meet RS-232C





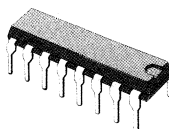
MC3479C

ADVANCE DATA

STEPPER MOTOR DRIVER

- SINGLE SUPPLY OPERATION +7.2V TO +16.5V
- 350mA/COIL DRIVE CAPABILITY
- CLAMP DIODES PROVIDED FOR BACK-EMF SUPPRESSION
- SELECTABLE $\overline{\text{CW}}$ /CCW AND $\overline{\text{FULL}}$ /HALF STEP OPERATION
- SELECTABLE HIGH/LOW OUTPUT IMPEDANCE (HALF STEP MODE)
- TTL/CMOS COMPATIBLE INPUTS
- INPUT HYSTERESIS: 250mV TYP.
- PHASE LOGIC CAN BE INITIALIZED TO PHASE A
- PHASE A OUTPUT DRIVE STATE INDICATION

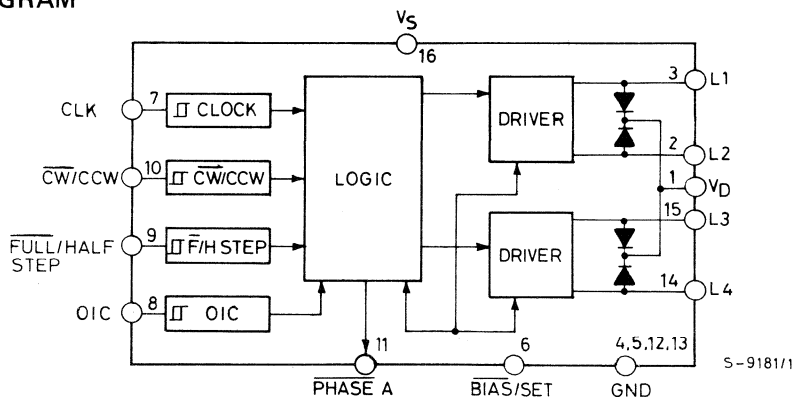
The MC3479C is designed to drive a two-phase stepper motor in the bipolar mode. The circuit consists of four input selections a logic decoding/sequencing section two driver stages for the motor coils and an output to indicate the Phase A drive state.



Powerdip
12 + 2 + 2

ORDERING NUMBER: MC3479C

BLOCK DIAGRAM



INPUT TRUTH TABLE

	INPUT LOW	INPUT HIGH
$\overline{\text{CW}}$ /CCW	CW	CCW
$\overline{\text{F}}$ /HS	Full Step	Half Step
OIC	High Z	Low Z
CLK	Positive Edge Triggered	



MC3479C

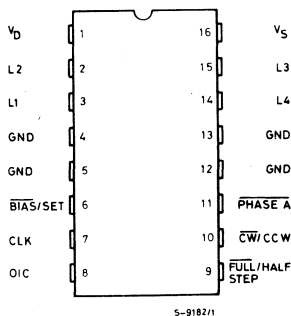
ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	18	V_{DC}
V_D	Clamp diode cathode voltage (Pin 1)	V_S	V_{DC}
V_{OD}	Driver output voltage (Pins 2, 3, 14, 15)	V_S	V_{DC}
I_{OD-}	Driver output current/coil	± 500	mA
V_{IN}	Input voltage (Pins 7, 8, 9, 10)	-0.5 to 7	V_{DC}
I_{BS}	Bias/set current (Pin 6)	10	mA
V_{OA}	Phase A output voltage (Pin 11)	18	V_{DC}
I_{OA}	Phase A sink current (Pin 11)	20	mA
T_J	Junction temperature	150	$^{\circ}C$
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}C$

RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_S	Supply voltage (DC)	7.2	16	V
V_D	Clamp diode cathode voltage (DC)	—	V_S	V
I_{OD}	Driver output current (per coil)	—	350	mA
V_i	DC input voltage (Pin 7, 8, 9, 10)	0	5.5	V
I_{BS}	Bias/set current (outputs active)	-300	75	μA
I_{OA}	Phase A sink current	0	8	mA
T_{amb}	Operating ambient temperature	0	70	$^{\circ}C$

CONNECTION DIAGRAM



THERMAL DATA

$R_{th J-amb}$	Thermal resistance junction-ambient	max	70	$^{\circ}C/W$
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**PIN DESCRIPTION**

NAME	SYMBOL	PINS	DESCRIPTION
POWER SUPPLY	V_S	16	Power supply pin for both the logic circuit and the motor coil current. Voltage range is 7.2V to 16V.
GROUND	GND	4-5-12-13	Ground pins for the logic circuit and the motor coil current. The physical configuration of the pins dissipating heat from within the package.
CLAMP DIODE	V_D	1	This pin is used to protect the outputs where large voltage spikes may occur as the motor coils are switched. Typically a diode is connected between this pin and pin 16. See fig. 5.
DRIVER OUTPUTS	L1, L2 L3, L4	2-3 14-15	High current outputs for the motor coils. L1 and L2 are connected to one coil and L3 and L4 to the other coil.
BIAS/SET	$\bar{B}/S$	6	This pins is typically 0.7V below V_S . The current out of this pin (through a resistor to ground) determines the maximum output sink current. If the pin is opened ($I_{BS} < 5.0\mu A$) the outputs assume a high impedance condition while the internal logic presets to a Phase A condition.
CLOCK	CK	7	The positive edge of the clock input switches the outputs to the next position. This input has no effect if pin 6 is open.
FULL/HALF STEP	$\bar{F}/HS$	9	When low (logic 0) each clock pulse will cause the motor to rotate one full step. When high, each clock pulse will cause the motor to rotate one-half step. (See fig. 4 for sequence).
CLOCKWISE COUNTERCLOCKWISE	$\bar{CW}/CCW$	10	This input allows reversing the rotation of the rotation of the motor. (See fig. 4 for sequence).
OUT IMPEDANCE CONTROL	OIC	8	This input is relevant only in the half step mode (pin 9 > 2V). When low (logic 0) the two driver out of the non-energized coil will be in a high impedance condition. When high the same driver outputs will be at a low impedance reference to V_S . (See fig. 4).
PHASE A	$\bar{Ph} A$	11	This outputs indicates (when low) that the driver outputs are in the phase A condition ($L1 = L3 = V_{OHD}$; $L2 = L4 = V_{OLD}$)



MC3479C

DC ELECTRICAL CHARACTERISTICS (Specifications apply over the recommended supply voltage and temperature range, unless otherwise noted)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
------------	-----------------	------	------	------	------

INPUT LOGIC LEVEL

V_{TLH}	Threshold voltage (LOW to HIGH)			2	V
V_{THL}	Threshold voltage (HIGH to LOW)	0.8			V
V_{HYS}	Hysteresis	0.25			V
I_{IL} I_{IH1} I_{IH2}	Current $V_I = 0.4V$ $V_I = 5.5V$ $V_I = 2.7V$	-100		100 20	μA

DRIVER OUTPUT LEVELS

V_{OHD}	Output high voltage	$I_{OD} = -350mA$ $I_{OD} = -0.1mA$ $I_{BS} = -300\mu A$	$V_S - 2.0$ $V_S - 1.2$		V V
V_{OLD}	Output low voltage	$I_{BS} = -300\mu A$ $I_{OD} = -350mA$		0.8	V
D_{VOD}	Difference mode out voltage difference	$I_{BS} = -300\mu A$ $I_{OD} = 350mA$		0.15	V
C_{VOD}	Common mode out voltage difference	$I_{BS} = -300\mu A$ $I_{OD} = -0.1mA$		0.15	V
I_{OZ1}	Out leakage-HiZ state	$0 < V_D < V_M, I_{BS} = 5\mu A$	-100	+100	μA
I_{OZ2}	Out leakage-HiZ state	$0 < V_{OD} < V_M, I_{BS} = -300\mu A$ Pin 9 = 2V Pin 8 = 0.8V	-100	+100	μA

CLAMP DIODES

V_{DF}	Forward voltage	$I_D = 350mA$		2.5	3	V
I_{DR}	Leakage current	$V_R = 21V$			100	μA

PHASE A OUTPUT

V_{OLA}	Out LOW voltage	$I_{OA} = 8mA$			0.4	V
	OFF state leakage current	$V_{OA} = 16.5V$			100	μA

POWER SUPPLY

I_{SSB}	Power supply current in stand by state	$V_{BS} = V_S$			12	mA
I_S	Power supply current ($I_{OD} = 0$; $I_{BS} = -300\mu A$)	$L1 = V_{OHD}$ $L3 = V_{OHD}$	$L2 = V_{OLD}$ $L4 = V_{OHD}$		75	mA

BIAS SET CURRENT

I_{BS}	Bias set current	to set PHASE A	-5			μA
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- NOTES 3.** $D_{VOD} = |V_{OD1.2} - V_{OD3.4}|$
 $V_{OD1.2} = (V_{OHD1} - V_{OHD2})$ or $(V_{OHD2} - V_{OLD1})$ and
 $V_{OD3.4} = (V_{OHD3} - V_{OHD4})$ or $(V_{OHD4} - V_{OHD3})$
4. $C_{VOD} = |V_{OHD1} - V_{OHD2}$ or $V_{OHD3} - V_{OHD4}|$

**MC3479C****AC SWITCHING CHARACTERISTICS** ($T_{amb} = 25^{\circ}\text{C}$; $V_M = 12\text{V}$)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{CK}	Clock frequency	0		30	KHz
PWCKH	Clock pulse width	HIGH	10		μs
PWCKL	Clock pulse width	LOW	20		μs
t_{SU}	Set-up time $\overline{CW}/\overline{CCW}$ and $\overline{F}/\overline{HS}$	5			μs
t_{HO}	Hold time $\overline{CW}/\overline{CCW}$ and $\overline{F}/\overline{HS}$	10			μs
t_{PCD}	Propagation delay CLK-to driver out		8		μs
t_{PBSD}	Propagation delay $\overline{\text{Bias}}/\text{set}$ to driver output		1		μs
t_{PHLA}	Propagation delay CLK-to phase A LOW		12		μs
t_{PLHA}	Propagation delay CLK-to phase A HIGH		5		μs

Fig. 1 - AC test circuit

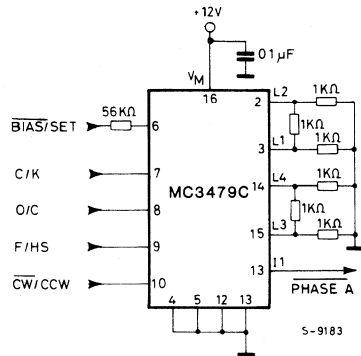


Fig. 2 - BIAS/SET TIMING (refer to fig. 1)

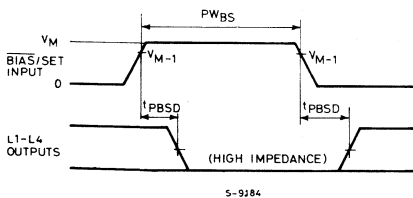
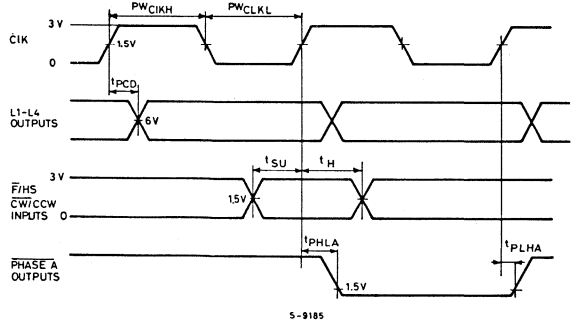


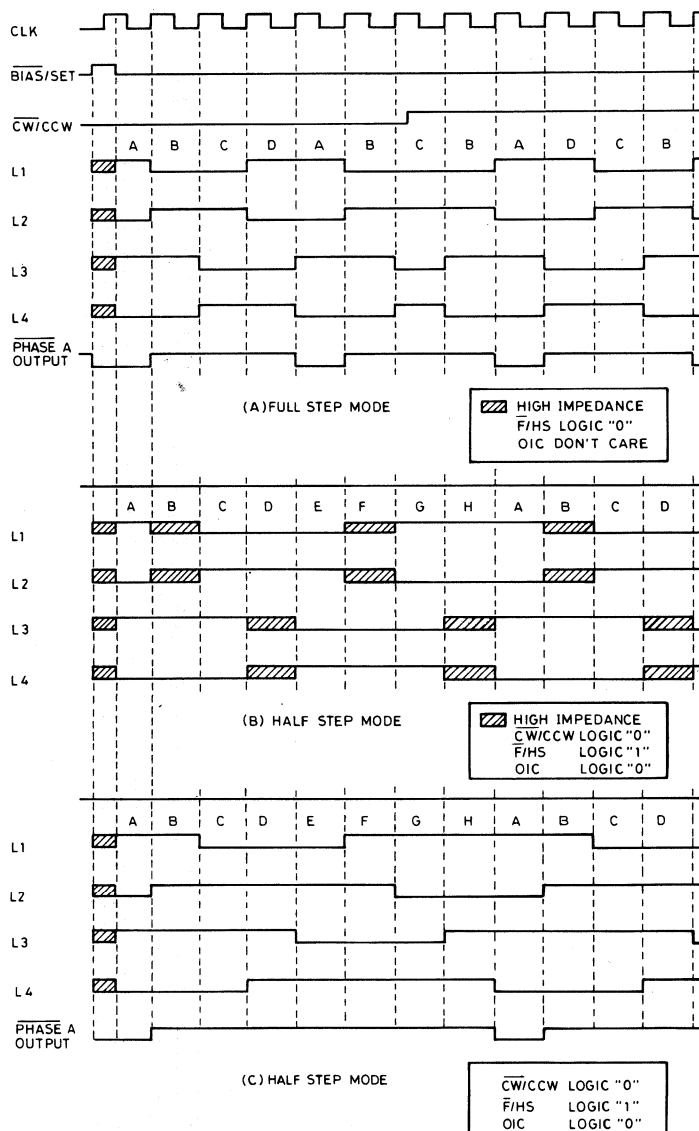
Fig. 3 - CLOCK TIMING (refer to fig. 1)





MC3479C

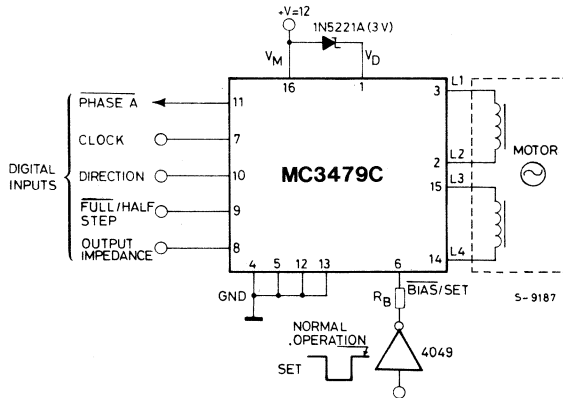
Fig. 4 - Output sequence





MC3479C

Fig. 5 - Typical application circuit





PBL3717A

PRELIMINARY DATA

STEPPER MOTOR DRIVER

- FULL STEP - HALF STEP - QUARTER STEP OPERATING MODE
- BIPOLAR OUTPUT CURRENT UP TO 1A
- FROM 10V UP TO 46V MOTOR SUPPLY VOLTAGE
- LOW SATURATION VOLTAGE WITH INTEGRATED BOOTSTRAP
- BUILT IN FAST PROTECTION DIODES
- EXTERNALLY SELECTABLE CURRENT LEVEL
- OUTPUT CURRENT LEVEL DIGITALLY OR ANALOGUE CONTROLLED
- THERMAL PROTECTION WITH SOFT INTERVENTION

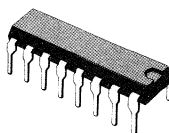
The PBL3717A is a monolithic IC which controls and drives one phase of a bipolar stepper motor with chopper control of the phase current. Current levels may be selected in three steps by means of two logic inputs which select one of three current comparators. When both of these inputs are high the device is disabled. A separate logic input controls the direction of current flow.

A monostable, programmed by an external RC network, sets the current decay time.

The power section is a full H-bridge driver with four internal clamp diodes for current recirculation. An external connection to the lower emitters is available for the insertion of a sensing resistor. Two PBL3717As and few external components form a complete stepper motor drive subsystem.

The recommended operating ambient temperature range is from 0 to 70°C.

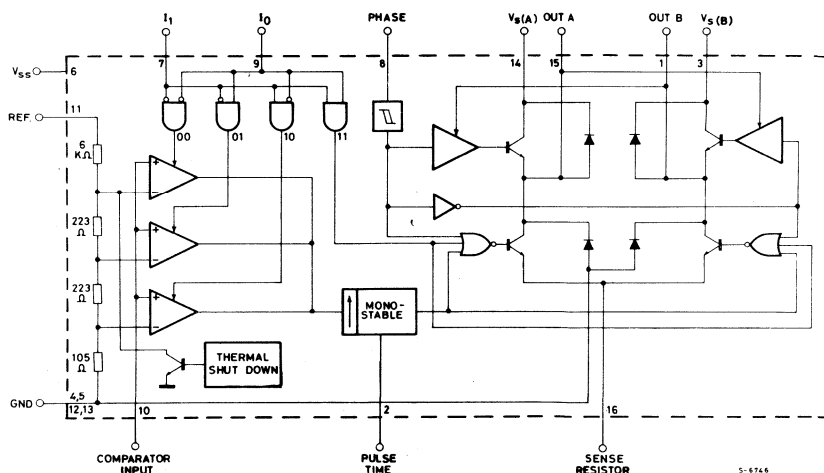
The PBL3717A is supplied in a 12 + 2 + 2 lead Powerdip package.



Powerdip
12 + 2 + 2

ORDERING NUMBER: PBL3717A

BLOCK DIAGRAM





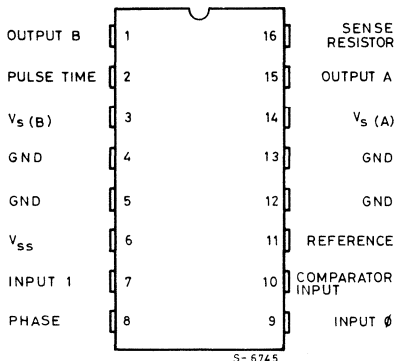
PBL3717A

ABSOLUTE MAXIMUM RATINGS

V_s	Power supply voltage (pins 14, 3)	50	V
V_{ss}	Logic supply voltage (pin 6)	7	V
V_i	Logic input voltage (pins 7, 8, 9)	6	V
V_c	Comparator input (pin 10)	V_{ss}	
V_r	Reference input voltage (pin 11)	15	V
I_o	Output current (DC operation)	1.2	A
T_{stg}	Storage temperature	-55 to + 150	°C
T_j	Operating junction temperature	150	°C

CONNECTION DIAGRAM

(top view)



TRUTH TABLE

Input 0 (pin 9)	Input 1 (pin 7)	
H	H	No current
L	H	Low current
H	L	Medium current
L	L	High current

THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	11	°C/W
$R_{th\ j-amb}$	Thermal resistance junction-ambient*	40	°C/W

* Soldered on a 35μ thick 20 cm² P.C. board copper area

**PIN FUNCTIONS**

N°	NAME	FUNCTION
1	OUTPUT B	Output connection (with pin 15). The output stage is a "H" bridge formed by four transistors and four diodes suitable for switching applications.
2	PULSE TIME	A parallel RC network connected to this pin sets the OFF time of the lower power transistors. The pulse generator is a monostable triggered by the rising edge of the output of the comparators ($t_{off} = 0.69 R_T C_T$).
3	SUPPLY VOLTAGE B	Supply voltage input for half output stage. see also pin 14.
4	GROUND	Ground connection. With pins 5, 12 and 13 also conducts heat from die to printed circuit copper.
5	GROUND	See pin 4.
6	LOGIC SUPPLY	Supply voltage input for logic circuitry.
7	INPUT 1	This pin and pin 9 (INPUT 0) are logic inputs which select the outputs of the three comparators to set the current level. Current also depends on the sensing resistor and reference voltage. See truth table.
8	PHASE	This TTL-compatible logic input sets the direction of current flow through the load. A high level causes current to flow from OUTPUT A (source) to OUTPUT B (sink). A schmitt trigger on this input provides good noise immunity and a delay circuit prevents output stage short circuits during switching.
9	INPUT 0	See INPUT 1 (pin 7).
10	COMPARATOR INPUT	Input connected to the three comparators. The voltage across the sense resistor is feedback to this input through the low pass filter $R_C C_C$. The lower power transistor are disabled when the sense voltage exceeds the reference voltage of the selected comparator. When this occurs the current decays for a time set by $R_T C_T$, $t_{off} = 0.69 R_T C_T$.
11	REFERENCE	A voltage applied to this pin sets the reference voltage of the three comparators, this determining the output current (also thus depending on R_s and the two inputs INPUT 0 and INPUT 1).
12	GROUND	See pin 4.

PIN FUNCTIONS (continued)

N°	NAME	FUNCTION
13	GROUND	See pin 4.
14	SUPPLY VOLTAGE A	Supply voltage input for half output stage. See also pin 13.
15	OUTPUT A	See pin 1.
16	SENSE RESISTOR	Connection to lower emitters of output stage for insertion of current sense resistor.

Fig. 1 – Test and application circuit

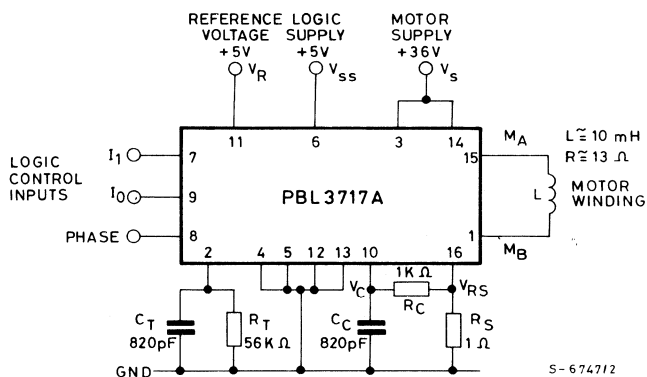
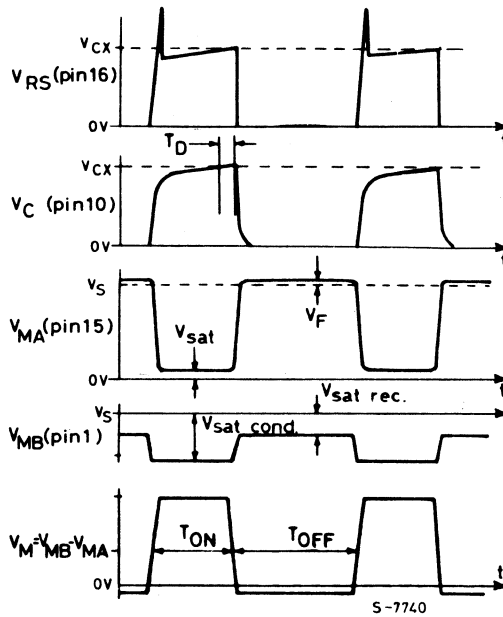


Fig. 2 - Waveforms with MA regulating (phase = 0)



ELECTRICAL CHARACTERISTICS (Refer to the test circuit $V_s = 36V$, $V_{ss} = 5V$, $T_{amb} = 25^\circ C$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s Supply voltage (pins 3, 14)		10		46	V
V_{ss} Logic supply voltage (pin 6)		4.75		5.25	V
I_{ss} Logic supply current (pin 6)			7	15	mA
I_R Reference input current (pin 11)	$V_R = 5V$		0.75	1	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
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LOGIC INPUTS

V_{IL}	Input low voltage (pins 7, 8, 9)			0.8	V
V_{IH}	Input high voltage (pin 7, 8, 9)	2		V_{SS}	V
I_{IL}	Low voltage input current (pins 7, 8, 9)	$V_I = 0.4V$	pin 8	-100	μA
			pins 7,9	-400	μA
I_{IH}	High voltage input current (pins 7, 8, 9)	$V_I = 2.4V$		10	μA

COMPARATORS

V_{CL}	Comparator low threshold voltage (pin 10)	$V_R = 5V$	$I_0 = L$ $I_1 = H$	66	78	90	mV
V_{CM}	Comparator medium threshold voltage (pin 10)	$V_R = 5V$	$I_0 = H$ $I_1 = L$	236	251	266	mV
V_{CH}	Comparator high threshold voltage (pin 10)	$V_R = 5V$	$I_0 = L$ $I_1 = L$	396	416	436	mV
I_C	Comparator input current (pin 10)					± 20	μA
t_{off}	Cutoff time	$R_T = 56 K\Omega$	$C_T = 820 pF$	25		35	μs
t_d	Turn off delay	(See fig. 2)				2	μs
I_{off}	Output leakage current (pins 1, 15)	$I_0 = H$	$I_1 = H$			100	μA

SOURCE DIODE-TRANSISTOR PAIR

V_{sat}	Saturation voltage (pins 1, 15)	$I_M = -0.5A$ (See fig. 2)	conduction period	1.7	2.1	V
			recirculation period	1.1	1.35	
V_{sat}	Saturation voltage (pins 1, 15)	$I_M = -1A$ (See fig. 2)	conduction period	2.1	2.8	V
			recirculation period	1.7	2.5	
I_{LK}	Leakage current	$V_S = 46V$			300	μA
V_F	Diode forward voltage	$I_M = -0.5A$		1	1.25	V
		$I_M = -1A$		1.3	1.7	
I_{SLK}	Substrate leakage current when clamped	$I_M = -0.5A$			2	mA
		$I_M = -1A$			5	

ELECTRICAL CHARACTERISTICS (continued)

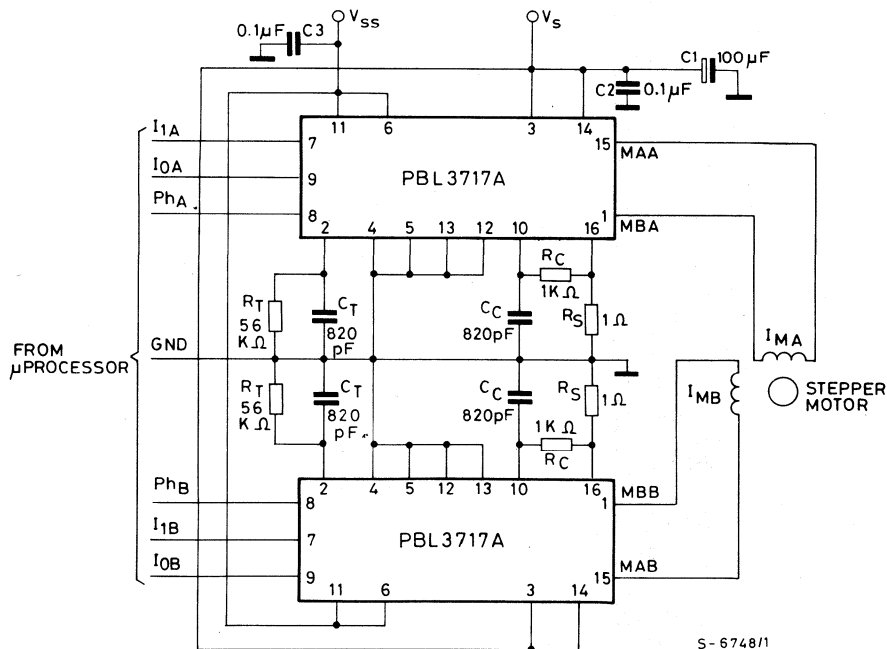
Parameter	Test conditions	Min.	Typ.	Max.	Unit
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SINK DIODE-TRANSISTOR PAIR

V_{sat}	Saturation voltage (pins 1, 15)	$I_M = 0.5A$		1.1	1.35	V
		$I_M = 1A$		1.6	2.3	V
I_{LK}	Leakage current	$V_s = 46V$			300	μA
V_F	Diode forward voltage	$I_M = 0.5A$		1.1	1.5	V
		$I_M = 1A$		1.4	2	

APPLICATION CIRCUIT

Fig. 3 - Two phase bipolar stepper motor driver



S-6748/1

APPLICATION CIRCUIT (continued)

Fig. 4 - P.C. board and component layout of the circuit of fig. 3 (1 : 1 scale)

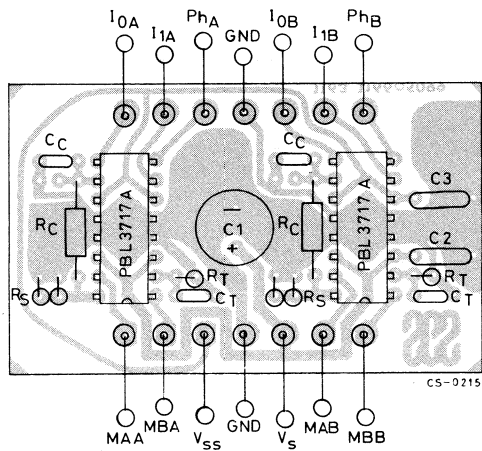
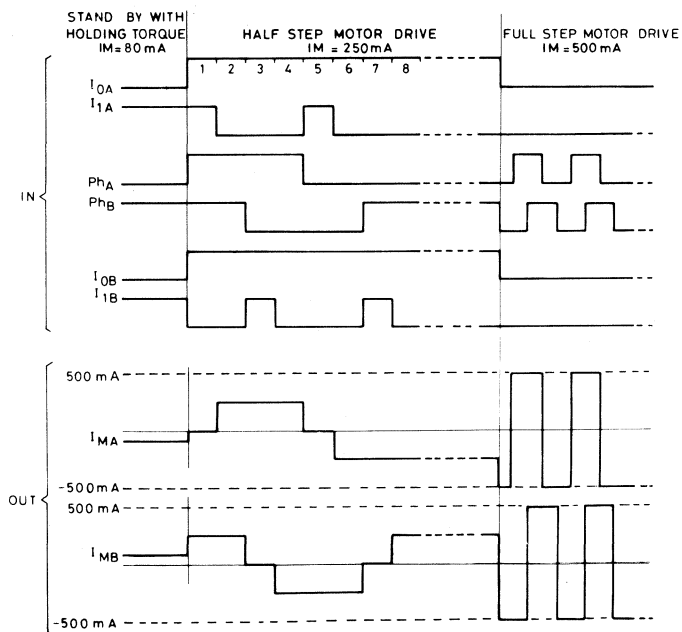


Fig. 5 - Input and output sequences for half step and full step operation



APPLICATION INFORMATION

Fig. 3 shows a typical application in which two PBL3717A control a two phase bipolar stepper motor.

Programming

The logic inputs I_0 and I_1 set at three different levels the amplitude of the current flowing in the motor winding according to the truth table of page 2. A high level on the "PHASE" logic input sets the direction of that current from output A to output B; a low level from output B to output A.

It is recommended that unused inputs are tied to pin 6 (V_{SS}) or pin 4 (GND) as appropriate to avoid noise problem.

The current levels can be varied continuously by changing the ref. voltage on pin 11.

Control of the motor

The stepper motor can rotate in either directions according to the sequence of the input signals. It is possible to obtain a full step, a half step and a quarter step operation.

Full step operation

Both the windings of the stepper motor are energized all the time with the same current $I_{MA} = I_{MB}$. I_0 and I_1 remain fixed at whatever torque value is required.

Calling A the condition with winding A energized in one direction and $\bar{A}$ in the other direction, the sequence for full step rotation is:

$$A B \rightarrow \bar{A} B \rightarrow \bar{A} \bar{B} \rightarrow A \bar{B} \text{ etc.}$$

For the rotation in the other direction the sequence must be reversed.

In the full step operation the torque is constant each step.

Half step operation

Power is applied alternately to one winding then

both according to the sequence:

$$A B \rightarrow B \rightarrow \bar{A} B \rightarrow \bar{A} \rightarrow \bar{A} \bar{B} \rightarrow \bar{B} \rightarrow A \bar{B} \rightarrow A \text{ etc.}$$

Like full step this can be done at any current level; the torque is not constant but it is lower when only one winding is energized

A coil is turned off by setting I_0 and I_1 both high.

Quarter step operation

It is preferable to realize the quarter step operation at full power otherwise the steps will be of very irregular size.

The extra quarter steps are added to the half step sequence by putting one coil on half current according to the sequence:

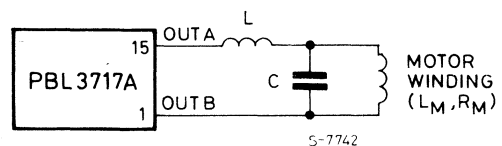
$$A B \rightarrow \frac{A}{2} B \rightarrow B \rightarrow \frac{\bar{A}}{2} B \rightarrow \bar{A} B \rightarrow \bar{A} \frac{B}{2} \rightarrow \bar{A} \text{ etc.}$$

Motor selection

As the PBL3717A provides constant current drive, with a switching operation, care must be taken to select stepper motors with low hysteresis losses to prevent motor over heat.

L-C filter

To reduce EMI and chopping losses in the motor a low pass L-C filter can be inserted across the outputs of the PBL3717A as shown on the following picture.



$$L \cong \frac{1}{10} L_M \quad C \cong \frac{4 \cdot 10^{-10}}{L}$$



PBL3717A

Fig. 6 - Source sat. voltage vs. output current (recirc. period)

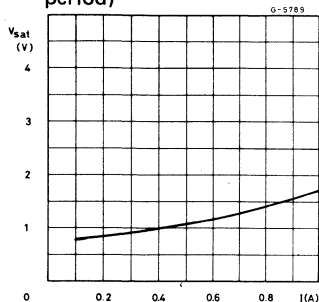


Fig. 7 - Source sat. voltage vs. output current (conduction period)

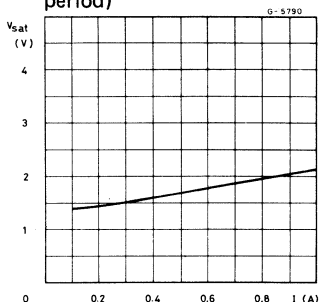


Fig. 8 - Sink sat. voltage vs. output current

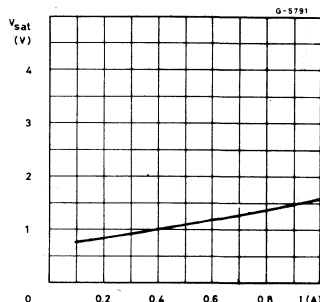
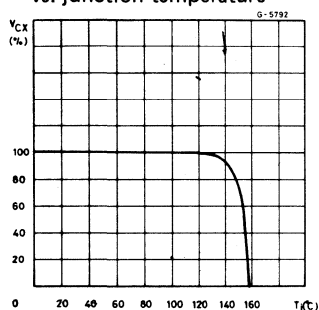


Fig. 9 - Comparator threshold vs. junction temperature



MOUNTING INSTRUCTIONS

The $R_{thj-amb}$ of the PBL 3717A can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heatsink.

The diagram of fig. 11 shows the maximum dissipable power P_{tot} and the $R_{thj-amb}$ as a function of the side "l" of two equal square copper areas having a thickness of 35μ (see fig. 10). The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 10 - Example of P.C. board copper area which is used as heatsink

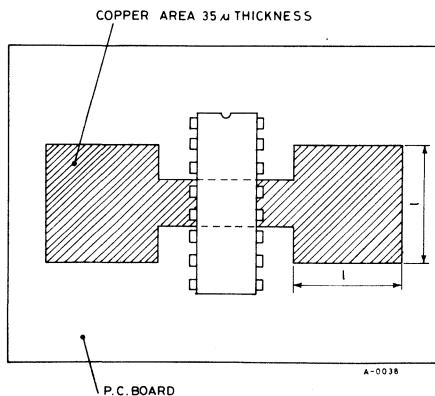
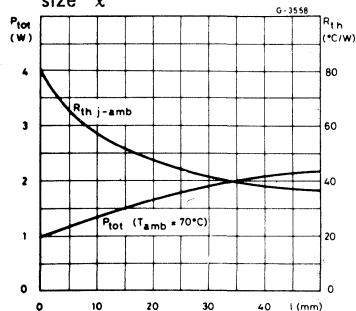


Fig. 11 - Max. dissipable power and junction to ambient thermal resistance vs. size "l"





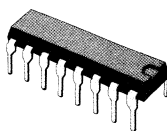
SG1524
SG2524
SG3524

REGULATING PULSE WIDTH MODULATORS

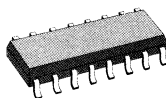
- COMPLETE PWM POWER CONTROL CIRCUITRY
- UNCOMMITTED OUTPUTS FOR SINGLE-ENDED OR PUSH PULL APPLICATIONS
- LOW STANDBY CURRENT..8mA TYPICAL
- OPERATION UP TO 300 KHz
- 1% MAXIMUM TEMPERATURE VARIATION OF REFERENCE VOLTAGE

The SG1524, SG2524, and SG3524 incorporate on a single monolithic chip all the function required for the construction of regulating power supplies inverters or switching regulators. They can also be used as the control element for high power-output applications. The SG1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency,

pulse-width modulation techniques. The dual alternating outputs allows either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry.



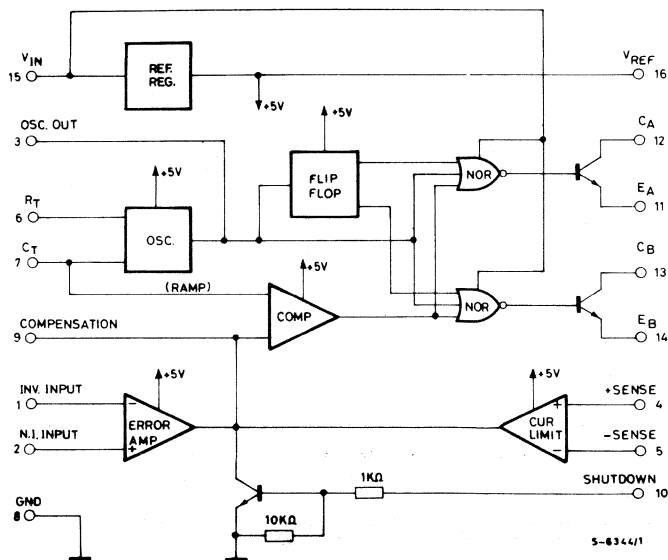
**DIP-16 Plastic (0.25)
and Ceramic**



SO-16P

ORDERING NUMBERS: SG1524J - SG2524J - SG3524J (Ceramic)
SG2524N - SG3524N (Plastic)
SG2524P - SG3524P (SO-16P)

BLOCK DIAGRAM



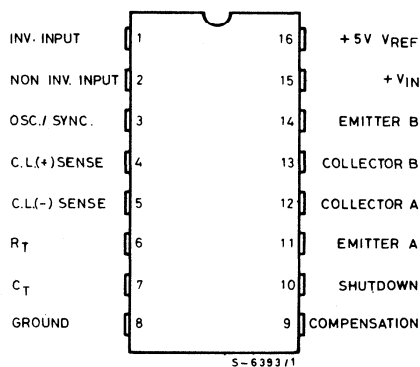


SG1524
SG2524
SG3524

ABSOLUTE MAXIMUM RATINGS

V_{IN}	Supply voltage	40	V
I_C	Collector output current	100	mA
I_R	Reference output current	50	mA
I_T	Current through C_T terminal	-5	mA
P_{tot}	Total power dissipation at $T_{amb} = 70^\circ\text{C}$	1000	mW
T_{stg}	Storage temperature range	-65 to 150	$^\circ\text{C}$
T_{op}	Operating ambient temperature range	-55 to 125	$^\circ\text{C}$
	SG1524	-25 to 85	$^\circ\text{C}$
	SG2524	0 to 70	$^\circ\text{C}$
	SG3524		

CONNECTION DIAGRAM



THERMAL DATA

			Plastic DIP-16	Ceramic DIP-16	SO-16P
R _{th j-amb}	Thermal resistance junction-ambient	max	80°C/W	150°C/W	—
R _{th j-alumina}	Thermal resistance junction-alumina	max	—	—	50°C/W

* Thermal resistance junction-alumina with the device soldered on the middle of an alumina supporting substrate measuring 15 x 20 mm; 0.65 mm thickness with infinite heatsink.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_j = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ for the SG1524, -25°C to $+85^{\circ}\text{C}$ for the SG2524, and 0°C to $+70^{\circ}\text{C}$ for the SG3524, $V_{IN} = 20\text{V}$, and $f = 20\text{KHz}$).

Parameter	Test condition	SG1524/SG2524			SG3524			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	

REFERENCE SECTION

V_{REF}	Output Voltage		4.8	5	5.2	4.6	5	5.4	V
ΔV_{REF}	Line Regulation	$V_{IN} = 8 \text{ to } 40\text{V}$		10	20		10	30	mV
ΔV_{REF}	Load Regulation	$I_L = 0 \text{ to } 20\text{mA}$		20	50		20	50	mV
	Ripple Rejection	$f = 120\text{Hz}, T_j = 25^{\circ}\text{C}$		66			66		dB
	Short Circuit Curr. Limit	$V_{REF} = 0, T_j = 25^{\circ}\text{C}$		100			100		mA
$\Delta V_{REF}/\Delta T$	Temp. Stability	Over Operating Temp. Range		0.3	1		0.3	1	%
ΔV_{REF}	Long Term Stability	$T_j = 25^{\circ}\text{C}, t = 1000 \text{ Hrs.}$		20			20		mV

OSCILLATOR SECTION

f_{MAX}	Maximum Frequency	$C_T = 0.001\mu\text{F}, R_T = 2\text{k}\Omega$		300			300		kHz
	Initial Accuracy	R_T and C_T Constant		5			5		%
	Voltage Stability	$V_{IN} = 8 \text{ to } 40\text{V}, T_j = 25^{\circ}\text{C}$			1			1	%
$\Delta f/\Delta T$	Temperature Stability	Over Operating Temp. Range			2			2	%
	Output Amplitude	Pin 3, $T_j = 25^{\circ}\text{C}$		3.5			3.5		V
	Output Pulse Width	$C_T = 0.01\mu\text{F}, T_j = 25^{\circ}\text{C}$		0.5			0.5		μs

ERROR AMPLIFIER SECTION

V_{OS}	Input Offset Voltage	$V_{CM} = 2.5\text{V}$		0.5	5		2	10	mV
I_b	Input Bias Current	$V_{CM} = 2.5\text{V}$		2	10		2	10	μA
G_V	Open Loop Volt. Gain		72	80		60	80		dB
CMV	Common Mode Volt.	$T_j = 25^{\circ}\text{C}$	1.8		3.4	1.8		3.4	V
CMR	Comm. Mode Rejec.	$T_j = 25^{\circ}\text{C}$		70			70		dB
B	Small Signal Bandwidth	$A_v = 0\text{dB}, T_j = 25^{\circ}\text{C}$		3			3		MHz
V_O	Output Voltage	$T_j = 25^{\circ}\text{C}$	0.5		3.8	0.5		3.8	V

COMPARATOR SECTION

	Duty-Cycle	% Each Output On	0		45	0		45	%
V_{IT}	Input Threshold	Zero Duty-Cycle		1			1		V
V_{IT}	Input Threshold	Maximum Duty-Cycle		3.5			3.5		V
I_b	Input Bias Current			1			1		μA

CURRENT LIMITING SECTION

	Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Max. Out, $T_j = 25^{\circ}\text{C}$	190	200	210	180	200	220	mV
	Sense Voltage T.C.			0.2			0.2		$\text{mV}/^{\circ}\text{C}$
CMV	Common Mode Volt.		-1		+1	-1		+1	V

OUTPUT SECTION (Each Output)

	Collector-Emitter Volt.		40			40			V
	Collector Leakage Cur.	$V_{CE} = 40\text{V}$		0.1	50		0.1	50	μA
	Saturation Voltage	$I_c = 50\text{mA}$		1	2		1	2	V
	Emitter Out. Voltage	$V_{IN} = 20\text{V}$	17	18		17	18		V
t_r	Rise Time	$R_c = 2\text{k}\Omega, T_j = 25^{\circ}\text{C}$		0.2			0.2		μs
t_f	Fall time	$R_c = 2\text{k}\Omega, T_j = 25^{\circ}\text{C}$		0.1			0.1		μs
I_q^*	Total Standby Curr.	$V_{IN} = 40\text{V}$		8	10		8	10	mA

(*) Excluding oscillator charging current, error and current limit dividers, and with outputs open.

Fig. 1 - Open-loop voltage amplification of error amplifier vs. frequency.

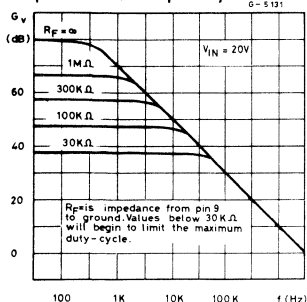


Fig. 4 Output saturation voltage vs. load current.

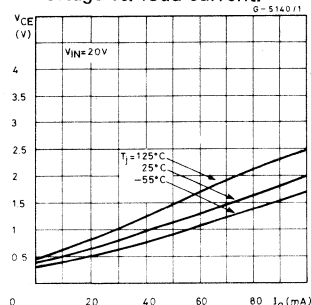


Fig. 2 - Oscillator frequency vs. timing components.

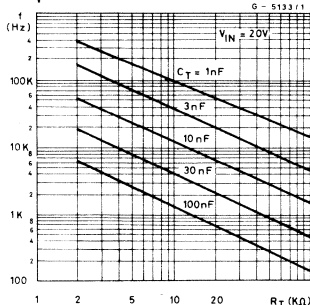


Fig. 3 - Output dead time vs. timing capacitance value.

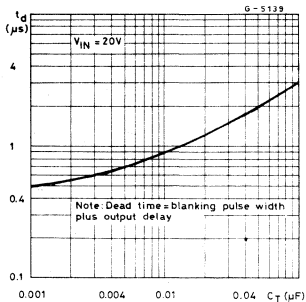
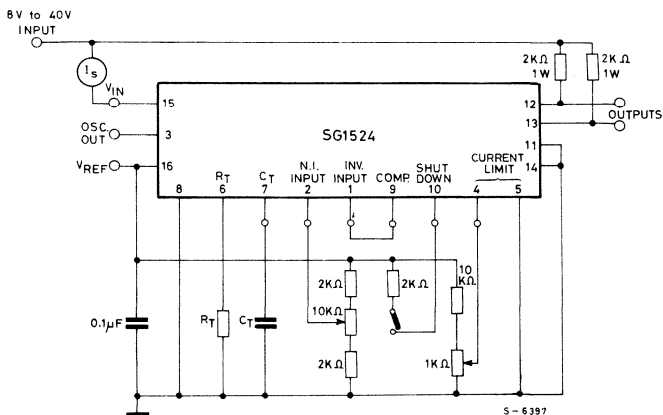


Fig. 5 - Open loop test circuit.



PRINCIPLES OF OPERATION

The SG1524 is a fixed-frequency pulse-with-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T) and one timing capacitor (C_T). R_T established a constant charging current for C_T . This results in a linear voltage ramp at C_T , which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The SG1524 contains, an on-board 5V regulator that serves as a reference as well as powering the SG1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode

range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T . The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistors (Q_A or Q_B) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of C_T . The



SG1524
SG2524
SG3524

outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier, or to provide additional control to the regulator.

RECOMMENDED OPERATING CONDITIONS

Supply voltage V_{IN}	8 to 40	V
Reference Output Current	0 to 20	mA
Current through C_T Terminal	-0.03 to -2	mA
Timing Resistor, R_T	1.8 to 100	K Ω
Timing Capacitor, C_T	0.001 to 0.1	μ F

TYPICAL APPLICATIONS DATA

Oscillator

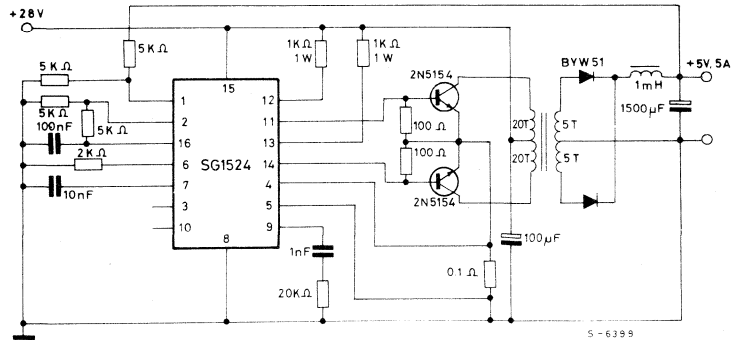
The oscillator controls the frequency of the SG1524 and is programmed by R_T and C_T according to the approximate formula:

$$f \approx \frac{1.18}{R_T C_T}$$

where R_T is in K Ω
 C_T is in μ F
 f is in KHz

Practical values of C_T fall between 0.001 and 0.1 μ F. Practical values of R_T fall between 1.8 and 100K Ω . This results in a frequency range typically from 120Hz to 500KHz.

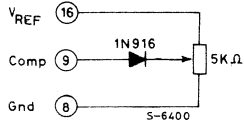
Fig. 7 - Push-pull transformer-coupled circuit.



Blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T . If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit below:

Fig. 6



Synchronous Operation

When an external clock is desired, a clock pulse of approximately 3V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2K Ω . In this configuration R_T C_T must be selected for a clock period slightly greater than that of the external clock.

If two more SG1524 regulators are to be operated synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to a single timing capacitor, and the timing resistor connected to a single R_T terminal. The other R_T terminals can be left open or shorted to V_{REF} . Minimum lead lengths should be used between the C_T terminals.



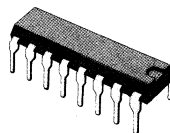
SG1525A/27A
SG2525A/27A
SG3525A/27A

REGULATING PULSE WIDTH MODULATORS

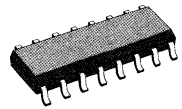
- 8 to 35V OPERATION
- 5.1V REFERENCE TRIMMED TO $\pm 1\%$
- 100Hz to 500KHz OSCILLATOR RANGE
- SEPARATE OSCILLATOR SYNC TERMINAL
- ADJUSTABLE DEADTIME CONTROL
- INTERNAL SOFT-START
- PULSE-BY-PULSE SHUTDOWN
- INPUT UNDERVOLTAGE LOCKOUT WITH HYSTERESIS
- LATCHING PWM TO PREVENT MULTIPLE PULSES
- DUAL SOURCE/SINK OUTPUT DRIVERS

The SG1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip + 5.1V reference is trimmed to $\pm 1\%$ and the input common-mode range of the error amplifier includes the reference voltage eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the C_T and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required.

A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. this lockout circuitry includes approximately 500mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulses has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The SG1525A output stage features NOR logic, giving a LOW output for an OFF state. The SG1527A utilizes OR logic which results in a HIGH output level when OFF.



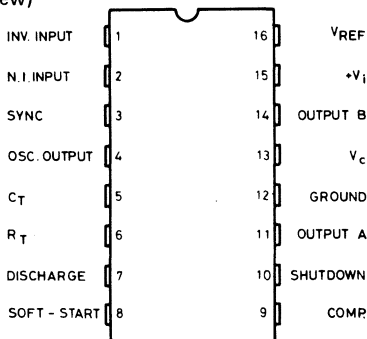
**DIP-16 Plastic (0.25)
and Ceramic**



SO-16P

CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)



S-6614

Type	Plastic DIP	Ceramic DIP	SO-16P
SG1525A	—	SG1525AJ	—
SG1527A	—	SG1527AJ	—
SG2525A	SG2525AN	SG2525AJ	SG2525AP
SG2527A	SG2527AN	SG2527AJ	SG2527AP
SG3525A	SG3525AN	SG3525AJ	SG3525AP
SG3527A	SG3527AN	SG3527AJ	SG3527AP



SG1525A/27A
SG2525A/27A
SG3525A/27A

ABSOLUTE MAXIMUM RATINGS

V_i	Supply voltage	40	V
V_C	Collector supply voltage	40	V
I_{osc}	Oscillator charging current	5	mA
I_o	Output current, source or sink	500	mA
I_R	Reference output current	50	mA
I_T	Current through C_T terminal	5	mA
	Logic inputs	-0.3 to +5.5	V
	Analog inputs	-0.3 to V_i	V
P_{tot}	Total power dissipation at $T_{amb} = 70^\circ\text{C}$	1000	mW
T_j	Junction temperature range	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature range	-65 to 150	$^\circ\text{C}$
T_{op}	Operating ambient temperature: SG1525A/27A SG2525A/27A SG3525A/27A	-55 to 125 -25 to 85 0 to 70	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$

THERMAL DATA (DIP-16)

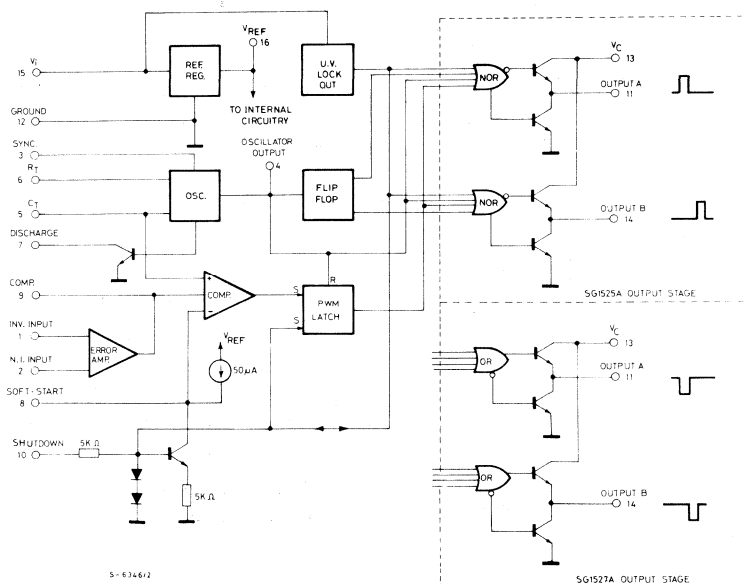
			Ceramic	Plastic
$R_{th\ j-pins}$	Thermal resistance junction-pins	max	—	50 $^\circ\text{C/W}$
$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	150 $^\circ\text{C/W}$	80 $^\circ\text{C/W}$

THERMAL DATA (SO-16P)

$R_{th\ j-alumina}^*$	Thermal resistance junction-alumina	max	50	$^\circ\text{C/W}$
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(*) Thermal resistance junction-alumina with the device soldered on the middle of an alumina supporting substrate measuring 15x20 mm; 0.65 mm thickness with infinite heatsink.

BLOCK DIAGRAM





SG1525A/27A
SG2525A/27A
SG3525A/27A

ELECTRICAL CHARACTERISTICS ($V_i = 20V$, and over operating temperature, unless otherwise specified)

Parameter	Test conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	

REFERENCE SECTION

V_{REF}	Output voltage	$T_j = 25^\circ C$	5.05	5.1	5.15	5	5.1	5.2	V
ΔV_{REF}	Line regulation	$V_i = 8 \text{ to } 35V$		10	20		10	20	mV
ΔV_{REF}	Load regulation	$I_L = 0 \text{ to } 20 \text{ mA}$		20	50		20	50	mV
$\Delta V_{REF}/\Delta T^*$	Temp. stability	Over operating range		20	50		20	50	mV
*	Total output variation	Line, load and temperature	5		5.2	4.95		5.25	V
	Short circuit current	$V_{REF} = 0 \quad T_j = 25^\circ C$		80	100		80	100	mA
*	Output noise voltage	$10\text{Hz} \leq f \leq 10\text{kHz}, T_j = 25^\circ C$		40	200		40	200	μV_{rms}
ΔV_{REF}^*	Long term stability	$T_j = 125^\circ C, 1000 \text{ hrs}$		20	50		20	50	mV

OSCILLATOR SECTION**

*, •	Initial accuracy	$T_j = 25^\circ C$		± 2	± 6		± 2	± 6	%
*, •	Voltage stability	$V_i = 8 \text{ to } 35V$		± 0.3	± 1		± 1	± 2	%
$\Delta f/\Delta T^*$	Temp. stability	Over operating range		± 3	± 6		± 3	± 6	%
f_{MIN}	Minim. frequency	$R_T = 200 \text{ K}\Omega \quad C_T = 0.1 \mu F$			120			120	Hz
f_{MAX}	Maxim. frequency	$R_T = 2 \text{ K}\Omega \quad C_T = 470 \text{ pF}$	400			400			KHz
	Current mirror	$I_{RT} = 2 \text{ mA}$	1.7	2	2.2	1.7	2	2.2	mA
*, •	Clock amplitude		3	3.5		3	3.5		V
*, •	Clock width	$T_j = 25^\circ C$	0.3	0.5	1	0.3	0.5	1	μs
	Sync threshold		1.2	2	2.8	1.2	2	2.8	V
	Sync input current	Sync voltage = 3.5V		1	2.5		1	2.5	mA

ERROR AMPLIFIER SECTION ($V_{CM} = 5.1V$)

V_{OS}	Input offset voltage		0.5	5		2	10	mV
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SG1525A/27A
SG2525A/27A
SG3525A/27A

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	SG 1525A/2525A SG 1527A/2527A			SG 3525A SG 3527A			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_b	Input bias current		1	10		1	10	μA
I_{os}	Input offset current			1			1	μA
	DC open loop gain	$R_L \geq 10 M\Omega$	60	75	60	75		dB
*	Gain bandwidth product	$G_v = 0 \text{ dB}$ $T_j = 25^\circ C$	1	2	1	2		MHz
*, ■	DC transconduct.	$30 K\Omega \leq R_L \leq 1 M\Omega$ $T_j = 25^\circ C$	1.1	1.5	1.1	1.5		mS
	Output low level		0.2	0.5	0.2	0.5		V
	Output high level		3.8	5.6	3.8	5.6		V
CMR	Comm.mode rejec.	$V_{CM} = 1.5 \text{ to } 5.2 V$	60	75	60	75		dB
PSR	Supply voltage rejection	$V_i = 8 \text{ to } 35 V$	50	60	50	60		dB

PWM COMPARATOR

	Minim. duty-cycle			0			0	%	
	Maxim. duty-cycle		45	49		45	49	%	
•	Input threshold	Zero duty-cycle	0.7	0.9		0.7	0.9	V	
		Maximum duty-cycle		3.3	3.6		3.3	3.6	V
*	Input bias current			0.05	1		0.05	1	μA

SHUTDOWN SECTION

	Soft start current	$V_{SD} = 0 V$, $V_{SS} = 0 V$	25	50	80	25	50	80	μA
	Soft start low level	$V_{SD} = 2.5 V$		0.4	0.7		0.4	0.7	V
	Shutdown threshold	To outputs, $V_{SS} = 5.1 V$ $T_j = 25^\circ C$	0.6	0.8	1	0.6	0.8	1	V
	Shutdown input current	$V_{SD} = 2.5 V$		0.4	1		0.4	1	mA
*	Shutdown delay	$V_{SD} = 2.5 V$ $T_j = 25^\circ C$		0.2	0.5		0.2	0.5	μs

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	

OUTPUT DRIVERS (Each output) ($V_C = 20V$)

Output low level	$I_{sink} = 20\text{ mA}$		0.2	0.4		0.2	0.4	V
	$I_{sink} = 100\text{ mA}$		1	2		1	2	V
Output high level	$I_{source} = 20\text{ mA}$	18	19		18	19		V
	$I_{source} = 100\text{ mA}$	17	18		17	18		V
Under-voltage lockout	V_{comp} and $V_{ss} = \text{high}$	6	7	8	6	7	8	V
I_C Collector leakage	$V_C = 35V$			200			200	μA
t_r^* Rise time	$C_L = 1\text{ nF}$, $T_j = 25^\circ C$		100	600		100	600	ns
t_f^* Fall time	$C_L = 1\text{ nF}$, $T_j = 25^\circ C$		50	300		50	300	ns

TOTAL STANDBY CURRENT

I_s Supply current	$V_i = 35V$		14	20		14	20	mA
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* These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

- Tested at $f_{osc} = 40\text{ KHz}$ ($R_T = 3.6\text{ K}\Omega$, $C_T = 0.1\text{ }\mu F$, $R_D = 0\Omega$). Approximate oscillator frequency is defined by:

$$f = \frac{1}{C_T (0.7 R_T + 3 R_D)}$$

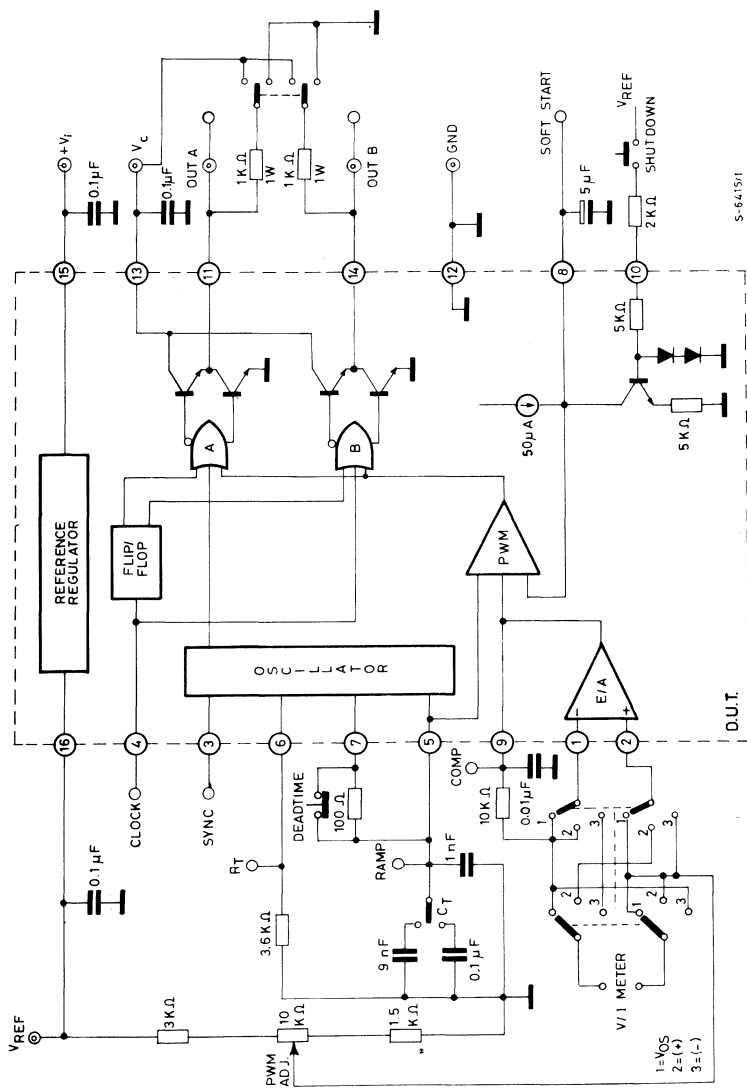
- DC transconductance (g_M) relates to DC open-loop voltage gain (G_V) according to the following equation: $G_V = g_M R_L$ where R_L is the resistance from pin 9 to ground. The minimum g_M specification is used to calculate minimum G_V when the error amplifier output is loaded.

RECOMMENDED OPERATING CONDITIONS (●)

Input voltage (V_i)	8 to 35 V
Collector supply voltage (V_C)	4.5 to 35 V
Sink/source load current (steady state)	0 to 100 mA
Sink/source load current (peak)	0 to 400 mA
Reference load current	0 to 20 mA
Oscillator frequency range	100 Hz to 400 KHz
Oscillator timing resistor	2 K Ω to 150 K Ω
Oscillator timing capacitor	0.001 μF to 0.1 μF
Dead time resistor range	0 to 500 Ω

(●) Range over which the device is functional and parameter limits are guaranteed.

TEST CIRCUIT





SG1525A/27A
SG2525A/27A
SG3525A/27A

Fig. 1 - Oscillator charge time vs. R_T and C_T

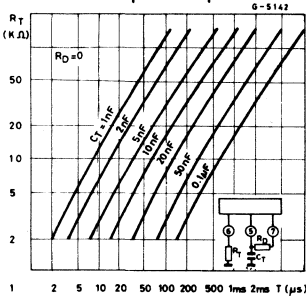


Fig. 2 - Oscillator discharge time vs. R_D and C_T

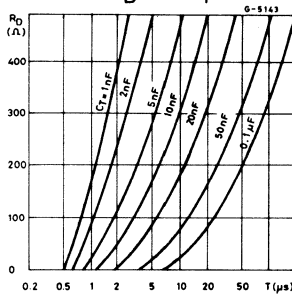


Fig. 3 - SG1525A output saturation characteristics

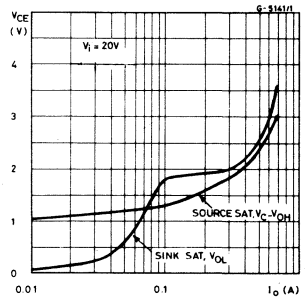


Fig. 4 - Error amplifier voltage gain and phase vs. frequency

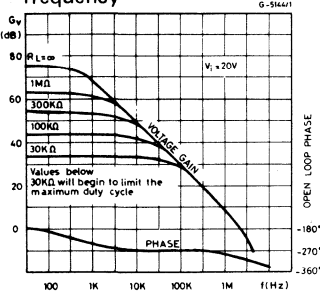
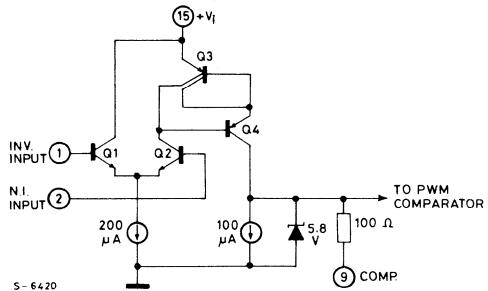


Fig. 5 - SG1525A error amplifier



PRINCIPLES OF OPERATION

SHUTDOWN OPTIONS (See Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 μ A to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is

immediately set providing the fastest turn-off signal to the outputs; and a 150 μ A current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

Fig. 6 - SG1525A oscillator schematic

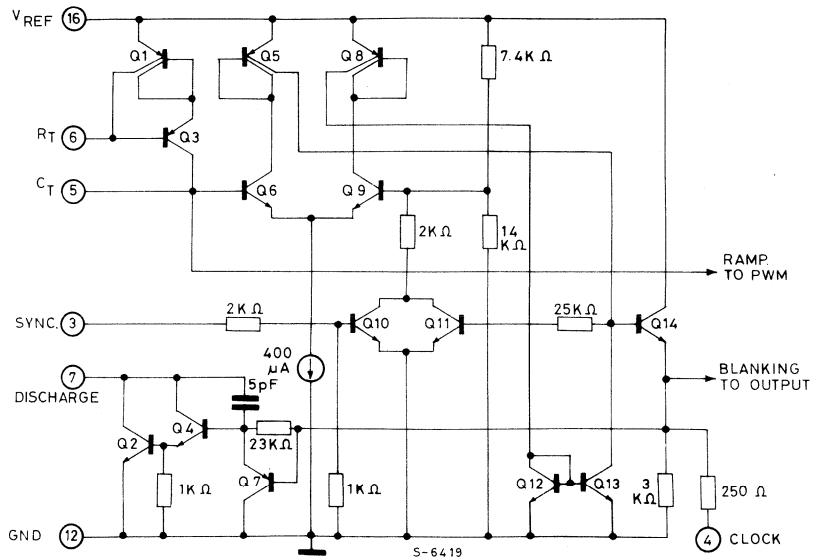


Fig. 7 - SG1525A output circuit (½ circuit shown)

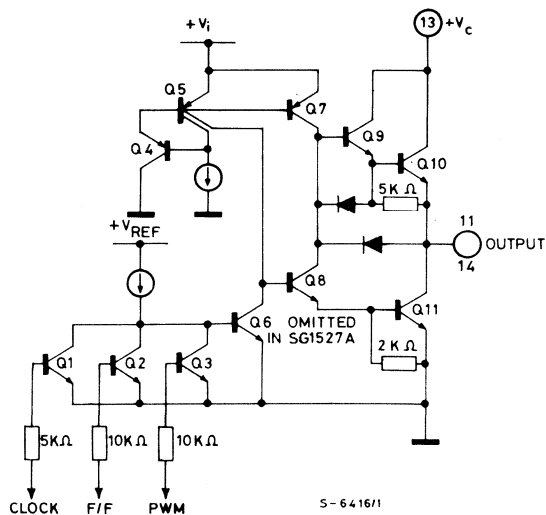
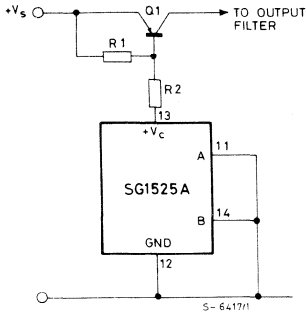
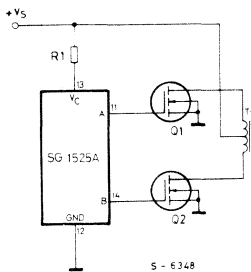


Fig. 7



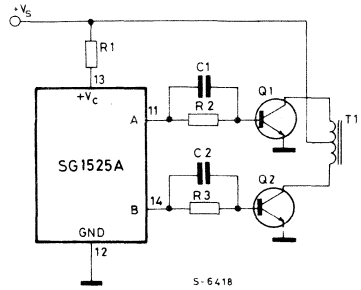
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

Fig. 9



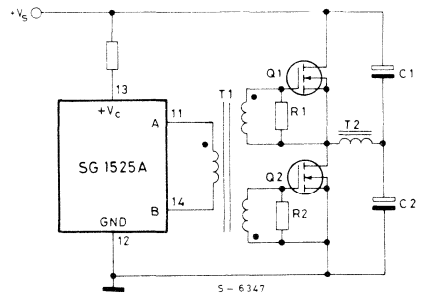
The low source impedance of the output drivers provides rapid charging of Power Mos input capacitance while minimizing external components.

Fig. 8



In conventional push-pull bipolar designs, forward base drive is controlled by R_1 – R_3 . Rapid turn-off times for the power devices are achieved with speed-up capacitors C_1 and C_2 .

Fig. 10



Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

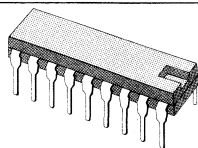
SWITCH-MODE POWER SUPPLY CONTROLLER

- LOW START-UP CURRENT
- DIRECT CONTROL OF SWITCHING TRANSISTOR
- COLLECTOR CURRENT PROPORTIONAL TO BASE-CURRENT INPUT
- REVERSE-GOING LINEAR OVERLOAD CHARACTERISTIC CURVE.

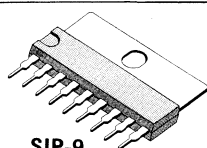
The TDA4601 is a monolithic integrated circuit designed to regulate and control the switching transistor of a switching power supply.

Because of its wide operational range and high

voltage stability even at high load changes: this IC can be used not only in TV receivers and video recorders but also in power supplies in Hi-Fi sets and active speakers.



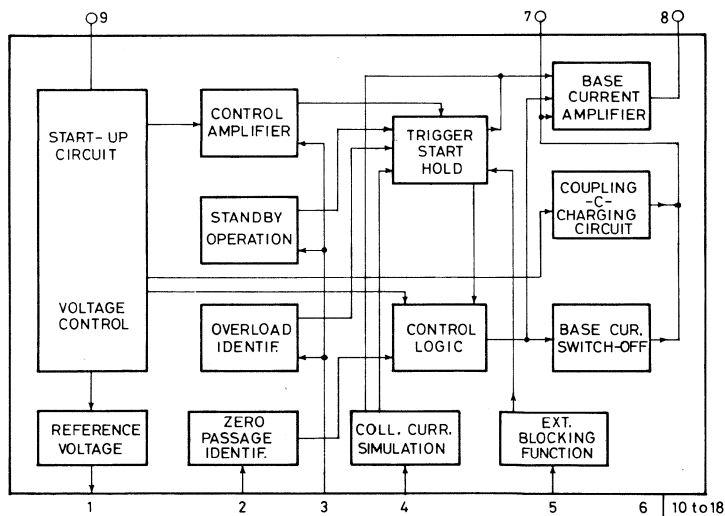
Powerdip (9 + 9)



SIP-9

ORDERING NUMBER: TDA4601 (SIP-9)
TDA4601B (9 + 9)

BLOCK DIAGRAM

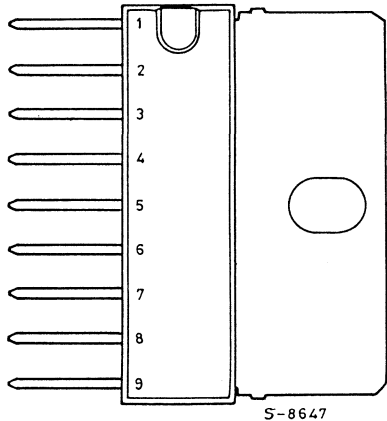
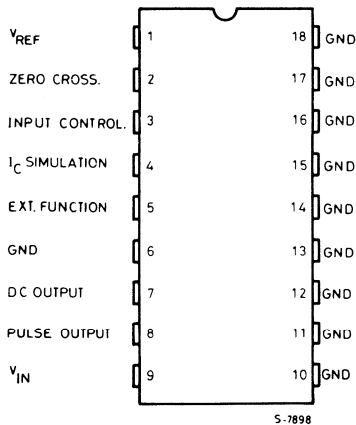


S-7897

ABSOLUTE MAXIMUM RATINGS

V_9	Supply voltage	20	V
V_1	Reference output	6	V
V_2	Identification input	-0.6 to 0.6	V
V_3	Controlled amplifier	3	V
V_4, V_5		8	V
V_7, V_8		V_9	
I_2, I_3		-3 to 3	mA
I_4		5	mA
I_5		5	mA
I_7		1.5	A
I_8		-1.5	A
T_{amb}	Operating Ambient Temperature	0 to 85	°C
T_{stg}	Storage temperature	-40 to 150	°C
T_j	Junction temperature	-40 to 125	°C
T_{amb}	Ambient temperature	0 to 85	°C

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction pins	max	15°C/W
$R_{th\ j-amb}$	Thermal resistance junction ambient	max	70°C/W

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_9 Operating supply voltage range		7.8		18	V

Start condition (according to test circuit of fig. 1)

I_9 Supply current (V_1 not yet switched on)	$V_9 = 2\text{V}$ $V_9 = 5\text{V}$ $V_9 = 10\text{V}$		1.5 2.4	0.5 2.0 3.2	mA mA mA
V_9 Switch threshold (V_1)		11	11.8	12.3	V

Normal operation ($V_9 = 10\text{V}$, $V_{cont} = -10\text{V}$, $V_{clock} = \pm 0.5\text{V}$, $f = 20\text{KHz}$, duty cycle 1:2 after switch on)

I_9 Supply current	$V_{cont} = -10\text{V}$ $V_{cont} = 0\text{V}$	110 50	135 75	160 100	mA mA
V_{ref} Voltage reference at pin 1	$I_1 < 0.1\text{ mA}$ $I_1 = 5\text{ mA}$	4 4	4.2 4.2	4.5 4.4	V V
V_3 Control voltage	$V_{cont} = 0\text{V}$	2.3	2.6	2.9	V
V_4 Collector current simulation voltage	$V_{cont} = 0\text{V}$ (see Note 1)	1.8	2.2	2.5	V
ΔV_4 Collector current simulation voltage	$V_{cont} = 0\text{V}$ to -10V (see note 1)	0.3	0.4	0.5	V
V_5 External protection threshold		6	7	8	V
V_7 Pin 7 output voltage	$V_{cont} = 0\text{V}$ (see note 1)	2.7	3.3	4.0	V
V_8 Pin 8 output voltage	$V_{cont} = 0\text{V}$ (see note 1)	2.7	3.4	4.0	V
V_8 Pin 8 output voltage change	$V_{cont} 0\text{V}$ to -10V (see note 1)	1.6	2	2.4	V
V_2 Feedback voltage	(see note 1)		0.2		V
T_{K1} Reference voltage temperature coeffic.			10^{-3}		1/K

Protection operation ($V_9 = 10\text{V}$; $V_{cont} = -10\text{V}$; $V_{clock} = \pm 0.5\text{V}$; $f = 20\text{KHz}$; duty cycle 1 : 2)

I_9 Supply current	$V_5 \leq 1.8\text{V}$	14	22	28	mA
V_7 Switch-off voltage	$V_5 \leq 1.8\text{V}$	1.3	1.5	1.8	V
V_4		1.8	2.1	2.5	V

ELECTRICAL CHARACTERISTICS (Continued)

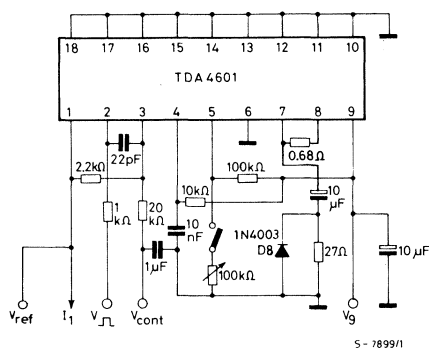
Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V ₅		V _{cont} = 0V	$\frac{V_1}{2} - 0.1$	$\frac{V_1}{2}$		V
V ₉	Supply voltage for V ₈ blocked	V _{cont} = 0V	6.7	7.4	7.8	V
ΔV ₉	Supply voltage for V ₁ off while further decreasing V ₉		0.3	0.6	1	V

Electrical characteristics (according to test circuit of fig. 2)

t_{on}	Secondary voltage switching time			350	450	ms
ΔV_2	Voltage variation with load	S_3 Closed $P_3 = 20W$		0.1	0.5	V
		S_2 Closed $P_2 = 15V$		0.5	1	V
ΔV_2	Stand by condition	S_1 Open $P_{load} = 3W$		20	30	V
f	Stand by frequency		70	75		KHz
P_P	Primary power consumption in stand by condition			10	12	VA

Note 1: only DC component

Fig. 1 – Test circuit



Test diagram: overload operation

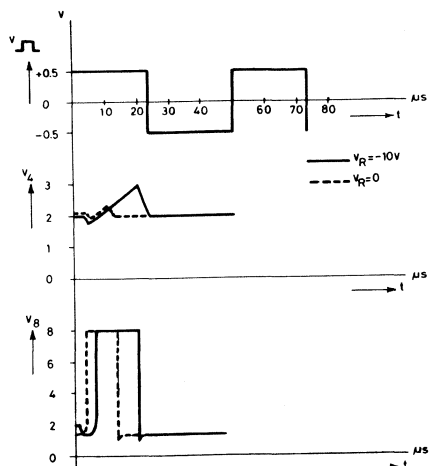
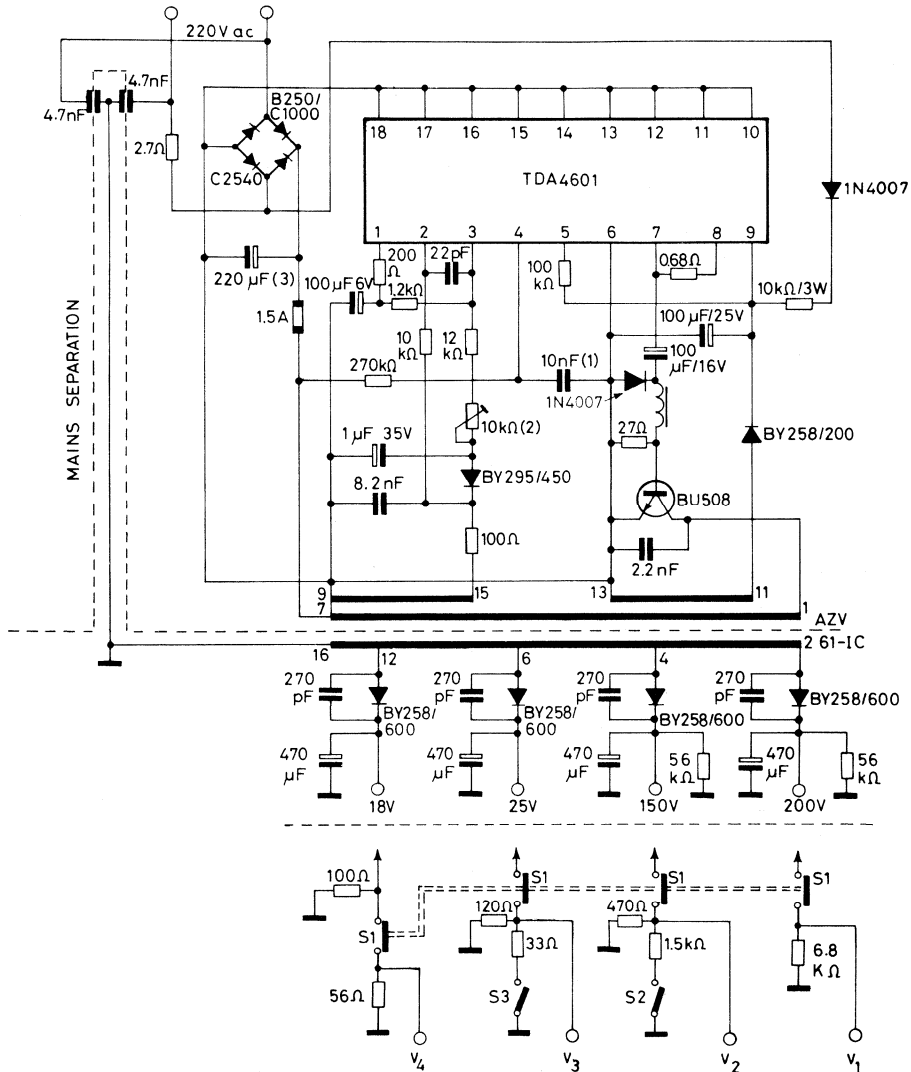


Fig. 2 – Test and application circuit



- 1) C limits the max. collector current of BU508 at overshooting the permissible output power.
- 2) Adjustment of secondary voltage.
- 3) Must be discharged before IC change.



Circuit description

The TDA 4601 regulates, controls, and protects the switching transistor in reverse converter power supplies at starting, normal, and overload operation.

Starting behaviour

During the start-up three consecutive operation states are passed.

1. An internal reference voltage is built up which supplies the voltage regulator and enables the supply to the coupling electrolytic capacitor and the switching transistor. Up to a supply voltage of $V_9 \approx 12V$, the current I_9 is less than 3.2 mA.
2. Release of the internal reference voltage $V_1 = 4V$. This voltage is abruptly available when $V_9 \approx 12V$ and enables all parts of the IC to be supplied from the control logic with a thermally stable and overload protected current supply.
3. Release of control logic. As soon as the reference voltage is available, the control logic is switched on through an additional stabilization circuit. Thus, the IC is ready for operation.

This start-up sequence is necessary to guarantee the supply through the coupling electrolytic capacitor to the switching transistor. Correct switching of the transistor is only in this way guaranteed.

Normal operation

Zero crossing of the feedback coil is registered at pin 2 and passed to the control logic.

At pin 3 (regulation of input, overload, and standby recognition) the rectified amplitude variations of the feedback coil are applied. The regulating amplifier works with an input voltage of about 2V and a current of about 1.4 mA.

Together with the collector current simulation pin 4, the overload recognition defines the operating region of the regulating amplifier depending on the internal reference voltage. The simulation of the collector current is generated by an external RC network at pin 4 an internally set voltage level. By increasing the capacitance (10 nF) the max. collector current of the switching transistor rises, thus setting the required operating range. The extent of the regulation lies between a 2V clamped DC voltage and an AC voltage rising in a sawtooth waveform, which

may vary up to a maximum amplitude of 4V (ref. voltage).

A reduction of the secondary load down to 20 watts causes the switching frequency to rise to about 50KHz at an almost constant pulse duty factor (period to on-time approx. 3). A further reduction of the secondary load down to about 1 watt results in changing the switching frequency to approx. 70KHz, and additionally the pulse duty factor rises to approx. 11. At the same time the collector peak current falls below 1 A.

In the trigger the output level of the regulating amplifier, the overload recognition, and the collector current simulation are compared and instructions are given to the control logic. There is an additional triggering and blocking possibility by means of pin 5. The output at pin 8 is blocked at a voltage of less than 2.2V at pin 5.

Depending on the start-up circuit, the zero crossing identification, and the release with the aid of the trigger, the control logic flip flops are set which control the base current amplifier and the base current shut-down. The base current amplifier moves the sawtooth voltage V_4 to pin 8. A current feed-back having an external resistance of $R = 0.68\Omega$ is inserted between pin 8 and pin 7. The resistance value determined the maximum amplitude of the base driving current for the switching transistor.

Protective measures

The base current shut-down, released by the control logic, clamps the output of pin 7 at 1.6V and thus blocks driving of the switching transistor. This protective measure will be released if the voltage at pin 9 reaches a value $\leq$ typ. 7.4V or if voltages of $\leq$ typ. 2.2V occur at pin 5. In the case of a short circuit of the secondary windings of the P.S.U., the IC continuously monitors the fault condition.

With the load completely removed from the secondary winding of the P.S.U., the IC is set to a low pulse duty factor. The total power consumption of the P.S.U. is held below $n = 6$ to 10 watts in both operating conditions. After having blocked the output, caused at a supply voltage $\leq$ typ. 7.4V, a further voltage reduction with $\Delta V_9 = 0.6V$ results in switching off the reference voltage (4V).

Fig. 3 - Frequency vs. output power (test circuit of fig. 2).

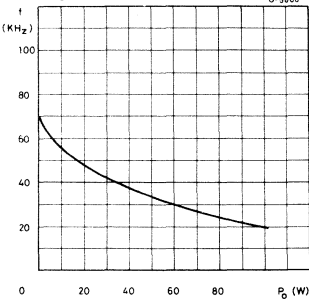


Fig. 4 - Efficiency vs. output power test circuit of fig. 2).

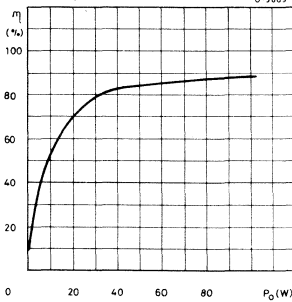


Fig. 5 - Load characteristics V_2 - f (I_{Q2}) (test circuit of fig. 2).

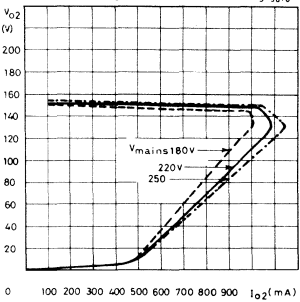


Fig. 6 - Output voltage V_2 (mains change) (test circuit of fig. 2).

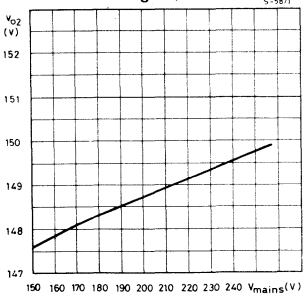
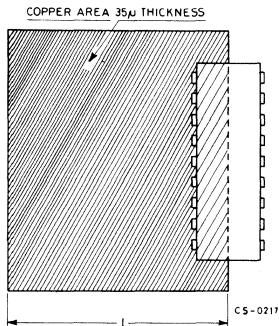


Fig. 7 - Example of a PC heatsink (35°C/W)





TDA7272

ADVANCE DATA

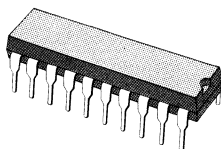
HIGH PERFORMANCE MOTOR SPEED REGULATOR

- TACHIMETRIC SPEED REGULATION WITH NO NEED FOR AN EXTERNAL SPEED PICK-UP
- V/I SUPPLEMENTARY PREREGULATION
- DIGITAL CONTROL OF DIRECTION AND MOTOR STOP
- SEPARATE SPEED ADJUSTMENT
- 5V TO 18V OPERATING SUPPLY VOLTAGE
- 1A PEAK OUTPUT CURRENT
- OUTPUT CLAMP DIODES INCLUDED
- SHORT CIRCUIT CURRENT PROTECTION
- THERMAL SHUT DOWN WITH HYSTeresis
- DUMP PROTECTION (40V)

TDA7272 is an high performance motor speed controller for small power DC motors as used in cassette players.

Using the motor as a digital tachogenerator itself the performance of true tacho controlled systems is reached.

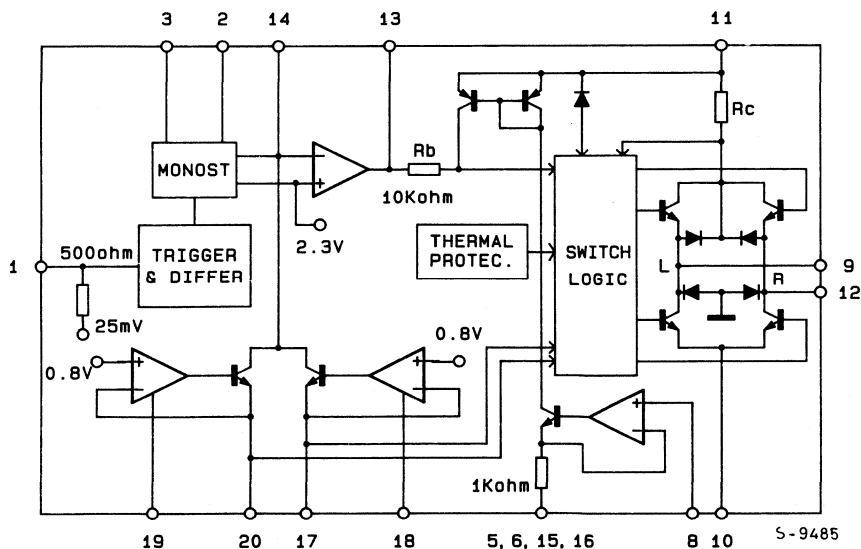
A dual loop control circuit provides long term stability and fast settling behaviour.



Powerdip
(16 + 2 + 2)

ORDERING NUMBER: TDA7272

BLOCK DIAGRAM





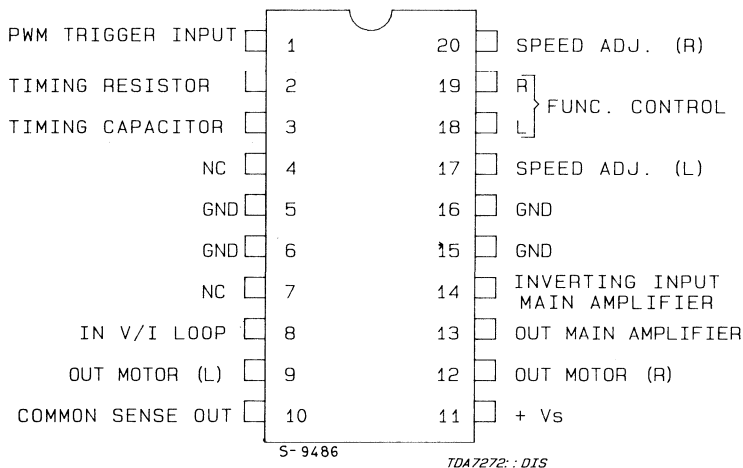
TDA7272

ABSOLUTE MAXIMUM RATINGS

V_S	DC supply voltage	24	V
V_S	Dump voltage (300ms)	40	V
I_O	Output current	internally limited	
P_{tot}	Power dissipation at $T_{pins} = 90^{\circ}C$ at $T_{amb} = 70^{\circ}C$	4.3	W
T_j	Operating junction temperature	1	W
T_{stg}	Storage temperature	-40 to 150	$^{\circ}C$
		-40 to 150	$^{\circ}C$

CONNECTION DIAGRAM

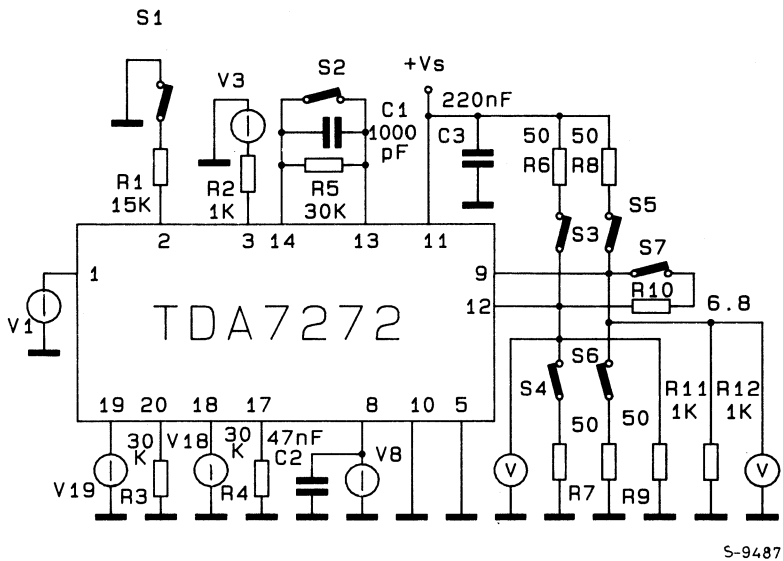
(Top view)



THERMAL DATA

$R_{thj-amb}$	Thermal resistance junction-ambient	max	80	$^{\circ}C/W$
$R_{thj-pins}$	Thermal resistance junction-pins	max	14	$^{\circ}C/W$

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; V_S = 13.5V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _S	Operating supply voltage	5		18	V
I _S	Supply current	No load	5	12	mA

OUTPUT STAGE

I _O	Output current pulse		1		A
I _O	Output current continuous		250		mA
V _{10-9, 12}	Voltage drop	I _O = 250mA	1.2	1.5	V
V _{11-9, 12}	Voltage drop	I _O = 250mA	1.7	2	V

**ELECTRICAL CHARACTERISTICS** (continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
MAIN AMPLIFIER					
R_{14}	Input resistance	100			$K\Omega$
I_b	Bias current		50		nA
V_{OFF}	Offset voltage		1	5	mV
V_R	Reference voltage	Internal at non inverting input		2.3	V

CURRENT SENSE AMPLIFIER V/T LOOP

R_8	Input resistance	100			$K\Omega$
G_L	Loop gain		9		V

TRIGGER AND MONOSTABLE STAGE

V_{IN1}	Input allowed voltage	-0.7		3	V
R_{IN1}	Input resistance		500		Ω
$V_{T Low}$	Trigger level		0		V
V_{TB}	Bias voltage (pin 1)	15	20	25	mV
V_{TH}	Trigger hysteresis		10		mV
$V_{2 REF}$	Reference voltage	750	800	850	mV

SPEED PROGRAMMING AND DIRECTION CONTROL LOGIC (and current source programming)

$V_{18, 19 Low}$	Input Low level			0.7	V
$V_{18, 19 High}$	Input High level	2			V
$I_{18, 19}$	Input current	$0 < V_{18, 19} < V_S$		2	μA
$V_{17, 20 REF}$	Reference voltage	750	800	850	mV

OPERATING PRINCIPLE

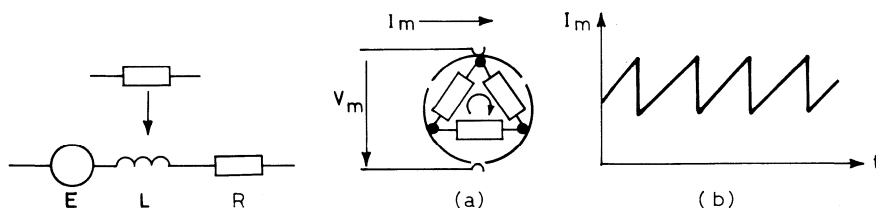
The TDA7272 novel applied solution is based on a tachometer control system without using such extra tachometer system. The information of the actual motor speed is extracted from the motor itself. A DC motor with an odd number of poles generates a motor current which contains a fixed number of discontinuities within each rotation. (6 for the 3 pole motor example on Fig. 1)

Deriving this inherent speed information from the motor current, it can be used as a replacement of a low resolution AC tachometer system. Because the settling time of the control loop is

limited on principle by the resolution in time of the tachometer, this control principle offers a poor reaction time for motors with a low number of poles. The realized circuit is extended by a second feed forward loop in order to improve such system by a fast auxiliary control path.

This additional path senses the mean output current and varies the output voltage according to the voltage drop across the inner motor resistance. Apart from a current averaging filter, there is no delay in such loop and a fast settling behaviour is reached in addition to the long term speed motor accuracy.

Fig. 1 - Equivalent of a 3 pole DC motor (a) and typical motor current waveform (b)



S - 9494

BLOCK DESCRIPTION

The principle structure of the element is shown in Fig. 2. As to be seen, the motor speed information is derived from the motor current sense drop across the resistor R_S ; capacitor CD together with the input impedance of 500Ω at pin 1 realizes a high pass filter.

This pin is internally biased at 25mV, each negative zero transition switches the input comparator. A 10mV hysteresis improves the noise immunity.

The trigger circuit is followed by an internal delay time differentiator.

Thus, the system becomes widely independent of the applied waveform at pin 1, the differentiator triggers a monostable circuit which provides a constant current duration. Both, output

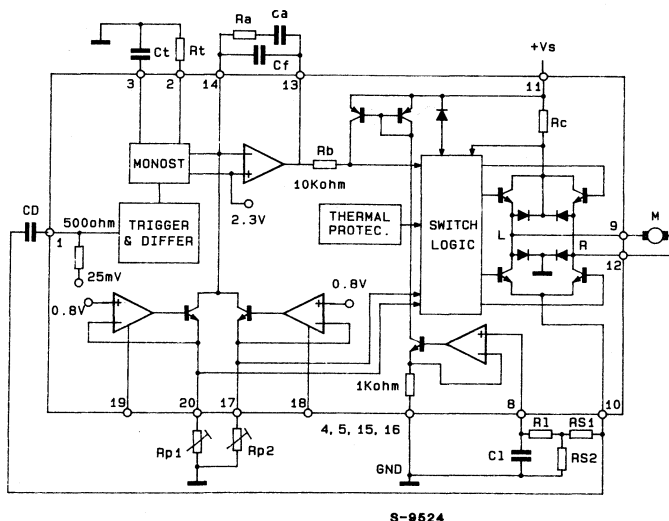
current magnitude and duration T , are adjustable by external elements CT and RT.

The monostable is retriggerable; this function prevents the system from fault stabilization at higher harmonics of the nominal frequency. The speed programming current is generated by two separate external adjustable current sources. A corresponding digital input signal enables each current source for left or right rotation direction. Resistor RP1 and RP2 define the speed, the logical inputs are at pin 18 and 19.

At the inverting input (pin 14) of the main amplifier the reference current is compared with the pulsed monostable output current.

For the correct motor speed, the reference current matches the mean value of the pulsed monostable current. In this condition the charge of the feedback capacitor becomes constant.

Fig. 2 - Block diagram



The speed n of a k pole motor results:

$$n = \frac{10,34}{K C_T R 17,20} (\text{min}^{-1})$$

and becomes independent of the resistor R_T which only determines the current level and the duty cycle which should be 1 : 1 at the nominal speed for minimum torque ripple.

The second fast loop consists of a voltage to current converter which is driven at pin 8 by the low pass filter R_L, C_L . The output current at this stage is injected by a PNP current mirror into the inner resistor R_B . So the driving voltage of the output stage consists of the integrator output voltage plus the fast loop voltage contribution across R_B .

The power output stage realizes different modes depending on the logic status at pin 18 and 19.

- Normal operation for left and right mode: each upper TR of the bridge is used as voltage follower whereas the lower acts as a switch.
- Stop mode where the upper half is open and the lower is conductive.
- High impedance status where all power elements are switched-off.

The high impedance status is also generated when the supply voltage overcomes the 5V to 20V operating range of when the chip temperature exceeds 150°C.

A short circuit protection limits the output current at 1.5A. Integrated diodes clamp spikes from the inductive load both at V_{CC} and ground.

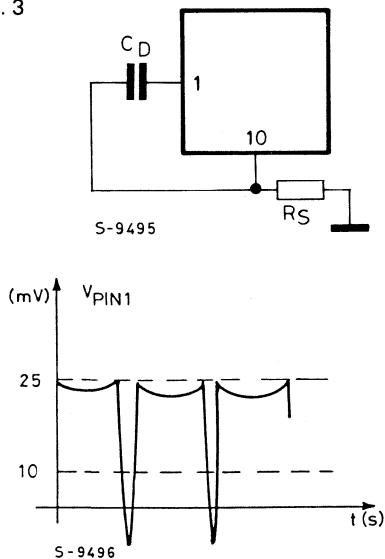
The reference voltages are derived from a common bandgap reference. All blocks are widely supplied by an internal 3.5V regulator which provides a maximum supply voltage rejection.

PIN FUNCTION AND APPLICATION INFORMATION

Pin 1

Trigger input. Receives a proper voltage which contains the information of the motor speed. The waveform can be derived directly by the motor current (Fig. 3). The external resistor generates a proper voltage drop. Together with the input resistance at pin 1 [$R_{IN} (1) = 500\Omega$] the external capacitor C_D realize a high pass filter which differentiates the commutation spikes of the motor current. The trigger level is 0V.

Fig. 3

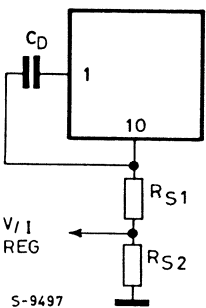


The biasing of the pin 1 is 25mV with a hysteresis of 10mV. So the sensing resistance must be chosen high enough in order to obtain a negative spike of the least 30mV on pin 1, also with minimum variation of motor current:

$$R_S \geq \frac{30\text{mV}}{\Delta I_{\text{MOT min.}}}$$

Such value can be too much high for the pre-regulation stage V-I and it could be necessary to split them into 2 series resistors $R_S = R_{S1} + R_{S2}$ (see fig. 4) as explained on pin 8 section.

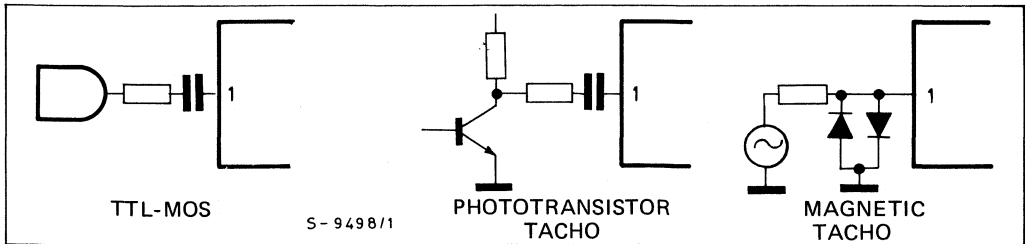
Fig. 4



The information can be taken also from an external tachogenerator. Fig. 5 shows various sources connections:

the input signal mustn't be lower than -0.7V.

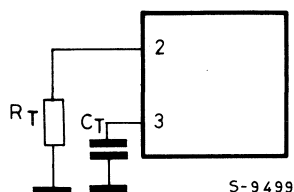
Fig. 5



Pin 2

Timing resistor. An internal reference voltage ($V_2 = 0.8V$) gives possibility to fix by an external resistor (R_T), from this pin and ground, the output current amplitude of the monostable circuit, which will be reflected into the timing capacitor (pin 3); the typical value would be about $50\mu A$.

Fig. 6



Pin 3

Timing capacitor. A constant current, determined by the pin 2 resistor, flowing into a capacitor between pin 3 and ground provides the output pulse width of the monostable circuit, the max voltage at pin 3 is fixed by an internal threshold: after reaching this value the capacitor is rapidly discharged and the pulse width is fixed to the value:

$$T_{on} = 2.88 R_T C_T \text{ (Fig. 6)}$$

Pin 4

Not connected.

Pin 5

Ground. Connected with pins 6, 15, 16.

Pin 6

Ground. Connected with pins 5, 15, 16.

Pin 7

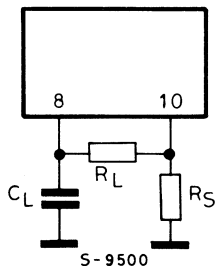
Not connected.

Pin 8

Input V/I loop. Receives from pin 10, through a low pass filter, the voltage with the information of the current flowing into the motor and produces a negative resistance output:

$$R_{out} = -9 R_S \text{ (Fig. 7)}$$

Fig. 7



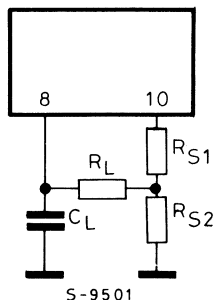
For compensating the motor resistance and avoiding instability:

$$R_S \leq \frac{R_{MOTOR}}{9}$$

The optimization of the resistor R_S for the tachometric control must not give a voltage too high for the V/I stage: one solution can be to divide in two parts, as shown in Fig. 8, with:

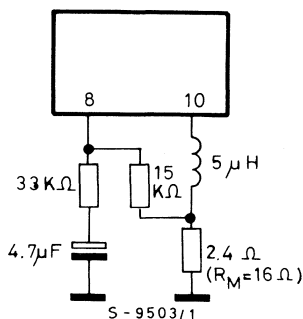
$$R_{S2} = \frac{R_M}{10} \text{ and } R_{S1} + R_{S2} \geq \frac{30mV}{\Delta I \text{ mot min}} \text{ (see pin 1 sect.)}$$

Fig. 8



The low pass filter R_L , C_L must be calculated in order to reduce the ripple of the motor commutation at least 20dB. Another example of possible pins 10-8 connections is showed on Fig. 9. A choke can be used in order to reduce the radiation.

Fig. 9



Pin 9

Output motor left. The four power transistors are realized as darlington structures. The arrangement is controlled by the logic status at pins 18 and 19.

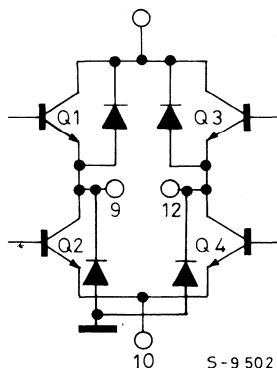
As before explained (see block description), in the normal left or right mode one of the lower darlington becomes saturated whereas the other remains open. The upper half of the bridge operates in the linear mode.

In stop condition both upper bridge darlingtones are off and both lower are on. In the high output impedance state the bridge is switched completely off.

Connecting the motor between pins 9 and 12 both left or right rotation can be obtained. If only one rotation sense is used the motor can be connected at only one output, by using only the upper bridge half. Two motors can be connected each at the each output: in such case they will work alternatively (See Application Section).

The internal diodes, together with the collector substrate diodes, protect the output from inductive voltage spikes during the transition phase.

Fig. 10



Pin 10

Common sense output. From this pin the output current of the bridge configuration (motor current) is fed into R_S external resistor in order to generate a proper voltage drop.

The drop is supplied into pin 1 for tachometric control and into pin 8 for V/I control (See pin 1 and pin 8 sections).

Pin 11

Supply voltage.

Pin 12

Output motor right. (See pin 9 section)

Pin 13

Output main amplifier. The voltage on this pin results from the tachometric speed control and feeds the output stage.

The value of the capacitor C_F (Fig. 4), connected from pins 13 and 14, must be chosen low enough in order to obtain a short reaction time of the tachometric loop, and high enough in order to reduce the output ripple.

A compromise is reached when the ripple voltage (peak-to-peak) V_{ROP} is equal to $0.1 V_{MOTOR}$:

$$C_F = 2.3 \frac{C_T}{V_{RIP}} \left(1 - \frac{R_T}{R_P}\right)$$

$$\text{with } V_{RIP} = \frac{V_{FEM} + I_{MOT} \cdot R_{MOT}}{10}$$

with duty cycle = 50%. (See pin 2-3 section)

Fig. 11

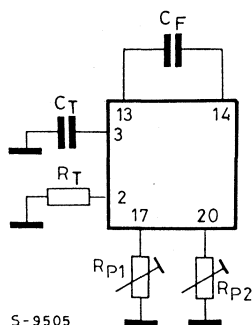
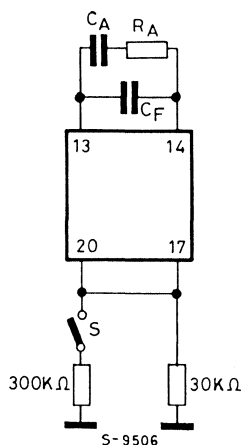


Fig. 12



In order to compensate the behaviour of the whole system regulator-motor-load (considering axis friction, load torque, inertias moment of the motor of the load. etc.) a RC series network is also connected between pins 13 and 14 (Fig. 12). The value of C_A and R_A must be chosen experimentally as follows:

- Increase of 10% the speed with respect to the nominal value by connecting in parallel to R_P a resistor with value about 10 time larger.

- Vary the R_A and C_A values in order to obtain at pin 13 a voltage signal with short response time and without oscillations. Fig. 13 shows the step response at pin 13 versus R_A and C_A values.

Fig. 13

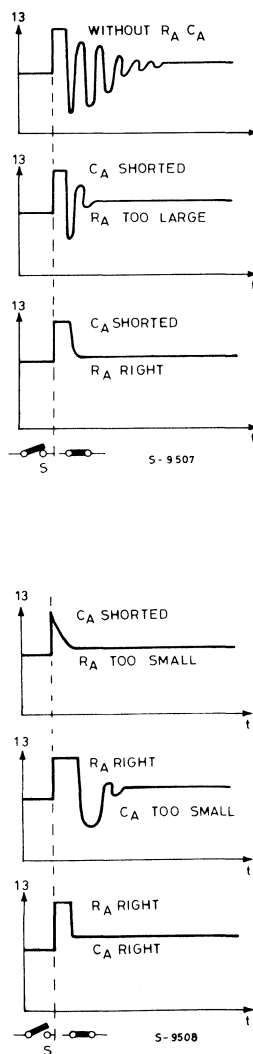
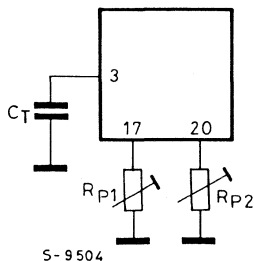


Fig. 14

Pin 14

Inverting input of main amplifier. In this pin the current reference programmed at pins 20, 17 is compared with the current from the monostable (stream of rectangular pulses).

In steady-state condition (constant motor speed) the values are equal and the capacitor C_F voltage is constant.

This means for the speed n (min⁻¹):

$$n = \frac{10.435}{C_T \cdot m \cdot R_P}$$

where "m" is the number of collector segments. (poles)

The non inverting input of the main amplifier is internally connected to a reference voltage (2.3V).

Pin 15

Ground.

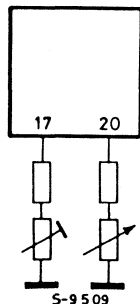
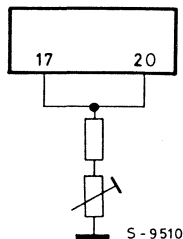
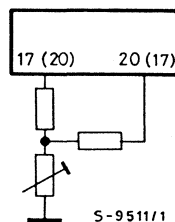
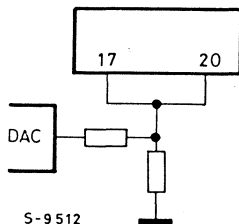
Pin 16

Ground.

Pin 17

Left speed adjustment. The voltage at this pin is fixed to a reference value of 0.8V. A resistor from this pin and ground (Fig. 14) fixes the reference current which will be compared with the medium output current of the monostable in order to fix the speed of the motor at the programmed value. The correct value of R_P would be:

$$R_P = \frac{10.435}{C_T \cdot m \cdot n} \quad \begin{matrix} n = \text{motor speed, (min}^{-1}\text{)} \\ m = \text{poles number} \end{matrix}$$

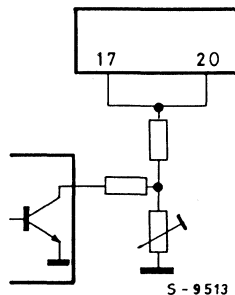
Fig. 15

Fig. 16

Fig. 17

Fig. 18


The control of speed can be done in different way:

- speed separately programmed in two senses of rotation (Figg. 14-15);
- only one speed for the two senses of rotation (Fig. 16);
- speeds of the two senses a bit different (i.e. for compensating different pulley effects) (Fig. 17);
- speed programmed with a DC voltage (Fig. 18) i.e. with DA converter;
- fast forward, by putting a resistor. In this case it is necessary that also at the higher speed for the duty cycle to be significantly less than 1 (see value of R_T , C_T on pin 2, pin 3 sections).

Fig. 19 shows the function controlled with a μP .

Fig. 19



Pin 18

Right function control. The voltages applied to this pin and to pin 19 determine the function, as showed in the table.

The typical value of the threshold (L-H) is 1.2V.

CONDITION		OUTPUT FUNCTION	OUTPUT VOLTAGE	
Pin 18	Pin 19		Pin 12	Pin 9
L	L	STOP	LOW	LOW
H	L	LEFT	LOW	REG
L	H	RIGHT	REG	LOW
H	H	OPEN	HIGH IMPEDANCE	

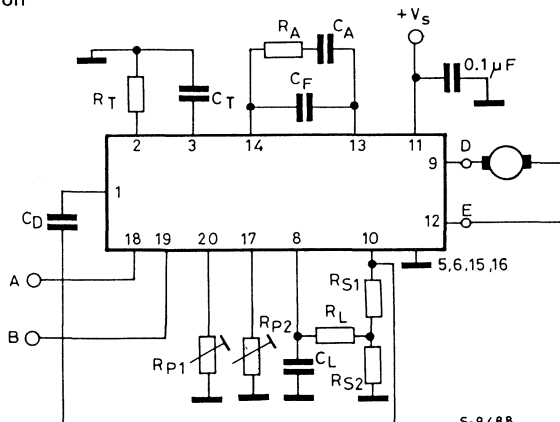
Pin 19

Left function control. (See pin 18 sect).

Pin 20

Right speed adjustment. (See pin 17 sect).

Fig. 20 - Typical application



S-9488

Fig. 21 - Tacho only speed regulation

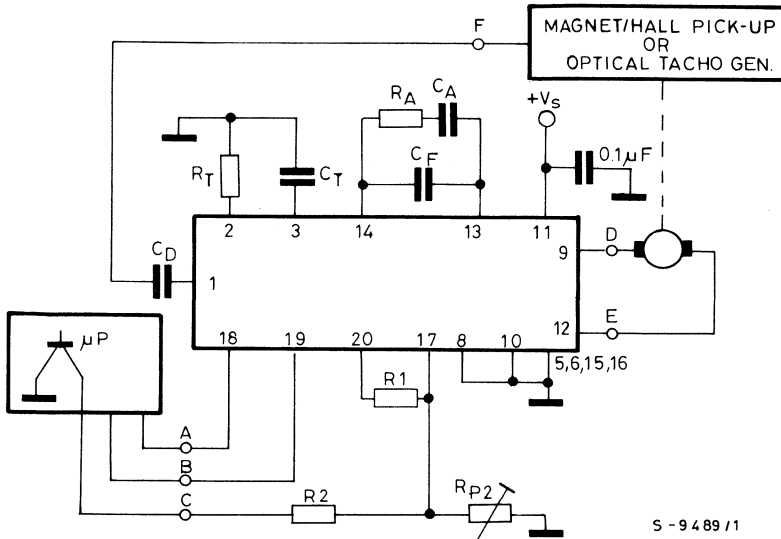


Fig. 22 - One direction reg. of one motor, or alternatively of two motors

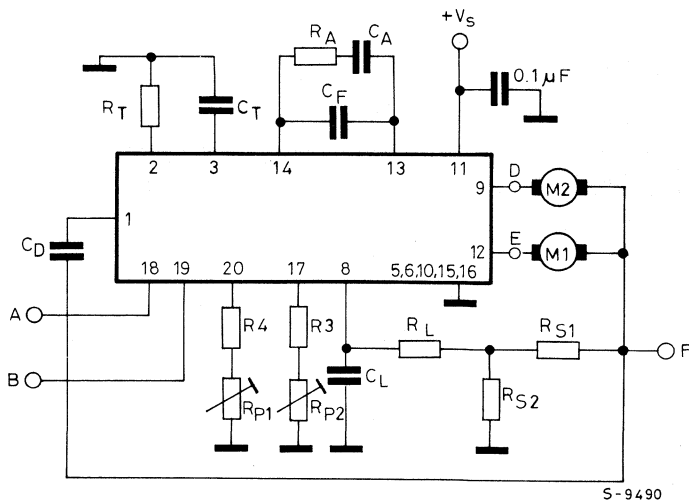
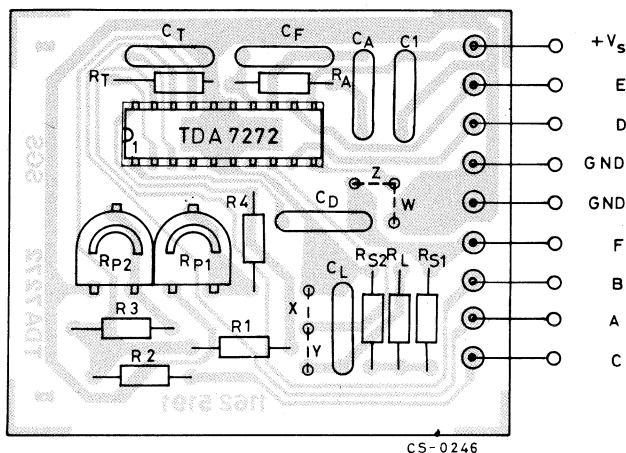


Fig. 23 – P.C. board and components layout of the circuits of Figg. 20, 21, 22



APPLICATION SUGGESTION (Fig. 20) – (For a 2000 r.p.m. 3 pole DC motor with $R_M = 16\Omega$)

Comp.	Recommended value	Purpose	If larger	If smaller	Allowed range	
					Min.	Max.
R_{S1}	1Ω	Current sensing tacho loop.		Tacho loop do not regulate.	0	
R_{S2}	1.5Ω	Curr. sensing V/I loop.	Instability may occur.	Motor regulator; undercompens.	0	$R_{MOT}/9$
$R_L; C_L$	$22K\Omega - 68nF$	Spike filtering.	Slow V/I regulator response.	High output ripple.		
C_D	$68nF$	Pulse transf.			$33nF$	$100nF$
$R_T; C_T$	$15K\Omega - 47nF$	Current source programming to obtain a 50% duty cycle.			$6K\Omega$	$30K\Omega$
$R_{P1}; R_{P2}$	$47K\Omega$ trim.	Set of speed.	Low speed.	High speed.	0	
C_F	Polyester $100nF$	Optimization of integrator ripple and loop response time.	Lower ripple, slower tacho-regulator response.	Higher ripple, faster response.	$10nF$	$470nF$
$R_A; C_A$	$220K\Omega - 220nF$	Fast response with no overshoot.	Depending on electromechanical system.		$10K\Omega$ $10nF$	$10M\Omega$ $1\mu F$

Fig. 24 - Speed regulation versus supply voltage
(Circuit of Fig. 20)

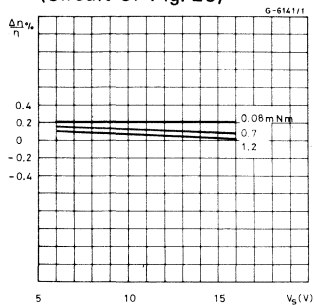


Fig. 25 - High current TDA7272 + 2 x L149 application

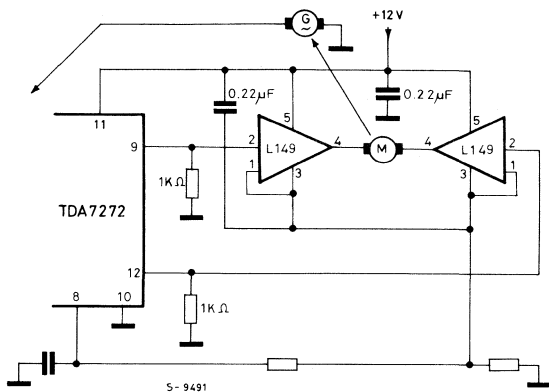
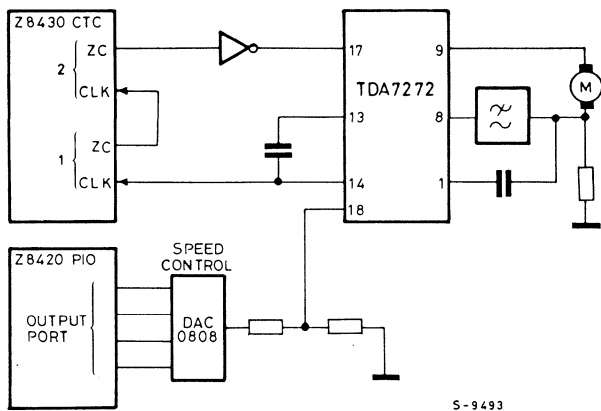


Fig. 26 - In connection with a presettable counter and I/O peripheral the TDA7272 controls the speed through a D/A converter





TDA8115

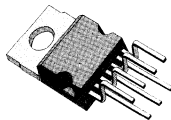
ADVANCE DATA

DUAL MOTOR DRIVER

- HIGH OUTPUT CURRENT, EACH CHANNEL UP TO 1A
- WIDE SUPPLY VOLTAGE RANGE, 4V UP TO 28V
- SHORT CIRCUIT PROTECTION
- SAFE OPERATING AREA CURRENT LIMITING
- TEMPERATURE SHUT DOWN WITH HYSTeresis
- HIGH INPUT IMPEDANCE
- GROUND COMPATIBLE INPUT

The TDA8115 is a monolithic integrated circuit

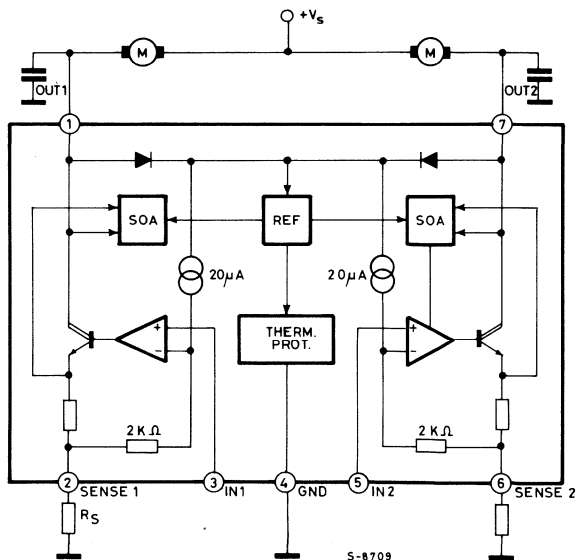
which realizes two independent programmable current sources. The device is well suited for motor driving applications such as reel motors in video recorders. A wide supply voltage range permits battery operation.



Heptawatt

ORDERING NUMBER: TDA8115

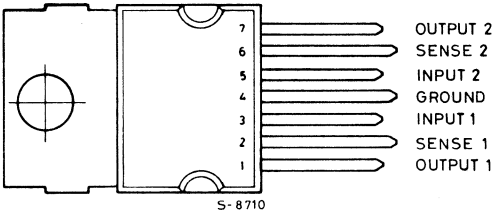
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	28	V
I_o	Output current (each channel)	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{op}	Operation junction temperature	-40 to +150	°C
T_{stg}	Storage temperature	-40 to +150	°C

CONNECTION DIAGRAM
(Top view)



Pin 4 connected to the TAB

THERMAL DATA

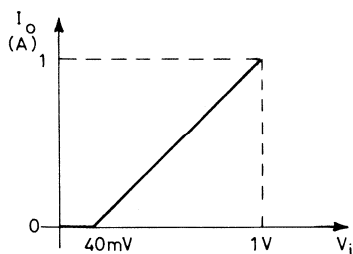
$R_{th\,j-case}$	Thermal resistance junction-case	max	3	°C/W
------------------	----------------------------------	-----	---	------



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _S Supply voltage		4		23	V
I _Q Quiescent current			2	5	mA
I _O Output current range				1	A
V _{IR} Input voltage range		0		V _S - 3	V
V _{OS} Positive input offset for current starting point		50	60	80	mV
	Thermal shut down		150		°C
	Hysteresis		20		°C
I _L Output current limit V _S = 10V V _S = 20V			1.4 0.4		A A
I _b Input bias current				1	μA
V _{sat} Saturation voltage	I _{OUT} = 0.9A		1.4	2	V
R _B Bond resistance			60		mΩ

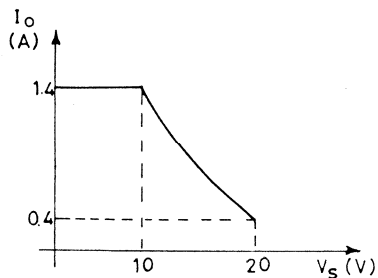
Fig. 1 – Transconductance characteristic



S-8711

$$\text{with } I_O = \frac{V_{IN} - 40\text{mV}}{(R_S + 60\text{m}\Omega)}$$

Fig. 2 – Max output current vs. supply voltage (SOA)



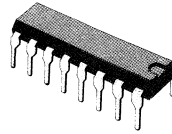
S-8712

FOUR PHASE BRUSHLESS MOTOR DRIVER

- WIDE OPERATING VOLTAGE RANGE 6V TO 14V
- HIGH CURRENT CAPABILITY UP TO 1A
- OUTPUT DC CURRENTS UP TO 0.4A
- TWO LOGICAL INPUTS FOR THE CODED COMMUNICATION SIGNAL
- LIMITED SLEW RATE OF THE OUTPUT VOLTAGE
- ANALOG INPUT WITH FIXED VOLTAGE GAIN
- INTEGRATED FLYBACK DIODES AT EACH OUTPUT
- THERMAL PROTECTION

The TDA 8116 is a monolithic integrated circuit in bipolar technology.

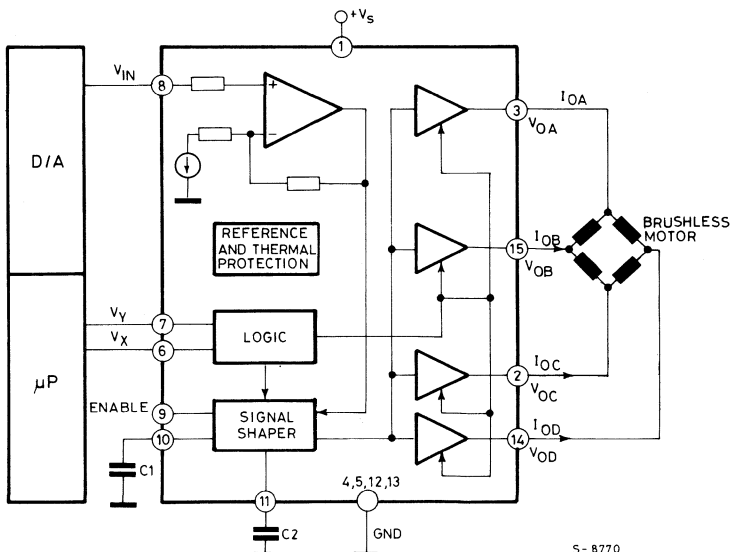
It is intended for driving a four phase brushless video head motor in microcomputer controlled servo systems.



Powerdip
12 + 2 + 2

ORDERING NUMBER: TDA 8116

BLOCK DIAGRAM



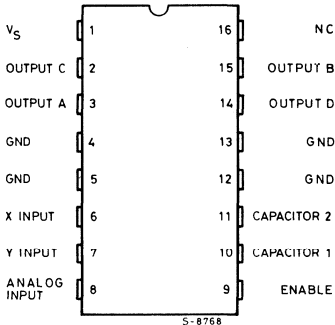
S- 8770

ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	-0.3 to 18	V
I_O	Output current DC	± 0.4	A
	Pulse output current (during start)	± 1	A
T_{JOP}	Operating junction temperature	0 to 150	°C
T_{stg}	Storage junction temperature	-40 to 150	°C
$V_{EN, IN, X, Y}$	Input voltage	-0.3 to 7	V
P_{tot}	Power dissipation at $T_{case} = 80^{\circ}C$	5	W

CONNECTION DIAGRAM

(Top view)



PIN FUNCTION

N°	NAME	FUNCTION
1	V_S	Supply voltage connection.
2	OUTC	Push-Pull type output for the C phase.
3	OUTA	Push-Pull type output for the A phase
4, 5, 12, 13	GND	Ground connection.
6	X INPUT	Commutation signal X input.
7	Y INPUT	Commutation signal Y input.
8	INPUT	Analog control signal input.
9	ENABLE	Enable input, with low level ($< 1,5V$) at this pin the device outputs are set into TRISTATE.
10, 11	CAPACITOR 1, 2	The shaping capacitors at these pins define the output signal shape of the A, C and B, D outputs respectively.
14	OUTD	Push-Pull type output for the D phase.
15	OUTB	Push-Pull type output for the B phase.
16	N.C.	No connection at this pin.

**THERMAL DATA**

Parameter		Min.	Typ.	Max.	Unit
T_{JSTD}	Thermal shut down threshold		150		$^{\circ}\text{C}$
T_{JSDH}	Thermal shut down hysteresis		20		$^{\circ}\text{C}$
$R_{th\ j-case}$	Thermal resistance junction-ground pins			14	$^{\circ}\text{C/W}$
$R_{th\ j-amb}$	Thermal resistance junction-ambient			80	$^{\circ}\text{C/W}$

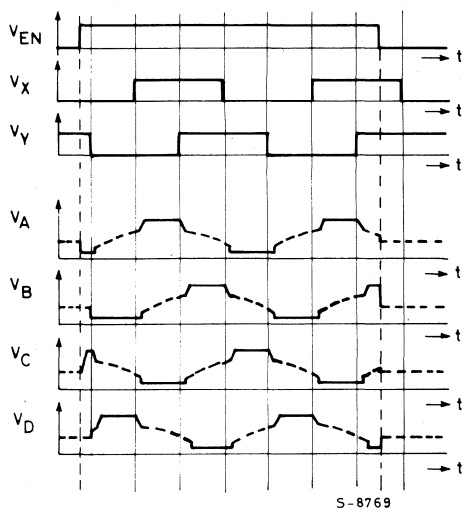
ELECTRICAL CHARACTERISTICS ($6\text{V} < V_S < 14\text{V}$, $T_J = 25^{\circ}\text{C}$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{Sop}	Operating supply voltage range		6		14	V
V_{SO}	Source stage saturation voltage	$V_{IN} = 5\text{V}$ $I_O = 0.4\text{A}$ $I_O = 1\text{A}$		1.4 1	2 1.4	V V
V_O	Sink stage saturation voltage	$V_{IN} = 5\text{V}$ $I_O = 0.4\text{A}$ $I_O = 1\text{A}$		1.4 1	2 1.4	V V
A_V	Voltage gain	$V_{IN} = 1\text{V}$ $R_L = 50\Omega$	2.5	2.75	3.0	V
V_{INth}	Input voltage threshold		0.6	0.7	0.8	V
I_N	Input current	$V_{IN} = 5\text{V}$	-5	-1	+5	μA
V_{IN}	Input voltage operating voltage range		0		$V_S - 1$	V
$V_{X,Y\ High}$	Control input HIGH level		1.7	2.4	7	V
$I_{X,Y\ High}$	Control input HIGH current	$V_{IN} = 5\text{V}$			20	μA
$V_{X,Y\ Low}$	Control input LOW level		0.3		0.8	V
$I_{X,Y\ Low}$	Control input LOW current	$V_{IN} = 0.4\text{V}$	-20		20	μA
$V_{EN\ Low}$	Enable input LOW level		-0.3		1.5	V
$V_{EN\ High}$	Enable input HIGH level		2.4		7	V
$I_{EN\ Low}$	Enable input LOW current	$V_{EN} = 0\text{V}$		-20	-40	μA
$I_{EN\ High}$	Enable input HIGH current	$V_{EN} = 5\text{V}$		1		μA
$V_{HX,Y,EN}$	Control and enable inputs hysteresis			150		mV
$\frac{dV_{out}}{dt}$	Output voltage slope	$C_{1,2} = 10\text{nF}$		6		V/ms
$ I_{OST} $	Starting output current	$V_{IN} = 5\text{V}$ $V_S = 12\text{V}$			1	A
I_S	Quiescent supply current	$V_{IN} = 0$		3	5	mA
I_S	Supply current	$V_{IN} = 5\text{V}$		8	15	mA



TDA8116

TYPICAL WAVEFORMS





CURRENT MODE PWM CONTROLLER

- FEW EXTERNAL COMPONENTS
- FIXED FREQUENCY OPERATION
- HIGH CURRENT TOTEM POLE OUTPUT
- INTERNALLY TRIMMED BAND GAP REFERENCE
- DOUBLE PULSE SUPPRESSION
- PULSE-BY-PULSE CURRENT LIMITING
- LOW START UP CURRENT ($< 1\text{mA}$)
- UNDER VOLTAGE LOCKOUT
- ANTIMAGNETIZATION CIRCUIT
- EXTERNAL DUTY-CYCLE LIMITATION

Designed primarily for TV/Monitor applications, the TDA8130 control IC provides the necessary

features to implement off line, fixed frequency current mode control schemes with a minimal external parts count.

The advantages for this technique can be measured in improved line regulation, enhanced load regulation and a simpler control loop.

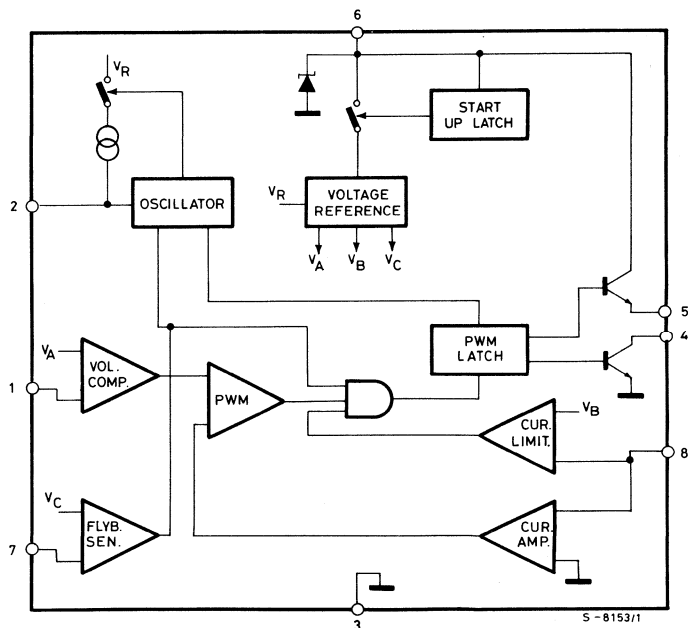
Protection circuitry includes built-in under voltage lockout, pulse-by-pulse current limiting and an antimagnetization circuit.



Plastic Minidip

ORDERING NUMBER: TDA8130

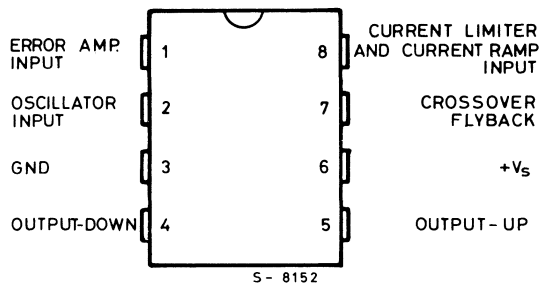
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	10	V
I_o	Source output current	500	mA
I_{os}	Sink output current	1	A
V_i	Analog inputs	-0.3 to V_s	V_s
P_{tot}	Power dissipation at $T_{amb} \leq 50^{\circ}C$	1	W
T_{stg}	Storage temperature range	-40 to 150	$^{\circ}C$
T_j	Junction temperature range	0 to 150	$^{\circ}C$
T_{amb}	Ambient temperature range	0 to 70	$^{\circ}C$

CONNECTION DIAGRAM (top view)



THERMAL DATA

$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	100	$^{\circ}C/W$
-----------------	-------------------------------------	-----	-----	---------------

**ELECTRICAL CHARACTERISTICS** ($V_S = 8V$, $T_{amb} = 25^{\circ}C$)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S Operating supply voltage	After start-up		8		V
I_S Supply current (without load)	$V_S = 8V$ after start-up		20		mA
V_{st} Start-up threshold			8.4		V
V_{so} Switch-off threshold			5.6		V
I_{sl} Supply current before start-up				1	mA
V_r Internal supply voltage			3.2		V
V_a Reference voltage			1.2		V
V_b Current limiter threshold			0.75		V
V_c Flyback sense threshold			0.4		V
f_o Oscillator free running frequency	with $C = 3.3nF$ $R = 3.3K\Omega$		40		kHz
f_m Maximum oscillator free running frequency		100			kHz
V_{oh} Source saturation voltage	$I_o = 100mA$			0.8	V
V_{ol} Sink saturation voltage	$I_o = 0.5A$			1	V

Fig. 1 - Oscillator frequency (f_o) vs. capacitor value (C_o)

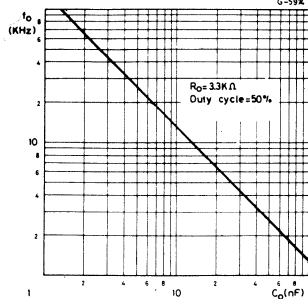


Fig. 2 - Duty-cycle vs. oscillator resistance (R_o)

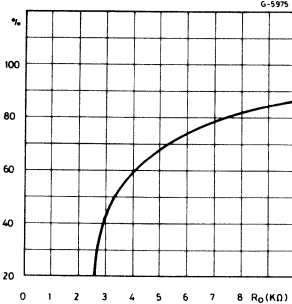


Fig. 3 - Application circuit for 117V off-line regulator using Darlington BU810

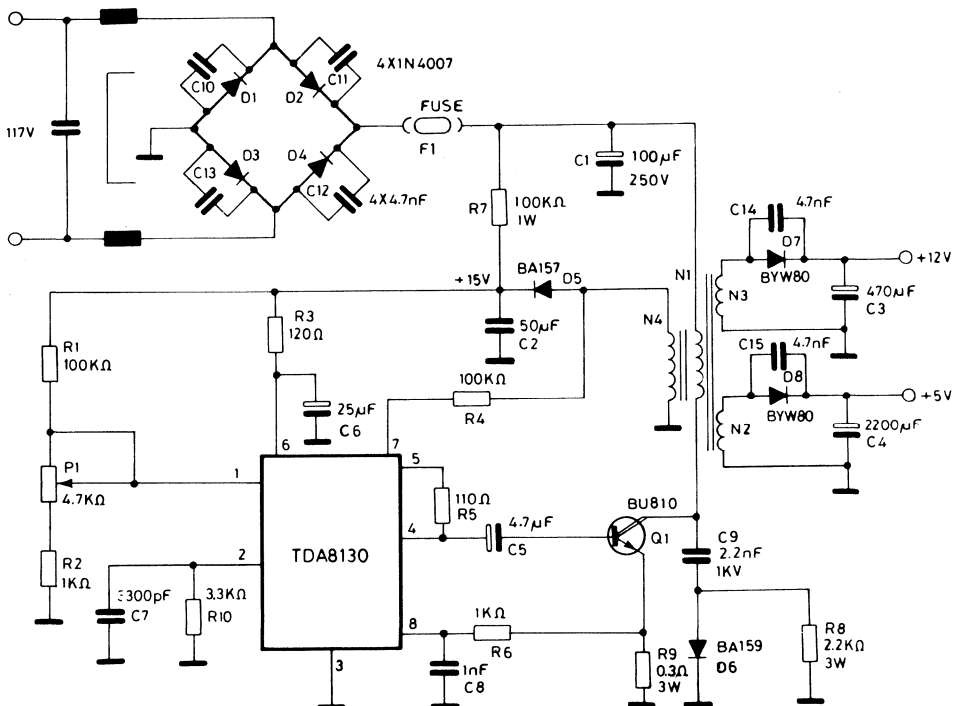


Fig. 4 - Printed circuit and component layout of the circuit of fig. 3 (1 : 1 scale)

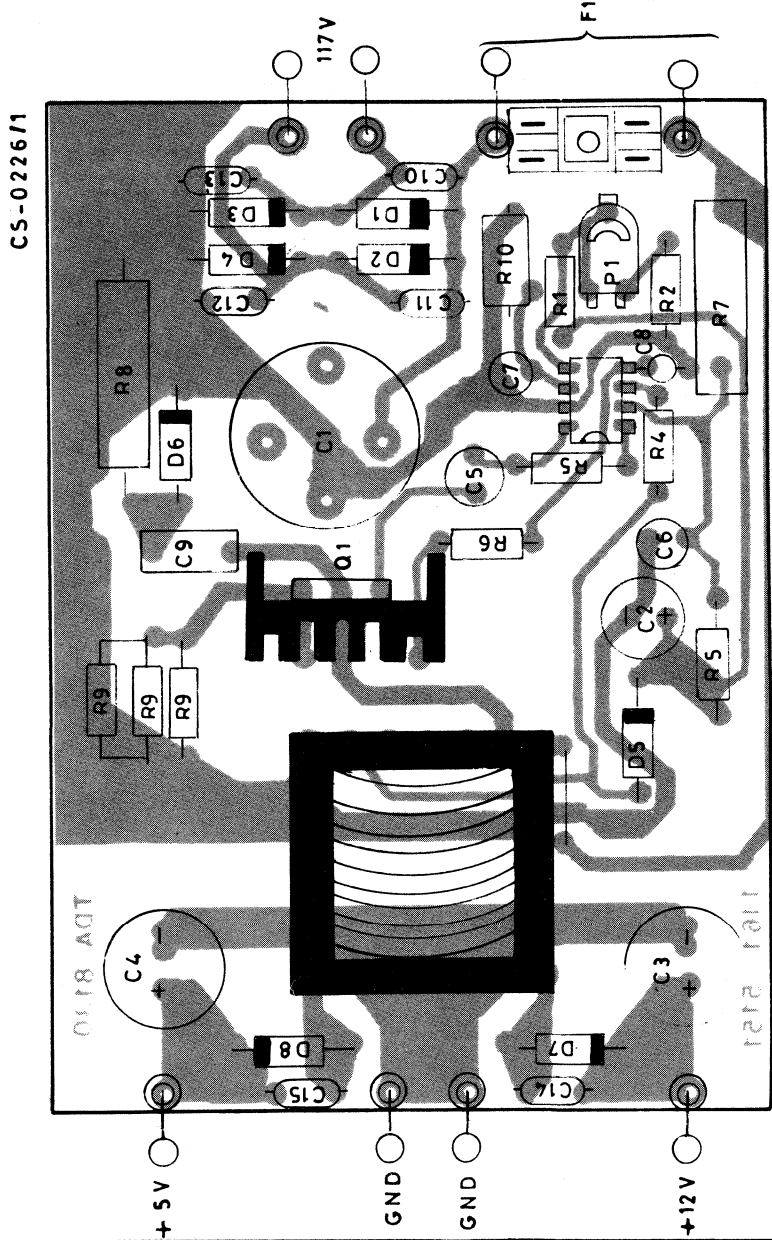


Fig. 5 - Application circuit for 220V off-line regulator using high voltage transistor BU426A

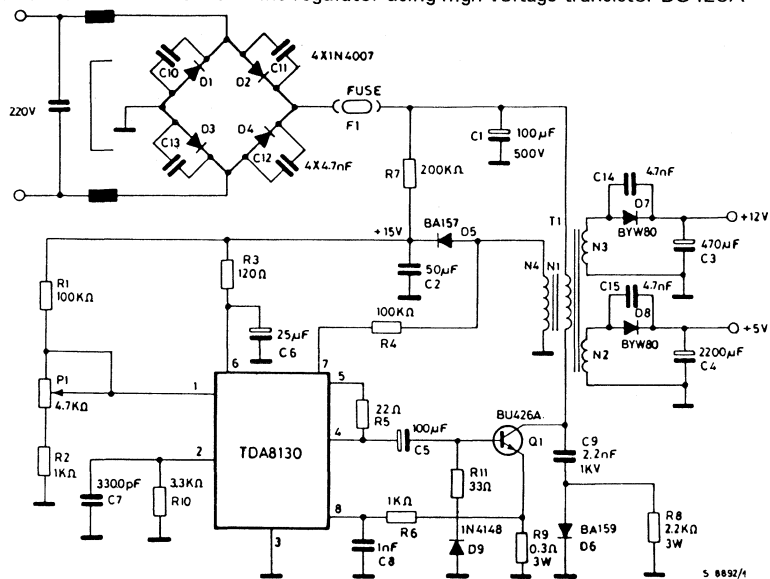


Fig. 6 - Output voltages vs. 5V output current (I_{O5})

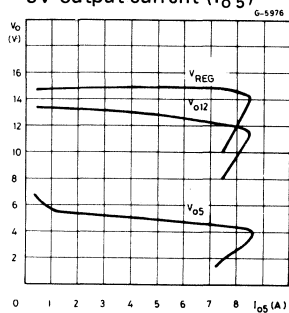
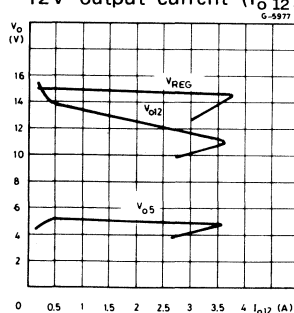


Fig. 7 - Output voltages vs. 12V output current (I_{O12})





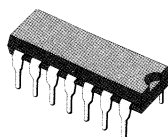
TDA8132

ADVANCE DATA

CURRENT MODE PWM CONTROLLER

- FIXED FREQUENCY OPERATION
- HIGH CURRENT TOTEM POLE OUTPUT
- INTERNALLY TRIMMED BAND GAP REFERENCE
- DOUBLE PULSE SUPPRESSION
- PULSE-BY-PULSE CURRENT LIMITING
- LOW START UP CURRENT ($< 1\text{mA}$)
- UNDER VOLTAGE LOCKOUT
- ANTIMAGNETIZATION CIRCUIT
- EXTERNAL DUTY CYCLE LIMITATION
- RAMP GENERATOR WITH SYNCHRONIZATION FACILITY
- ENABLE INPUT
- OVER AND UNDER VOLTAGE DETECTORS
- OVERLOAD IDENTIFICATION

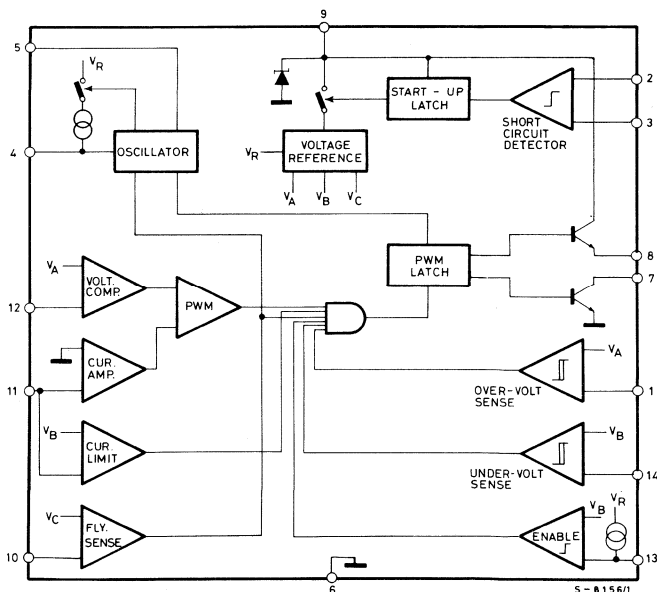
Designed primarily for TV/Monitor applications, the TDA8132 control IC provides the necessary features to implement off line, fixed frequency current mode control schemes with a minimal external parts count. The advantages of this technique can be measured in improved line regulation, enhanced load regulation and a simpler control loop. Protection circuitry includes built-in under voltage, lockout, phase-by-pulse current limiting and an antimagnetization circuit.



DIP-14 Plastic

ORDERING NUMBER: TDA8132

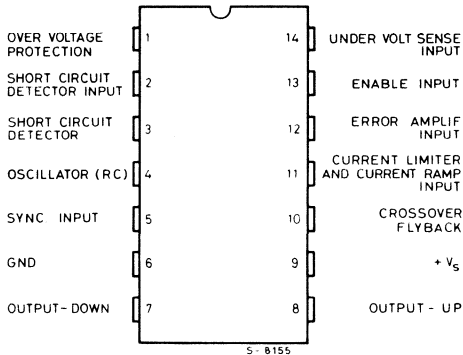
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	10	V
I_o	Source output current	500	mA
I_{os}	Sink output current	1	A
V_i	Analog inputs	-0.3 to V_s	
P_{tot}	Power dissipation at $T_{amb} \leq 50^{\circ}C$	1	W
T_{stg}	Storage temperature range	-40 to 150	$^{\circ}C$
T_j	Junction temperature range	0 to 150	$^{\circ}C$
T_{amb}	Ambient temperature range	0 to 70	$^{\circ}C$

CONNECTION DIAGRAM (top view)



THERMAL DATA

$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	100	$^{\circ}C/W$
-----------------	-------------------------------------	-----	-----	---------------

ELECTRICAL CHARACTERISTICS ($V_S = 8V$, $T_{amb} = 25^\circ C$)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S Operating supply voltage	After start-up		8		V
I_S Supply current (without load)	$V_S = 8V$ after start-up		20		mA
V_{st} Start-up threshold			8.4		V
V_{so} Switch-off threshold			5.6		V
I_{sl} Supply current before start-up				1	mA
V_r Internal supply voltage			3.2		V
V_a Reference voltage			1.2		V
V_b Current limiter threshold			0.75		V
V_c Flyback sense threshold			0.4		V
f_o Oscillator free running frequency	with $C = 3.3nF$ $R = 3.3K\Omega$		40		kHz
f_m Maximum oscillator free running frequency		100			kHz
V_{oh} Source saturation voltage	$I_o = 100mA$			0.8	V
V_{ol} Sink saturation voltage	$I_o = 0.5A$			1.5	V
I_{sync} Synchronous input current (positive going)		100			μA
V_{ov} Over-voltage threshold			1.2		V
V_{uv} Under-voltage threshold			0.75		V
V_e Enable threshold			0.5		V



TDA8132

Fig. 1 - Oscillator frequency (f_o) vs. capacitor value (C_o)

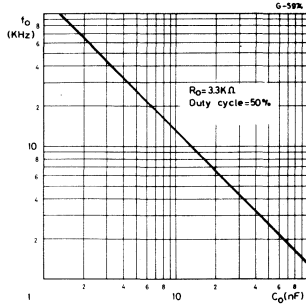


Fig. 2 - Duty-cycle vs. oscillator resistance (R_o)

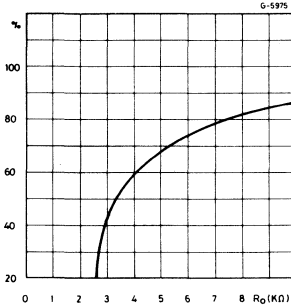


Fig. 3 - Application circuit for 220V off-line regulator using high voltage transistor BU426A

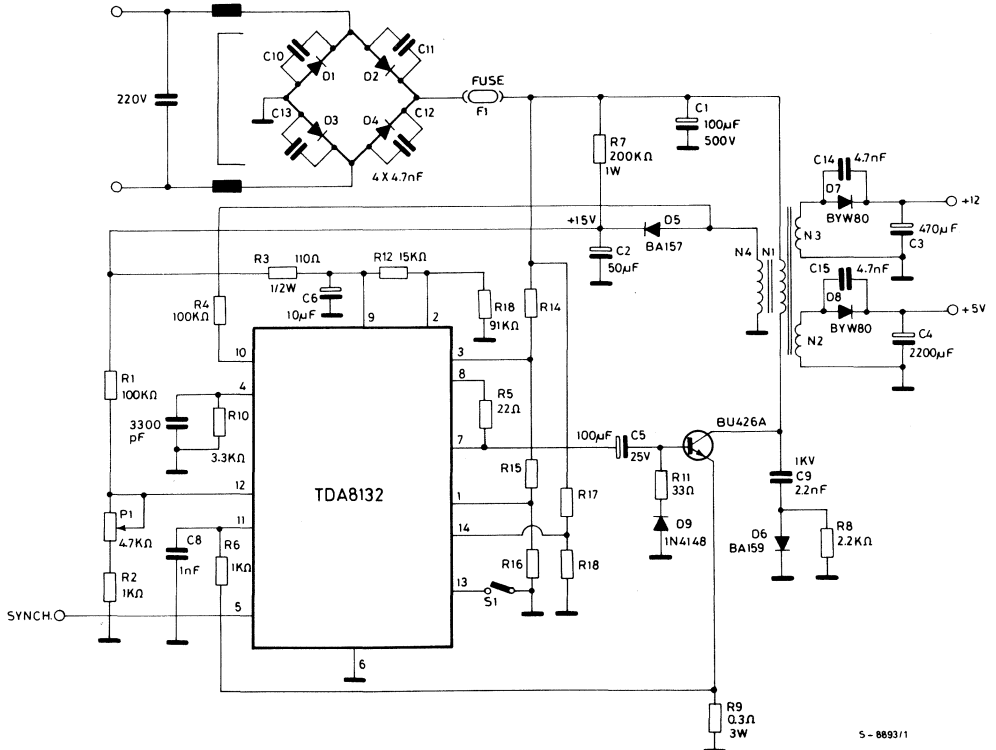


Fig.4 - Output voltages vs.
5V output current (I_{O5})

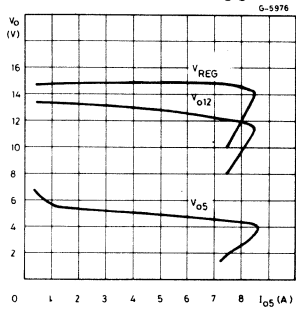
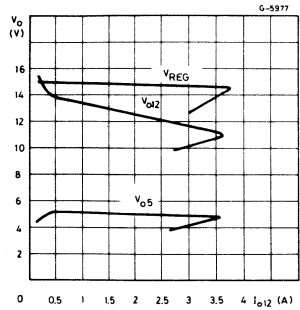


Fig.5 - Output voltages vs.
12V output current (I_{O12})



SUPPLY VOLTAGE SUPERVISORS

- POWER-ON RESET GENERATOR
- AUTOMATIC RESET GENERATION AFTER VOLTAGE DROP
- WIDE SUPPLY VOLTAGE RANGE . . . 3V TO 18V
- PRECISION VOLTAGE SENSOR
- TEMPERATURE-COMPENSATED VOLTAGE REFERENCE
- TRUE AND COMPLEMENT RESET OUTPUTS
- EXTERNALLY ADJUSTABLE PULSE WIDTH

The TL7700A series are monolithic integrated circuit supply voltage supervisors specifically designed for use as reset controllers in microcomputer and microprocessor systems. During power-up the device tests the supply voltage and keeps the RESET and RESET outputs active (high and low, respectively) as long as the supply voltage has not reached its nominal voltage value. Taking $\overline{\text{RESIN}}$ low has the same effect. To ensure that the microcomputer system has reset, the TL7700A then initiates an internal time

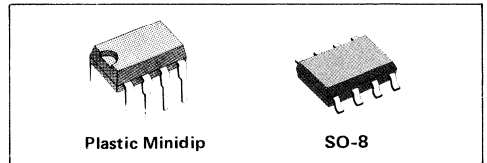
delay that delays the return of the reset outputs to their inactive states. Since the time delay for most microcomputers and microprocessors is in the order of several machine cycles, the device internal time delay is determined by an external time delay is determined by an external capacitor connected to the C_T input (pin 3).

$$t_d = 1.3 \times 10^4 \times C_T$$

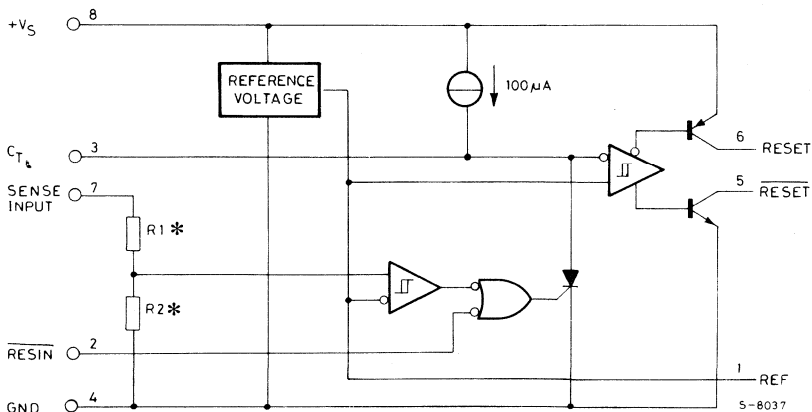
Where: C_T is in farads (F) and t_d is in seconds(s)

In addition, when the supply voltage drops below the nominal value, the outputs will be active until the supply voltage returns to the nominal value. An external capacitor (typically 0.1 μ F) must be connected to the REF output (pin 1) to reduce the influence of fast transients in the supply voltage.

The TL7700AI series is characterized for operation from -25°C to 85°C; the TL7700AC series is characterized from 0°C to 70°C.



BLOCK DIAGRAM



* TL7702A R1 = 0 Ω , R2 = open; TL7705A R1 = 7.8K Ω , R2 = 10K Ω ; TL7709A R1 = 19.7K Ω , R2 = 10K Ω ; TL7712A R1 = 32.7K Ω , R2 = 10K Ω ; TL7715A R1 = 43.4K Ω , R2 = 10K Ω

ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage, V_{CC} (see Note 1)	20	V
V_i	Input voltage range at $\overline{\text{RESIN}}$	-0.3 to 20	V
V_i	Input voltage at SENSE: TL7702A (see Note 2)	-0.3 to 6	V
	TL7705A	-0.3 to 10	V
	TL7709A	-0.3 to 15	V
	TL7712A	-0.3 to 20	V
	TL7715A	-0.3 to 20	V
I_{OH}	High-level output current at $\overline{\text{RESET}}$	-30	mA
I_{OL}	Low-level output current at $\overline{\text{RESET}}$	30	mA
T_{amb}	Operating free-air temperature range: TL77XXAI	-40 to 85	$^{\circ}\text{C}$
	TL77XXAC	0 to 70	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-65 to 150	$^{\circ}\text{C}$

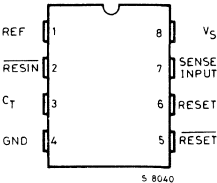
Notes: 1. All voltage values are with respect to the network ground terminal
2. For the TL7702A, the voltage applied to the SENSE terminal must never exceed V_S

RECOMMENDED OPERATING CONDITIONS

Parameters			Min.	Max.	Unit
V _S	Supply voltage		3.6	18	V
V _{IH}	High-level input voltage at RESIN		2		V
V _{IL}	Low-level input voltage at RESIN			0.6	V
V _i	Voltage at sense input	TL7702A	0	See Note 3	V
		TL7705A	0	10	
		TL7709A	0	15	
		TL7712A	0	20	
		TL7715A	0	20	
I _{OH}	High-level output current at RESET			-16	mA
I _{OL}	Low-level output current at $\overline{\text{RESET}}$			16	mA
T _{amb}	Operating free-air temperature range	TL77 - AI	-40	85	°C
		TL77 - AC	0	70	

Note 3: For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed $V_S - 1\text{V}$ or 6V, whichever is less

CONNECTION DIAGRAM AND ORDERING NUMBER



Temperature range	Plastic Minidip	SO-8
Commercial 0 to 70 $^{\circ}\text{C}$	TL77XXACP	TL77XXACD
Industrial -40 to 85 $^{\circ}\text{C}$	TL77XXAIP	TL77XXAID



THERMAL DATA

$R_{th\ j-amb}$	Thermal resistance junction-ambient	max.	120	°C/W
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ELECTRICAL CHARACTERISTICS These specifications unless otherwise specified, apply for:
 $T_{amb} = -40$ to 85°C (TL77XXAI); $T_{amb} = 0$ to 70°C (TL77XXAC)

Parameter		Test Conditions (1)	Min.	Typ.	Max.	Unit
V_{OH}	High-level output voltage at RESET	$I_{OH} = -16\text{mA}$	$V_S - 1.5$			V
V_{OL}	Low-level output voltage at RESET	$I_{OL} = 16\text{mA}$			0.4	V
V_{ref}	Reference voltage	$T_{amb} = 25^{\circ}\text{C}$	2.48	2.53	2.58	V
V_T	Threshold Voltage at SENSE input	TL7702A	2.48	2.53	2.58	V
		TL7705A	4.5	4.55	4.6	
		TL7709A	7.5	7.6	7.7	
		TL7712A	10.6	10.8	11.0	
		TL7715A	13.2	13.5	13.8	
V_T	Threshold voltage at SENSE input	TL7702A	2.45	2.53	2.58	V
		TL7705A	4.45	4.55	4.6	
		TL7709A	7.4	7.6	7.7	
		TL7712A	10.4	10.8	11.0	
		TL7715A	13.0	13.5	13.8	
V_{T+}, V_{T-}	Hysteresis (2) at SENSE input	TL7702A		10		mV
		TL7705A		15		
		TL7709A		20		
		TL7712A		35		
		TL7715A		45		
I_I	Input current at RESET input	$V_I = 2.4\text{V to } V_S$			20	μA
		$V_I = 0.4\text{V}$			-100	
I_I	Input current at SENSE input	TL7702A	$V_{ref} < V_I < V_S - 1.5\text{V}$	0.5	2	
I_{OH}	High-level output current at RESET	$V_O = 18\text{V}$			50	
I_{OL}	Low-level output current at RESET	$V_O = 0\text{V}$			-50	
I_S	Supply current	All inputs and out. open		1.8	3	mA

- All characteristics are measured with $C = 0.1\mu\text{F}$ from Pin 1 to GND, and with $C = 0.1\mu\text{F}$ from Pin 3 to GND
- Hysteresis is the difference between the positive going input threshold voltage, V_{T+} , and the negative going input threshold voltage, V_{T-} .

SWITCHING CHARACTERISTICS

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{pi}	Pulse width at SENSE input	$V_{ih} = V_{i typ} + 0.04 \times V_i$ $V_{il} = V_{i typ} - 0.04 \times V_i$	0.9		μs
t_{pi}	Pulse width at RESIN input	0.4			μs
t_{po}	Pulse width at output	$C_f = 0.1 \mu F$	0.65	1.3	ms
$t_{pd HL}$	Propagation delay time from $\overline{RESIN}$ to $\overline{RESET}$	$C_L = 100 pF$ $V_S = 5V$ $R_L = 4.7 K\Omega$		1	μs
$t_{r/f}$	Rise/Falltime at RESET and $\overline{RESET}$	$C_L = 10 pF$ $V_S = 5V$ $R_L = 4.7 K\Omega$		1	μs

Fig. 1 - Multiple power supply system reset generation

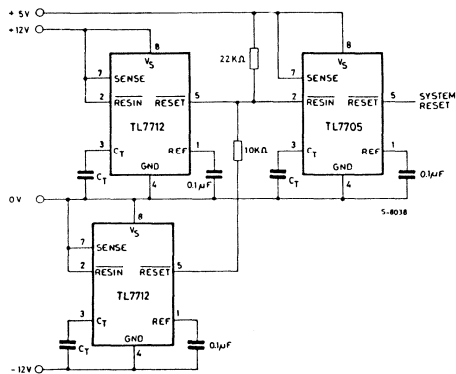
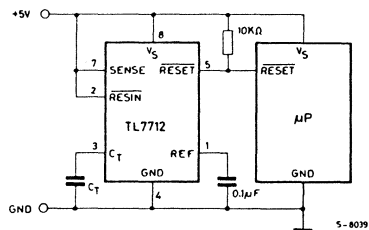
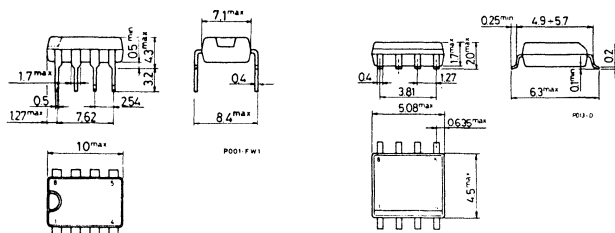


Fig. 2 - Reset controller for μP



MECHANICAL DATA (Dimensions in mm)





UC1840
UC2840
UC3840

PRELIMINARY DATA

PROGRAMMABLE, OFF-LINE, PWM CONTROLLER

- ALL CONTROL, DRIVING, MONITORING, AND PROTECTION FUNCTIONS INCLUDED
- LOW-CURRENT, OFF-LINE START CIRCUIT
- FEED-FORWARD LINE REGULATION OVER 4 TO 1 INPUT RANGE
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- PULSE-BY-PULSE CURRENT LIMITING PLUS SHUTDOWN FOR OVER-CURRENT FAULT
- NO START-UP OR SHUTDOWN TRANSIENTS
- SLOW TURN-ON AND MAXIMUM DUTY-CYCLE CLAMP
- SHUTDOWN UPON OVER- OR UNDER-VOLTAGE SENSING
- LATCH OFF OR CONTINUOUS RETRY AFTER FAULT
- REMOTE, PULSE-COMMANDABLE START/STOP
- PWM OUTPUT SWITCH USABLE TO 1A PEAK CURRENT
- 1% REFERENCE ACCURACY
- 500 kHz OPERATION

Although containing most of the features required by all types of switching power supply controllers, the UC1840 family has been optimized for highly-efficient boot-strapped primary-side operation in forward or flyback power converters. Two important features for this mode are a starting circuit which requires little current from the primary input voltage and feed-forward control for constant volt-second operation over

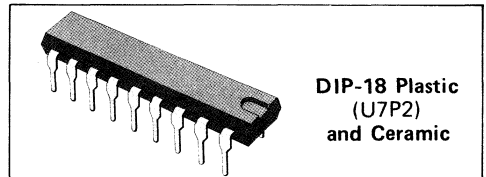
a wide input voltage range.

In addition to startup and normal regulating PWM functions, these devices offer built-in protection from over-voltage, under-voltage, and over-current fault conditions. This monitoring circuitry contains the added features that any fault will initiate a complete shutdown with provisions for either latch off or automatic restart. In the latch-off mode, the controller may be started and stopped with external pulsed or steady-state commands.

Other performance features of these devices include a 1% accurate reference, provision for slow-turn-on and duty-cycle limiting, and high-speed pulse-by-pulse current limiting in addition to current fault shutdown.

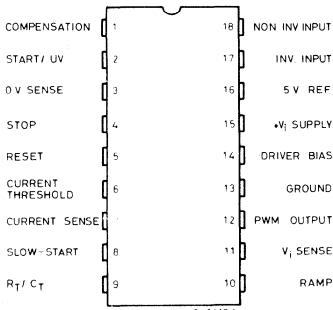
The UC1840's PWM output stage includes a latch to insure only a single pulse per period and is designed to optimize the turn off of an external switching device by conducting during the "OFF" time with a capability for both high peak current and low saturation voltage. These devices are available in an 18-pin dual-in-line plastic or ceramic package.

The UC1840 is characterized for operation over the full military temperature range of -55°C to +125°C. The UC2840 and UC3840 are designed for operation from -25°C to +85°C and 0°C to +70°C, respectively.



CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)



Type	Plastic	Ceramic
UC1840	—	UC1840J
UC2840	UC2840N	UC2840J
UC3840	UC3840N	UC3840J

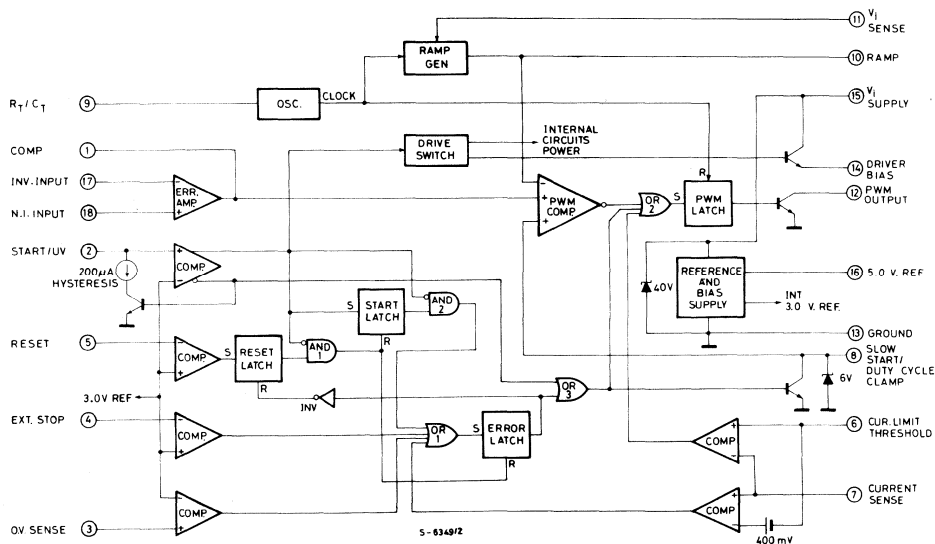


UC1840
UC2840
UC3840

ABSOLUTE MAXIMUM RATINGS

V_i	Supply voltage + V_i (pin 15)		
	Voltage driven	32	V
	Current driven 100 mA maximum	self limiting	
V_o	PWM output voltage (pin 12)	40	V
I_o	PWM output current, steady-state (pin 12)	400	mA
E_{op}	PWM output peak energy discharge	20	μ J
	Driver bias current (pin 14)	-200	mA
$I_{o(REF)}$	Reference output current (pin 16)	-50	mA
	Slow start sink current (pin 8)	20	mA
	V_i sense current (pin 11)	10	mA
	Current limit inputs (pin 6, 7)	-0.5 to +5.5	V
	Comparator inputs (pins 2, 3, 4, 5, 17, 18)	-0.3 to +32	V
P_{tot}	Power dissipation at $T_{amb} = 70^\circ\text{C}$	1000	mW
T_j	Junction temperature range	-55 to 150	$^\circ\text{C}$
T_{op}	Operating ambient temperature range: UC1840	-55 to 125	$^\circ\text{C}$
	UC2840	-25 to 85	$^\circ\text{C}$
	UC3840	0 to 70	$^\circ\text{C}$
T_{stg}	Storage temperature	-65 to + 150	$^\circ\text{C}$

BLOCK DIAGRAM





UC1840
UC2840
UC3840

THERMAL DATA

$R_{th\ j-amb}$ Thermal resistance junction-ambient	max 80 °C/W
---	-------------

FUNCTIONAL DESCRIPTION

Name	Function
------	----------

PWM CONTROL

OSCILLATOR	Generates a fixed-frequency internal clock from an external R_T and C_T . $\text{Frequency} = \frac{K_c}{R_T C_T}$ where K_c is a first-order correction factor $\approx 0.3 \log (C_T \times 10^{12})$.
RAMP GENERATOR	Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R} \cdot C_R$ is normally selected $\leq C_T$ and its value will have some effect upon valley voltage. C_R terminal can be used as an input port for current mode control.
ERROR AMPLIFIER	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance: unity-gain stable.
REFERENCE GENERATOR	Precision 5.0V for internal and external usage to 50 mA. Tracking 3.0V reference for internal usage only with nominal accuracy of $\pm 2\%$. 40V clamp zener for chip O.V. protection, 100mA maximum current.
PWM COMPARATOR	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
PWM LATCH	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets with each internal clock pulse.
PWM OUTPUT SWITCH	Transistor capable of sinking current to ground which is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400mA saturated with peak capacitance discharge in excess of one amp.



UC1840
UC2840
UC3840

FUNCTIONAL DESCRIPTION (continued)

Name	Function
------	----------

SEQUENCING FUNCTIONS

START/U.V. SENSE

This comparator performs three functions.
With an increasing voltage, it generates a turn-on signal at a start threshold.
With a decreasing voltage, it generates a U.V. fault signal at a lower level separated by a 200 μ A hysteresis current.
At the U.V. threshold, it also resets the Error Latch if the Reset Latch has been set.

DRIVE SWITCH

Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.

DRIVE BIAS

Supplies drive current to external power switch to provide turn-on bias.

SLOW START

Clamps low to hold PWM OFF. Upon release, rises with rate controlled by $R_S C_S$ for slow increase of output pulse width.
Also used to clamp maximum duty cycle with divider $R_S R_{DC}$.

START LATCH

Keeps low input voltage at initial turn-on from being defined as a U.V. fault. Sets at start level to monitor for U.V. fault.

RESET LATCH

When reset, this latch insures no reset signal to either Start or Error latches so that first fault will lock the PWM off.
When set, this latch resets the Start and Error latches at the U.V. low threshold, allowing a restart.

PROTECTION FUNCTIONS

ERROR LATCH

When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset.
Inputs to Error Latch are:
a. U.V. low (after turn-on)
b. O.V. high
c. Step low
d. Current Sense 400mV over threshold.
Error Latch resets at U.V. threshold if Reset Latch is set.

CURRENT LIMITING

Differential input comparator terminates individual output pulses each time sense voltage rises above threshold.
When sense voltage rises to 400 mV above threshold, a shutdown signal is sent to Error Latch.



UC1840
UC2840
UC3840

ELECTRICAL CHARACTERISTICS (Refer to the test circuit. Unless otherwise stated, these specifications apply for $T_i = -55$ to $+125^\circ\text{C}$ for the UC1840, -25°C to $+85^\circ\text{C}$ for the UC2840 and 0 to 70°C for the UC3840; $V_i = 20\text{V}$, $R_T = 20\text{K}\Omega$, $C_T = 0.001\ \mu\text{F}$, $C_R = 0.001\ \mu\text{F}$, current limit threshold = 200mV)

Parameter	Test conditions	UC1840 UC2840			UC3840			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	

POWER INPUTS

I_{ST}	Start-up current	$V_i = 30\text{V}$, Pin 2= 2.5V , $T_j = 25^\circ\text{C}$		4	5.5		4	5.5	mA
	*Start-up current T.C.	$V_i = 30\text{V}$, Pin 2= 2.5V		-0.1	-0.2		-0.1	-0.2	$\%/^\circ\text{C}$
I_i	Operating current	$V_i = 30\text{V}$, Pin 2= 3.5V	5	10	15	5	10	15	mA
V_{SOV}	Supply O.V. clamp	$I_i = 20\text{mA}$	33	40	45	33	40	48	V

REFERENCE SECTION

V_{REF}	Reference voltage	$T_j = 25^\circ\text{C}$	4.95	5	5.05	4.9	5	5.1	V
ΔV_{REF}	Line regulation	$V_i = 8$ to 30V		10	15		10	20	mV
ΔV_{REF}	Load regulation	$I_L = 0$ to 20mA		10	20		10	30	mV
$\Delta V_{REF}/\Delta T$	* Temperat. coeff.	Over op. temp. range			± 0.4			± 0.4	$\text{mV}/^\circ\text{C}$
I_{SC}	Short circuit curr.	$V_{REF} = 0$, $T_j = 25^\circ\text{C}$		-80	-100		-80	-100	mA

OSCILLATOR

f_s	Nominal frequency	$T_j = 25^\circ\text{C}$	47	50	53	45	50	55	KHz
	Voltage stability	$V_i = 8$ to 30V		0.5	1		0.5	1	%
	* Temperature coeff.	Over op. temp. range			± 0.8			± 0.8	$\%/^\circ\text{C}$
$f_{s(\text{max})}$	Maxim. frequency	$R_T = 2\text{K}\Omega$, $C_T = 330\text{pF}$	500			500			KHz

RAMP GENERATOR

	Ramp current min.	$I_{SENSE} = -10\ \mu\text{A}$		-11	-14		-11	-14	μA
	Ramp current max.	$I_{SENSE} = 1\text{mA}$	-0.9	-0.95		-0.9	-0.95		mA
	Ramp valley		0.3	0.5	0.7	0.3	0.5	0.7	V
	Ramp peak	Clamping level	3.9	4.2	4.5	3.9	4.2	4.5	V

ERROR AMPLIFIER

V_{os}	Input offset voltage	$V_{CM} = 5\text{V}$		0.5	5		2	10	mV
I_b	Input bias current			0.5	2		1	5	μA
I_{os}	Input offset current				0.5			0.5	μA
G_v	Open loop gain	$\Delta V_o = 1$ to 3V	60	66		60	66		dB
	Output swing (max Out $\leq$ Ramp peak -100mV)	Minimum total range	0.3		3.5	0.3		3.5	V
CMR	Common mode rejection	$V_{CM} = 1.5$ to 5.5V	70	80		70	80		dB
SVR	Supply voltage rejection	$V_i = 8$ to 30V	40	50		40	50		dB



UC1840
UC2840
UC3840

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	UC1840 UC2840			UC3840			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{SC}	Short circuit curr.	$V_{comp} = 0V$		-4	-10			mA
B^*	Gain bandwidth	$T_J = 25^\circ C, G_V = 0 \text{ dB}$		1	2			MHz
SR^*	Slew rate	$T_J = 25^\circ C, G_V = 0 \text{ dB}$		0.8		0.8		V/ μs

PWM SECTION

	* Continuous duty cycle range (other than zero)	Min. total cont. range Ramp peak < 4.2V	5		95	5		95	%
$V_{O(sat)}$	Output saturation	$I_O = 20 \text{ mA}$		0.2	0.4		0.2	0.4	V
$V_{O(sat)}$	Output saturation	$I_O = 200 \text{ mA}$		1.7	2.2		1.7	2.2	V
I_{OL}	Output leakage	$V_O = 40V$		0.1	10		0.1	10	μA
τ_d	* Comparator delay	Pin 8 to pin 12 $T_J = 25^\circ C, R_L = 1 \text{ K}\Omega$		300	500		300	500	ns

SEQUENCING FUNCTIONS

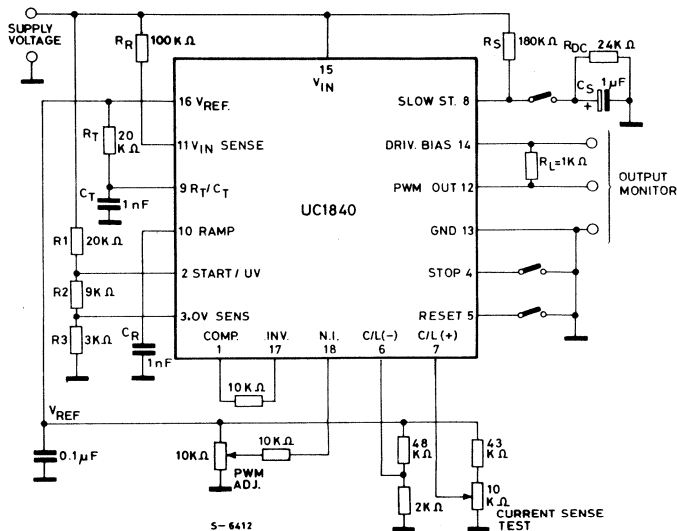
V_T	Comparator threshold	Pins 2, 3, 4, 5	2.8	3	3.2	2.8	3	3.2	V
I_b	Input bias current	Pins 3, 4, 5 = 0V		-1	-3		-1	-3	μA
	Start/UV Hysteresis current	Pin 2 = 2.5V, $T_J = 25^\circ C$	180	200	220	170	200	230	μA
	Input leakage	$V_I = 20V$		0.1	10		0.1	10	μA
	Driver bias saturation voltage $V_{IN-V_{OH}}$	$I_B = -50 \text{ mA}$		2	3		2	3	V
	Driver bias leakage	$V_B = 0V$		-0.1	-10		-0.1	-10	μA
	Slow-start saturat.	$I_s = 2 \text{ mA}$		0.2	0.5		0.2	0.5	V
	Slow-start leakage	$V_s = 4.5V$		0.1	2		0.1	2	μA

CURRENT CONTROL

	Current limit offset			0	5		0	10	mV
	Current shutdown offset		370	400	430	360	400	440	mV
I_b	Input bias current	Pin 7 = 0V		-2	-5		-2	-5	μA
	* Common mode range		-0.4		3	-0.4		3	V
τ_d^*	Current limit delay	$T_J = 25^\circ C, \text{ Pin 7 to 12, } R_L = 1 \text{ K}\Omega$		200	400		200	400	ns

* Guaranteed by design. Not 100% tested in production.

Fig. 1 – Open loop test circuit



$$\text{Nominal frequency} = \frac{1}{R_T C_T} = 50 \text{ kHz}$$

$$\text{Start voltage} = 3 \left(\frac{R_1 + R_2 + R_3}{R_2 + R_3} \right) + 0.2 R_1 = 12V$$

$$\text{U.V. fault voltage} = 3 \left(\frac{R_1 + R_2 + R_3}{R_2 + R_3} \right) = 8V$$

$$\text{O.V. fault voltage} = 3 \left(\frac{R_1 + R_2 + R_3}{R_3} \right) = 32V$$

Current limit = 200 mV
Current fault voltage = 600 mV
Duty cycle clamp = 50%

Fig. 2 - Start U.V. hysteresis current

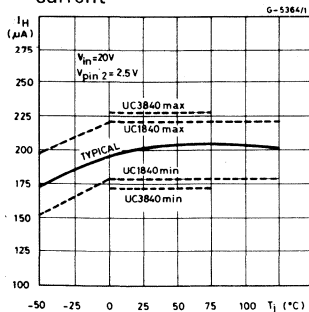


Fig. 3 - PWM Output saturation voltage

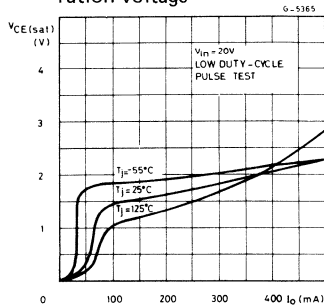


Fig. 4 – Oscillator frequency

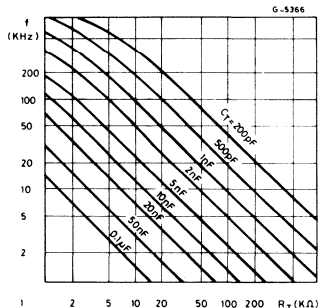


Fig. 5 - PWM output minimum pulse width

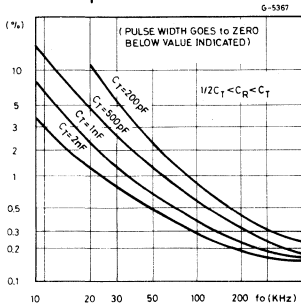


Fig. 6 - Error amplifier open-loop gain and phase

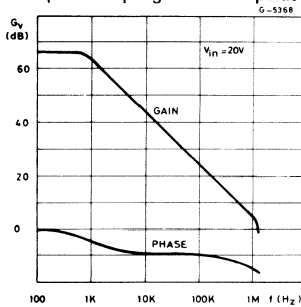
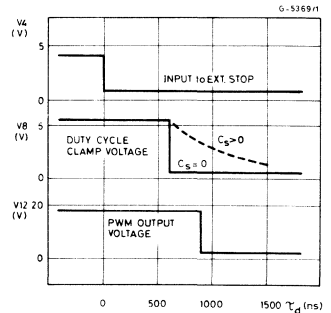
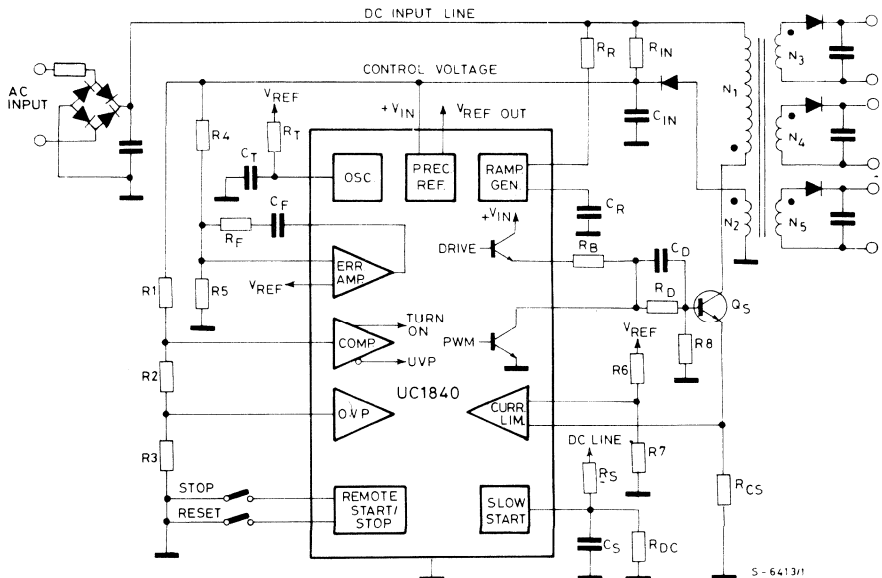


Fig. 7 - Shutdown timing



APPLICATION INFORMATION

Fig. 8 - Programmable PWM controller in a simplified flyback regulator



APPLICATION INFORMATION (continued)

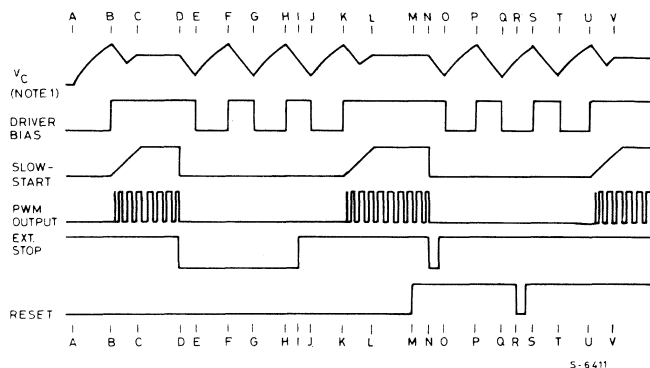
In this application (see Fig. 8) complete control is maintained on the primary side. Control power is provided by R_{IN} and C_{IN} during start-up, and by a primary-referenced low voltage winding, N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling — a task made even easier with the UC1840's feed-forward line

regulation.

The UC1840 will readily accept digital start/stop commands transmitted from the secondary side by means of optical couplers.

Not shown are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Q_s , or the application.

Fig. 9 – Power sequencing functions

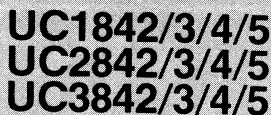


- Notes:**
1. V_c represents an analog of the output voltage generated by a primary-referenced secondary winding on the power transformer. It is the voltage monitored by the start/U.V. comparator and, in most cases, is the supply voltage, V_i , for the UC1840.
 2. Although input to External Stop, Pin 4, is shown, results are the same for any fault input which sets the Error Latch.

Power Frequency Functions

Time	Event
A	Initial turn-on, V_c rises with light load
B	Start threshold. Driver Bias loads V_c
C	Operating PWM regulates V_c
D	Stop input sets Error Latch turning off PWM
E	U.V. low threshold. Error Latch remain set
F	Start turns on Driver Bias bus Error Latch still set
G } H }	V_c and Driver Bias continue to cycle
I	Stop command removed
J	Error Latch reset at U.V. low threshold
K	Start threshold now removes slow-start clamp

Time	Event
L	Return to normal run state
M	Reset Latch set signal removed
N	Error Latch set with momentary fault
O	Error Latch does not reset as Reset Latch is reset
P } Q }	V_c and Driver Bias recycle with no turn-on
R	Reset Latch set is set with momentary Reset signal
S	V_c must complete cycle to turn-on
T	Start and Error Latches reset
U	Normal start initiated
V	Return to normal run state

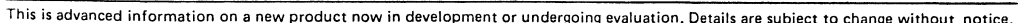
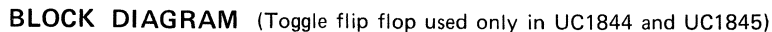


CURRENT MODE PWM CONTROLLER

- OPTIMIZED FOR OFF-LINE AND DC TO DC CONVERTERS
- LOW START-UP CURRENT ($< 1\text{mA}$)
- AUTOMATIC FEED FORWARD COMPENSATION
- PULSE-BY-PULSE CURRENT LIMITING
- ENHANCED LOAD RESPONSE CHARACTERISTICS
- UNDER-VOLTAGE LOCKOUT WITH HYSTeresis
- DOUBLE PULSE SUPPRESSION
- HIGH CURRENT TOTEM POLE OUTPUT
- INTERNALLY TRIMMED BANDGAP REFERENCE
- 500KHz OPERATION
- LOW R_O ERROR AMP

insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off-state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.5V and 7.9V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to $< 50\%$ is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.



ABSOLUTE MAXIMUM RATINGS *

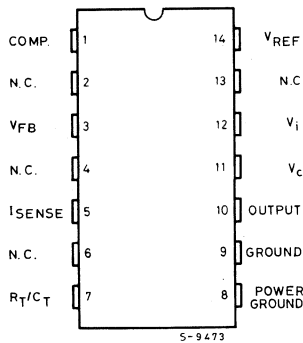
V_i	Supply voltage (Low impedance source)	30	V
V_i	Supply voltage ($I_i < 30\text{mA}$)	Self limiting	
I_o	Output current	± 1	A
E_o	Output energy (capacitive load)	5	μJ
	Analog inputs (Pins 2, 3)	-0.3 to 6.3	V
	Error amplifier output sink current	10	mA
P_{tot}	Power dissipation at $T_{\text{amb}} \leq 50^{\circ}\text{C}$ (Minidip, DIP-14)	1	W
P_{tot}	Power dissipation at $T_{\text{amb}} \leq 25^{\circ}\text{C}$ (SO-14)	725	mW
T_{stg}	Storage temperature range	-65 to 150	$^{\circ}\text{C}$
T_L	Lead temperature (Soldering 10s)	300	$^{\circ}\text{C}$

* All voltages are with respect to pin 5, all currents are positive into the specified terminal.

CONNECTION DIAGRAMS

(Top view)

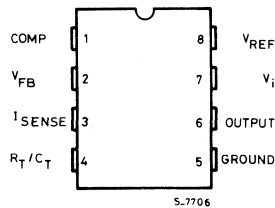
DIP-14 / SO-14



ORDERING NUMBERS

TYPE	PLASTIC MINIDIP	CERAMIC MINIDIP	DIP-14	SO-14
UC1842 UC1843 UC1844 UC1845		UC1842J UC1843J UC1844J UC1845J		
UC2842 UC2843 UC2844 UC2845	UC2842N UC2843N UC2844N UC2845N	UC2842J UC2843J UC2844J UC2845J	UC2842B UC2843B UC2844B UC2845B	UC2842D UC2843D UC2844D UC2845D
UC3842 UC3843 UC3844 UC3845	UC3842N UC3843N UC3844N UC3845N	UC3842J UC3843J UC3844J UC3845J	UC3842B UC3843B UC3844B UC3845B	UC3842D UC3843D UC3844D UC3845D

Minidip Plastic and Ceramic





UC1842/3/4/5
UC2842/3/4/5
UC3842/3/4/5

THERMAL DATA

		Ceramic Minidip	Plastic Minidip	DIP-14 Plastic	SO-14
$R_{th j-amb}$	Thermal resistance junction-ambient	200°C/W	100°C/W	100°C/W	165°C/W

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $-55 \leq T_{amb} \leq 125^\circ\text{C}$ for UC184X; $-25 \leq T_{amb} \leq 85^\circ\text{C}$ for UC284X; $0 \leq T_{amb} \leq 70^\circ\text{C}$ for UC384X; $V_i = 15\text{V}$ (Note 5); $R_T = 10\text{K}$; $C_T = 3.3\text{nF}$)

Parameter	Test Conditions	UC184X UC284X			UC384X			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	

REFERENCE SECTION

V_{REF}	Output voltage	$T_j = 25^\circ\text{C}$	$I_o = 1\text{mA}$	4.95	5.00	5.05	4.90	5.00	5.10	V
ΔV_{REF}	Line regulation	$12\text{V} < V_i < 25\text{V}$			6	20		6	20	mV
ΔV_{REF}	Load regulation	$1 \leq I_o \leq 20\text{mA}$			6	25		6	25	mV
$\Delta V_{REF}/\Delta T$	Temperature stability	(Note 2)			0.2	0.4		0.2	0.4	mV/°C
	Total output variation	Line, Load, Temperature (Note 2)		4.9		5.1	4.82		5.18	V
e_N	Output noise voltage	$10\text{Hz} < f < 10\text{KHz}$ $T_j = 25^\circ\text{C}$ (Note 2)			50			50		μV
	Long term stability	$T_{amb} = 125^\circ\text{C}$, 1000 Hrs (Note 2)			5	25		5	25	mV
I_{sc}	Output short circuit			-30	-100	-180	-30	-100	-180	mA

OSCILLATOR SECTION

f_s	Initial accuracy	$T_j = 25^\circ\text{C}$ (Note 6)	47	52	57	47	52	57	KHz
	Voltage stability	$12 \leq V_i \leq 25\text{V}$		0.2	1		0.2	1	%
	Temperature stability	$T_{MIN} < T_{amb} < T_{MAX}$ (Note 2)		5			5		%
V_4	Amplitude	V_{PIN4} peak to peak		1.7			1.7		V

ERROR AMP SECTION

V_2	Input voltage	$V_{PIN1} = 2.5\text{V}$	2.45	2.50	2.55	2.42	2.50	2.58	V
I_b	Input bias current			-0.3	-1		-0.3	-2	μA
	A_{VOL}	$2 \leq V_o \leq 4\text{V}$	65	90		65	90		dB
B	Unity gain bandwidth	(Note 2)	0.7	1		0.7	1		MHz
SVR	Supply voltage rejection	$12 \leq V_i \leq 25\text{V}$	60	70		60	70		dB
I_o	Output sink current	$V_{PIN2} = 2.7\text{V}$ $V_{PIN1} = 1.1\text{V}$	2	6		2	6		mA
I_o	Output source current	$V_{PIN2} = 2.3\text{V}$ $V_{PIN1} = 5\text{V}$	-0.5	-0.8		-0.5	-0.8		mA
	V_{OUT} High	$V_{PIN2} = 2.3\text{V}$; $R_L = 15\text{K}\Omega$ to ground	5	6		5	6		V
	V_{OUT} Low	$V_{PIN2} = 2.7\text{V}$, $R_L = 15\text{K}\Omega$ to Pin 8		0.7	1.1		0.7	1.1	V



UC1842/3/4/5
UC2842/3/4/5
UC3842/3/4/5

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	UC184X UC284X			UC384X			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	

CURRENT SENSE SECTION

G_V	Gain	(Notes 3 & 4)		2.85	3	3.15	2.85	3	3.15	V/V
V_3	Maximum input signal	$V_{PIN1} = 5V$ (Note 3)		0.9	1	1.1	0.9	1	1.1	V
SVR	Supply voltage rejection	$12 \leq V_i \leq 25V$ (Note 3)			70			70		dB
I_b	Input bias current				-2	-10		-2	-10	μA
	Delay to output				150	300		150	300	ns

OUTPUT SECTION

I_{OL}	Output low level	$I_{SINK} = 20mA$			0.1	0.4		0.1	0.4	V
		$I_{SINK} = 200mA$			1.5	2.2		1.5	2.2	
I_{OH}	Output high level	$I_{SOURCE} = 20mA$		13	13.5		13	13.5		V
		$I_{SOURCE} = 200mA$		12	13.5		12	13.5		
t_r	Rise time	$T_j = 25^\circ C$ $C_L = 1nF$ (Note 2)			50	150		50	150	ns
t_f	Fall time	$T_j = 25^\circ C$ $C_L = 1nF$ (Note 2)			50	150		50	150	ns

UNDER-VOLTAGE LOCKOUT SECTION

Start threshold	X842/4	15	16	17	14.5	16	17.5	V
	X843/5	7.8	8.4	9.0	7.8	8.4	9.0	
Min. operating voltage after turn-on	X842/4	9	10	11	8.5	10	11.5	V
	X843/5	7.0	7.6	8.2	7.0	7.6	8.2	

PWM SECTION

Maximum duty cycle	X842/3	95	97	100	95	97	100	%
	X844/5	46	48	50	47	48	50	
Minimum duty cycle				0			0	%

TOTAL STANDBY CURRENT

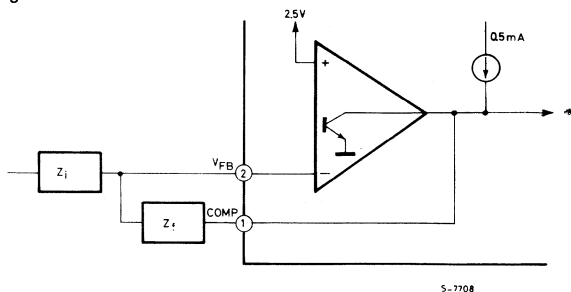
I _{st}	Start-Up current			0.5	1		0.5	1	mA
I _i	Operating supply current	V _{PIN2} = V _{PIN3} = 0V		11	17		11	17	mA
V _{iz}	Zener voltage	I _i = 25mA		34			34		V

- Notes:** 2. These parameters, although guaranteed, are not 100% tested in production
3. Parameter measured at trip point of latch with $V_{PIN2} = 0$.
4. Gain defined as:

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}}; 0 \leq V_{PIN3} \leq 0.8V$$

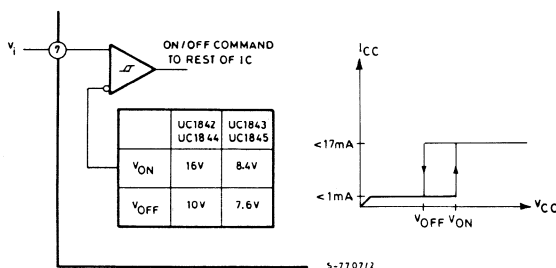
5. Adjust V_i above the start threshold before setting at 15V.
6. Output frequency equals oscillator frequency for the UC1842 and UC1843.
Output frequency is one half oscillator frequency for the UC1844 and UC1845.

Fig. 1 - Error amp configuration



Error amp can source or sink up to 0.5mA

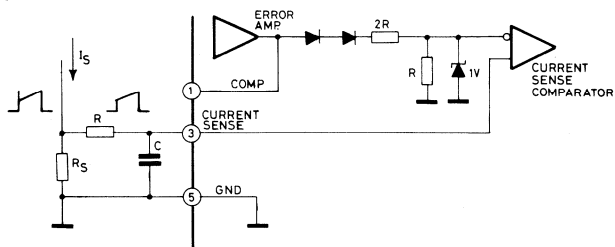
Fig. 2 - Under voltage lockout



During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder

resistor to prevent activating the power switch with extraneous leakage currents.

Fig. 3 - Current sense circuit



PEAK CURRENT (I_S) IS DETERMINED BY THE FORMULA

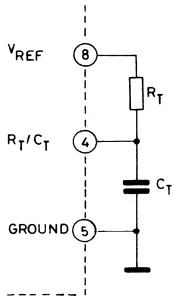
$$I_{S\max} \approx \frac{1.0V}{R_S}$$

A SMALL RC FILTER MAY BE REQUIRED TO SUPPRESS SWITCH TRANSIENTS.



UC1842/3/4/5
UC2842/3/4/5
UC3842/3/4/5

Fig. 4



$$\text{for } R_T > 5K\Omega \quad f = \frac{1.72}{R_T C_T}$$

Fig. 5 - Deadtime vs. C_T
($R_T > 5K\Omega$)

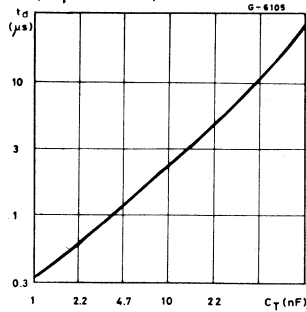


Fig. 6 - Timing resistance vs. frequency

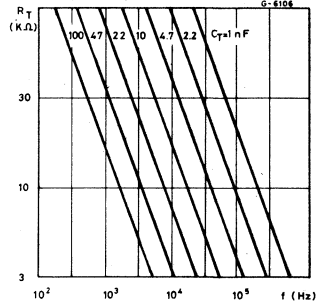


Fig. 7 - Output saturation characteristics

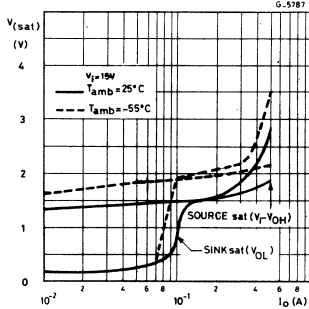


Fig. 8 - Error amplifier open-loop frequency response

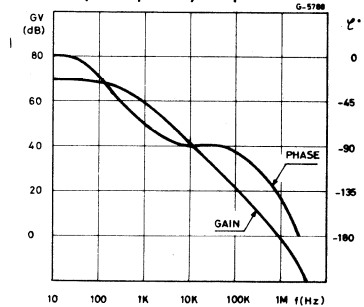
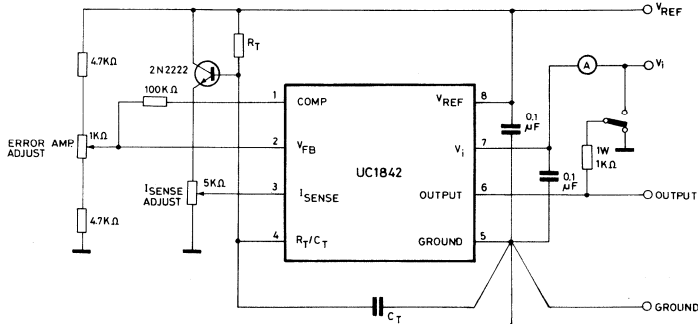


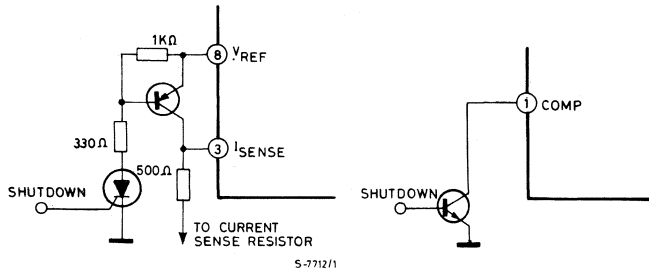
Fig. 9 - Open loop test circuit



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground.

The transistor and 5KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

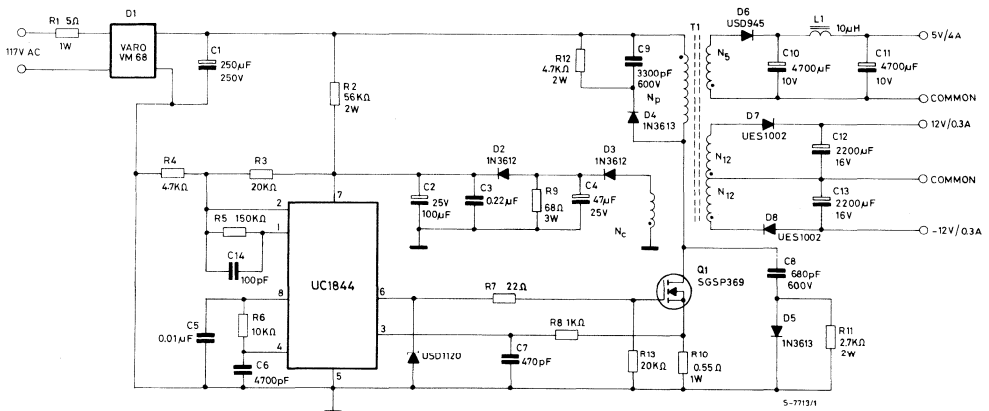
Fig. 10 – Shutdown techniques



Shutdown of the UC1842 can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either method cause the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock

cycle after the shutdown condition at pins 1 and/ or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_i below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

Fig. 11 - Off-line flyback regulator



Power Supply Specifications

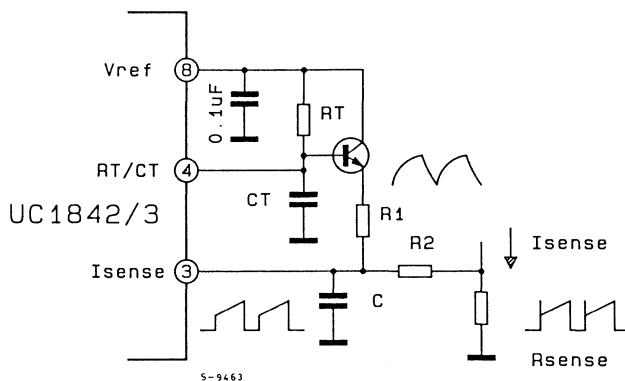
1. Input Voltage: 95VAC to 130VAC (50Hz/60Hz)
2. Line Isolation: 3750V
3. Switching Frequency: 40KHz
4. Efficiency @ Full Load: 70%

5. Output Voltage:
- A. +5V, $\pm 5\%$: 1A to 4A load
Ripple voltage: 50mV P-P Max.
 - B. +12V, $\pm 3\%$: 0.1A to 0.3A load
Ripple voltage: 100mV P-P Max.
 - C. -12V, $\pm 3\%$: 0.1A to 0.3A load
Ripple voltage: 100mV P-P Max.



UC1842/3/4/5
UC2842/3/4/5
UC3842/3/4/5

Fig. 12 - Slope compensation



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.

Note that capacitor, C , forms a filter with R_2 to suppress the leading edge switch spikes.



SEVEN DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500mA PER DRIVER (600mA PEAK)
- OUTPUT VOLTAGE 50V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

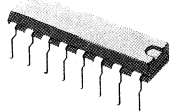
The ULN2001A, ULN2002A, ULN2003A and ULN2004A are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500mA and can withstand peak currents of 600mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

The four versions interface to all common logic families:

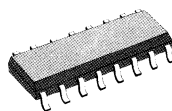
ULN2001A	General purpose, DTL, TTL, PMOS, CMOS
ULN2002A	14-25V PMOS
ULN2003A	5V TTL, CMOS
ULN2004A	6-15V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays filament lamps, thermal printheads and high power buffers.

The ULN2001A/2002A/2003A and 2004A are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance. They are available also in small outline package (SO-16) as ULN2001D/2002D/2003D/2004D.



DIP-16 Plastic (0.25)



SO-16

ORDERING NUMBER:

ULN2001A/2A/3A/4A (DIP-16)
ULN2001D/2D/3D/4D (SO-16)

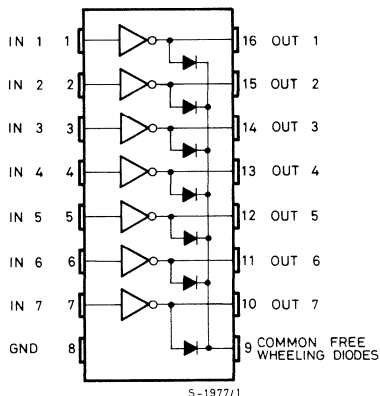
ABSOLUTE MAXIMUM RATINGS

V_o	Output voltage	50	V
V_{in}	Input voltage (for ULN2002A/D - 2003A/D - 2004A/D)	30	V
I_c	Continuous collector current	500	mA
I_b	Continuous base current	25	mA
T_{amb}	Operating ambient temperature range	-20 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Junction temperature	150	°C

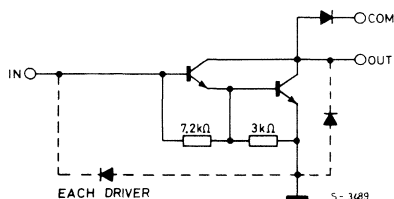


ULN2001A
ULN2002A
ULN2003A
ULN2004A

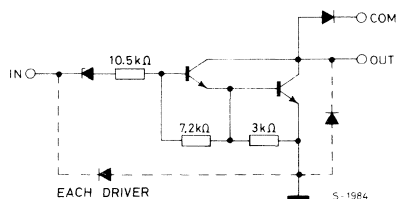
CONNECTION DIAGRAM



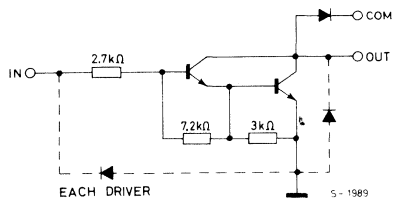
SCHEMATIC DIAGRAM



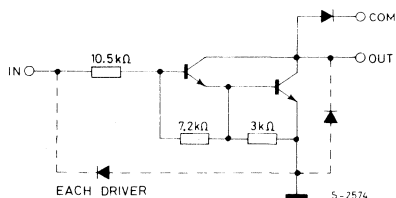
Series ULN-2001A
(each driver)



Series ULN-2002A
(each driver)



Series ULN-2003A
(each driver)



Series ULN-2004A
(each driver)

THERMAL DATA

THERMAL DATA			DIP-16	SO-16
$R_{thj-amb}$	Thermal resistance junction-ambient	max	70°C/W	165°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit	Fig.	
I_{CEX}	Output leakage current	$V_{CE} = 50V$	$V_{CE} = 50V$			50	μA	1a	
		$T_{amb} = 70^{\circ}C$			100	μA	1a		
		$T_{amb} = 70^{\circ}C$ for ULN2002A		$V_i = 6V$		500	μA	1b	
		$V_{CE} = 50V$ for ULN2004A $V_{CE} = 50V$		$V_i = 1V$		500	μA	1b	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$I_C = 100mA$	$I_B = 250 \mu A$		0.9	1.1	V	2	
		$I_C = 200mA$	$I_B = 350 \mu A$		1.1	1.3	V	2	
		$I_C = 350mA$	$I_B = 500 \mu A$		1.3	1.6	V	2	
$I_{i(on)}$	Input current	for ULN2002A	$V_i = 17V$		0.82	1.25	mA	3	
		for ULN2003A	$V_i = 3.85V$		0.93	1.35	mA	3	
		for ULN2004A	$V_i = 5V$		0.35	0.5	mA	3	
		$V_i = 12V$		1	1.45	mA	3		
$I_{i(off)}$	Input current	$T_{amb} = 70^{\circ}C$	$I_C = 500 \mu A$	50	65		μA	4	
$V_{i(on)}$	Input voltage	for ULN2002A	$I_C = 300 mA$			13	V	5	
		$V_{CE} = 2V$							
		for ULN2003A		$I_C = 200 mA$			2.4	V	5
		$V_{CE} = 2V$		$I_C = 250 mA$			2.7	V	5
		$V_{CE} = 2V$		$I_C = 300 mA$			3	V	5
		for ULN2004A							
		$V_{CE} = 2V$		$I_C = 125 mA$			5	V	5
		$V_{CE} = 2V$		$I_C = 200 mA$			6	V	5
		$V_{CE} = 2V$		$I_C = 275 mA$			7	V	5
$V_{CE} = 2V$	$I_C = 350 mA$			8	V	5			
h_{FE}	DC forward current gain	for ULN2001A $V_{CE} = 2V$	$I_C = 350 mA$	1000			—	2	
C_i	Input capacitance				15	25	pF	—	
t_{PLH}	Turn-on delay time	$0.5 V_i$ to $0.5 V_o$			0.25	1	μs	—	
t_{PHL}	Turn-off delay time	$0.5 V_i$ to $0.5 V_o$			0.25	1	μs	—	
I_R	Clamp diode leakage current	$V_R = 50V$	$V_R = 50V$			50	μA	6	
		$T_{amb} = 70^{\circ}C$			100	μA	6		
V_F	Clamp diode forward voltage	$I_F = 350 mA$			1.7	2	V	7	

TEST CIRCUITS

Fig. 1a

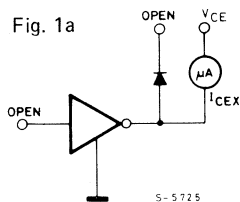


Fig. 2

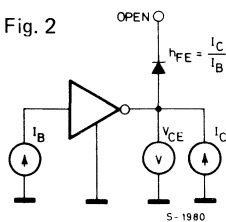


Fig. 4

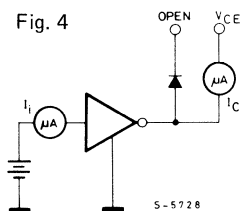


Fig. 6

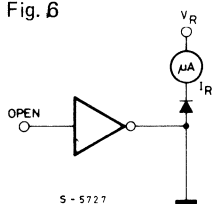


Fig. 1b

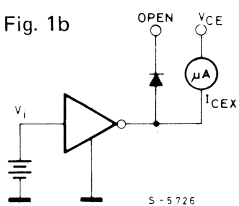


Fig. 3

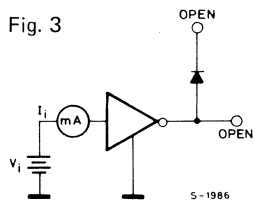


Fig. 5

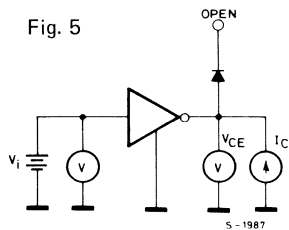
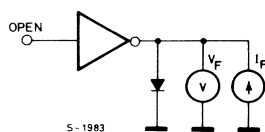


Fig. 7





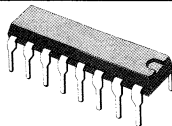
ULN2064B ULN2070B
ULN2066B ULN2074B
ULN2068B ULN2076B

50V - 1.5A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5A EACH DARLINGTON
- MINIMUM BREAKDOWN 50V
- SUSTAINING VOLTAGE AT LEAST 35V
- INTEGRAL SUPPRESSION DIODES (ULN2064B, ULN2066B, ULN2068B AND ULN2070B)
- ISOLATED DARLINGTON PINOUT (ULN2074B, ULN2076B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5A with a specified minimum breakdown of 50V and a sustaining voltage of

35V measured at 100mA. The ULN2064B, ULN2066B, ULN2068B and ULN2070B contain integral suppression diodes for inductive loads have common emitters. The ULN2074B and ULN2076B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2064B, ULN2068B and ULN2074B are compatible with popular 5V logic families and the ULN2066B and ULN2076B are compatible with 6-15V CMOS and PMOS. Types ULN2068B and ULN2070B include a predriver stage to reduce loading on the control logic.

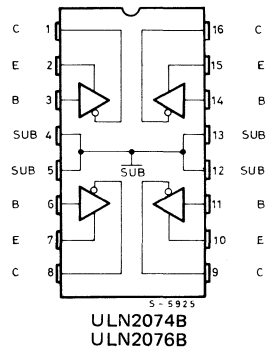
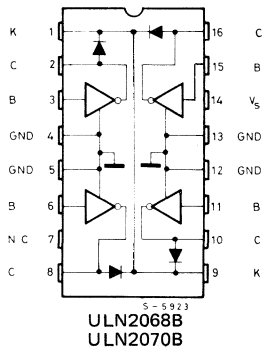
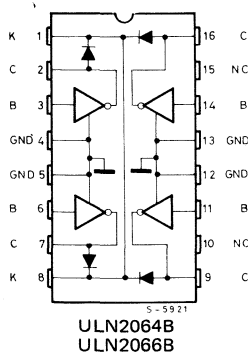


Powerdip
12 + 2 + 2

ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Output voltage	50	V
$V_{CE(sus)}$	Output sustaining voltage	35	V
I_o	Output current	1.75	A
V_i	Input voltage for ULN2066B/70B/74B/76B for ULN2064B/68B	30	V
		15	V
I_i	Input current	25	mA
V_s	Supply voltage for ULN2068B for ULN2070B	10	V
		20	V
P_{tot}	Power dissipation: at $T_{amb} = 90^\circ\text{C}$ at $T_{amb} = 70^\circ\text{C}$	4.3	W
		1	W
T_{amb}	Operating ambient temperature range	-20 to 85	$^\circ\text{C}$
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$

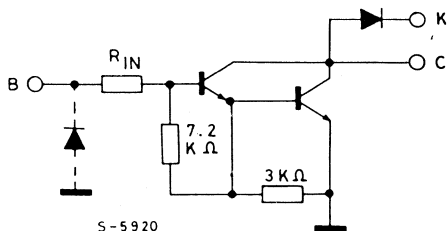
CONNECTION DIAGRAM (Top view) and ORDERING NUMBERS





ULN2064B
ULN2066B
ULN2068B
ULN2070B
ULN2074B
ULN2076B

SCHEMATIC DIAGRAM



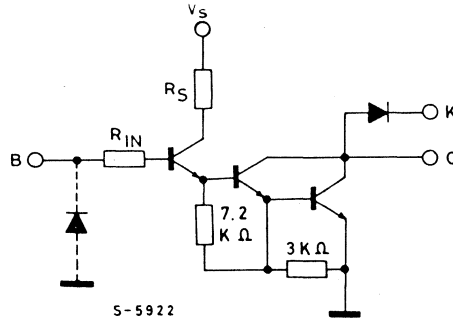
ULN2064B : $R_{IN} = 350\Omega$
ULN2066B : $R_{IN} = 3\text{ k}\Omega$

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX} Output leakage current	for ULN2064B-ULN2066B $V_{CE} = 50\text{V}$ $V_{CE} = 50\text{V}$ $T_{amb} = 70^\circ\text{C}$			100 500	μA μA	1
$V_{CE(sus)}$ Collector-emitter sustaining voltage	for ULN2064B-ULN2066B $I_C = 100\text{mA}$ $V_i = 0.4\text{V}$	35			V	2
$V_{CE(sat)}$ Collector-emitter saturation voltage	$I_C = 500\text{mA}$ $I_B = 625\mu\text{A}$ $I_C = 750\text{mA}$ $I_B = 935\mu\text{A}$ $I_C = 1\text{A}$ $I_B = 1.25\text{mA}$ $I_C = 1.25\text{A}$ $I_B = 2\text{mA}$			1.1 1.2 1.3 1.4	V V V V	3
$I_{i(on)}$ Input current	for ULN2064B $V_i = 2.4\text{V}$ for ULN2064B $V_i = 3.75\text{V}$ for ULN2066B $V_i = 5\text{V}$ for ULN2066B $V_i = 12\text{V}$	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$ Input voltage	for ULN2064B $V_{CE} = 2\text{V}$ $I_C = 1\text{A}$ $V_{CE} = 2\text{V}$ $I_C = 1.5\text{A}$ for ULN2066B $V_{CE} = 2\text{V}$ $I_C = 1\text{A}$ $V_{CE} = 2\text{V}$ $I_C = 1.5\text{A}$			2 2.5 6.5 10	V V V V	5
t_{PLH} Turn-on delay time	$0.5V_i$ to $0.5V_o$			1	μs	
t_{PHL} Turn-off delay time	$0.5V_i$ to $0.5V_o$			1.5	μs	
I_R Clamp diode leakage current	for ULN2064B-ULN2066B $V_R = 80\text{V}$ $V_R = 80\text{V}$ $T_{amb} = 70^\circ\text{C}$			50 100	μA μA	6
V_F Clamp diode forward voltage	$I_F = 1\text{A}$ $I_F = 1.5\text{A}$			1.75 2	V V	7

NOTE: 1 — Input voltage is with reference to the substrate (no connection to any other pins) for the ULN2074B and ULN2076B reference is ground for all other types
2 — Input current may be limited by maximum allowable input voltage

SCHEMATIC DIAGRAM



ULN2068B : $R_{IN} = 2.5 \text{ k}\Omega$ $R_S = 900\Omega$
ULN2070B : $R_{IN} = 11.6 \text{ k}\Omega$ $R_S = 3.4 \text{ k}\Omega$

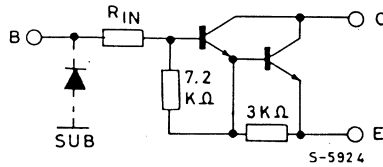
ELECTRICAL CHARACTERISTICS ($V_S = 5\text{V}$ for ULN2068B, $V_S = 12\text{V}$ for ULN2070B, $T_{amb} = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX} Output leakage current	for ULN2068B-ULN2070B $V_{CE} = 50\text{V}$ $V_{CE} = 50\text{V}$ $T_{amb} = 70^\circ\text{C}$			100 500	μA μA	1
$V_{CE(sus)}$ Collector-emitter sustaining voltage	for ULN2068B-ULN2070B $I_C = 100\text{mA}$ $V_i = 0.4\text{V}$	35			V	2
$V_{CE(sat)}$ Collector-emitter saturation voltage	for ULN2068B $I_C = 500\text{mA}$ $V_i = 2.75\text{V}$ $I_C = 750\text{mA}$ $V_i = 2.75\text{V}$ $I_C = 1\text{A}$ $V_i = 2.75\text{V}$ $I_C = 1.25\text{A}$ $V_i = 2.75\text{V}$ for ULN2070B $I_C = 500\text{mA}$ $V_i = 5\text{V}$ $I_C = 750\text{mA}$ $V_i = 5\text{V}$ $I_C = 1\text{A}$ $V_i = 5\text{V}$ $I_C = 1.25\text{A}$ $V_i = 5\text{V}$			1.1 1.2 1.3 1.4 1.1 1.2 1.3 1.4	V V V V V V V V	2
$I_{i(on)}$ Input current	for ULN2068B $V_i = 2.75\text{V}$ for ULN2068B $V_i = 3.75\text{V}$ for ULN2070B $V_i = 5\text{V}$ for ULN2070B $V_i = 12\text{V}$			550 1000 400 1250	μA μA μA μA	4
$V_{i(on)}$ Input voltage	$V_{CE} = 2\text{V}$ $I_C = 1.5\text{A}$ for ULN2068B for ULN2070B			2.75 5	V V	5
I_S Supply current	for ULN2068B $I_C = 500\text{mA}$ $V_i = 2.75\text{V}$ for ULN2070B $I_C = 500\text{mA}$ $V_i = 5\text{V}$			6 4.5	mA mA	8
t_{PLH} Turn-on delay time	$0.5V_i$ to $0.5V_o$			1	μs	
t_{PHL} Turn-off delay time	$0.5V_i$ to $0.5V_o$ $I_C = 1.25\text{A}$			1.5	μs	
I_R Clamp diode leakage current	for ULN2068B-ULN2070B $V_R = 50\text{V}$ $V_R = 50\text{V}$ $T_{amb} = 70^\circ\text{C}$			50 100	μA μA	6
V_F Clamp diode forward voltage	$I_F = 1\text{A}$ $I_F = 1.5\text{A}$			1.75 2	V V	7



ULN2064B
ULN2066B
ULN2068B
ULN2070B
ULN2074B
ULN2076B

SCHEMATIC DIAGRAM



ULN2074B : $R_{IN} = 350\Omega$

ULN2076B : $R_{IN} = 3\text{ k}\Omega$

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX} Output leakage current	for ULN2074B-ULN2076B $V_{CE} = 50\text{V}$ $V_{CE} = 50\text{V}$ $T_{amb} = 70^\circ\text{C}$			100 500	μA μA	1
$V_{CE(sus)}$ Collector-emitter sustaining voltage	for ULN2074B-ULN2076B $I_C = 100\text{mA}$ $V_i = 0.4\text{V}$	35			V	2
$V_{CE(sat)}$ Collector-emitter saturation voltage	$I_C = 500\text{mA}$ $I_B = 625\mu\text{A}$ $I_C = 750\text{mA}$ $I_B = 935\mu\text{A}$ $I_C = 1\text{A}$ $I_B = 1.25\text{mA}$ $I_C = 1.25\text{A}$ $I_B = 2\text{mA}$			1.1 1.2 1.3 1.4	V V V V	3
$I_{i(on)}$ Input current	for ULN2074B $V_i = 2.4\text{V}$ for ULN2074B $V_i = 3.75\text{V}$ for ULN2076B $V_i = 5\text{V}$ for ULN2076B $V_i = 12\text{V}$	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$ Input voltage	for ULN2074B $V_{CE} = 2\text{V}$ $I_C = 1\text{A}$ $V_{CE} = 2\text{V}$ $I_C = 1.5\text{A}$ for ULN2076B $V_{CE} = 2\text{V}$ $I_C = 1\text{A}$ $V_{CE} = 2\text{V}$ $I_C = 1.5\text{A}$			2 2.5 6.5 10	V V V V	5
t_{PLH} Turn-on delay time	$0.5V_i$ to $0.5V_o$			1	μs	
t_{PHL} Turn-off delay time	$0.5V_i$ to $0.5V_o$			1.5	μs	

TEST CIRCUITS

Fig. 1

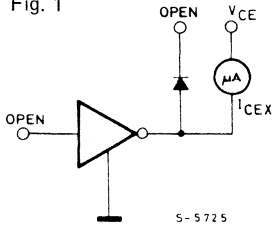


Fig. 2

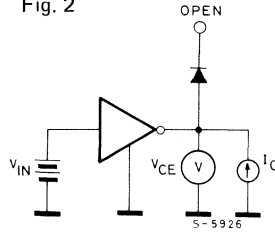


Fig. 3

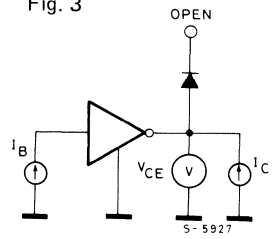


Fig. 4

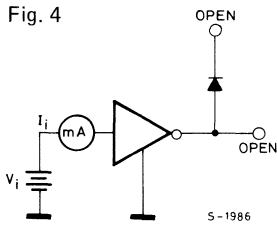


Fig. 5

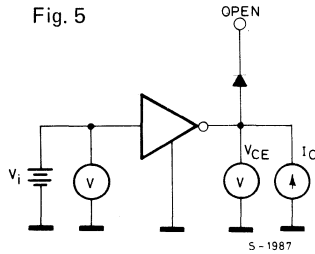


Fig. 6

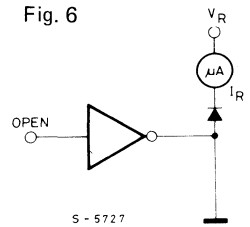


Fig. 7

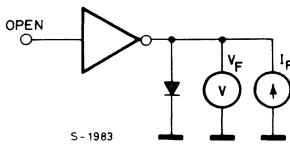


Fig. 8

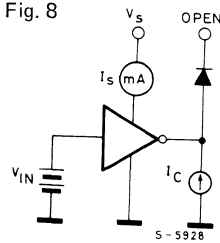


Fig. 9 - Input current as a function of input voltage

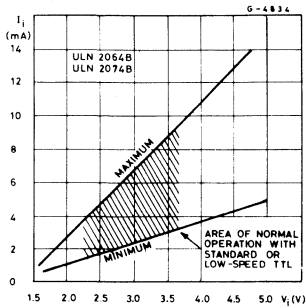


Fig. 10 - Input current as a function of input voltage

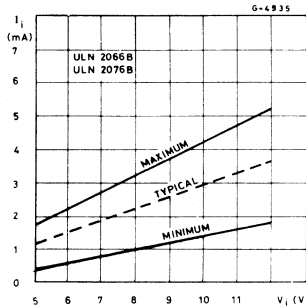
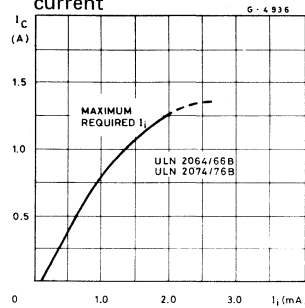


Fig. 11 - Collector current as a function of input current



TYPICAL APPLICATIONS

Fig. 12 - Common-anode LED drivers

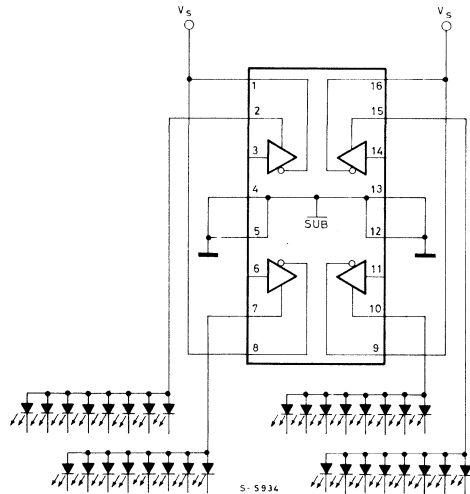
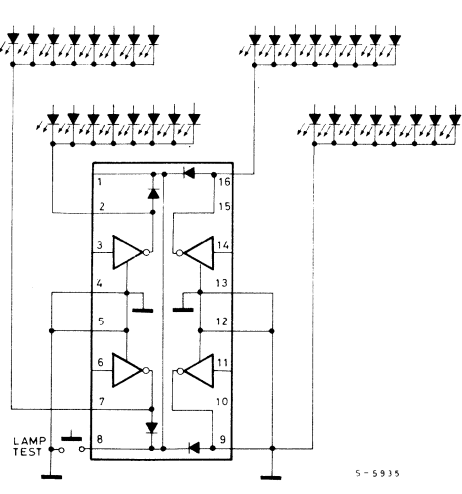


Fig. 13 - Common-cathode LED drivers



MOUNTING INSTRUCTIONS

The $R_{thj-amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 14) or to an external heatsink (Fig. 15).

The diagram of figure 16 shows the maximum dissippable power P_{tot} and the $R_{thj-amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (1.4 mils).

During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 14 - Example of P.C. board copper area which is used as heatsink.

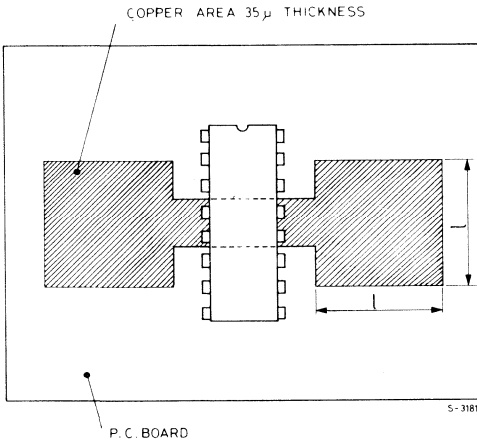


Fig. 15 - External heatsink mouting example

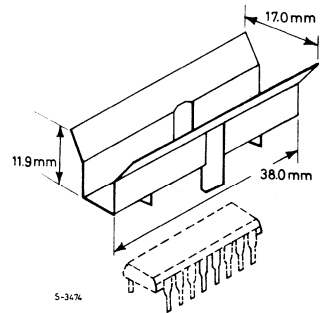


Fig. 16 - Maximum dissippable power and junction to ambient thermal resistance vs. side "ℓ"

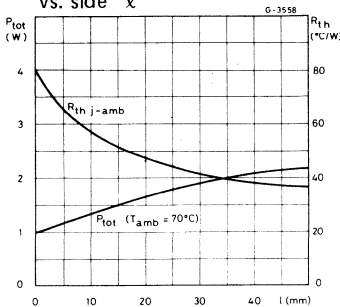
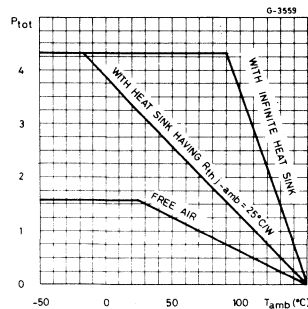


Fig. 17 - Maximum allowable power dissipation vs. ambient temperature





ULN2065B ULN2071B
ULN2067B ULN2075B
ULN2069B ULN2077B

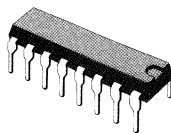
PRELIMINARY DATA

80V - 1.5A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5A EACH DARLINGTON
- MINIMUM BREAKDOWN 80V
- SUSTAINING VOLTAGE AT LEAST 50V
- INTEGRAL SUPPRESSION DIODES (ULN2065B, ULN2067B, ULN2069B AND ULN2071B)
- ISOLATED DARLINGTON PINOUT (ULN2075B AND ULN2077B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5A with a specified minimum breakdown of 80V and a sustaining voltage of 50V. The ULN2065B, ULN2067B, ULN2069B

and ULN2071B contain integral suppression diodes for inductive loads and have common emitters; the ULN2075B and ULN2077B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2065B, ULN2069B and ULN2075B are compatible with popular 5V logic families and the ULN2067B, ULN2071B and ULN2077B are compatible with 6-15 CMOS and PMOS. The ULN2069B and ULN2071B include a predriver stage to provide extragain, reducing the load on control logic.

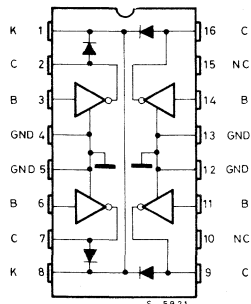


Powerdip
12 + 2 + 2

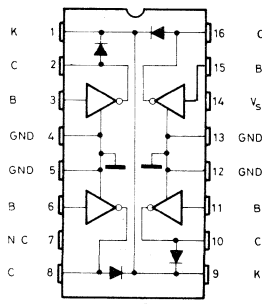
ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Output voltage	80	V
$V_{CE(sus)}$	Output sustaining voltage	50	V
I_o	Output current	1.75	A
V_i	Input voltage	60	V
	for ULN2075B - 2077B	30	V
	for ULN2067B - 2071B	15	V
	for ULN2065B - 2069B	25	mA
I_i	Input current	10	V
V_s	Supply voltage for ULN2069B	20	V
	for ULN2071B	4.3	W
P_{tot}	Power dissipation: at $T_{pins} = 90^{\circ}C$	1	W
	at $T_{amb} = 70^{\circ}C$	-20 to 85	$^{\circ}C$
T_{amb}	Operating ambient temperature range	-55 to 150	$^{\circ}C$
T_{stg}	Storage temperature		

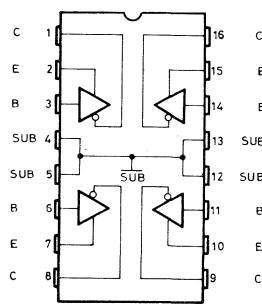
CONNECTIONS DIAGRAMS (Top view) and ORDERING NUMBERS



ULN2065B
ULN2067B



ULN2069B
ULN2071B

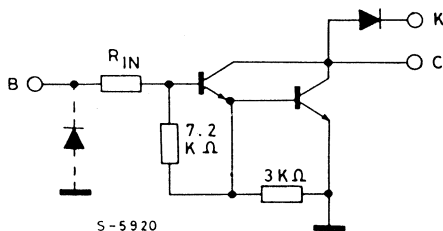


ULN2075B
ULN2077B



ULN2065B
ULN2067B
ULN2069B
ULN2071B
ULN2075B
ULN2077B

SCHEMATIC DIAGRAM



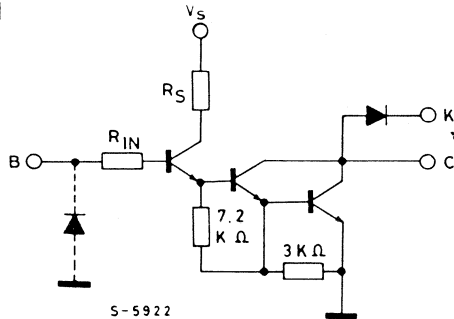
ULN2065B : $R_{IN} = 350\Omega$
ULN2067B : $R_{IN} = 3\text{ k}\Omega$

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX} Output leakage current	for ULN2065B-ULN2067B $V_{CE} = 80\text{V}$ $V_{CE} = 80\text{V}$ $T_{amb} = 70^\circ\text{C}$			100 500	μA μA	1
$V_{CE(sus)}$ Collector-emitter sustaining voltage	for ULN2065B-ULN2067B $I_C = 100\text{mA}$ $V_i = 0.4\text{V}$	50			V	2
$V_{CE(sat)}$ Collector-emitter saturation voltage	$I_C = 500\text{mA}$ $I_B = 625\mu\text{A}$ $I_C = 750\text{mA}$ $I_B = 935\mu\text{A}$ $I_C = 1\text{A}$ $I_B = 1.25\text{mA}$ $I_C = 1.25\text{A}$ $I_B = 2\text{mA}$ for ULN2065B-ULN2067B $I_C = 1.5\text{A}$ $I_B = 2.25\text{mA}$			1.1 1.2 1.3 1.4 1.5	V V V V V	3
$I_{i(on)}$ Input current	for ULN2065B $V_i = 2.4\text{V}$ for ULN2065B $V_i = 3.75\text{V}$ for ULN2067B $V_i = 5\text{V}$ for ULN2067B $V_i = 12\text{V}$	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$ Input voltage	for ULN2065B $V_{CE} = 2\text{V}$ $I_C = 1\text{A}$ $V_{CE} = 2\text{V}$ $I_C = 1.5\text{A}$ for ULN2067B $V_{CE} = 2\text{V}$ $I_C = 1\text{A}$ $V_{CE} = 2\text{V}$ $I_C = 1.5\text{A}$			2 2.5 6.5 10	V V V V	5
t_{PLH} Turn-on delay time	$0.5V_i$ to $0.5V_o$			1	μs	
t_{PHL} Turn-off delay time	$0.5V_i$ to $0.5V_o$			1.5	μs	
I_R Clamp diode leakage current	for ULN2065B-ULN2067B $V_R = 80\text{V}$ $V_R = 80\text{V}$ $T_{amb} = 70^\circ\text{C}$			50 100	μA μA	6
V_F Clamp diode forward voltage	$I_F = 1\text{A}$ $I_F = 1.5\text{A}$			1.75 2	V V	7

NOTE: 1 — Input voltage is with reference to the substrate (no connection to any other pins) for the ULN2075B and ULN2077B reference is ground for all other types
2 — Input current may be limited by maximum allowable input voltage

SCHEMATIC DIAGRAM



ULN2069B : $R_{IN} = 2.5 \text{ k}\Omega$, $R_S = 900\Omega$
ULN2071B : $R_{IN} = 11.6 \text{ k}\Omega$, $R_S = 3.4 \text{ k}\Omega$

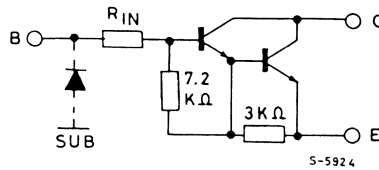
ELECTRICAL CHARACTERISTICS ($V_S = 5\text{V}$ for ULN2069B, $V_S = 12\text{V}$ for ULN2071B, $T_{amb} = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX} Output leakage current	for ULN2069B-ULN2071B $V_{CE} = 80\text{V}$ $V_{CE} = 80\text{V}$ $T_{amb} = 70^\circ\text{C}$			100 500	μA μA	1
$V_{CE(sus)}$ Collector-emitter sustaining voltage	for ULN2069B-ULN2071B $I_C = 100\text{mA}$ $V_i = 0.4\text{V}$	50			V	2
$V_{CE(sat)}$ Collector-emitter saturation voltage	for ULN2069B $I_C = 500\text{mA}$ $V_i = 2.75\text{V}$ $I_C = 750\text{mA}$ $V_i = 2.75\text{V}$ $I_C = 1\text{A}$ $V_i = 2.75\text{V}$ $I_C = 1.25\text{A}$ $V_i = 2.75\text{V}$ $I_C = 1.5\text{A}$ $V_i = 2.75\text{V}$ for ULN2071B $I_C = 500\text{mA}$ $V_i = 5\text{V}$ $I_C = 750\text{mA}$ $V_i = 5\text{V}$ $I_C = 1\text{A}$ $V_i = 5\text{V}$ $I_C = 1.25\text{A}$ $V_i = 5\text{V}$ $I_C = 1.5\text{A}$ $V_i = 5\text{V}$			1.1 1.2 1.3 1.4 1.5 1.1 1.2 1.3 1.4 1.5	V V V V V V V V V	2
$I_{i(on)}$ Input current	for ULN2069B $V_i = 2.75\text{V}$ for ULN2069B $V_i = 3.75\text{V}$ for ULN2071B $V_i = 5\text{V}$ for ULN2071B $V_i = 12\text{V}$			550 1000 400 1250	μA μA μA μA	4
$V_{i(on)}$ Input voltage	$V_{CE} = 2\text{V}$ $I_C = 1.5\text{A}$ for ULN2069B for ULN2071B			2.75 5	V	5
I_S Supply current	for ULN2069B $I_C = 500\text{mA}$ $V_i = 2.75\text{V}$ for ULN2071B $I_C = 500\text{mA}$ $V_i = 5\text{V}$			6 4.5	mA mA	8
t_{PLH} Turn-on delay time	$0.5V_i$ to $0.5V_o$			1	μs	
t_{PHL} Turn-off delay time	$0.5V_i$ to $0.5V_o$ $I_C = 1.25\text{A}$			1.5	μs	
I_R Clamp diode leakage current	for ULN2069B-ULN2071B $V_R = 80\text{V}$ $V_R = 80\text{V}$ $T_{amb} = 70^\circ\text{C}$			50 100	μA μA	6
V_F Clamp diode forward voltage	$I_F = 1\text{A}$ $I_F = 1.5\text{A}$			1.75 2	V V	7



ULN2065B
ULN2067B
ULN2069B
ULN2071B
ULN2075B
ULN2077B

SCHEMATIC DIAGRAM



ULN2075B : $R_{IN} = 350\Omega$
ULN2077B : $R_{IN} = 3\text{ k}\Omega$

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX} Output leakage current	for ULN2075B-ULN2077B $V_{CE} = 80\text{V}$ $V_{CE} = 80\text{V}$ $T_{amb} = 70^\circ\text{C}$			100 500	μA μA	1
$V_{CE(sus)}$ Collector-emitter sustaining voltage	for ULN2075B-ULN2077B $I_C = 100\text{mA}$ $V_i = 0.4\text{V}$	50			V	2
$V_{CE(sat)}$ Collector-emitter saturation voltage	$I_C = 500\text{mA}$ $I_B = 625\mu\text{A}$ $I_C = 750\text{mA}$ $I_B = 935\mu\text{A}$ $I_C = 1\text{A}$ $I_B = 1.25\text{mA}$ $I_C = 1.25\text{A}$ $I_B = 2\text{mA}$ for ULN2075B-ULN2077B $I_C = 1.5\text{A}$ $I_B = 2.25\text{mA}$			1.1 1.2 1.3 1.4 1.5	V V V V V	3
$I_{i(on)}$ Input current	for ULN2075B $V_i = 2.4\text{V}$ for ULN2075B $V_i = 3.75\text{V}$ for ULN2077B $V_i = 5\text{V}$ for ULN2077B $V_i = 12\text{V}$	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$ Input voltage	for ULN2075B $V_{CE} = 2\text{V}$ $I_C = 1\text{A}$ $V_{CE} = 2\text{V}$ $I_C = 1.5\text{A}$ for ULN2077B $V_{CE} = 2\text{V}$ $I_C = 1\text{A}$ $V_{CE} = 2\text{V}$ $I_C = 1.5\text{A}$			2 2.5 6.5 10	V V V V	5
t_{PLH} Turn-on delay time	$0.5V_i$ to $0.5V_o$			1	μs	
t_{PHL} Turn-off delay time	$0.5V_i$ to $0.5V_o$			1.5	μs	

TEST CIRCUITS

Fig. 1

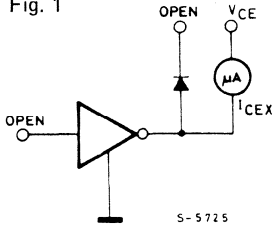


Fig. 2

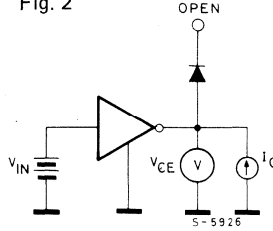


Fig. 3

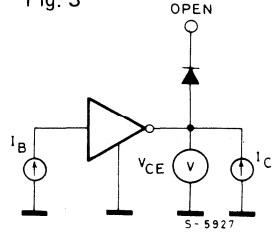


Fig. 4

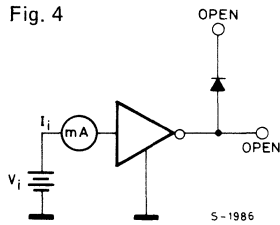


Fig. 5

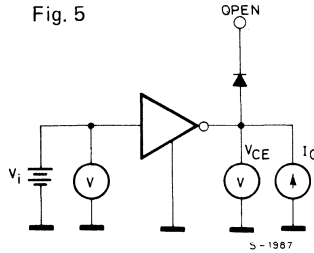


Fig. 6

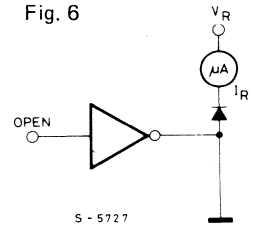


Fig. 7

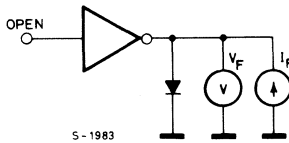


Fig. 8

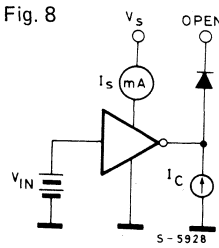


Fig. 9 - Input current as a function of input voltage

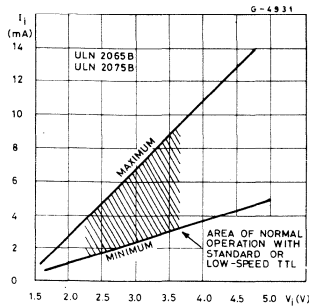


Fig. 10 - Input current as a function of input voltage

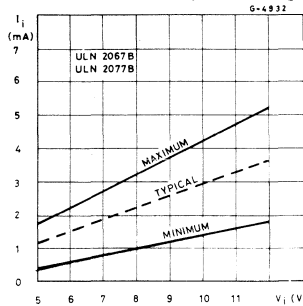
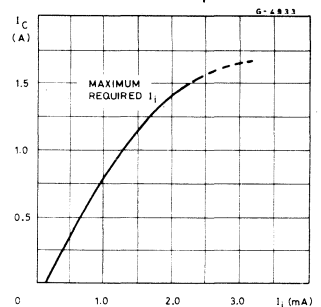


Fig. 11 - Collector current as a function of input current



MOUNTING INSTRUCTIONS

The $R_{thj-amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 12) or to an external heatsink (Fig. 13). The diagram of figure 14 shows the maximum dissippable power P_{tot} and the $R_{thj-amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (1.4 mils). During soldering the pins temperature must not exceed $260^{\circ}C$ and the soldering time must not be longer than 12 seconds. The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 12 – Example of P.C. board copper area which is used as heatsink.

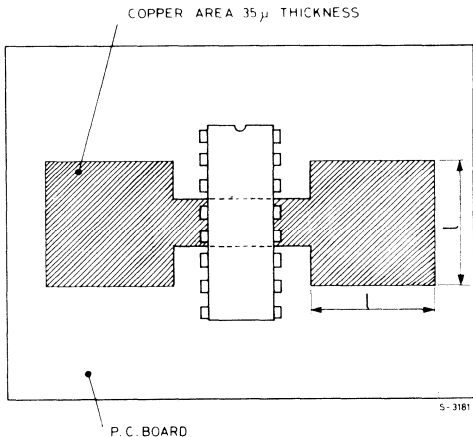


Fig.13 – External heatsink mounting example

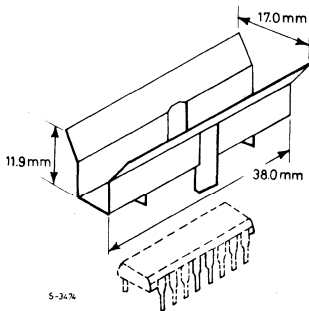


Fig. 14 – Maximum dissippable power and junction to ambient thermal resistance vs. side "ℓ"

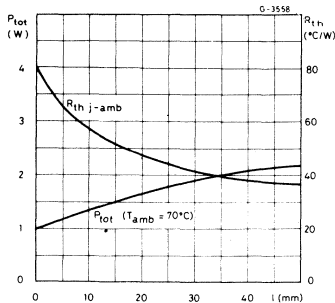
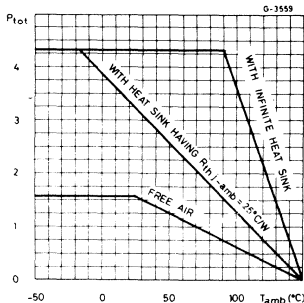


Fig. 15 – Maximum allowable power dissipation vs. ambient temperature





ULN2801A ULN2804A
ULN2802A ULN2805A
ULN2803A

EIGHT DARLINGTON ARRAYS

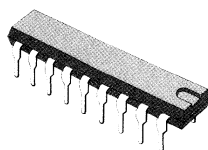
- EIGHT DARLINGTONS WITH COMMON EMITTERS
- OUTPUT CURRENT TO 500mA
- OUTPUT VOLTAGE TO 50V
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR ALL POPULAR LOGIC FAMILIES
- OUTPUT CAN BE PARALLELED
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY BOARD LAYOUT

The ULN2801A -ULN2805A each contain eight darlington transistors with common emitters and integral suppression diodes for inductive loads. Each darlington features a peak load current rating of 600mA (500mA continuous) and can withstand at least 50V in the off state. Outputs may be paralleled for higher current capability.

Five versions are available to simplify interfacing to standard logic families: the ULN2801A is

designed for general purpose applications with a current limit resistor; the ULN2802A has a 10.5K Ω input resistor and zener for 14-25V PMOS; the ULN2803A has a 2.7K Ω input resistor for 5V TTL and CMOS; the ULN2804A has a 10.5K Ω input resistor for 6-15V CMOS and the ULN2805A is designed to sink a minimum of 350mA for standard and Schottky TTL where higher output current is required.

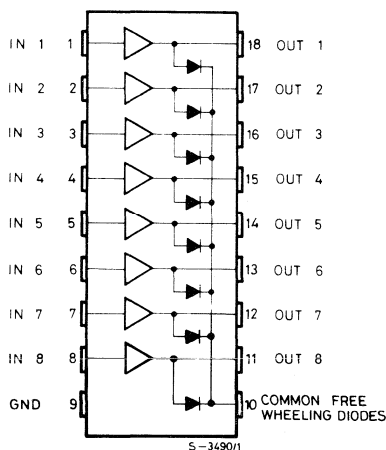
All types are supplied in a 18-lead plastic DIP with a copper lead from and feature the convenient input-opposite-output pinout to simplify board layout,



DIP-18 Plastic
(U7P2)

CONNECTION DIAGRAM

(top view)



S-34901



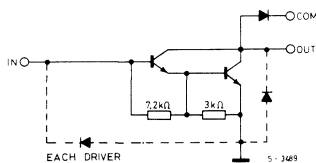
ULN2801A
ULN2802A
ULN2803A
ULN2804A
ULN2805A

ABSOLUTE MAXIMUM RATINGS

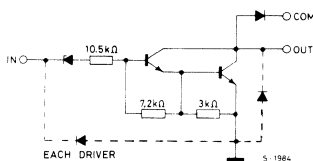
V_o	Output voltage	50	V
V_i	Input voltage for ULN 2802A, 2803A, 2804A for ULN 2805A	30 15	V V
I_C	Continuous collector current	500	mA
I_B	Continuous base current	25	mA
P_{tot}	Power dissipation (one Darlington pair) (total package)	1.0 2.25	W W
T_{amb}	Operating ambient temperature range	-20 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

SCHEMATIC DIAGRAMS

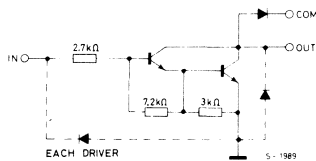
For ULN 2801A (each driver
for PMOS-CMOS)



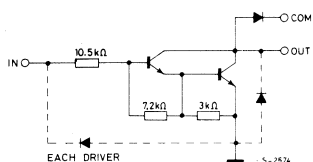
For ULN 2802A (each driver
for 14-15V PMOS)



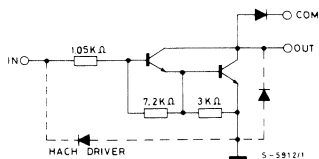
For ULN 2803A (each driver
for 5V, TTL/CMOS)



For ULN 2804A (each driver for
6-15V CMOS/PMOS)



For ULN 2805A (each driver for
high out TTL)



THERMAL DATA

$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	55	°C/W
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ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX} Output leakage current	$V_{CE} = 50\text{V}$ $T_{amb} = 70^{\circ}\text{C}$ $T_{amb} = 70^{\circ}\text{C}$ for ULN 2802A $V_{CE} = 50\text{V}$ $V_i = 6\text{V}$ for ULN 2804A $V_{CE} = 50\text{V}$ $V_i = 1\text{V}$			50 100 500 500	μA μA μA μA	1a 1a 1b 1b
$V_{CE(sat)}$ Collector-emitter saturation voltage	$I_C = 100\text{ mA}$ $I_B = 250\text{ }\mu\text{A}$ $I_C = 200\text{ mA}$ $I_B = 350\text{ }\mu\text{A}$ $I_C = 350\text{ mA}$ $I_B = 500\text{ }\mu\text{A}$		0.9 1.1 1.3	1.1 1.3 1.6	V V V	2
$I_{i(on)}$ Input current	for ULN 2802A $V_i = 17\text{V}$ for ULN 2803A $V_i = 3.85\text{V}$ for ULN 2804A $V_i = 5\text{V}$ $V_i = 12\text{V}$ for ULN 2805A $V_i = 3\text{V}$		0.82 0.93 0.35 1 1.5	1.25 1.35 0.5 1.45 2.4	mA mA mA mA mA	3
$I_{i(off)}$ Input current	$T_{amb} = 70^{\circ}\text{C}$ $I_C = 500\text{ }\mu\text{A}$	50	65		μA	4
$V_{i(on)}$ Input voltage	for ULN 2802A $V_{CE} = 2\text{V}$ $I_C = 300\text{ mA}$ for ULN 2803A $V_{CE} = 2\text{V}$ $I_C = 200\text{ mA}$ $V_{CE} = 2\text{V}$ $I_C = 250\text{ mA}$ $V_{CE} = 2\text{V}$ $I_C = 300\text{ mA}$ for ULN 2804A $V_{CE} = 2\text{V}$ $I_C = 125\text{ mA}$ $V_{CE} = 2\text{V}$ $I_C = 200\text{ mA}$ $V_{CE} = 2\text{V}$ $I_C = 275\text{ mA}$ $V_{CE} = 2\text{V}$ $I_C = 350\text{ mA}$ for ULN 2805A $V_{CE} = 2\text{V}$ $I_C = 350\text{ mA}$			13 2.4 2.7 3 5 6 7 8 2.4	V V V V V V V V V	5
h_{FE} DC forward current gain	for ULN 2801A $V_{CE} = 2\text{V}$ $I_C = 350\text{ mA}$	1000			—	2
C_i Input capacitance			15	25	pF	—
t_{PLH} Turn-on delay time	$0.5\text{ }V_i$ to $0.5\text{ }V_o$		0.25	1	μs	—
t_{PHL} Turn-off delay time	$0.5\text{ }V_i$ to $0.5\text{ }V_o$		0.25	1	μs	—
I_R Clamp diode leakage current	$V_R = 50\text{V}$ $T_{amb} = 70^{\circ}\text{C}$ $V_R = 50\text{V}$			50 100	μA μA	6
V_F Clamp diode forward voltage	$I_F = 350\text{ mA}$		1.7	2	V	7



ULN2801A
ULN2802A
ULN2803A
ULN2804A
ULN2805A

TEST CIRCUITS

Fig. 1a

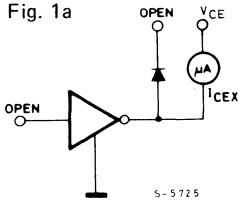


Fig. 1b

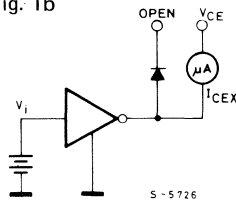


Fig. 2

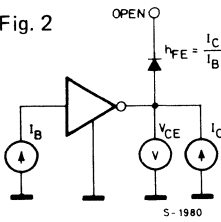


Fig. 3

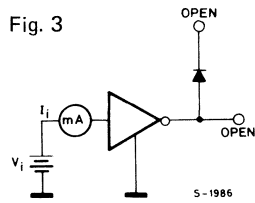


Fig. 4

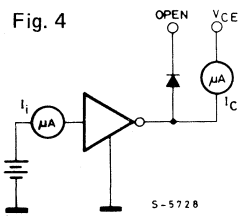


Fig. 5

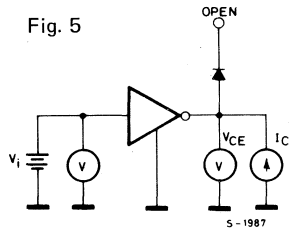


Fig. 6

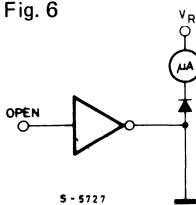
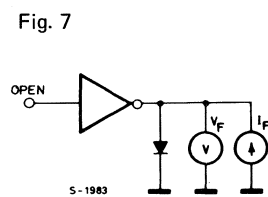


Fig. 7





ULN2801A
ULN2802A
ULN2803A
ULN2804A
ULN2805A

Fig. 8 - Collector current as a function of saturation voltage

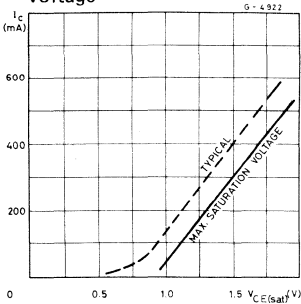


Fig. 9 - Collector current as a function of input current

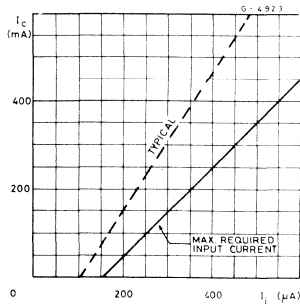


Fig. 10 - Allowable average power dissipation as a function of ambient temperature

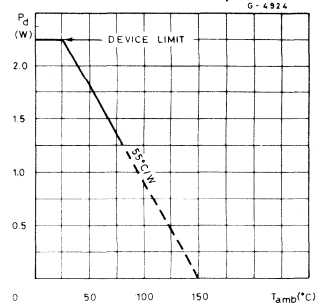


Fig. 11 - Peak collector current as a function of duty cycle

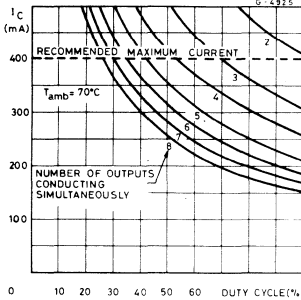


Fig. 12 - Peak collector current as a function of duty cycle

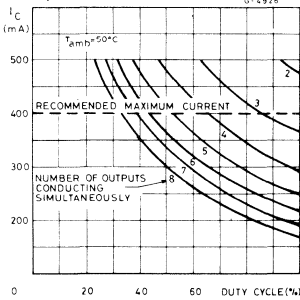


Fig. 13 - Input current as a function of input voltage (for ULN 2802A)

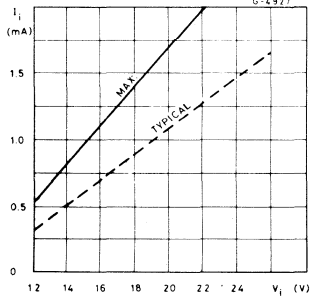


Fig. 14 - Input current as a function of input voltage (for ULN 2804A)

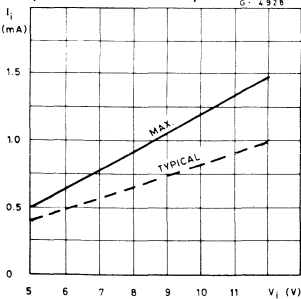


Fig. 15 - Input current as a function of input voltage (for ULN 2803A)

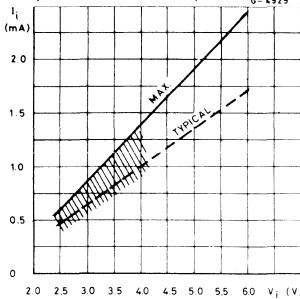
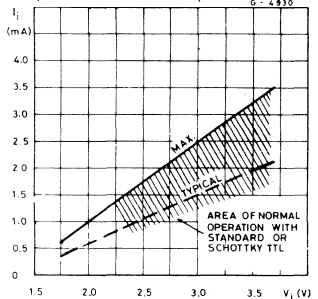


Fig. 16 - Input current as a function of input voltage (for ULN 2805A)





ULQ2001R
ULQ2002R
ULQ2003R
ULQ2004R

SEVEN DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500mA PER DRIVER (600mA PEAK)
- OUTPUT VOLTAGE 50V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

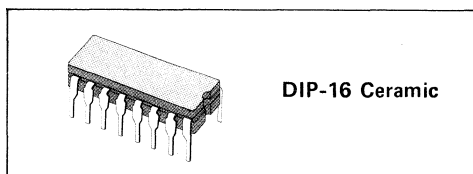
The ULQ2001R, ULQ2002R, ULQ2003R and ULQ2004R are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500mA and can withstand peak currents of 600mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

The four versions interface to all common logic families.

ULQ2001R	General purpose, DTL, TTL, CMOS
ULQ2002R	14-25V PMOS
ULQ2003R	5V TTL, CMOS
ULQ2004R	6-15V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays, filament lamps, thermal printheads and high power buffers.

The ULQ2001R, ULQ2002R, ULQ2003R and ULQ2004R are supplied in 16 pin ceramic DIP packages.



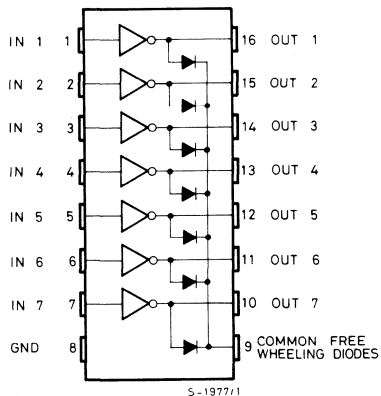
ABSOLUTE MAXIMUM RATINGS

V_o	Output voltage	50	V
V_{in}	Input voltage (for ULQ2002R/2003R/2004R)	30	V
I_c	Continuous collector current	500	mA
I_b	Continuous base current	25	mA
T_{amb}	Operating ambient temperature range	-20 to + 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

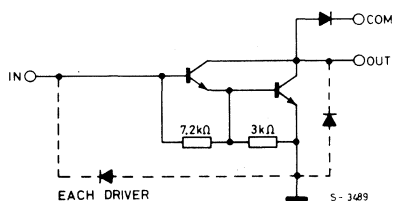


ULQ2001R
ULQ2002R
ULQ2003R
ULQ2004R

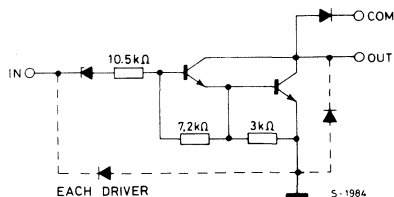
CONNECTION DIAGRAM



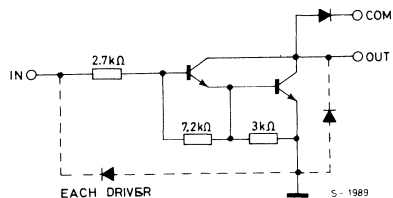
SCHEMATIC DIAGRAM



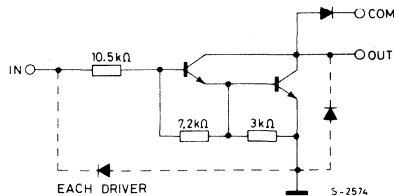
Series ULQ2001R
(each driver)



Series ULQ2002R
(each driver)



Series ULQ2003R
(each driver)



Series ULQ2004R
(each driver)

THERMAL DATA

$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	150	$^{\circ}\text{C/W}$
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ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX} Output leakage current	$V_{CE} = 50\text{V}$ $T_{amb} = 70^{\circ}\text{C}$ $T_{amb} = 70^{\circ}\text{C}$ for ULQ2002R $V_{CE} = 50\text{V}$ for ULQ2004R $V_{CE} = 50\text{V}$			50	μA	1a
	$V_{CE} = 50\text{V}$			100	μA	1a
	$V_i = 6\text{V}$			500	μA	1b
	$V_i = 1\text{V}$			500	μA	1b
$V_{CE(sat)}$ Collector-emitter saturation voltage	$I_C = 100\text{mA}$		0.9	1.1	V	2
	$I_B = 250\mu\text{A}$		1.1	1.3	V	2
	$I_C = 200\text{mA}$ $I_B = 350\mu\text{A}$ $I_C = 350\text{mA}$ $I_B = 500\mu\text{A}$		1.3	1.6	V	2
$I_{i(on)}$ Input current	for ULQ2002R for ULQ2003R for ULQ2004R $V_i = 12\text{V}$		$V_i = 17\text{V}$ $V_i = 3.85\text{V}$ $V_i = 5\text{V}$	1.25 1.35 0.5 1.45	mA mA mA mA	3 3 3 3
				0.82 0.93 0.35 1		
$I_{i(off)}$ Input current	$T_{amb} = 70^{\circ}\text{C}$ $I_C = 500\mu\text{A}$	50	65		μA	4
$V_{i(on)}$ Input voltage	for ULQ2002R $V_{CE} = 2\text{V}$ for ULQ2003R $V_{CE} = 2\text{V}$ $V_{CE} = 2\text{V}$ $V_{CE} = 2\text{V}$ for ULQ2004R $V_{CE} = 2\text{V}$ $V_{CE} = 2\text{V}$ $V_{CE} = 2\text{V}$ $V_{CE} = 2\text{V}$			13	V	5
	$I_C = 300\text{mA}$					
	$I_C = 200\text{mA}$			2.4	V	5
	$I_C = 250\text{mA}$			2.7	V	5
	$I_C = 300\text{mA}$			3	V	5
	$I_C = 125\text{mA}$			5	V	5
	$I_C = 200\text{mA}$			6	V	5
	$I_C = 275\text{mA}$ $I_C = 350\text{mA}$			7 8	V V	5 5
h_{FE} DC forward current gain	for ULQ2001R $V_{CE} = 2\text{V}$ $I_C = 350\text{mA}$	1000			—	2
C_i Input capacitance			15	25	pF	—
t_{PLH} Turn-on delay time	$0.5 V_i$ to $0.5 V_o$		0.25	1	μs	—
t_{PHL} Turn-off delay time	$0.5 V_i$ to $0.5 V_o$		0.25	1	μs	—
I_R Clamp diode leakage current	$V_R = 50\text{V}$ $T_{amb} = 70^{\circ}\text{C}$			50	μA	6
	$V_R = 50\text{V}$			100	μA	6
V_F Clamp diode forward voltage	$I_F = 350\text{mA}$		1.7	2	V	7

TEST CIRCUITS

Fig. 1a

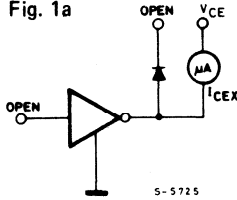


Fig. 1b

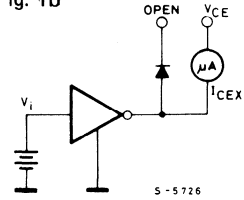


Fig. 2

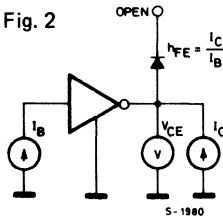


Fig. 3

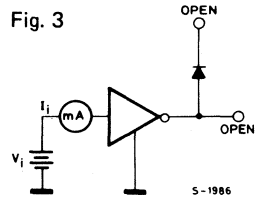


Fig. 4

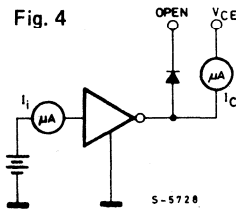


Fig. 5

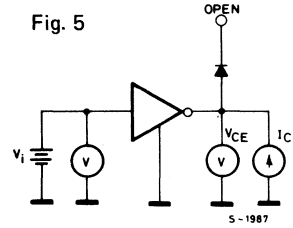


Fig. 6

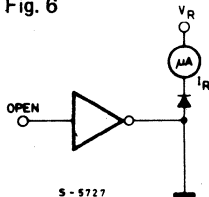
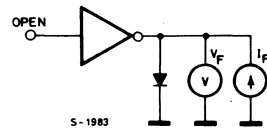


Fig. 7





VB010

ADVANCE DATA

A MONOLITHIC HIGH VOLTAGE DARLINGTON WITH ON-CHIP INTELLIGENCE FOR PROTECTION AND DIAGNOSTIC OUTPUT

- CONTROL CIRCUIT AND POWER ON ONE CHIP
- 10A OUTPUT CURRENT
- INTEGRATED 400V POWER DARLINGTON
- PROGRAMMABLE BASE CURRENT
- SHORT CIRCUIT PROTECTION
- DIRECT SOA PROTECTION
- THERMAL SHUTDOWN
- DIAGNOSTIC OUTPUT
- TTL/CMOS COMPATIBLE INPUT
- STAND BY MODE

The VB010 is a fully protected high voltage darlington with a TTL/CMOS compatible driving circuit.

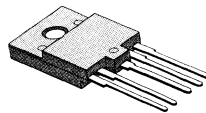
Features of the device include programmable base current, thermal shutdown, short circuit protection, a combined voltage and current detection circuit for direct SOA protection and a diagnostic output.

The VB010 is mounted in the fully isolated ISOWATT5 package and needs no external components.

The VB010 can be used in numerous applications which require an intelligent high voltage, high current power switch driven by a logic level input. The base current is externally programmed by a resistor on the control circuit supply.

A series of built-in protection circuits switch-off the power darlington before safe operating levels are exceeded.

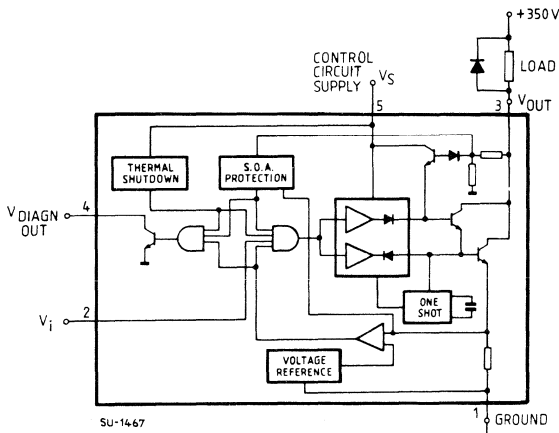
VIpower™ Technology



ISOWATT5

ORDERING NUMBER: VB010

BLOCK DIAGRAM



**VB010****ABSOLUTE MAXIMUM RATINGS**

V_{CC}	Supply voltage	450	V
V_S	Control circuit supply voltage	18	V
V_{IN}	Input voltage	18	V
I_C	Collector current (Power stage)	15	A
I_S	Supply current (Control stage)	200	mA
P_{tot}	Power dissipation	internally limited	
T_J	Junction operating temperature	-45 to 150	°C
T_{stg}	Storage temperature	-40 to 150	°C

THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max	2.5	°C/W
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FURTHER INFORMATION ABOUT THIS PRODUCT IS AVAILABLE ON REQUEST.



VB100

ADVANCE DATA

AN INTELLIGENT HIGH VOLTAGE DUTY CYCLE CONTROLLER FOR D.C. MOTOR CONTROL AND INDUCTIVE LOAD DRIVER APPLICATIONS

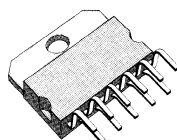
- CONTROL CIRCUIT AND POWER ON ONE CHIP
- 3A OUTPUT CURRENT
- INTEGRATED 450V POWER DARLINGTON
- PROGRAMMABLE DRIVER CURRENT
- SWITCHING FREQUENCY UP TO 100KHz
- THERMAL SHUTDOWN
- COMPARATOR INPUT PROTECTION
- HIGH IMPEDANCE DIFFERENTIAL INPUTS
- DUTY CYCLE CONTROL LINEARITY WITHIN 1.5%
- MINIMUM EXTERNAL COMPONENTS

The VB100 is mounted in a 11-lead Multiwatt[®] plastic power package and requires very few external components.

The VB100 can be used as a D.C. motor controller and driver or as a high voltage inductive load driver, the output voltage duty cycle is adjusted as a function of the input control voltage, at a frequency set by a stable internal sawtooth generator.

A built-in thermal shutdown circuit switches off the power darlington whenever the junction temperature exceeds an internally set value.

VIpower™ Technology



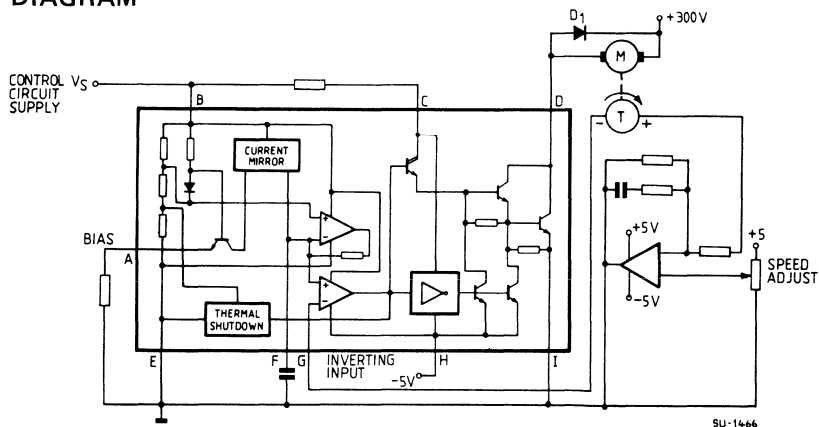
Multiwatt-11[®]

ORDERING NUMBER: VB100

The VB100 is an intelligent duty cycle controller with a high voltage, high current open collector darlington output.

Features of the device include programmable driver current, thermal protection, high impedance differential input, integrated protection at comparator inputs and switching frequency up to 100KHz.

BLOCK DIAGRAM



**VB100****ABSOLUTE MAXIMUM RATINGS**

V_{CC}	Supply voltage	450	V
V_S	Control circuit supply voltage	18	V
V_{IN}	Input voltage	18	V
I_C	Collector current (Power stage)	10	A
I_S	Supply current (Control stage)	200	mA
P_{tot}	Power dissipation	internally limited	
T_j	Junction operating temperature	-45 to 150	°C
T_{stg}	Storage temperature	-40 to 150	°C

THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max	2.5	°C/W
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FURTHER INFORMATION ABOUT THIS PRODUCT IS AVAILABLE ON REQUEST.



**BUR50
BUR50S**

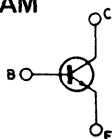
HIGH CURRENT, HIGH SPEED, HIGH POWER TRANSISTOR

The BUR50 is a silicon multi-epitaxial planar NPN transistor in modified Jedec TO-3 metal case, the BUR50S is the same type in Jedec TO-3 metal case, intended for use, in switching and linear applications in military and industrial equipment.

ABSOLUTE MAXIMUM RATINGS

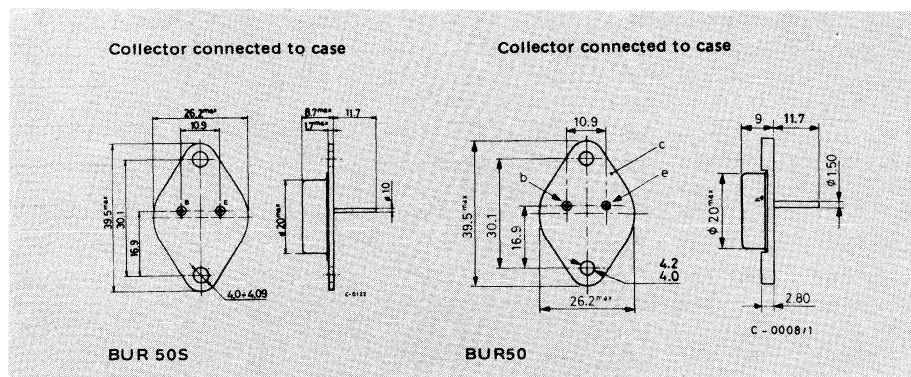
V_{CBO}	Collector-base voltage ($I_E = 0$)	200	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	125	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	10	V
I_C	Collector current	70	A
I_{CM}	Collector peak current ($t_p = 10$ ms)	100	A
I_B	Base current	20	A
P_{tot}	Total power dissipation at $T_{case} \leq 25^\circ\text{C}$	350	W
T_{stg}	Storage temperature	-65 to 200	$^\circ\text{C}$
T_j	Junction temperature	200	$^\circ\text{C}$

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max 0.5 °C/W
------------------	----------------------------------	--------------

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

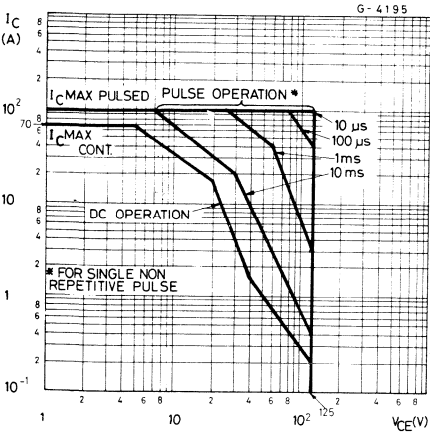
Parameter	Test conditions	Min. Typ. Max.	Unit
I_{CBO} Collector cutoff current ($I_E = 0$)	$V_{CB} = 200V$ $V_{CB} = 200V$ $T_{case} = 125^{\circ}C$	0.2 2	mA mA
I_{CEO} Collector cutoff current ($I_B = 0$)	$V_{CE} = 125V$	1	mA
I_{EBO} Emitter cutoff current ($I_C = 0$)	$V_{EB} = 7V$	0.2	mA
$V_{CEO(sus)}$ *Collector-emitter sustaining voltage	$I_C = 200mA$	125	V
V_{EBO} Emitter-base voltage ($I_C = 0$)	$I_E = 10mA$	10	V
$V_{CE(sat)}$ * Collector-emitter saturation voltage	$I_C = 35A$ $I_B = 2A$ $I_C = 70A$ $I_B = 7A$	1 0.8 1.5	V V
$V_{BE(sat)}$ * Base-emitter saturation voltage	$I_C = 35A$ $I_B = 2A$ $I_C = 70A$ $I_B = 7A$	1.8 1.6 2	V V
h_{FE} * DC current gain	$I_C = 5A$ $V_{CE} = 4V$ $I_C = 50A$ $V_{CE} = 4V$	20 100 15	— —
$I_{s/b}$ Second breakdown collector current	$V_{CE} = 20V$ $t = 1s$	17.5	A
f_T Transition frequency	$I_C = 1A$ $V_{CE} = 5V$ $f = 1MHz$	10 16	MHz

ELECTRICAL CHARACTERISTICS (continued)

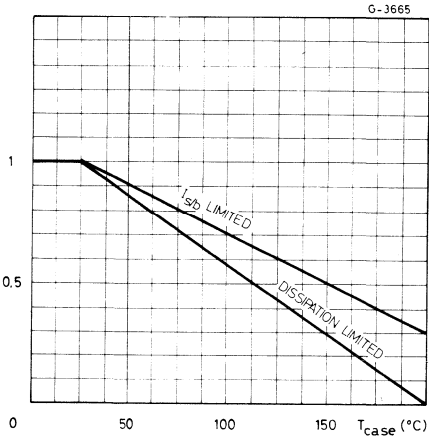
Parameter		Test conditions		Min. Typ. Max.	Unit
t _{on}	Turn-on time (fig. 2)	I _C =70A V _{CC} =60V	I _{B1} =7A	0.5 1.2	μs
t _s	Storage time (fig. 2)	I _C =70A I _{B2} =-7A	I _{B1} =7A V _{CC} =60V	0.82 2	μs
t _f	Fall time (fig. 2)			0.1 0.5	μs
Clamped E _{s/b} Collector current (fig. 1)		V _{clamp} =125V L =500μH		70	A

* Pulsed: pulse duration = 300 μs , duty cycle $\leq 2\%$

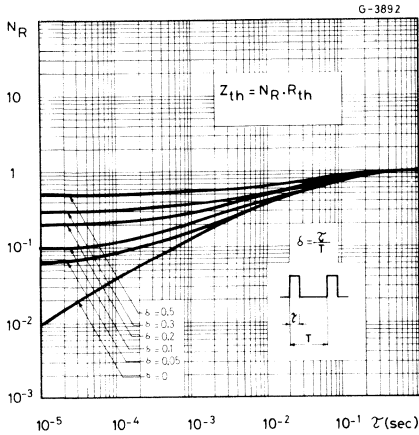
Safe operating areas



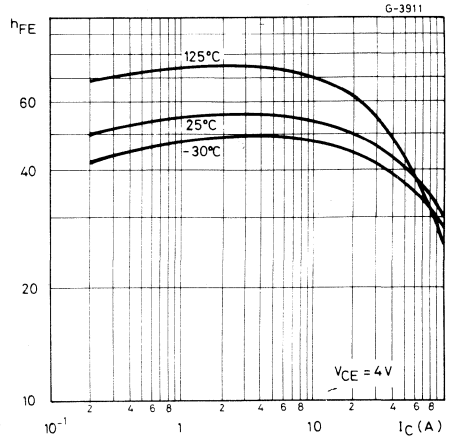
Derating curves



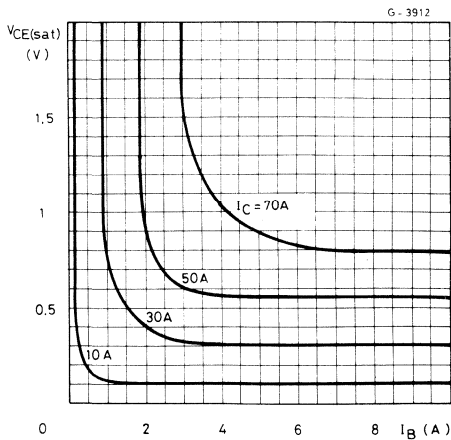
Thermal transient response



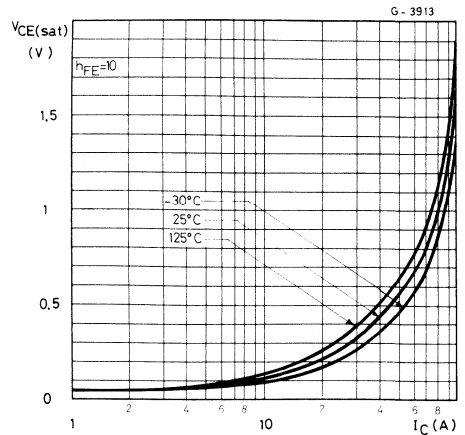
DC current gain



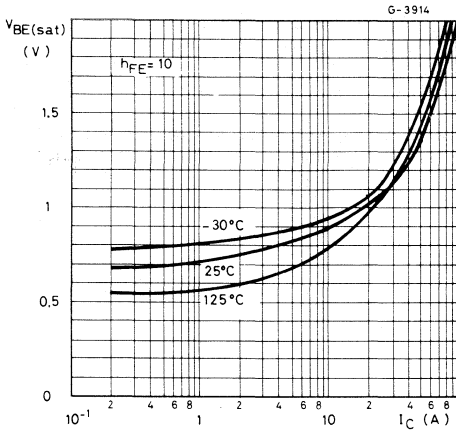
Collector-emitter saturation voltage



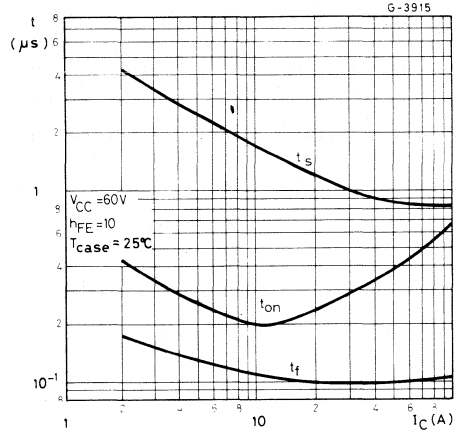
Collector-emitter saturation voltage



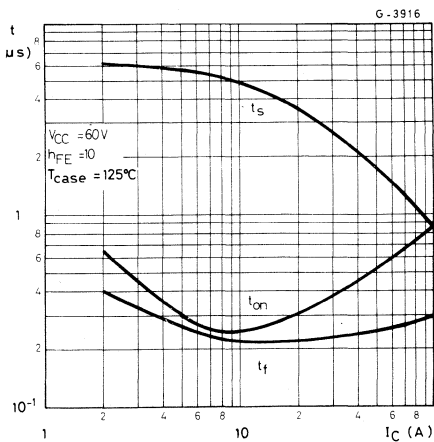
Base-emitter saturation voltage



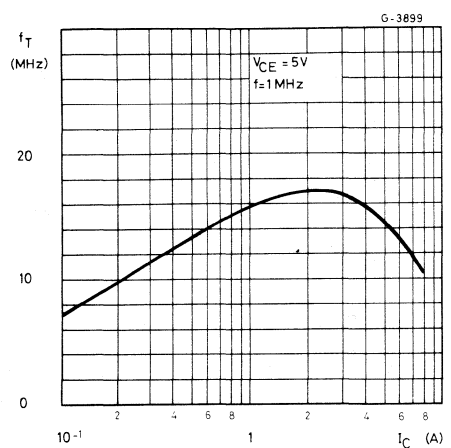
Saturated switching characteristics



Saturated switching characteristics



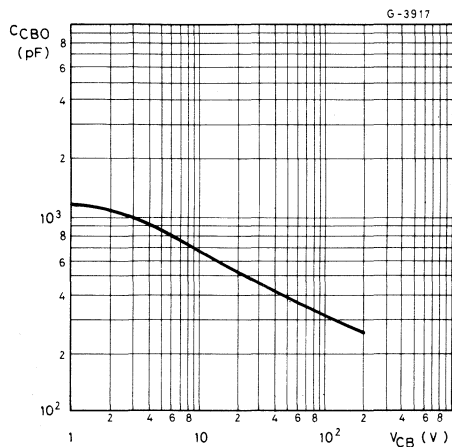
Transition frequency





BUR50
BUR50S

Collector-base capacitance



Clamped reverse bias safe operating areas

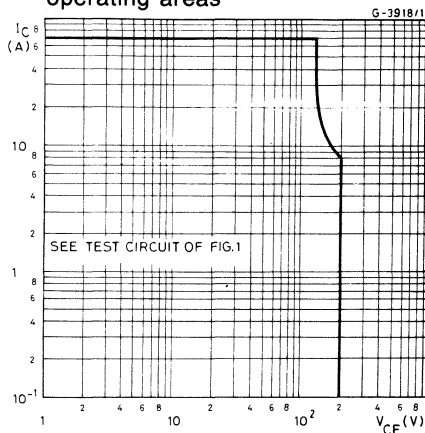


Fig. 1 — Clamped $E_{s/b}$ test circuit

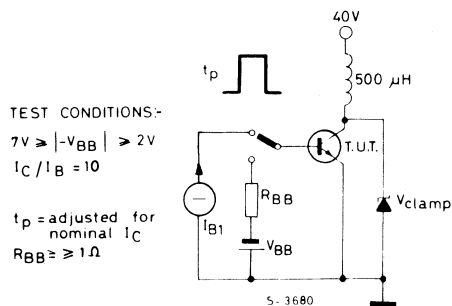
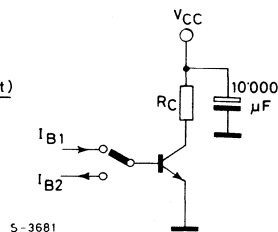


Fig. 2 — Switching times test circuit (resistive load)

TEST CONDITIONS:
 $V_{CC} = 60V$
 $R_C = \frac{V_{CC} - V_{CE(sat)}}{I_C}$
 INPUT PULSE
 pulse width = $10\mu s$
 $t_r, t_f \leq 50ns$
 duty cycle = 1%





BUR51

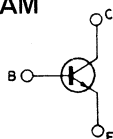
HIGH CURRENT, HIGH SPEED, HIGH POWER TRANSISTOR

The BUR 51 is a silicon multiepitaxial planar NPN transistor in modified Jedec TO-3 metal case, intended for use in switching and linear applications in military and industrial equipment.

ABSOLUTE MAXIMUM RATINGS

V_{CBO}	Collector-base voltage ($I_E = 0$)	300	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	200	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	10	V
I_C	Collector current	60	A
I_{CM}	Collector peak current ($t_p = 10$ ms)	80	A
I_B	Base current	16	A
P_{tot}	Total power dissipation at $T_{case} \leq 25^\circ\text{C}$	350	W
T_{stg}	Storage temperature	-65 to 200	$^\circ\text{C}$
T_j	Junction temperature	200	$^\circ\text{C}$

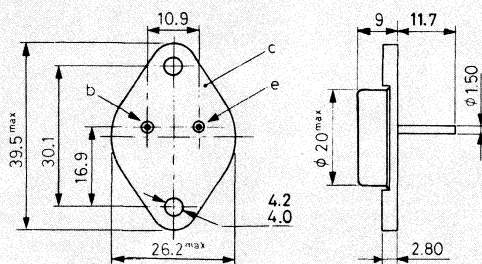
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Collector connected to case



C - 0008 / 1

Modified TO-3



BUR51

THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max	0.5	$^{\circ}C/W$
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ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

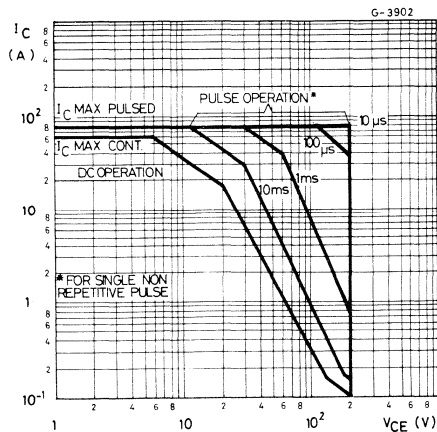
Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CBO} Collector cutoff current ($I_E = 0$)	$V_{CB} = 300V$ $V_{CB} = 300V$ $T_{case} = 125^{\circ}C$		0.2	2	mA
I_{CEO} Collector cutoff current ($I_B = 0$)	$V_{CE} = 200V$		1		mA
I_{EBO} Emitter cutoff current ($I_C = 0$)	$V_{EB} = 7V$		0.2		mA
$V_{CEO(sus)}$ *Collector-emitter sustaining voltage	$I_C = 200mA$	200			V
V_{EBO} Emitter-base voltage ($I_C = 0$)	$I_E = 10mA$	10			V
$V_{CE(sat)}$ * Collector-emitter saturation voltage	$I_C = 30A$ $I_B = 2A$ $I_C = 50A$ $I_B = 5A$		0.9	1.5	V
$V_{BE(sat)}$ * Base-emitter saturation voltage	$I_C = 30A$ $I_B = 2A$ $I_C = 50A$ $I_B = 5A$		1.55	1.8	V
h_{FE} * DC current gain	$I_C = 5A$ $V_{CE} = 4V$ $I_C = 50A$ $V_{CE} = 4V$	20		100	—
$I_{s/b}$ Second breakdown collector current	$V_{CE} = 20V$ $t = 1s$	17.5			A
f_T Transition frequency	$I_C = 1A$ $V_{CE} = 5V$ $f = 1MHz$	10	16		MHz

ELECTRICAL CHARACTERISTICS (continued)

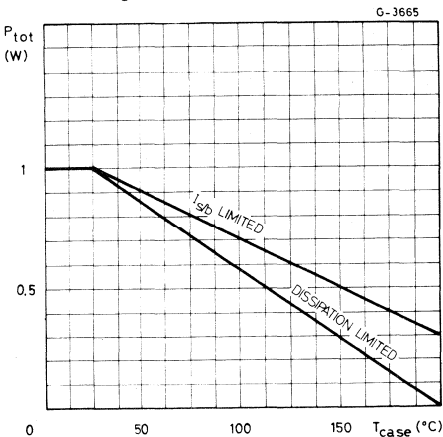
Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{on} Turn-on time (fig. 2)	$I_C = 50A$ $I_{B1} = 5A$ $V_{CC} = 100V$	0.35		1	μs
t_s Storage time (fig. 2)	$I_C = 50A$ $I_{B1} = 5A$ $I_{B2} = -5A$ $V_{CC} = 100V$	0.9		2	μs
t_f Fall time (fig. 2)		0.24		0.6	μs
Clamped $E_{s/b}$ Collector current (fig. 1)	$V_{clamp} = 200V$ $L = 500\mu H$	50			A

* Pulsed: pulse duration =300 μs , duty cycle $\leq 2\%$

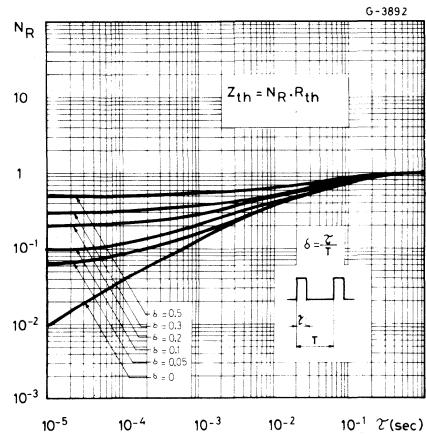
Safe operating areas



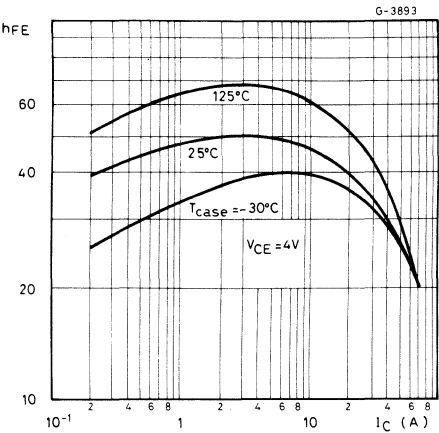
Derating curves



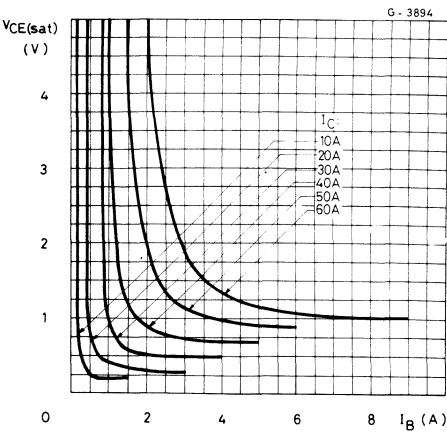
Thermal transient response



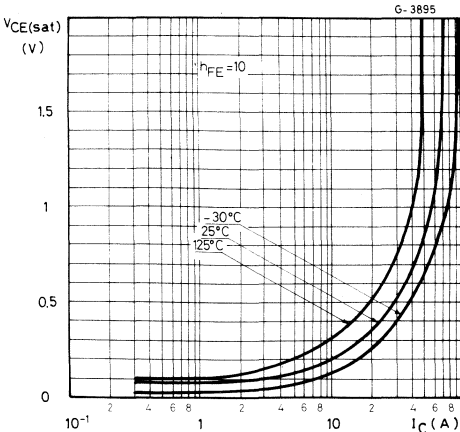
DC current gain



Collector-emitter saturation voltage



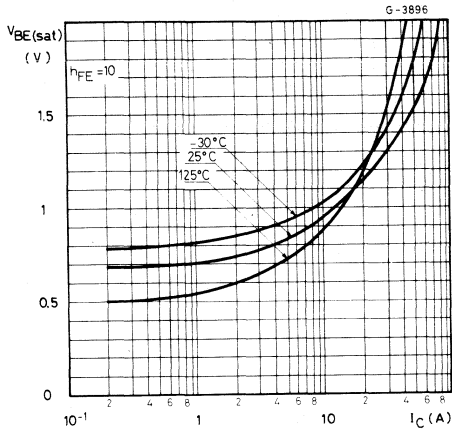
Collector-emitter saturation voltage



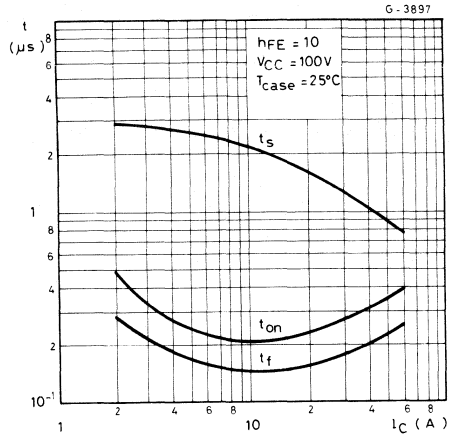


BUR51

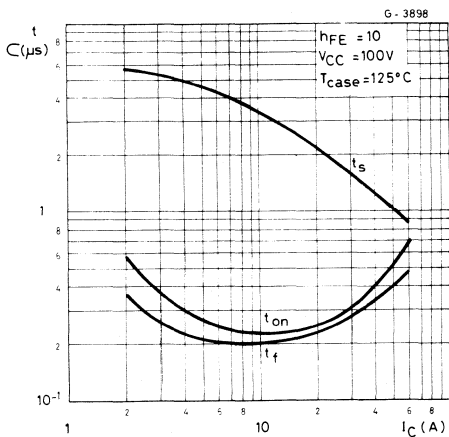
Base-emitter saturation voltage



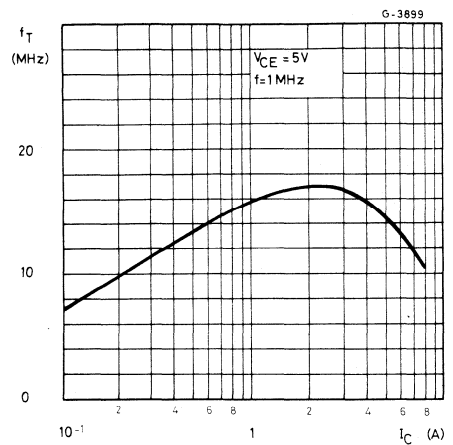
Saturated switching characteristics



Saturated switching characteristics



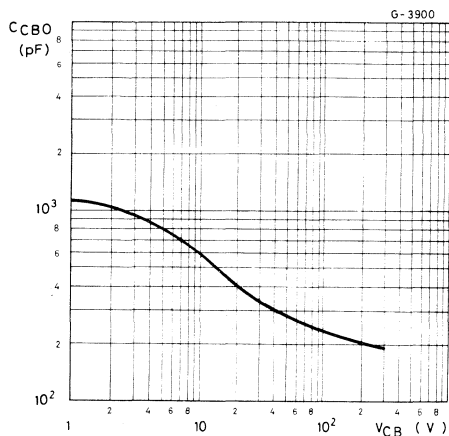
Transition frequency





BUR51

Collector-base capacitance



Clamped reverse bias safe operating areas

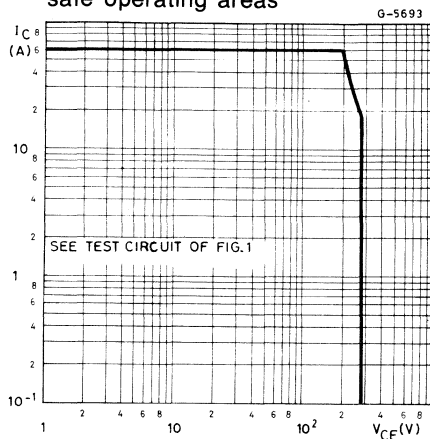


Fig. 1 — Clamped $E_{s/b}$ test circuit

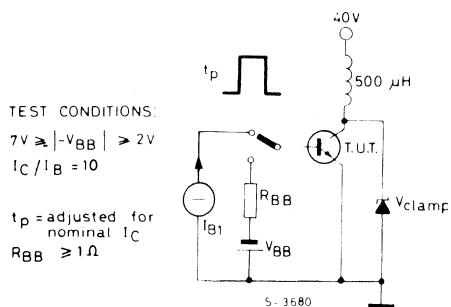


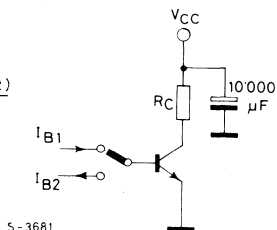
Fig. 2 — Switching times test circuit (resistive load)

TEST CONDITIONS:

$V_{CC} = 100V$

$$R_C = \frac{V_{CC} - V_{CE(sat)}}{I_C}$$

INPUT PULSE
 pulse width = 10 μs
 $t_r, t_f \leq 50ns$
 duty cycle $\approx 1\%$





BUR52

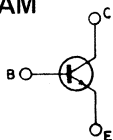
HIGH CURRENT, HIGH SPEED, HIGH POWER TRANSISTOR

The BUR 52 is a silicon multiepitaxial planar NPN transistor in modified Jødec TO-3 metal case, intended for use in switching and linear applications in military and industrial equipment.

ABSOLUTE MAXIMUM RATINGS

V_{CBO}	Collector-base voltage ($I_E = 0$)	350	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	250	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	10	V
I_C	Collector current	60	A
I_{CM}	Collector peak current ($t_p = 10$ ms)	80	A
I_B	Base current	16	A
P_{tot}	Total power dissipation at $T_{case} \leq 25^\circ C$	350	W
T_{stg}	Storage temperature	-65 to 200	$^\circ C$
T_j	Junction temperature	200	$^\circ C$

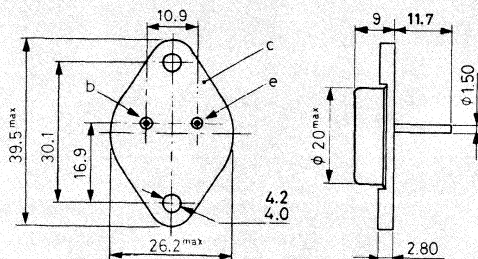
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Collector connected to case



C - 0008 / 1

Modified TO-3

**BUR52****THERMAL DATA**

$R_{th\ j-case}$	Thermal resistance junction-case	max	0.5	°C/W
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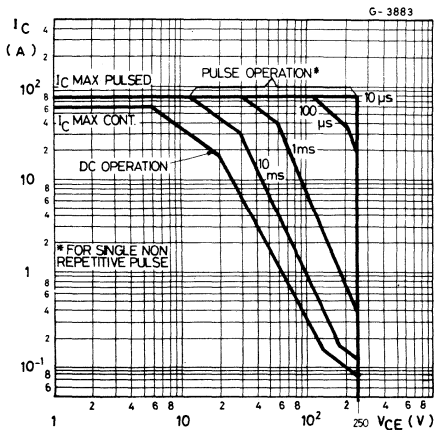
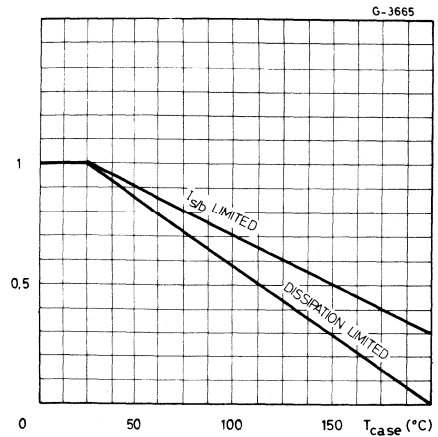
ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CBO} Collector cutoff current ($I_E = 0$)	$V_{CB} = 350\text{V}$ $V_{CB} = 350\text{V}$ $T_{case} = 125^{\circ}\text{C}$		0.2	2	mA mA
I_{CEO} Collector cutoff current ($I_B = 0$)	$V_{CE} = 250\text{V}$		1		mA
I_{EBO} Emitter cutoff current ($I_C = 0$)	$V_{EB} = 7\text{V}$		0.2		mA
$V_{CEO(sus)}$ *Collector-emitter sustaining voltage	$I_C = 200\text{mA}$	250			V
V_{EBO} Emitter-base voltage ($I_C = 0$)	$I_E = 10\text{mA}$	10			V
$V_{CE(sat)}$ * Collector-emitter saturation voltage	$I_C = 25\text{A}$ $I_B = 2\text{A}$ $I_C = 40\text{A}$ $I_B = 4\text{A}$		1	0.70 1.5	V V
$V_{BE(sat)}$ * Base-emitter saturation voltage	$I_C = 25\text{A}$ $I_B = 2\text{A}$ $I_C = 40\text{A}$ $I_B = 4\text{A}$		1.8	1.5 2	V V
h_{FE} * DC current gain	$I_C = 5\text{A}$ $V_{CE} = 4\text{V}$ $I_C = 40\text{A}$ $V_{CE} = 4\text{V}$	20		100	— —
$I_{s/b}$ Second breakdown collector current	$V_{CE} = 20\text{V}$ $t = 1\text{s}$	17.5			A
f_T Transition frequency	$I_C = 1\text{A}$ $V_{CE} = 5\text{V}$ $f = 1\text{MHz}$	10	16		MHz
t_{on} Turn-on time (fig. 2)	$I_C = 40\text{A}$ $I_{B1} = 4\text{A}$ $V_{CC} = 100\text{V}$	0.3	1		μs

**BUR52****ELECTRICAL CHARACTERISTICS** (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_s Storage time (fig. 2)	$I_C = 40A$ $I_{B1} = 4A$ $I_{B2} = -4A$ $V_{CC} = 100V$	1.2		2	μs
t_f Fall time (fig. 2)		0.20		0.6	μs
Clamped $E_{s/b}$ Collector current (fig. 1)	$V_{clamp} = 250V$ $L = 500\mu H$	40			A

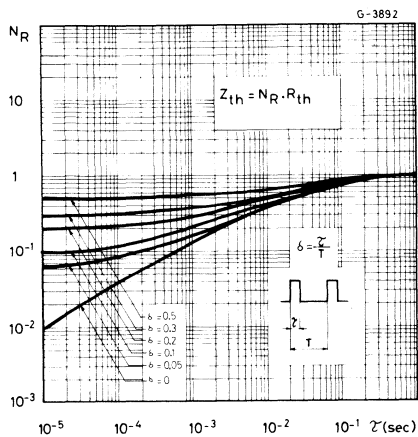
* Pulsed: pulse duration = 300 μs , duty cycle $\leq 2\%$

Safe operating areas**Derating curves**

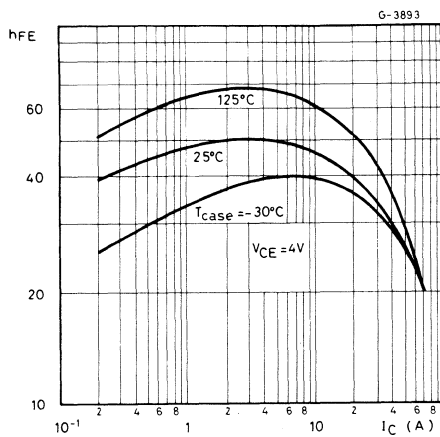


BUR52

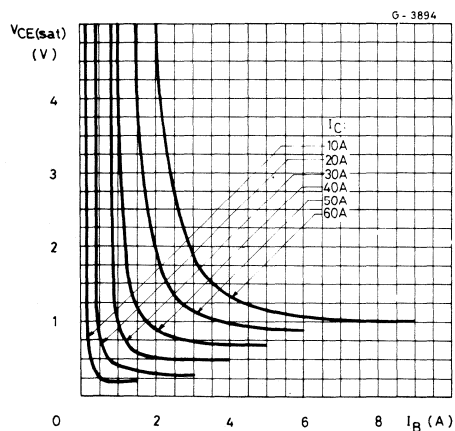
Thermal transient response



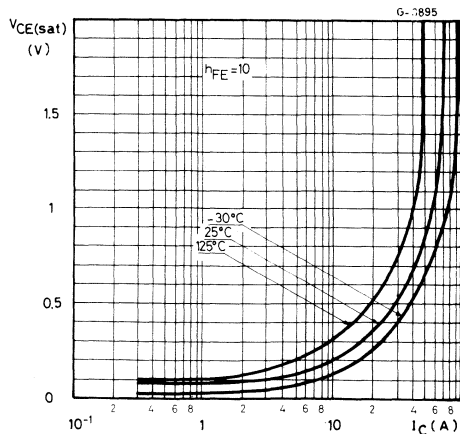
DC current gain

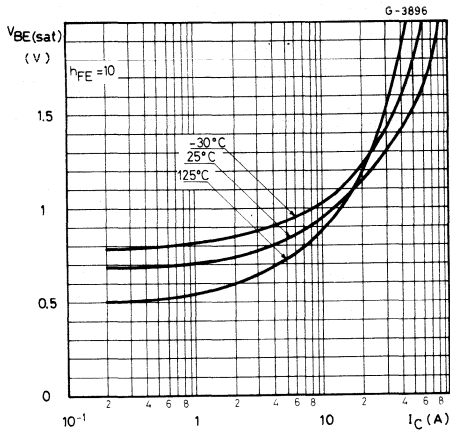
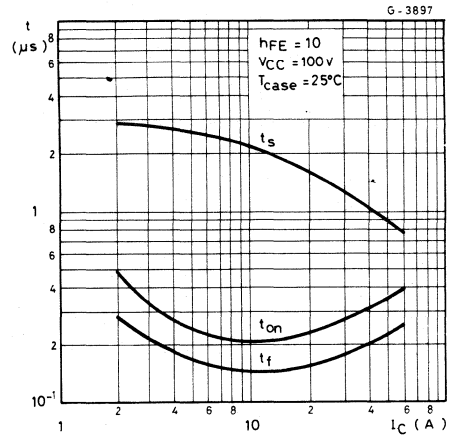
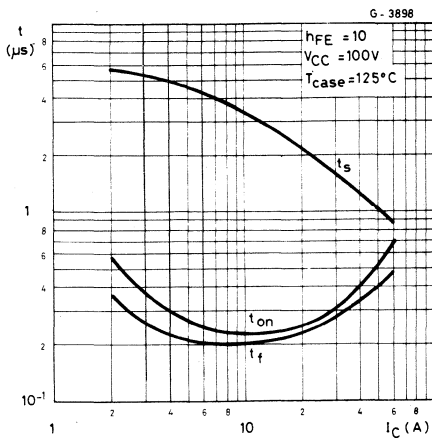
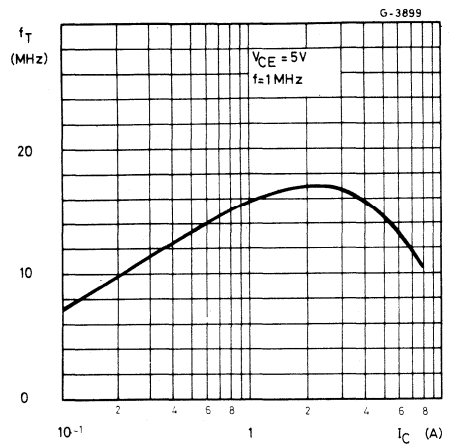


Collector-emitter saturation voltage



Collector-emitter saturation voltage

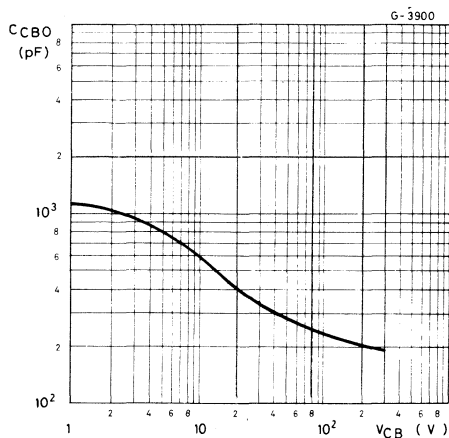


**BUR52****Base-emitter saturation voltage****Saturated switching characteristics****Saturated switching characteristics****Transition frequency**



BUR52

Collector-base capacitance



Clamped reverse bias safe operating areas

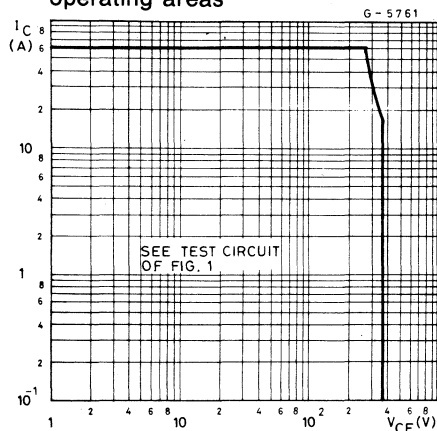


Fig. 1 — Clamped $E_{s,b}$ test circuit

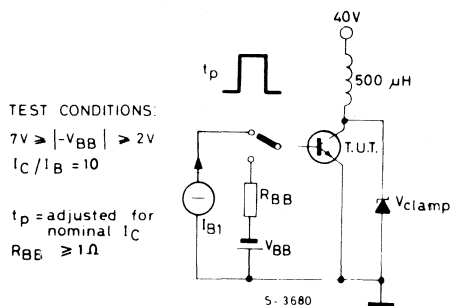


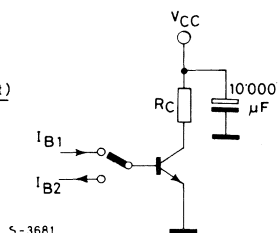
Fig. 2 — Switching times test circuit (resistive load)

TEST CONDITIONS:

$V_{CC} = 100V$

$$R_C = \frac{V_{CC} - V_{CE(sat)}}{I_C}$$

INPUT PULSE
 pulse width = $10\mu s$
 $t_r, t_f \leq 50ns$
 duty cycle = 1%





BUW22
BUW22A
BUW22AP
BUW22P

ADVANCE DATA

ADVANCE DATA

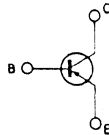
HIGH VOLTAGE POWER SWITCH

The BUW22, BUW22A are silicon multiepitaxial mesa PNP transistor, in Jedec TO-3, metal case, particularly intended for high voltage, fast switching applications.
The BUW22P, BUW22AP are mounted in TO-220 plastic package.

ABSOLUTE MAXIMUM RATINGS

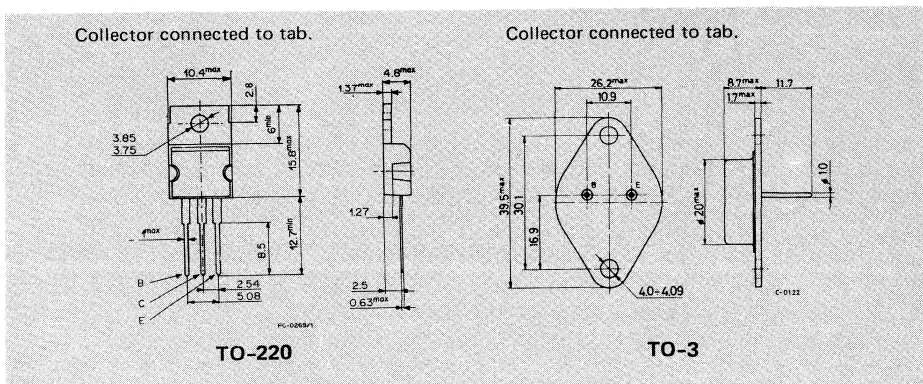
		BUW22/P	BUW22A/P
V_{CES}	Collector-emitter voltage ($V_{BE} = 0$)	-400V	-450V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	-350V	-400V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	-5V	-7V
I_C	Collector current	-6A	
I_{CM}	Collector peak current ($t_p \leq 10ms$)	-8A	
I_B	Base current	-2A	
I_{BM}	Base peak current ($t_p \leq 10ms$)	-4A	
P_{tot}	Total power dissipation at $T_{case} \leq 25^\circ C$	(TO-3) 75W	(TO-220) 60W
T_{stg}	Storage temperature	-65 to $175^\circ C$	-65 to $150^\circ C$
T_j	Junction temperature	$175^\circ C$	$150^\circ C$

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.



THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max	2	$^{\circ}C/W$
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ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

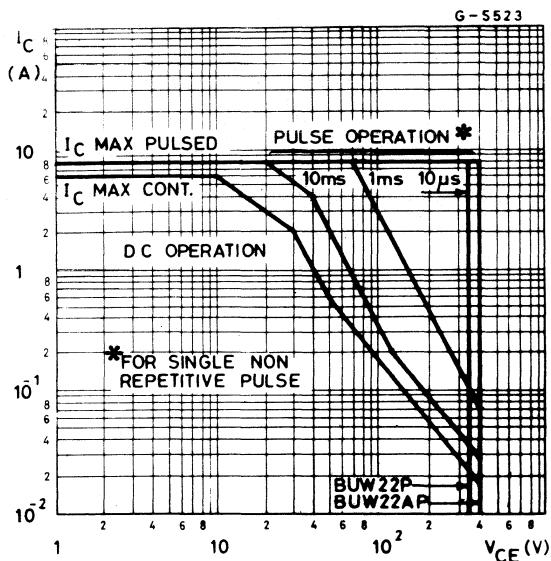
Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector cutoff current ($V_{BE} = 0$)			-1	mA
	$V_{CE} = \text{Rated } V_{CES}$ $T_{case} = 125^{\circ}C$ $V_{CE} = \text{Rated } V_{CES}$			-5	mA
I_{EBO}	Collector cutoff Current ($I_C = 0$)			-1	mA
$V_{CEO(sus)}^*$	Collector-emitter sustaining voltage ($I_B = 0$)				
	$I_C = -100mA$ for BUW22/P for BUW22A/P	-350			V
		-400			V
$V_{CE(sat)}^*$	Base-emitter saturation voltage			-1.5	V
	$I_C = -2.5A$ $I_B = -1A$				
$V_{BE(sat)}^*$	Base-emitter saturation voltage			-1.6	V
	$I_C = -2.5A$ $I_B = -1A$				
h_{FE}^*	DC current gain			12	—
	$I_C = 0.5A$ $V_{CE} = -5V$				
$I_{s/b}$	Second breakdown collector current				
	$V_{CE} = -30V$ for BUW22/A for BUW22P/AP	-2.5			A
		-2			A
t_{on}	Turn-on time		0.4	0.8	μs
	Resistive load $V_{CC} = -250V$				
t_s	Storage time		0.6	1.5	μs
	$I_C = -2.5A$				
t_f	Fall time		0.3	0.7	μs
	$I_{B1} = -I_{B2} = -0.5A$				

* Pulsed: pulse duration = $300\mu s$, duty cycle = 1.5%

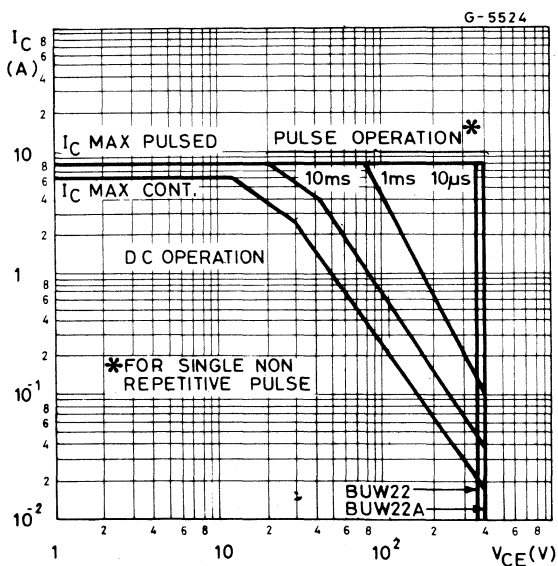


BUW22
BUW22A
BUW22AP
BUW22P

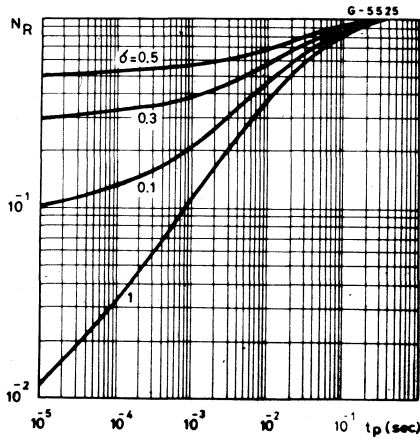
Safe operating areas
(BUW22AP - BUW22P)



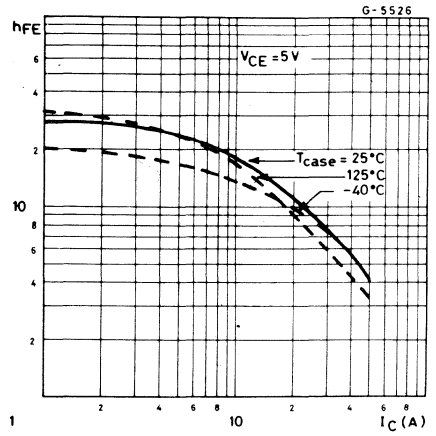
Safe operating areas
(BUW22 - BUW22A)



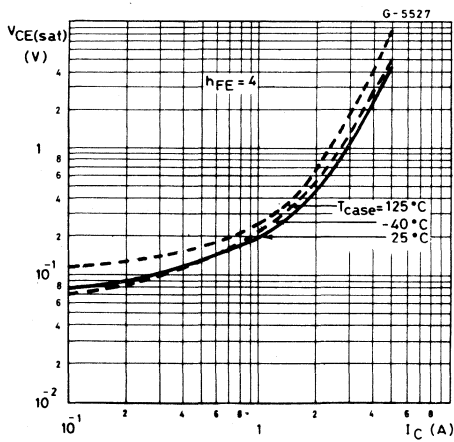
Transient thermal response



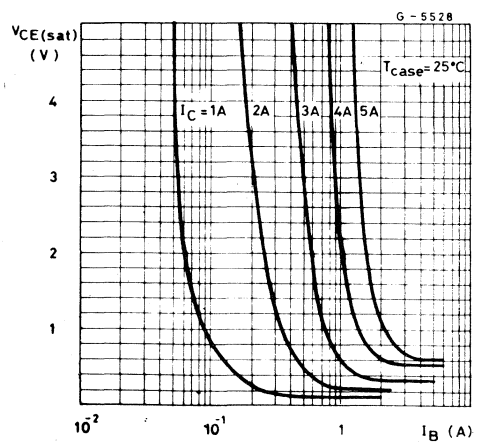
DC current gain



Collector-emitter saturation voltage



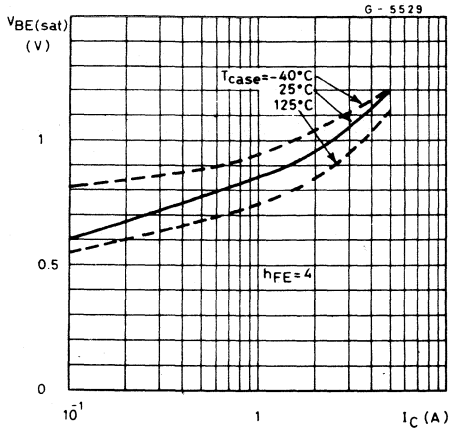
Collector-emitter saturation voltage



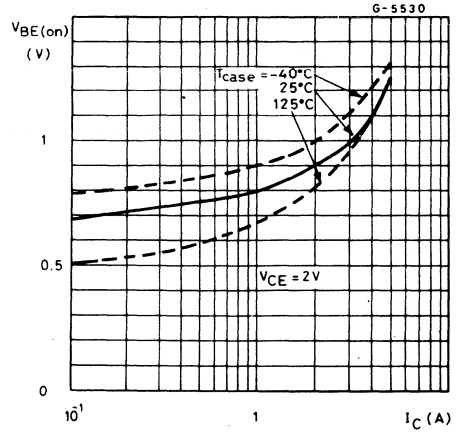


BUW22
BUW22A
BUW22AP
BUW22P

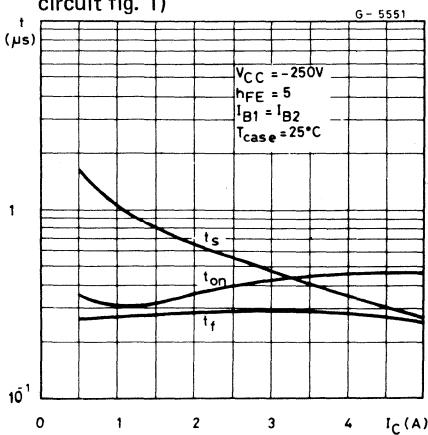
Base-emitter saturation voltage



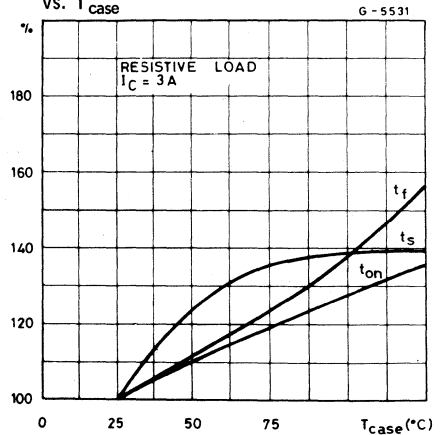
Base-emitter on voltage



Switching times resistive load (test circuit fig. 1)



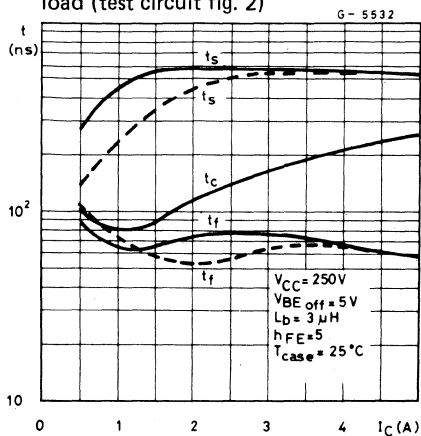
Switching times percentage variation vs. T_{case}



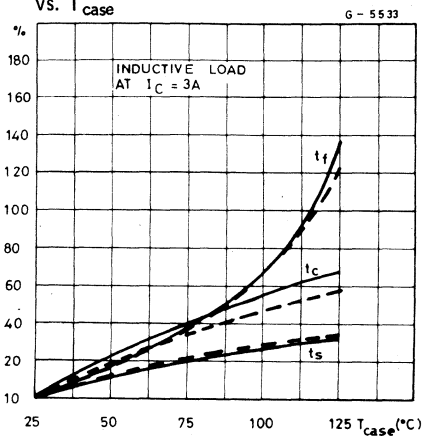


BUW22
BUW22A
BUW22AP
BUW22P

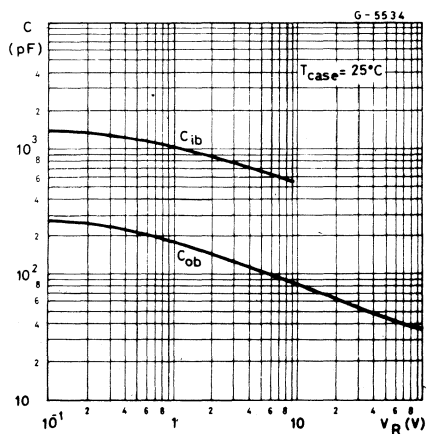
Turn off switching times inductive load (test circuit fig. 2)



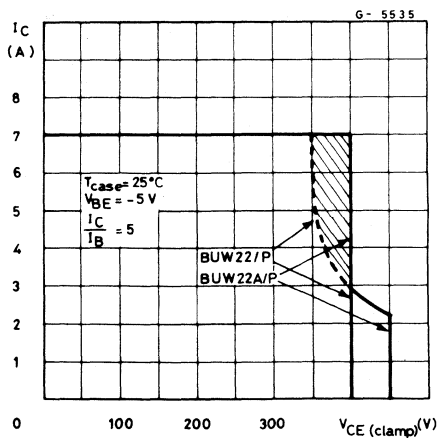
Switching times percentage variation vs. T_{case}



Capacitance



Reserve biased safe operating area



TEST CIRCUITS

Fig. 1

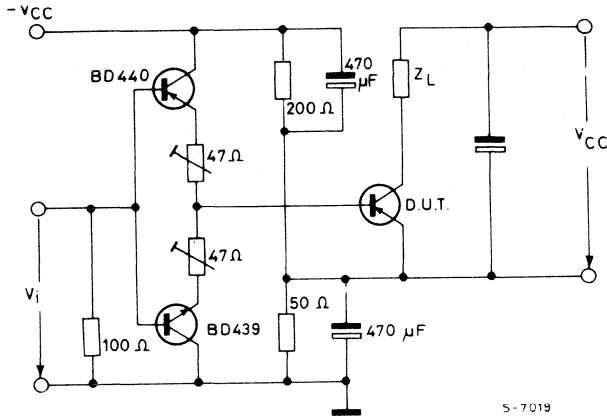
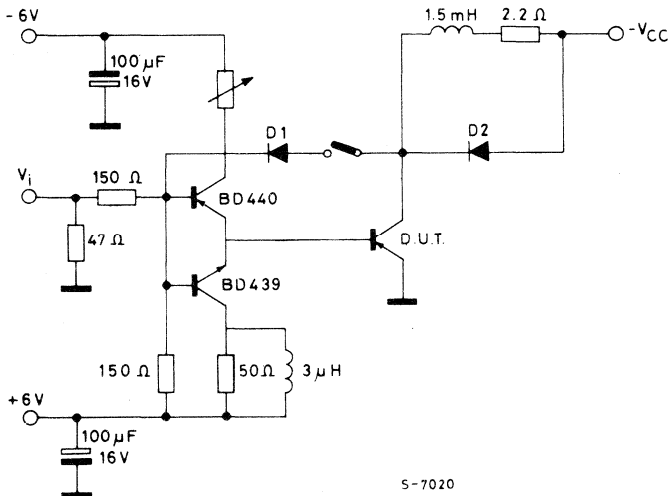


Fig. 2



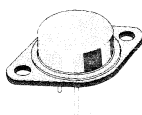


**BUW32/BUW32A
BUW32P/BUW32AP
SGSIW32/SGSIW32A**

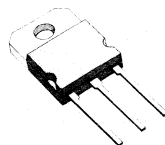
HIGH VOLTAGE POWER SWITCH

- FAST SWITCHING APPLICATIONS
- INDUSTRIAL APPLICATION

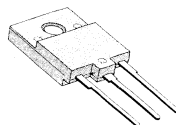
The BUW32/A, BUW32P/AP and SGSIW32/A are silicon multiepitaxial mesa PNP transistors mounted respectively in TO-3 metal case, SOT-93 plastic package and ISOWATT218 fully isolated package.



TO-3

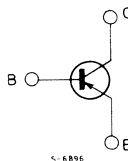


SOT-93 (TO-218)



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-3	BUW32 BUW32P SGSIW32	BUW32A BUW32AP SGSIW32A	
		SOT-93			
		ISOWATT218			
V_{CES}	Collector-emitter voltage ($V_{BE} = 0$)		-400	-450	V
V_{CEO}	Collector-emitter voltage ($I_{BE} = 0$)		-350	-400	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)		-5	-7	V
I_C	Collector current			-10	A
I_B	Base current			-5	A
			TO-3	SOT-93	ISOWATT218
V_{ISO}	Isolation voltage (DC)				4000 V
P_{tot}	Total dissipation at $T_C \leq 25^\circ\text{C}$		125	105	50 W
T_{stg}	Storage temperature		-65 to 175	-65 to 150	-65 to 150 $^\circ\text{C}$
T_j	Max. operating junction temperature		175	150	150 $^\circ\text{C}$



BUW32/BUW32A
BUW32P/BUW32AP
SGSIW32/SGSIW32A

THERMAL DATA

			TO-3	SOT-93	ISOWATT218
$R_{th J-case}$	Thermal resistance junction-case	max	1.19	1.19	2.5• °C/W

• See notes on ISOWATT218 in this datasheet.

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector cutoff current ($V_{BE} = 0$)	$V_{CE} = \text{rated } V_{CES}$ $V_{CE} = \text{rated } V_{CES} \quad T_c = 125^{\circ}\text{C}$		- 1 - 5	mA mA
I_{EBO}	Emitter cutoff current ($I_C = 0$)	$V_{EB} = \text{rated } V_{EBO}$		- 1	mA
$V_{CE(sus)}^*$	Collector-emitter sustaining voltage ($I_B = 0$)	$I_C = -100\text{mA}$ for BUW32/BUW32P/SGSIW32 for BUW32A/BUW32AP/SGSIW32A	- 350 - 400		V V
$V_{CE(sat)}^*$	Collector-emitter saturation voltage	$I_C = -5 \text{ A} \quad I_B = -1.5 \text{ A}$		- 1.5	V
$V_{BE(sat)}^*$	Base-emitter saturation voltage	$I_C = -5 \text{ A} \quad I_B = -1.5 \text{ A}$		- 1.6	V
h_{FE}^*	DC current gain	$I_C = -1 \text{ A} \quad V_{CE} = -5 \text{ V}$	12		
$I_{s b}$	Second breakdown collector current	$V_{CE} = -30 \text{ V}$ for BUW32/A for BUW32P/AP for SGSIW32/A	- 4.2 - 3.5 - 1.7		A A A

RESISTIVE LOAD

t_{on}	Turn-on time	$V_{CC} = -250 \text{ V} \quad I_C = -5 \text{ A}$		0.3	0.6	μs
t_s	Storage time	$I_{B1} = -I_{B2} = -1 \text{ A}$		0.7	1.5	μs
t_f	Fall time			0.25	0.6	μs

* Pulsed: Pulse duration - 300 μs , duty cycle - 1.5%



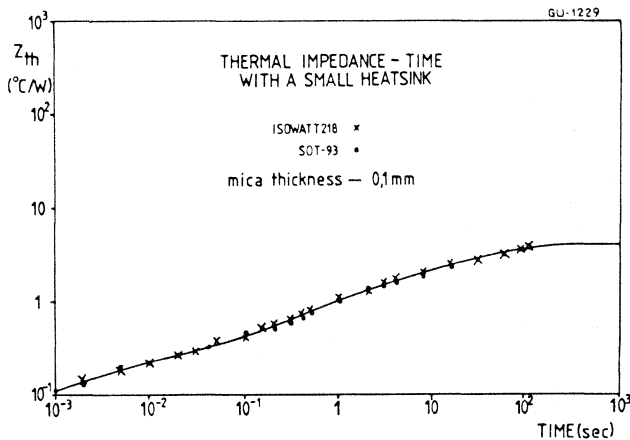
BUW32/BUW32A
BUW32P/BUW32AP
SGSIW32/SGSIW32A

THERMAL RESISTANCE OF THE ISOWATT218

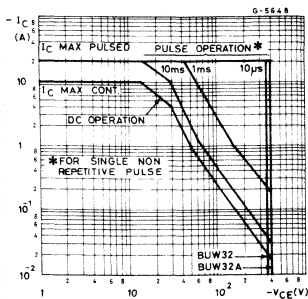
The junction to case thermal resistance of 2.5 °C/W for the ISOWATT218 package may seem quite high at first glance but if compared to a conventional SOT-93 (TO-218) package with a 0.1 mm mica insulating washer, the differences are marginal. The 0.1 mm isolating washer gives 1500V to 2000V DC isolation for the SOT-93 package, SGS guarantee 4000V DC isolation for the ISOWATT 218.

The comparison in fig. 1 shows the dynamic thermal resistance of both devices mounted using a thermal compound. The test illustrate that the ISOWATT218 has an R_{th} very close to that of conventional SOT-93 (TO-218) and any small increase is more than compensated for by the convenience of the ISOWATT218 package. The collector to heatsink capacitance of the ISOWATT218 is typically 17pF.

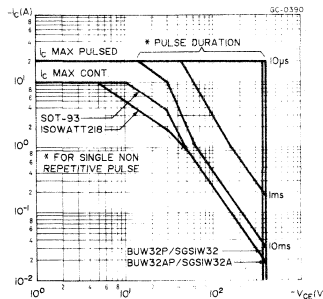
Fig. 1



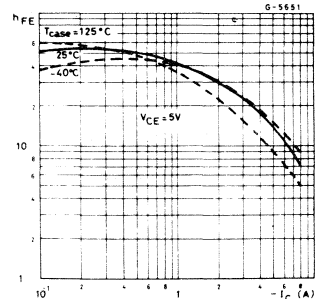
Safe operating areas



Safe operating areas



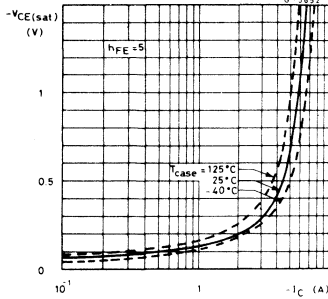
DC current gain



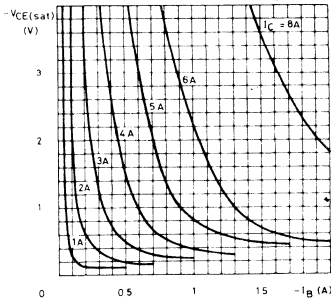


BUW32/BUW32A
BUW32P/BUW32AP
SGSIW32/SGSIW32A

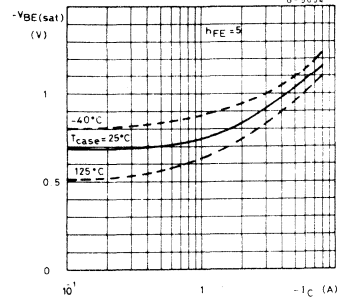
Collector-emitter saturation voltage



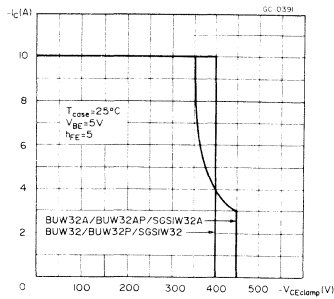
Collector-emitter saturation voltage



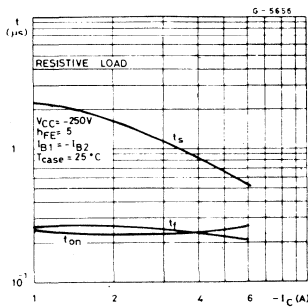
Base-emitter saturation voltage



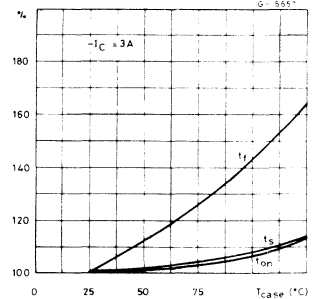
Clamped reverse bias safe operating areas



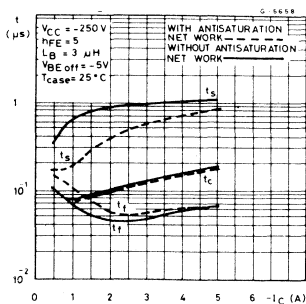
Saturated switching characteristics



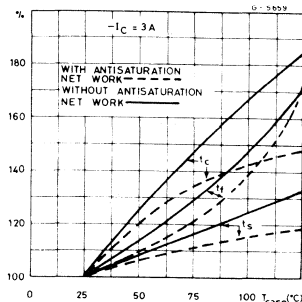
Switching times percentage variation vs. T_{case} resistive load



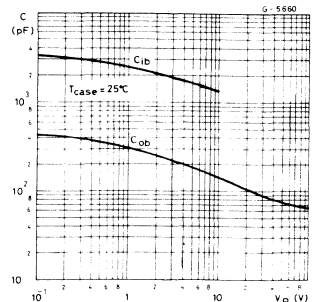
Switching times inductive load (fig. 2)



Switching times percentage variation vs. T_{case} inductive load



Capacitance variation





BUW32/BUW32A
BUW32P/BUW32AP
SGSIW32/SGSIW32A

TEST CIRCUITS

Fig. 1

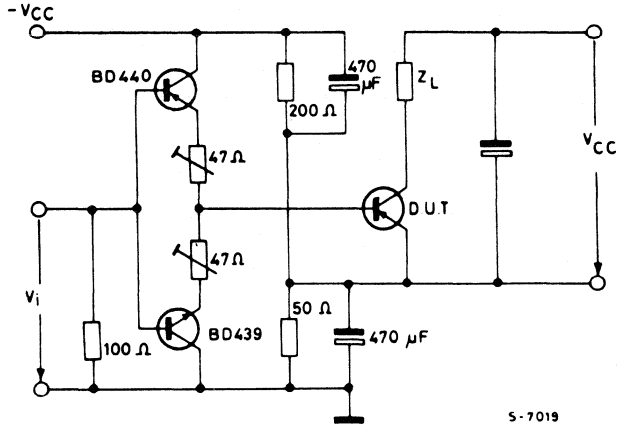
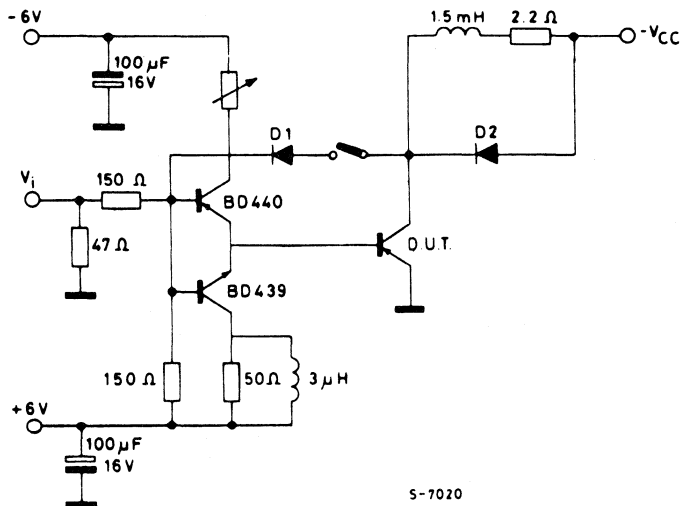


Fig. 2



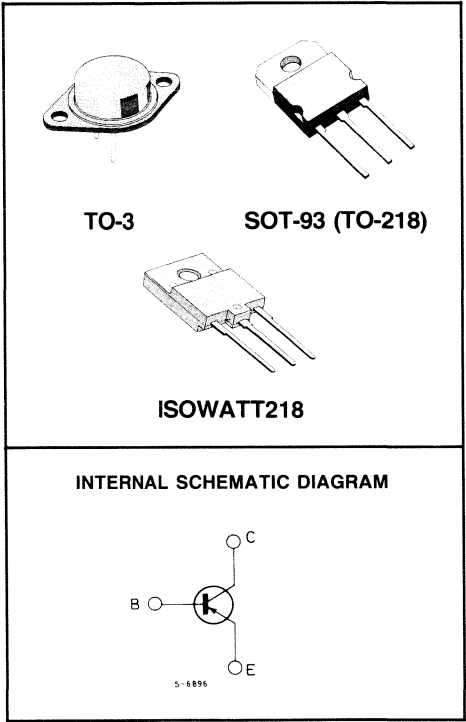


BUW42/BUW42A
BUW42P/BUW42AP
SGSIW42/SGSIW42A

HIGH VOLTAGE POWER SWITCH

- FAST SWITCHING APPLICATIONS
- INDUSTRIAL APPLICATION

The BUW42/A, BUW42P/AP and SGSIW42/A are silicon multiepitaxial mesa PNP transistors mounted respectively in TO-3 metal case, SOT-93 plastic package and ISOWATT218 fully isolated package.



ABSOLUTE MAXIMUM RATINGS		TO-3		BUW42	BUW42A	
		SOT-93		BUW42P	BUW42AP	
		ISOWATT218		SGSIW42	SGSIW42A	
V _{CES}	Collector-emitter voltage (V _{BE} = 0)			−400	−450	V
V _{CEO}	Collector-emitter voltage (I _{BE} = 0)			−350	−400	V
V _{EBO}	Emitter-base voltage (I _C = 0)			−5	−7	V
I _C	Collector current				−15	A
I _{CM}	Collector peak current				−30	A
I _B	Base current				−10	A
		TO-3	SOT-93	ISOWATT218		
V _{ISO}	Isolation voltage (DC)				4000	V
P _{tot}	Total dissipation at T _c ≤ 25°C	150	105	50		W
T _{stg}	Storage temperature	−65 to 175	−65 to 150	−65 to 150		°C
T _j	Max. operating junction temperature	175	150	150		°C

THERMAL DATA				TO-3	SOT-93	ISOWATT218	
$R_{th\ j-case}$	Thermal resistance junction-case	max		1	1.2	2.5•	°C/W

• See notes on ISOWATT218 in this datasheet.

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CES} Collector cutoff current ($V_{BE} = 0$)	$V_{CE} = \text{rated } V_{CES}$			− 1	mA
I_{EBO} Emitter cutoff current	$V_{EB} = \text{rated } V_{EBO}$			− 1	mA
$V_{CEO(sus)}^{*}$ Collector emitter sustaining voltage ($I_B = 0$)	$I_C = 100\text{mA}$ for BUW42/BUW42P/SGSIW42 for BUW42A/BUW42AP/SGSIW42A	−350 −400			V V
$V_{CE(sat)}^{*}$ Collector-emitter saturation voltage	$I_C = -10\text{ A } I_B = -3\text{ A}$			− 1.5	V
$V_{BE(sat)}^{*}$ Base-emitter saturation voltage	$I_C = -10\text{ A } I_B = -3\text{ A}$			− 2	V
h_{FE}^{*} DC current gain	$I_C = -3\text{ A } V_{CE} = -5\text{ V}$	12		80	

RESISTIVE LOAD

t_{on} Turn-on time	$V_{CC} = -250\text{ V } I_C = -10\text{ A}$		0.3	0.6	μs
t_s Storage time	$I_{B1} = -I_{B2} = -3.3\text{ A}$		0.5	1.5	μs
t_f Fall time			0.3	0.6	μs

* Pulsed: Pulse duration = 300 μs , duty cycle = 1.5%



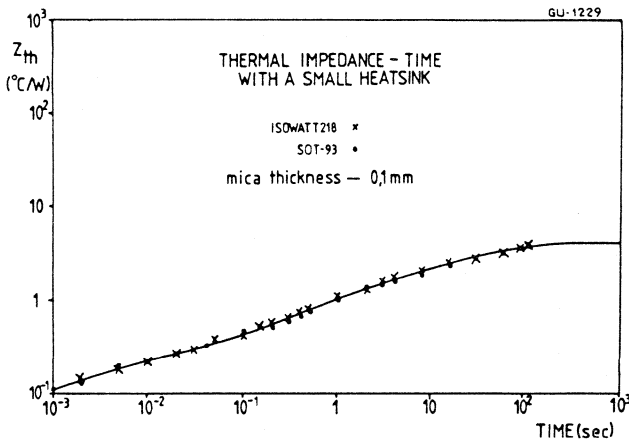
BUW42/BUW42A
BUW42P/BUW42AP
SGSIW42/SGSIW42A

THERMAL RESISTANCE OF THE ISOWATT218

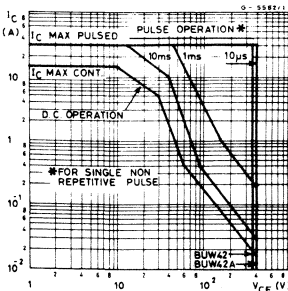
The junction to case thermal resistance of 2.5 °C/W for the ISOWATT218 package may seem quite high at first glance but if compared to a conventional SOT-93 (TO-218) package with a 0.1 mm mica insulating washer, the differences are marginal. The 0.1 mm isolating washer gives 1500V to 2000VDC isolation for the SOT-93 package, SGS guarantee 4000V DC isolation for the ISOWATT 218.

The comparison in fig. 1 shows the dynamic thermal resistance of both devices mounted using a thermal compound. The test illustrate that the ISOWATT218 has an R_{th} very close to that of conventional SOT-93 (TO-218) and any small increase is more than compensated for by the convenience of the ISOWATT218 package. The collector to heatsink capacitance of the ISOWATT218 is typically 17pF.

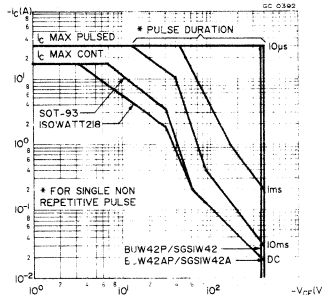
Fig. 1



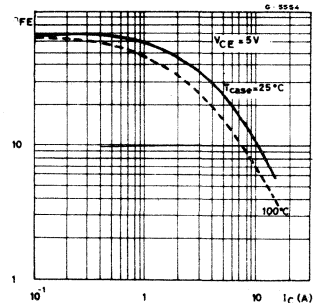
Safe operating area



Safe operating areas



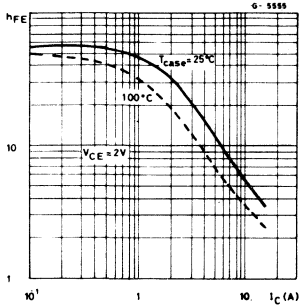
DC current gain



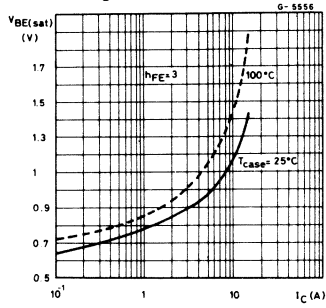


BUW42/BUW42A
BUW42P/BUW42AP
SGSIW42/SGSIW42A

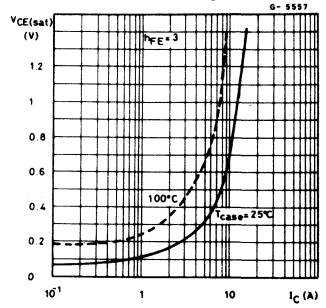
DC current gain



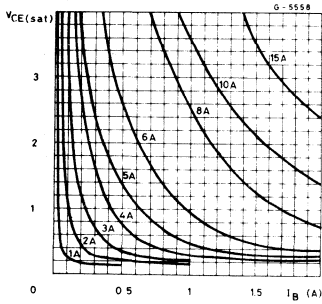
Base-emitter saturation voltage



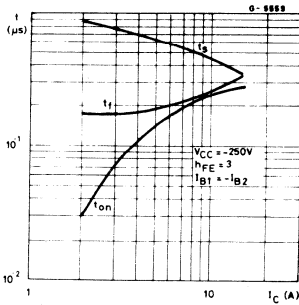
Collector-emitter saturation voltage



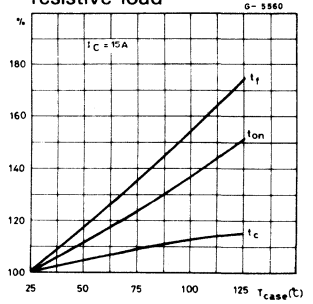
Collector-emitter saturation voltage



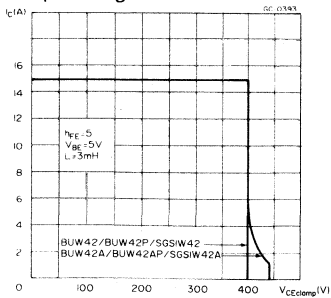
Saturated switching times resistive load



Switching times percentage variation vs. T_{case} resistive load



Clamped reverse bias safe operating areas





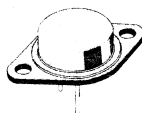
BUX48/ BUX48A
BUV48/ BUV48A
SGSIV48/ SGSIV48A

HIGH VOLTAGE POWER SWITCH

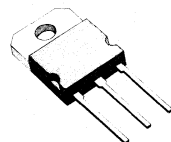
- DC, AC MOTOR CONTROL
- SWITCH MODE POWER SUPPLY

The BUX48, BUX48A, BUV48, BUV48A, SGSIV48 and SGSIV48A are multi-epitaxial mesa NPN transistors mounted in respectively in TO-3 metal case, SOT-93 plastic package and ISOWATT218 fully isolated package.

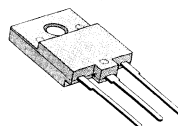
They are particularly intended for switching applications directly from the 220V and 380V mains.



TO-3

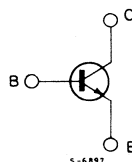


SOT-93 (TO-218)



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-3 SOT-93 ISOWATT218	BUX48 BUV48 SGSIV48	BUX48A BUV48A SGSIV48A	
V_{CES}	Collector-emitter voltage ($V_{BE} = 0$)		850	1000	V
V_{CER}	Collector-emitter voltage ($R_{BE} = 10\Omega$)		850	1000	V
V_{CEO}	Collector-emitter voltage ($I_{BE} = 0$)		400	450	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)			7	V
I_C	Collector current			15	A
I_{CM}	Collector peak current (I_{CP} ($t_p \leq 5$ ms))			30	A
I_{CP}	Collector peak current non rep. ($t_p \leq 20$ μ s)			55	A
I_B	Base current			4	A
I_{BM}	Base peak current ($t_p \leq 5$ ms)			20	A
			TO-3	SOT-93	ISOWATT218
V_{ISO}	Isolation voltage (DC)				4000 V
P_{tot}	Total dissipation at $T_c \leq 25^\circ\text{C}$		175	125	50 W
T_{stg}	Storage temperature		-65 to 200	-65 to 150	-65 to 150 $^\circ\text{C}$
T_j	Max. operating junction temperature		200	150	150 $^\circ\text{C}$



BUX48/BUX48A
BUV48/BUV48A
SGSIV48/SGSIV48A

THERMAL DATA

			TO-3	SOT-93	ISOWATT218	
$R_{th\ j-case}$	Thermal resistance junction-case	max	1	1	2.5•	°C/W

• See notes on ISOWATT218 in this datasheet.

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CER} Collector cutoff current ($R_{BE} = 10\Omega$)	$V_{CE} = \text{rated}$ V_{CER} $V_{CE} = \text{rated}$ V_{CER} $T_c = 125^{\circ}C$			500 4	μA mA
I_{CES} Collector cutoff current ($V_{BE} = 0$)	$V_{CE} = \text{rated}$ V_{CER} $V_{CE} = \text{rated}$ V_{CER} $T_c = 125^{\circ}C$			200 2	μA mA
I_{EBO} Emitter cutoff current ($I_C = 0$)	$V_{EB} = 5\ V$			1	mA
$V_{CEO(sus)}$ * Collector emitter sustaining voltage ($I_B = 0$)	$I_C = 200mA$ $L = 25mH$ for BUX48/BUV48/SGSIV48 for BUX48A/BUV48A/SGSIV48A	400 450			V V
V_{EBO} Emitter-base voltage ($I_C = 0$)	$I_E = 50mA$	7		30	V
$V_{CE(sat)}$ Collector-emitter saturation voltage	for BUX48/BUV48/SGSIV48 $I_C = 10\ A$ $I_B = 2\ A$ $I_C = 15\ A$ $I_B = 4\ A$ $I_C = 15\ A$ $I_B = 3\ A$ for BUX48A/BUV48A/SGSIV48A $I_C = 8\ A$ $I_B = 1.6\ A$ $I_C = 12\ A$ $I_B = 2.4\ A$			1.5 3.5 5 1.5 5	V V V V V
$V_{BE(sat)}$ * Base-emitter saturation voltage	for BUX48/BUV48/SGSIV48 $I_C = 10\ A$ $I_B = 2\ A$ for BUX48A/BUV48A/SGSIV48A $I_C = 8\ A$ $I_B = 1.6\ A$			1.6 1.6	V V

• Pulsed: Pulse duration = 300 μs , duty cycle = 1.5%.



BUX48/BUX48A
BUV48/BUV48A
SGSIV48/SGSIV48A

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
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RESISTIVE LOAD

t_{on} Turn-on time	for BUX48/BUV48/SGSIV48 $V_{CC} = 150\text{ V}$ $I_C = 10\text{ A}$ $I_{B1} = 2\text{ A}$ for BUX48A/BUV48A/SGSIV48A $V_{CC} = 150\text{ V}$ $I_C = 8\text{ A}$ $I_{B1} = 1.6\text{ A}$			1 1	μS μS
t_s Storage time	for BUX48/BUV48/SGSIV48 $V_{CC} = 150\text{ V}$ $I_C = 10\text{ A}$ $I_{B1} = -I_{B2} = 2\text{ A}$ for BUX48A/BUV48A/SGSIV48A $V_{CC} = 150\text{ V}$ $I_C = 8\text{ A}$ $I_{B1} = -I_{B2} = 1.6\text{ A}$			3 3	μS μS
t_f Fall time	for BUX48/BUV48/SGSIV48 $V_{CC} = 150\text{ V}$ $I_C = 10\text{ A}$ $I_{B1} = -I_{B2} = 2\text{ A}$ for BUX48A/BUV48A/SGSIV48A $V_{CC} = 150\text{ V}$ $I_C = 8\text{ A}$ $I_{B1} = -I_{B2} = 1.6\text{ A}$			0.8 0.8	μS μS

INDUCTIVE LOAD

t_s Storage time	for BUX48/BUV48/SGSIV48 $V_{CC} = 300\text{ V}$ $I_C = 10\text{ A}$ $L_B = 3\mu\text{H}$ $I_{B1} = 2\text{ A}$ $V_{BE} = -5\text{ V}$ same $T_c = 125^{\circ}\text{C}$ for BUX48A/BUV48A/SGSIV48A $V_{CC} = 300\text{ V}$ $I_C = 8\text{ A}$ $L_B = 3\mu\text{H}$ $I_{B1} = 1.6\text{ A}$ $V_{BE} = -5\text{ V}$ same $T_c = 125^{\circ}\text{C}$		2.7 3	5 5	μS μS
t_f Fall time	for BUX48/BUV48/SGSIV48 $V_{CC} = 300\text{ V}$ $I_C = 10\text{ A}$ $L_B = 3\mu\text{H}$ $I_{B1} = 2\text{ A}$ $V_{BE} = -5\text{ V}$ same $T_c = 125^{\circ}\text{C}$ for BUX48A/BUV48A/SGSIV48A $V_{CC} = 300\text{ V}$ $I_C = 8\text{ A}$ $L_B = 3\mu\text{H}$ $I_{B1} = 1.6\text{ A}$ $V_{BE} = -5\text{ V}$ same $T_c = 125^{\circ}\text{C}$		0.16 0.13	0.4 0.4	μS μS



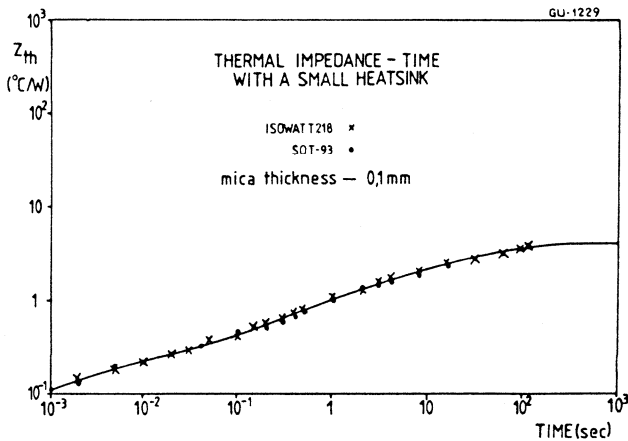
BUX48/BUX48A
BUV48/BUV48A
SGSIV48/SGSIV48A

THERMAL RESISTANCE OF THE ISOWATT218

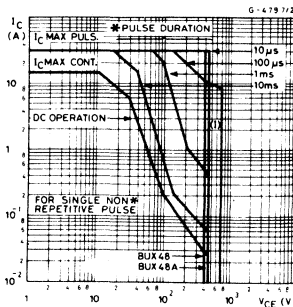
The junction to case thermal resistance of 2.5 °C/W for the ISOWATT218 package may seem quite high at first glance but if compared to a conventional SOT-93 (TO-218) package with a 0.1 mm mica insulating washer, the differences are marginal. The 0.1 mm isolating washer gives 1500V to 2000VDC isolation for the SOT-93 package, SGS guarantee 4000V DC isolation for the ISOWATT 218.

The comparison in fig. 1 shows the dynamic thermal resistance of both devices mounted using a thermal compound. The test illustrate that the ISOWATT218 has an R_{th} very close to that of conventional SOT-93 (TO-218) and any small increase is more than compensated for by the convenience of the ISOWATT218 package. The collector to heatsink capacitance of the ISOWATT218 is typically 17pF.

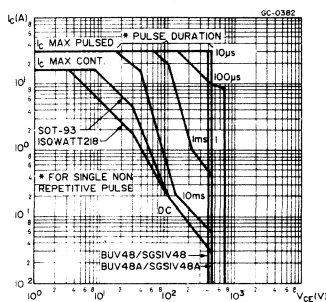
Fig. 1



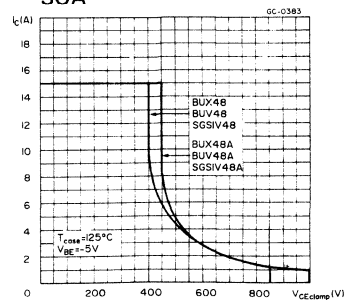
Safe operating areas



Safe operating areas



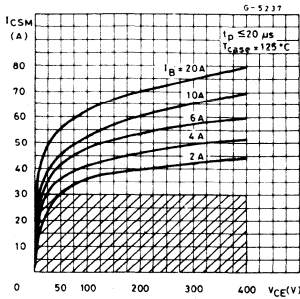
Clamped reverse biased SOA



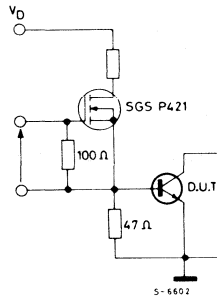


BUX48/BUX48A
BUV48/BUV48A
SGSIV48/SGSIV48A

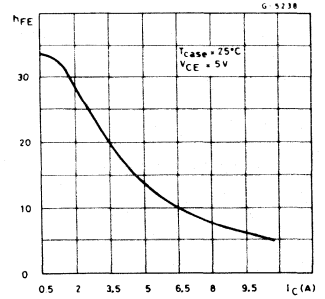
Forward biased accidental overload area



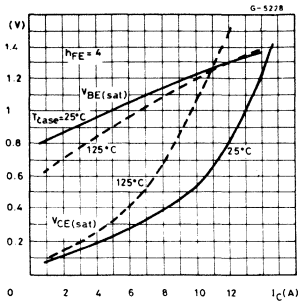
Forward biased accidental overload area test circuit.



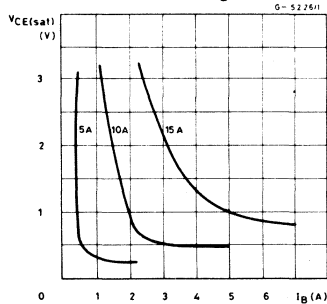
DC current gain



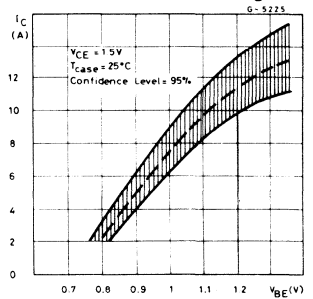
Saturation voltages



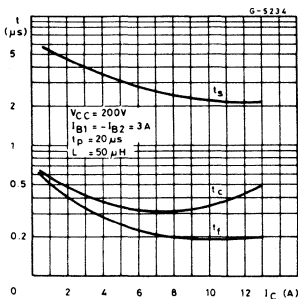
Collector-emitter saturation voltage



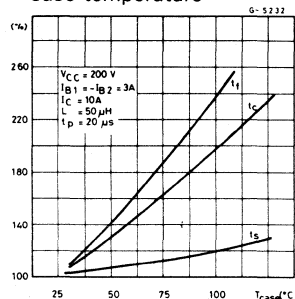
Collector current spread vs. base emitter voltage



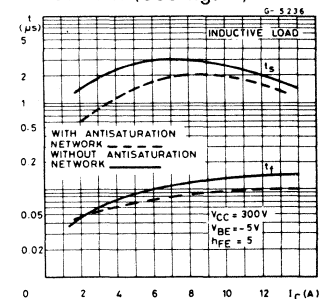
Switching times vs. collector current with I_B constant



Switching times percentage variation vs. case temperature



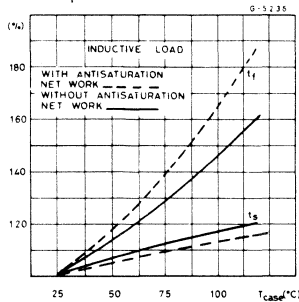
Switching times with and without antisaturation network (See fig.6)



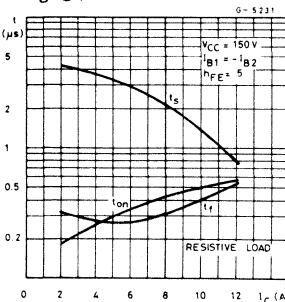


BUX48/BUX48A
BUV48/BUV48A
SGSIV48/SGSIV48A

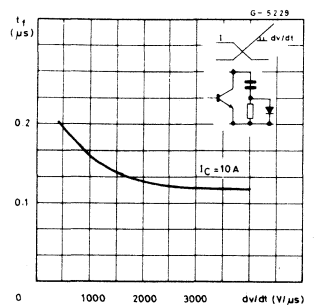
Switching times
percentage vs. case
temperature



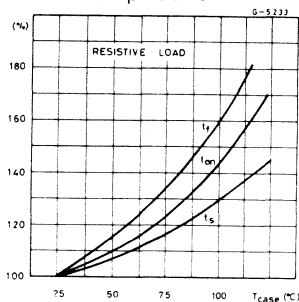
Switching times vs.
collector current (See
fig. 5)



Fall time vs. voltage slope
(See fig. 5)



Switching times
percentage variation vs.
case temperature



Dynamic collector-emitter
saturation voltage (See
fig. 3)

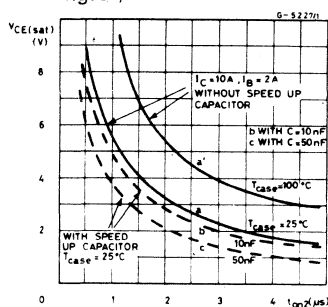


Fig. 2 Equivalent input
schematic circuit at turn-on.

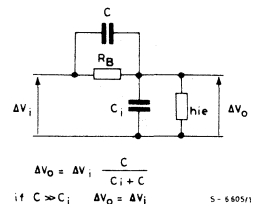


Fig. 3 $V_{CE(sat)}$ dyn. test circuit.

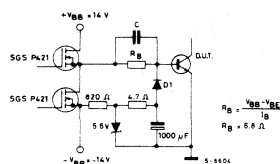


Fig. 4 Remarks to $V_{CE(sat)}$
dyn. test circuit

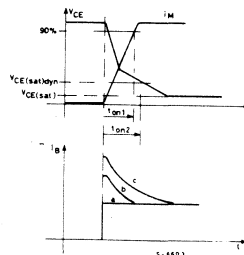


Fig. 5 - Switching times test circuit on resistive load.

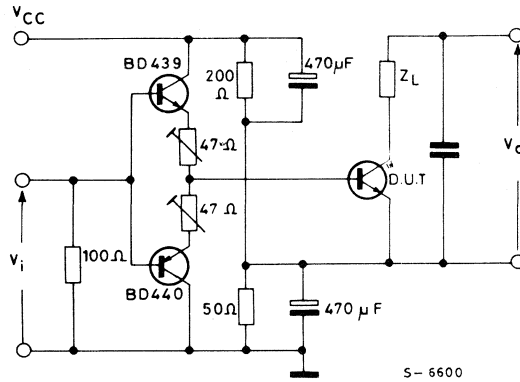
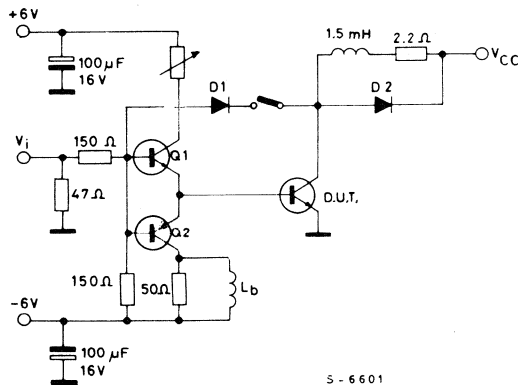


Fig.6 - Switching times test circuit on inductive load, with and without antisaturation network



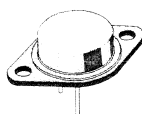
D1, D2 - Fast recovery diodes
 Q1, Q2 - Transistors SGS: 2N5191, 2N5195

HIGH VOLTAGE POWER SWITCHING

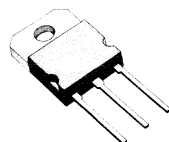
• INDUSTRIAL APPLICATIONS

The BUX48B, BUX48C, BUV48B, BUV48C and SGSIV48C are multiepitaxial mesa NPN transistors mounted respectively in TO-3 metal case SOT-93 plastic package and ISOWATT218 fully isolated package.

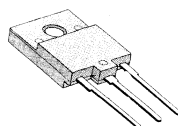
They are particularly intended for switching and industrial applications from single and three-phase mains.



TO-3

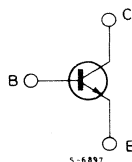


SOT-93 (TO-218)



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

TO-3
SOT-93
ISOWATT218

BUX48B
BUV48B

BUX48C
BUV48C
SGSIV48C

V_{CER}	Collector-emitter voltage ($R_{BE} = 10\Omega$)
V_{CES}	Collector-emitter voltage ($V_{BE} = 0$)
V_{CEO}	Collector-emitter voltage ($I_B = 0$)
V_{EBO}	Emitter-base voltage ($I_C = 0$)
I_C	Collector current
I_{CM}	Collector peak current ($t_p \leq 5$ ms)
I_{CP}	Collector peak current non rep. ($t_p \leq 20\mu s$)
I_B	Base peak current
I_{BM}	Base peak current ($t_p \leq 5$ ms)
V_{ISO}	Isolation voltage (DC)
P_{tot}	Total dissipation at $T_C \leq 25^\circ C$
T_{stg}	Storage temperature
T_j	Max. operating junction temperature

1200		1200	V
1200		1200	V
600		700	V
	7		V
	15		A
	30		A
	55		A
	4		A
	20		A
TO-3	SOT-93	ISOWATT218	
175	120	4000	V
-65 to 200	-65 to 150	50	W
200	150	150	$^\circ C$



BUX48B/BUX48C
BUV48B/BUV48C
SGSIV48C

THERMAL DATA

		TO-3	SOT-93	ISOWATT218
R_{th} j-case	Thermal resistance junction-case max	1	1	2.5• °C/W

• See notes on ISOWATT218 in this datasheet.

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CER} Collector cutoff current ($R_{BE} = 10\Omega$)	$V_{CE} = V_{CES}$ $V_{CE} = V_{CES}$ $T_c = 125^{\circ}\text{C}$			500 4	μA mA
I_{CES} Collector cutoff current ($V_{BE} = 0$)	$V_{CE} = V_{CES}$ $V_{CE} = V_{CES}$ $T_c = 125^{\circ}\text{C}$			500 3	μA mA
V_{CEO} Collector cutoff current ($I_B = 0$)	$V_{CE} = V_{CEO}$			1	mA
I_{EBO} Emitter cutoff current ($I_C = 0$)	$V_{EB} = 6\text{ V}$			1	mA
$V_{CEO(sus)}$ * Collector emitter sustaining voltage ($I_B = 0$)	$I_C = 100\text{mA}$ for BUX48B/BUV48B for BUX48C/BUV48C/SGSIV48C	600 700			V V
$V_{CER(sus)}$ * Collector emitter sustaining voltage ($R_{BE} = 10\Omega$)	$I_C = 0.5\text{ A}$ $V_{clamp} = 1200\text{V}$ $L = 2\text{mH}$	1200			V
$V_{CE(sat)}$ * Collector-emitter saturation voltage	$I_C = 6\text{ A}$ $I_B = 1.5\text{ A}$ $I_C = 10\text{ A}$ $I_B = 4\text{ A}$			1.5 3	V V
$V_{BE(sat)}$ * Base-emitter saturation voltage	$I_C = 6\text{ A}$ $I_B = 1.5\text{ A}$ $I_C = 10\text{ A}$ $I_B = 4\text{ A}$			1.5 2	V V

RESISTIVE LOAD

t_{on} Turn-on time	$V_{CC} = 250\text{ V}$ $I_C = 6\text{ A}$		0.5	1	μs
t_s Storage time	$I_{B1} = -I_{B2} = 1.5\text{ A}$		1.5	3	μs
t_f Fall time			0.2	0.7	μs

INDUCTIVE LOAD

t_s Storage time	$V_{CC} = 250\text{ V}$ $I_C = 6\text{ A}$		2		μs
t_r Rise time	$I_{B1} = -I_{B2} = 1.5\text{ A}$		0.15		μs
t_s Storage time	$V_{CC} = 250\text{ V}$ $I_C = 6\text{ A}$		3	6	μs
t_r Rise time	$I_{B1} = -I_{B2} = 1.5\text{ A}$ $T_c = 125^{\circ}\text{C}$		0.33	0.60	μs



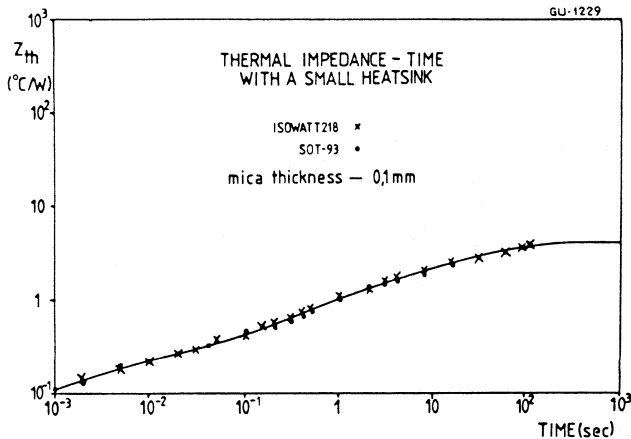
BUX48B/BUX48C
BUV48B/BUV48C
SGSIV48C

THERMAL RESISTANCE OF THE ISOWATT218

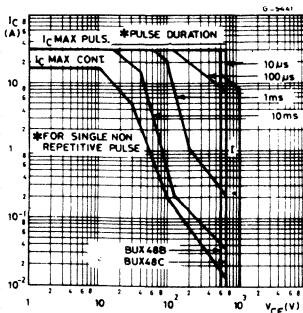
The junction to case thermal resistance of 2.5 °C/W for the ISOWATT218 package may seem quite high at first glance but if compared to a conventional SOT-93 (TO-218) package with a 0.1 mm mica insulating washer, the differences are marginal. The 0.1 mm isolating washer gives 1500V to 2000V DC isolation for the SOT-93 package, SGS guarantee 4000V DC isolation for the ISOWATT 218.

The comparison in fig. 1 shows the dynamic thermal resistance of both devices mounted using a thermal compound. The test illustrate that the ISOWATT218 has an R_{th} very close to that of conventional SOT-93 (TO-218) and any small increase is more than compensated for by the convenience of the ISOWATT218 package. The collector to heatsink capacitance of the ISOWATT218 is typically 17pF.

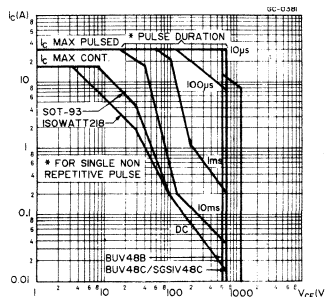
Fig. 1



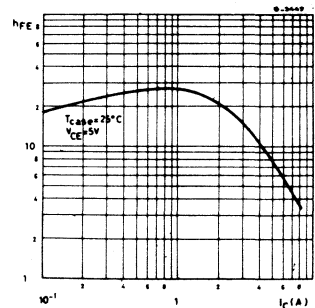
Safe operating areas



Safe operating areas



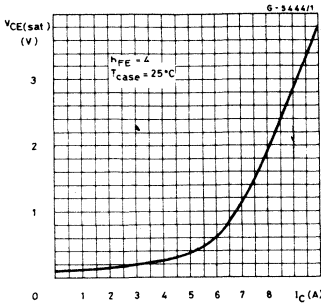
DC current gain



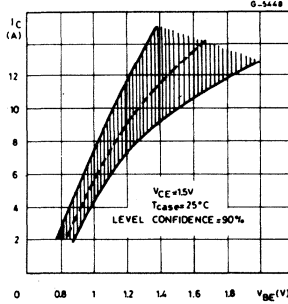


BUX48B/BUX48C
BUV48B/BUV48C
SGSIV48C

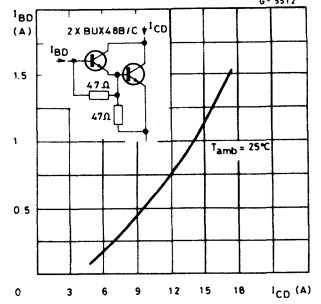
Collector-emitter
saturation voltage



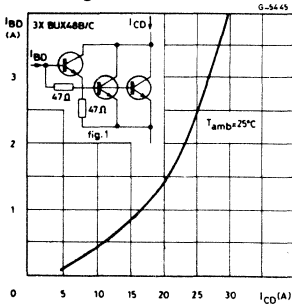
Collector current spread
vs. base emitter voltage



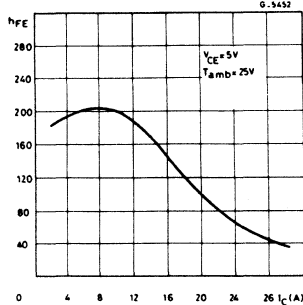
Minimum base current I_{BD}
to saturate the discrete
darlington



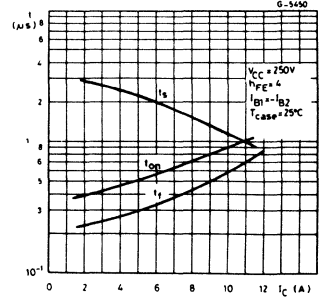
Minimum base current I_{BD}
to saturate the discrete
darlington



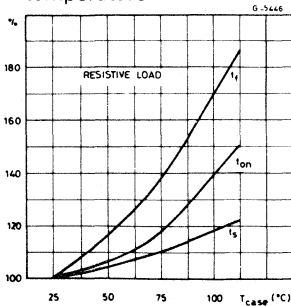
DC current gain for
darlington configuration



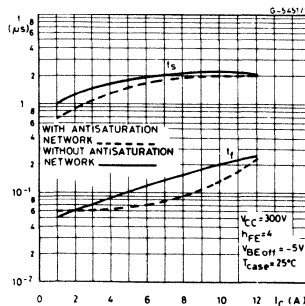
Switching times resistive
load (fig.2)



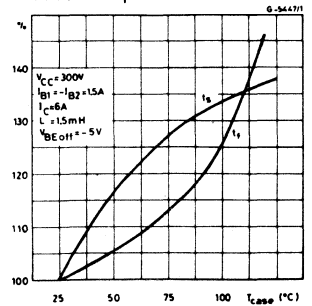
Switching times percent-
age variation vs. case
temperature



Switching times inductive
load (See fig.3)



Switching times
percentage variation vs.
case temperature





BUX48B/BUX48C
BUV48B/BUV48C
SGSIV48C

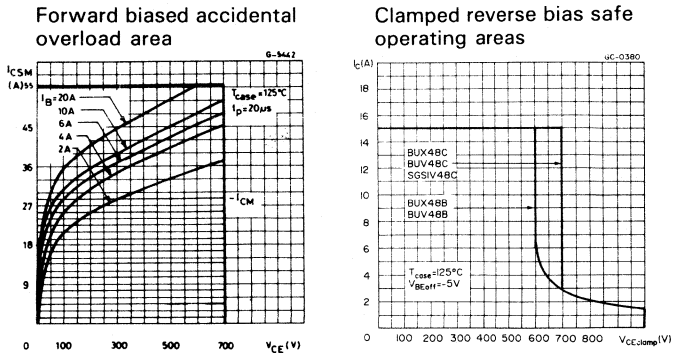


Fig. 2 - Switching times test circuit on resistive load.

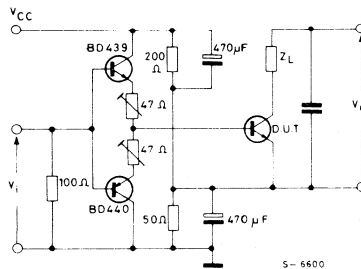
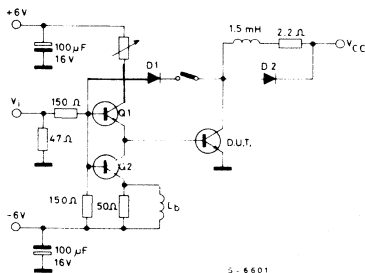


Fig.3 - Switching times test circuit on inductive load, with and without antisaturation network



D1, D2 - Fast recovery diodes
Q1, Q2 - Transistors SGS: 2N5191, 2N5195



BUX98 BUX98A

ADVANCE DATA

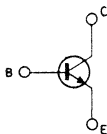
HIGH VOLTAGE FAST SWITCHING

The BUX98 and BUX98A are silicon multi-epitaxial mesa NPN transistors in Jedec TO-3 metal-case intended for use in switching and industrial applications from single and three-phase mains operation.

ABSOLUTE MAXIMUM RATINGS

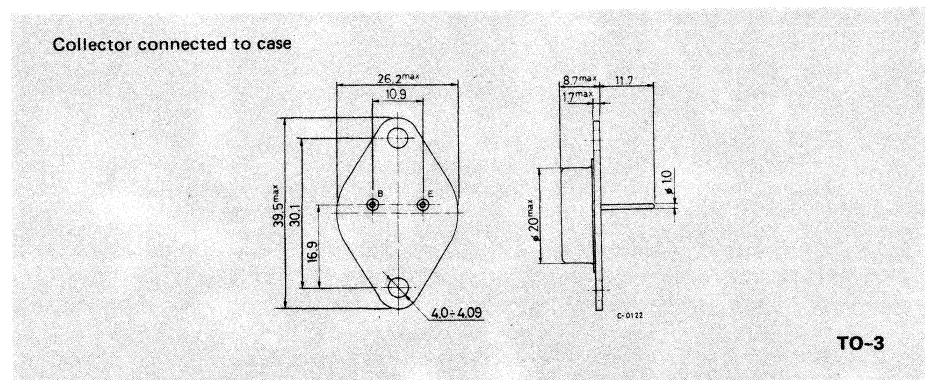
		BUX98	BUX98A
V_{CE}	Collector-emitter voltage ($R_{BE} = 10\Omega$)	850V	1000V
V_{CE}	Collector-base voltage ($V_{BE} = 0$)	850V	1000V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	400V	450V
V_{EBO}	Emitter-base voltage ($I_C = 0$)		7V
I_C	Collector current		30A
I_{CM}	Collector peak current ($t_p < 5ms$)		60A
I_{CP}	Collector peak current non rep. ($t_p < 20\mu s$)		80A
I_B	Base current		8A
I_{BM}	Base peak current ($t_p < 5ms$)		30A
P_{tot}	Total power dissipation at $T_{case} < 25^\circ C$		250W
T_{stg}	Storage temperature	-65 to $200^\circ C$	
T_j	Junction temperature	$200^\circ C$	

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.



BUX98
BUX98A

THERMAL DATA

$R_{th \text{ J-case}}$	Thermal resistance junction-case	max	0.7	$^{\circ}\text{C/W}$
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ELECTRICAL CHARACTERISTICS ($T_{\text{case}} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CER}	Collector cutoff current ($R_{\text{BE}} = 10\Omega$) $V_{\text{CE}} = V_{\text{CES}}$ $V_{\text{CE}} = V_{\text{CES}}$ $T_{\text{case}} = 125^{\circ}\text{C}$		1	8	μA mA
I_{CES}	Collector cutoff current ($V_{\text{BE}} = 0$) $V_{\text{CE}} = V_{\text{CES}}$ $V_{\text{CE}} = V_{\text{CES}}$ $T_{\text{case}} = 125^{\circ}\text{C}$		400	4	μA mA
I_{CEO}	Collector cutoff current ($I_{\text{B}} = 0$) $V_{\text{CE}} = V_{\text{CEO}}$		2		mA
I_{EBO}	Emitter cutoff current ($I_{\text{C}} = 0$) $V_{\text{BE}} = 5\text{V}$		2		mA
$V_{\text{CEO (sus)}}$ *	Collector-emitter sustaining voltage $I_{\text{C}} = 200\text{mA}$ for BUX98 for BUX98A	400		450	V V
$V_{\text{CER (sus)}}$ *	Collector-emitter sustaining voltage $L = 2\text{mH}$ $I_{\text{C}} = 1\text{A}$ for BUX98 for BUX98A	850		1000	V V
$V_{\text{CE (sat)}}$ *	Collector-emitter saturation voltage for BUX98 $I_{\text{C}} = 20\text{A}$ $I_{\text{B}} = 4\text{A}$ for BUX98A $I_{\text{C}} = 16\text{A}$ $I_{\text{B}} = 3.2\text{A}$ $I_{\text{C}} = 24\text{A}$ $I_{\text{B}} = 5\text{A}$		1.5		V V V
$V_{\text{CE (sat)}}$ *	Collector-emitter saturation voltage for BUX98 $I_{\text{C}} = 20\text{A}$ $I_{\text{B}} = 4\text{A}$ for BUX98A $I_{\text{C}} = 16\text{A}$ $I_{\text{B}} = 3.2\text{A}$		1.6		V V
t_{on}	Turn-on time for BUX98 $V_{\text{CC}} = 150\text{V}$		1		μs
t_{s}	Storage time $I_{\text{C}} = 20\text{A}$, $I_{\text{B1}} = I_{\text{B2}} = 4\text{A}$		3		μs
t_{f}	Fall time		0.8		μs
t_{on}	Turn-on time for BUX98A $V_{\text{CC}} = 150\text{V}$		1		μs
t_{s}	Storage time $I_{\text{C}} = 16\text{A}$; $I_{\text{B1}} = I_{\text{B2}} = 3.2\text{A}$		3		μs
t_{f}	Fall time		0.8		μs

* Pulsed: pulse duration = $300\mu\text{s}$, duty cycle = 1.5%



BUX98C

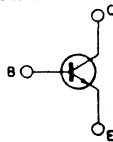
HIGH VOLTAGE SWITCH

The BUX98C, is a multiepitaxial mesa NPN transistors in Jedec TO-3 metal-case intended for use in switching and industrial applications from single and three-phase mains operation.

ABSOLUTE MAXIMUM RATINGS

V_{CER}	Collector-emitter voltage ($R_{BE} = 10\Omega$)	1200	V
V_{CES}	Collector-base voltage ($V_{BE} = 0$)	1200	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	700	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	7	V
I_C	Collector current	30	A
I_{CM}	Collector peak current ($tp < 5ms$)	60	A
I_{CP}	Collector peak current non repetitive ($tp < 20\mu s$)	80	A
I_B	Base current	8	A
I_{BM}	Base peak current ($tp < 5ms$)	30	A
P_{tot}	Total power dissipation at $T_{case} < 25^\circ C$	250	W
T_{stg}	Storage temperature	-65 to 200	$^\circ C$
T_J	Junction temperature	200	$^\circ C$

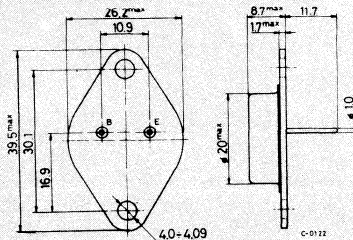
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Collector connected to case



TO-3



THERMAL DATA

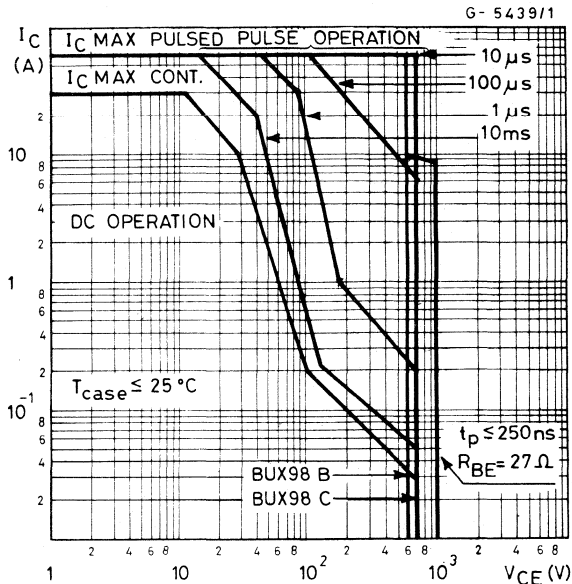
$R_{th\ j-case}$	Thermal resistance junction-case	max.	max.	0.7	$^{\circ}C/W$
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ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

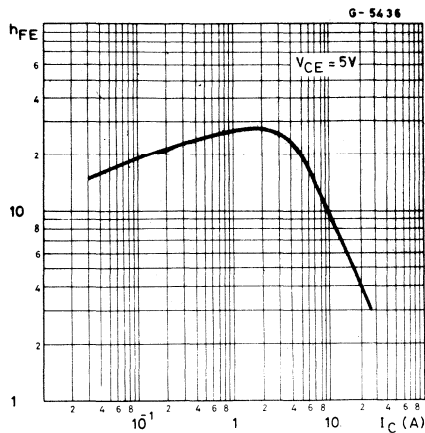
Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CER} Collector cutoff current ($R_{BE} = 10\Omega$)	$V_{CE} = V_{CES}$ $V_{CE} = V_{CES}$ $T_{case} = 125^{\circ}C$			1 8	mA mA
I_{CES} Collector cutoff current ($V_{BE} = 0$)	$V_{CE} = V_{CES}$ $V_{CE} = V_{CES}$ $T_{case} = 125^{\circ}C$			1 6	mA mA
I_{CEO} Collector cutoff current ($I_B = 0$)	$V_{CE} = V_{CEO}$			2	mA
I_{EBO} Emitter cutoff current ($I_C = 0$)	$V_{BE} = 5V$			2	mA
$V_{CEO(sus)}$ * Collector-emitter sustaining voltage	$I_C = 100mA$	700			V
$V_{CE(sat)}$ * Collector-emitter saturation voltage	$I_C = 12A$ $I_B = 3A$ $I_C = 16A$ $I_B = 5A$ $I_C = 20A$ $I_B = 8A$			1.5 2 3	V V V
$V_{BE(sat)}$ * Base-emitter saturation voltage	$I_C = 12A$ $I_B = 3A$ $I_C = 20A$ $I_B = 8A$			1.6 2	V V
t_{on} Turn-on time	RESISTIVE LOAD $V_{CC} = 250V$ $I_C = 12A$ $I_{B1} = -I_{B2} = 3A$		0.5	1	μs
t_s Storage time			1.5	3	μs
t_f Fall time			0.2	0.8	μs

* Pulsed : pulse duration = 300 μs , duty cycle = 1.5%

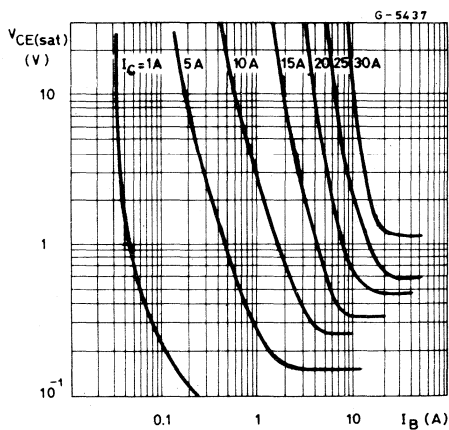
Safe operating areas



DC current gain



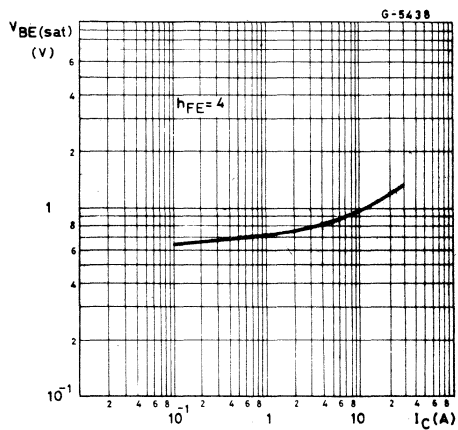
Collector-emitter saturation voltage



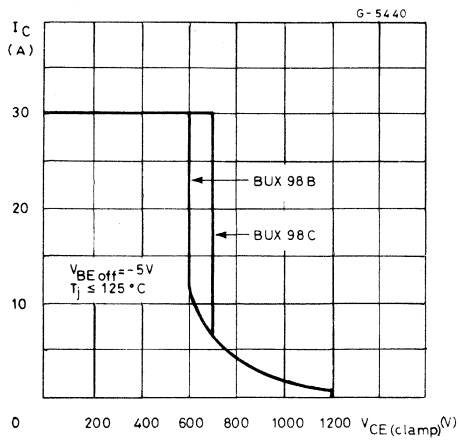


BUX98C

Base-emitter saturation voltage



Reverse biased operating area



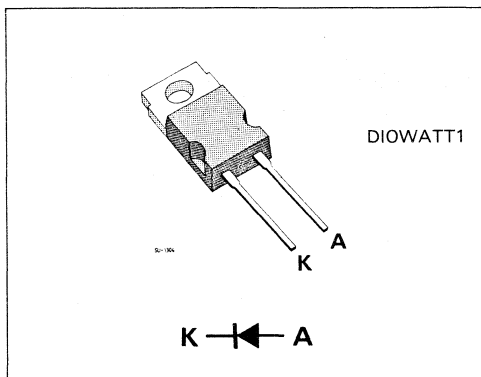


BYW29-50
BYW29-100
BYW29-150
BYW29-200

HIGH SPEED SWITCHING APPLICATIONS SECONDARY RECTIFICATION

- VOLTAGE RANGE: 50V - 200V
- AVERAGE CURRENT: 7.6A
- VERY LOW REVERSE RECOVERY TIME: t_{rr} 35ns
- VERY LOW SWITCHING LOSSES
- LOW NOISE TURN-OFF SWITCHING

Typical applications include secondary rectification in high frequency switching power supplies and freewheel diodes in stepper motor control systems.



ABSOLUTE MAXIMUM RATINGS

		BYW29				
		- 50	- 100	- 150	- 200	
V_{RRM}	Peak repetitive reverse voltage	50	100	150	200	V
V_{RWM}	Working peak reverse voltage	50	100	150	200	V
V_R	Continuous reverse voltage	50	100	150	200	V
I_{FRM}	Repetitive peak forward current ($t = 10\mu s$)	80				A
$I_{F(AV)}$	Average forward current $T_{case} = 70^\circ C$ (switching operation, $\delta = 0.5$)	7.6				A
I_{FSM}	Surge non repetitive forward current ($t = 10ms$)	80				A
P_{tot}	Total dissipation at $T_{case} = 70^\circ C$	18				W
T_{stg}	Storage temperature	- 40 to 150				$^\circ C$
T_j	Max. junction temperature	150				$^\circ C$



THERMAL DATA

$R_{thj-case}$	Thermal resistance junction-case	max 2.7 °C/W
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ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

Parameters		Test Contitions	Min.	Typ.	Max.	Unit
I_R	Reverse Current	$V = V_{RRM} \quad T_J = 100^{\circ}C$			0.6	mA
V_F	Forward voltage	$I_F = 5A \quad T_{case} = 100^{\circ}C$			0.85	V
		$I_F = 20A \quad T_{case} = 25^{\circ}C$			1.3	V
t_{rr}	Reverse recovery time	$I_F = 1A \quad di/dt = -50A/\mu s \quad V_R = 30V$			35	ns
		$I_F = 2A \quad di/dt = -20A/\mu s \quad V_R = 30V$			50	ns
Q_{rr}	Recovered charge	$I_F = 2A \quad di/dt = -20A/\mu s \quad V_R = 30V$			15	nC
V_{FP}	Forward recovery overvoltage	$I_F = 1A \quad di/dt = 10A/\mu s$		1		V

for typical curves see SGS8R05→20 datasheet



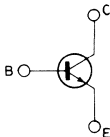
**MJE13006
MJE13007
MJE13007A**

MOTOR CONTROL, SWITCH REGULATORS

The MJE13006, MJE13007 and MJE13007A are silicon multiepitaxial mesa NPN transistors. They are mounted in Jedec TO-220 plastic package, intended for use in motor controls, switching regulator's etc.

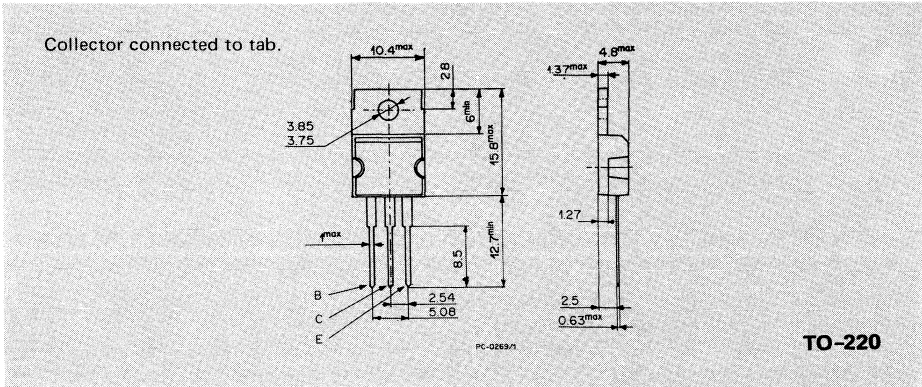
ABSOLUTE MAXIMUM RATINGS		MJE13006	MJE13007	MJE13007A
V_{CEO}	Collector-emitter voltage ($V_B = 0$)	300V	400V	400V
V_{CEV}	Collector-emitter voltage	600V	700V	850V
V_{EBO}	Emitter-base voltage ($I_C = 0$)		9V	
I_C	Collector current		8A	
I_{CM}	Collector peak current		16A	
I_B	Base current		4A	
I_{BM}	Base peak current		8A	
I_E	Emitter current		12A	
I_{EM}	Emitter peak current		24A	
P_{tot}	Total power dissipation at $T_{case} \leq 25^{\circ}C$		80W	
T_{stg}	Storage temperature		-65 to 150°C	
T_j	Junction temperature		150°C	

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm





MJE13006
MJE13007
MJE13007A

THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max	1.56	$^{\circ}C/W$
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ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{EBO} Emitter cutoff current ($I_C = 0$)	$V_{EB} = 9V$		1		mA
I_{CEV} Collector cutoff current ($V_{BE} = 1.5V$)	$V_{CEV} = \text{Rated value}$ $V_{CEV} = \text{Rated value}$ $T_{case} = 100^{\circ}C$	1		5	mA mA
$V_{CEO(sus)}^*$ Collector-emitter sustaining voltage ($I_B = 0$)	$I_C = 10mA$ for MJE13006 for MJE13007/13007A	300 400			V V
$V_{CE(sat)}^*$ Collector-emitter saturation voltage	$I_C = 2A$ $I_B = 0.4A$ $I_C = 5A$ $I_B = 1A$ $I_C = 8A$ $I_B = 2A$ $I_C = 5A$ $I_B = 1A$ $T_{case} = 100^{\circ}C$		1 1.5 3 2		V V V V
$V_{BE(sat)}^*$ Base-emitter saturation voltage	$I_C = 2A$ $I_B = 0.4A$ $I_C = 5A$ $I_B = 1A$ $I_C = 5A$ $I_B = 1A$ $T_{case} = 100^{\circ}C$		1.2 1.6 1.5		V V V
h_{FE}^* DC current gain	$I_C = 2A$ $V_{CE} = 5V$ $I_C = 5A$ $V_{CE} = 5V$	8 6	40 30		— —
f_T Transition frequency	$I_C = 500mA$ $V_{CE} = 10V$ $f = 1MHz$	4			MHz
C_{CBO} Output capacitance	$V_{CB} = 10V$ $I_E = 0$ $f = 0.1MHz$		110		pF



MJE13006
MJE13007
MJE13007A

ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Test conditions	Min. Typ. Max.	Unit
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RESISTIVE SWITCHING TIMES (Fig. 2)

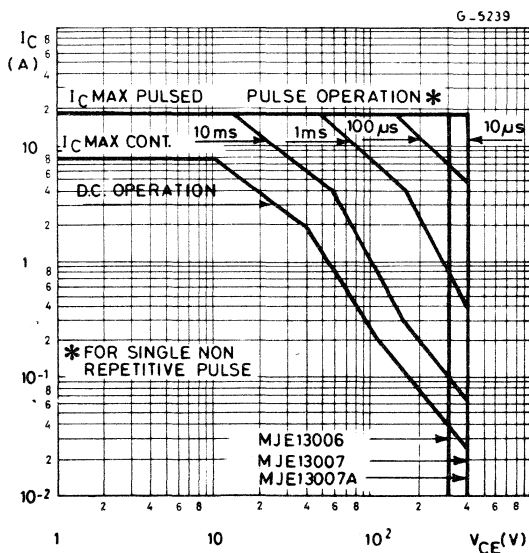
t_{on}	Turn-on time	$V_{CC} = 125V \quad I_C = 5A$ $I_{B1} = -I_{B2} = 1A$	0.7	μs
t_s	Storage time		3	μs
t_f	Fall time	$t_p = 25\mu s$ Duty Cycle $< 1\%$	0.7	μs

INDUCTIVE SWITCHING TIMES (Fig. 1)

t_f	Fall time	$V_{CC} = 125V \quad I_C = 5A$ $I_{B1} = 1A$ $t_p = 25\mu s$ Duty cycle $< 1\%$ $T_{case} = 100^\circ C$	0.3	μs
		$V_{CC} = 125V \quad I_C = 5A$ $I_{B1} = 1A$ $t_p = 25\mu s$ Duty cycle $\leq 1\%$	0.6	μs

* Pulsed: pulse duration $\leq 300\mu s$, duty cycle $\leq 1.5\%$

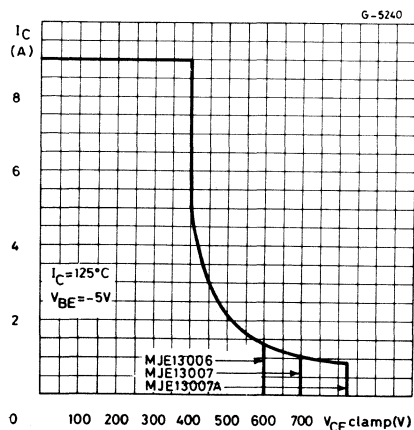
Safe operating areas



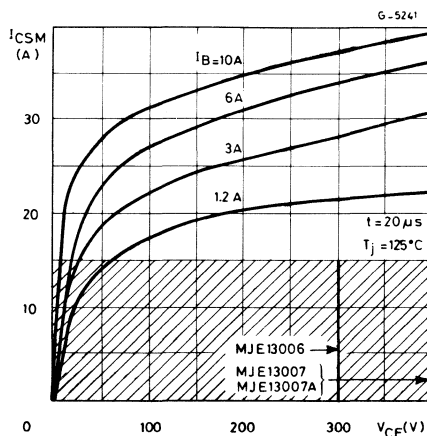


MJE13006
MJE13007
MJE13007A

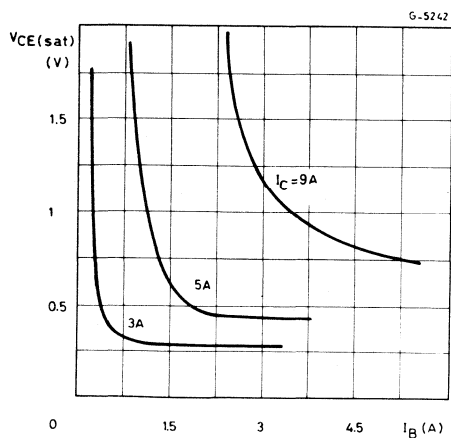
Clamped reverse bias safe operating areas



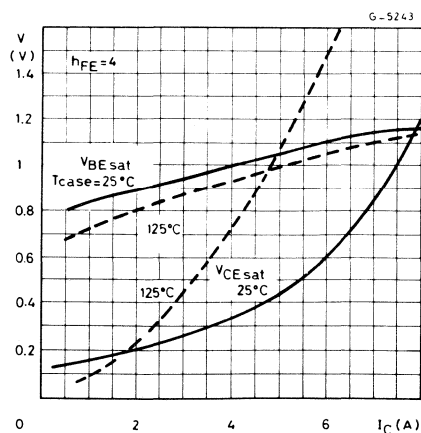
Forward biased accidental overload area (See fig. 3)



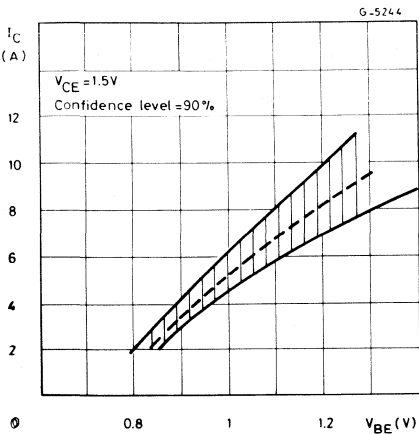
Collector saturation voltage



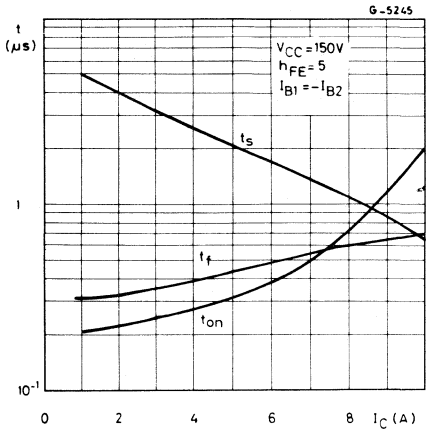
Saturation voltages



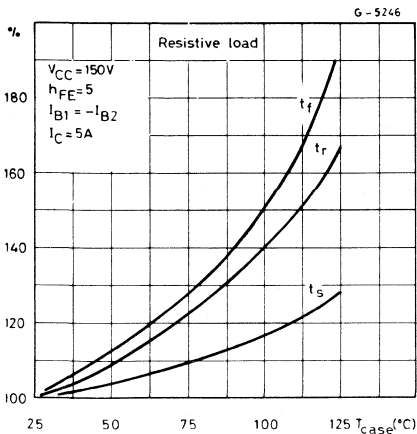
Collector current spread vs. base emitter voltage



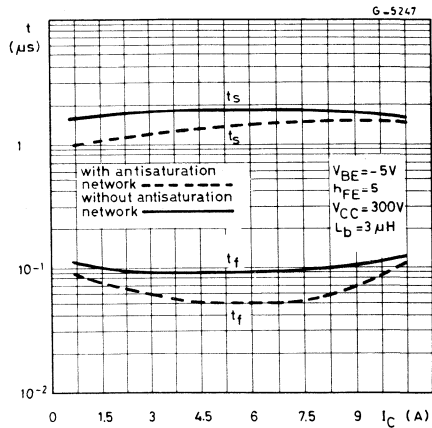
Switching times resistive load
(See fig. 2)



Switching times percentage variation vs. case temperature



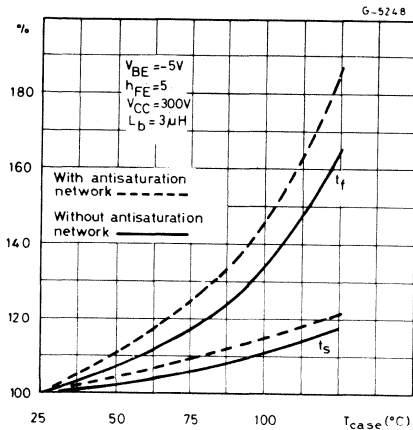
Switching times inductive load
(See fig. 1)



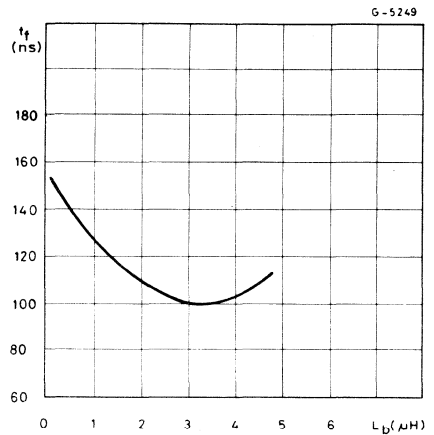


**MJE13006
MJE13007
MJE13007A**

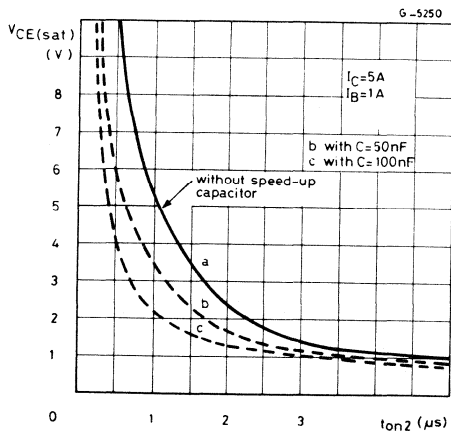
Switching times inductive load vs. case temperature



Fall times vs. L_b (See fig. 1)



Dynamic collector-emitter saturation voltage (See fig. 4)



DC current gain

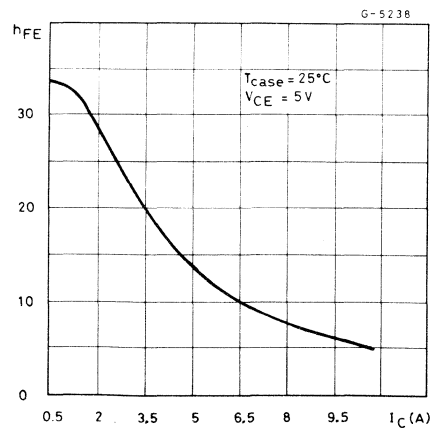
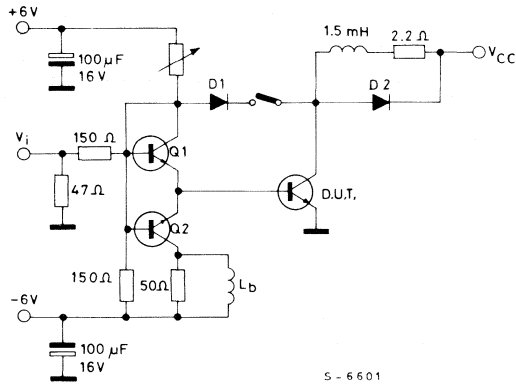


Fig. 1 - Switching times test circuit on inductive load, with and without antisaturation network



D1, D2 - Fast recovery diodes
Q1, Q2 - Transistors SGS: 2N5191, 2N5195

Fig. 2 - Switching times test circuit on resistive load.

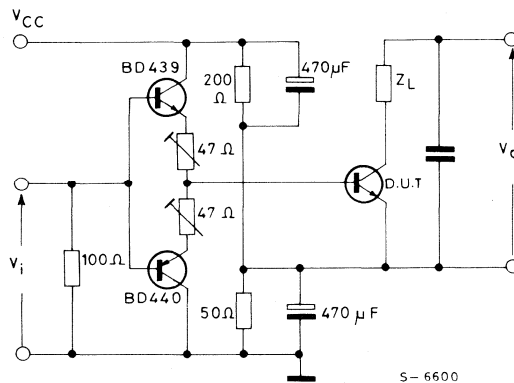


Fig. 3 - Forward biased accidental overload area test circuit.

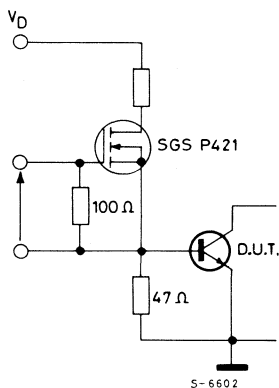


Fig. 4 - $V_{CE(sat)}$ dyn. test circuit.

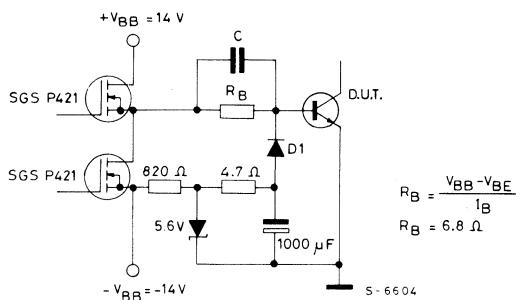
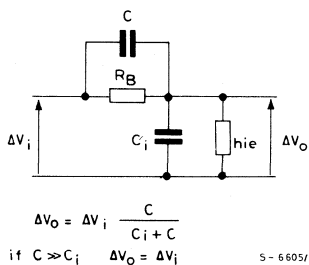
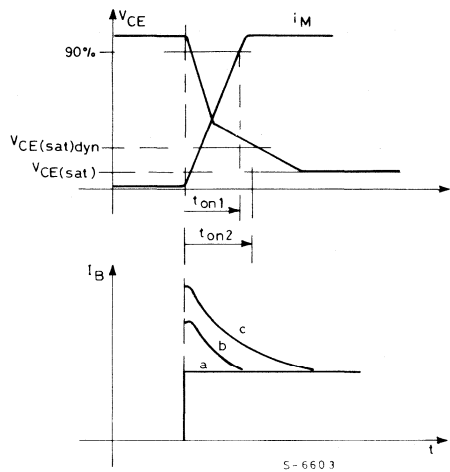


Fig. 5 - Equivalent input schematic circuit at turn-on.



S-6605/1

Fig. 6 - Remarks to $V_{CE(sat)}$ dyn. test circuit (fig. 4)

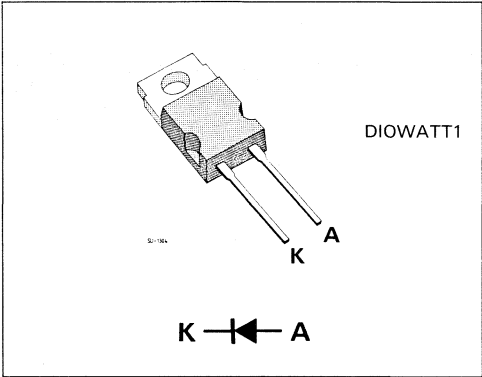


The speed-up capacitor decreases the $V_{CE(sat)}$ dyn. as shown in diagram (figure 6).
The 50nF capacitor modifies the shape of base current with a overshoot.

HIGH SPEED SWITCHING APPLICATIONS SECONDARY RECTIFICATION

- VOLTAGE RANGE: 50V - 200V
- AVERAGE CURRENT: 8A
- VERY LOW REVERSE RECOVERY TIME: t_{rr} 35ns
- VERY LOW SWITCHING LOSSES
- LOW NOISE TURN-OFF SWITCHING

Typical applications include secondary rectification in high frequency switching power supplies and freewheel diodes in stepper motor control systems.



ABSOLUTE MAXIMUM RATINGS

		SGS				
		8R05	8R10	8R15	8R20	
V _{RRM}	Peak repetitive reverse voltage	50	100	150	200	V
V _{RWM}	Working peak reverse voltage	50	100	150	200	V
V _R	Continuous reverse voltage	50	100	150	200	V
I _{FRM}	Repetitive peak forward current (t = 10μs)	100				A
I _{F(AV)}	Average forward current T _{case} = 70°C (switching operation, δ = 0.5)	8				A
I _{FSM}	Surge non repetitive forward current (t = 10ms)	80				A
P _{tot}	Total dissipation at T _{case} = 70°C	50				W
T _{stg}	Storage temperature	− 65 to 150				°C
T _j	Max. operating junction temperature	150				°C

THERMAL DATA

R _{thj-case}	Thermal resistance junction-case	max 1.6 °C/W
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ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters	Test Condtions	Min.	Typ.	Max.	Unit
I _R Reverse Current	V = V _R T _j = 25°C V = V _R T _j = 100°C			10 0.6	μA mA
V _F (*) Forward voltage	I _F = 5A T _{case} = 100°C I _F = 20A T _{case} = 25°C I _F = 8A T _{case} = 25°C			0.85 1.3 1	V V V
t _{rr} Reverse recovery time	I _F = 1A di/dt = 50A/μs V _R = 30V I _F = 2A di/dt = 20A/μs V _R = 30V I _F = 2A di/dt = 20A/μs T _j = 100°C			35 50 70	ns ns ns
Q _{rr} Recovered charge	I _F = 2A di/dt = 20A/μs V _R = 30V			15	nC
V _{FP} Forward recovery overvoltage	I _F = 1A di/dt = 10A/μs		1		V

* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%

Fig. 1 Average forward current vs. air temperature and cooling system

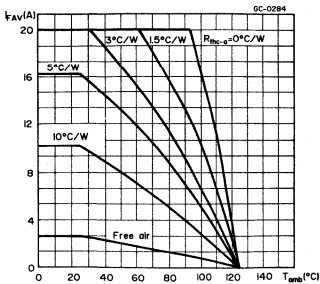


Fig. 2 Voltage drop vs. forward current

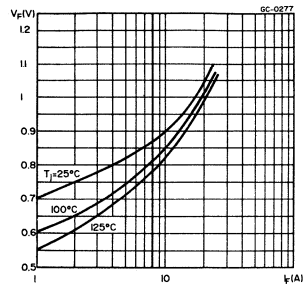


Fig. 3 Reverse leakage current vs. junction temperature.

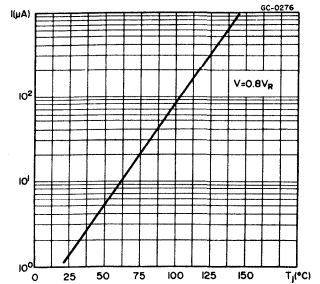


Fig. 4 Recovery time and peak reverse current vs. I_F

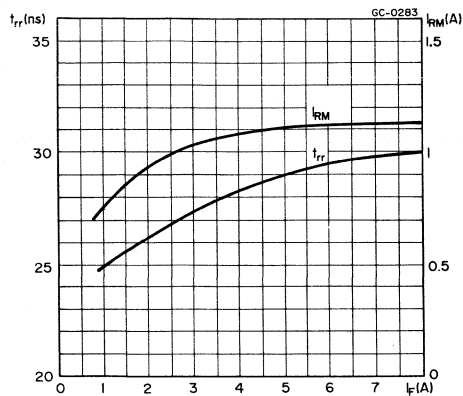


Fig. 5 Recovered charge vs. dI_F/dt

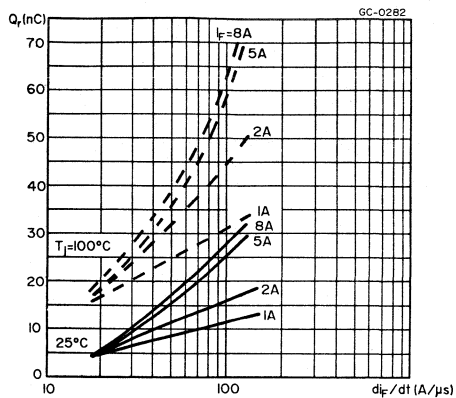


Fig. 6 Recovery time vs. dI_F/dt

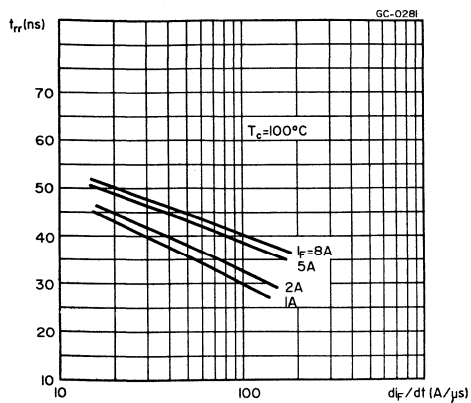
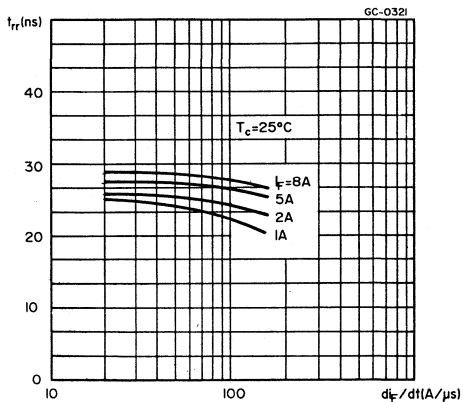


Fig. 7 Recovery time vs. dI_F/dt





SGS15DB070D
SGS15DB080D

TRANSPACK NPN POWER DARLINGTON MODULE

APPLICATIONS: These products are silicon NPN power darlington transistors in half bridge configuration for industrial switching applications with three-phase mains operation.

ISOLATED POWER MODULE (15KVA - 375W)

FAST FREEWHEEL DIODES

ABSOLUTE MAXIMUM RATINGS

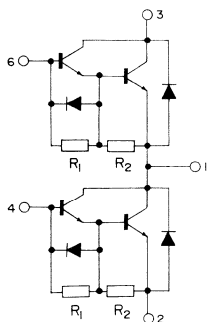
V_{CBO}	Collector-base voltage ($I_E = 0$)
V_{CES}	Collector-emitter voltage ($V_{BE} = 0$)
V_{CEX}	Collector-emitter voltage ($V_{BE} = -1.5V$)
V_{CEO}	Collector-emitter voltage ($I_B = 0$)
V_{CEOL}	Overload switch-off at 1.5 times I_C (sat)
V_{EBO}	Emitter-base voltage ($I_C = 0$)
I_C	Collector current
I_{CM}	Collector peak current ($t_p < 10$ ms)
I_{CP}	Collector peak current non repetitive ($t_p < 20$ μ s)
I_B	Base current
I_{BP}	Base peak current non repetitive ($t_p < 20$ μ s)
T_{stg}	Storage temperature
T_j	Max. operating junction temperature (continuous)
T_j	Max. operating junction temperature (1 minute)

SGS15DB070D

SGS15DB080D

1000	1200	V
1000	1200	V
1000	1200	V
700	800	V
650		V
7		V
23		A
60		A
100		A
6		A
30		A
- 40 to 150		°C
150		°C
175		°C

INTERNAL SCHEMATIC DIAGRAM



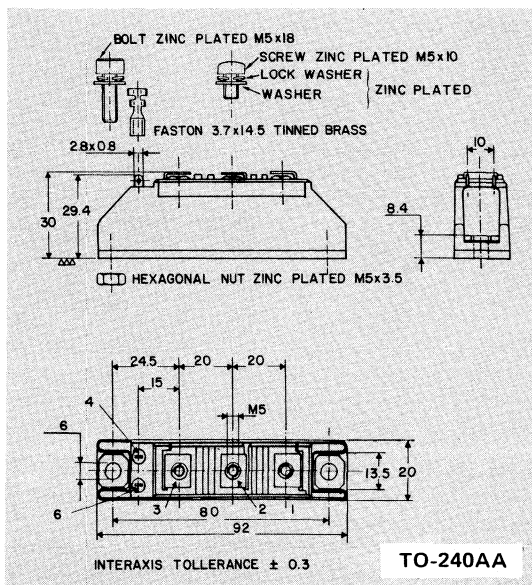
SC-0161

R_1 typ. 10 Ω

R_2 typ. 50 Ω

MECHANICAL DATA

Dimensions in mm



TO-240AA



SGS15DB070D
SGS15DB080D

THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case (quarter bridge)	max 0.66°C/W
$R_{th\ j-case}$	Thermal resistance junction-case (diode)	max 1.10°C/W
$R_{th\ c-h}$	Thermal resistance case-heatsink	max 0.20°C/W

ELECTRICAL CHARACTERISTICS

($T_j = 25^\circ\text{C}$ unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I _{CES}	Collector cutoff current (V _{BE} = 0)	V _{CE} = V _{CES}		0.05	2	mA
		V _{CE} = V _{CEOL} T _j = 125°C		3	10	mA
I _{CEX}	Collector cutoff current	V _{CE} = V _{CEX} V _{BE} = −1.5V		0.05	2	mA
		V _{CE} = V _{CEOL} V _{BE} = −1.5V T _j = 125°C		3	10	mA
I _{EBO}	Emitter cutoff current (I _C = 0)	V _{BE} = −2V			120	mA
V _{CEO (sus)*}	Collector emitter sustaining voltage	I _C = 0.2A for SGS15DB070D L = 2mH for SGS15DB080D	700 800			V V
V _{CEOL}	Max voltage to switch-off 1.5 times I _{C (sat)} (top right corner of RBSOA)	I _C = 23A	650			V
V _{CE (sat)*}	Collector-emitter saturation voltage	I _C = 15 A I _B = 1.5 A		1.6	3	V
		I _C = 20 A I _B = 4 A		1.6	3	V
V _{BE (sat)*}	Base-emitter saturation voltage	I _C = 15 A I _B = 1.5 A			2.5	V
		I _C = 20 A I _B = 4 A			3.5	V
h _{FE} *	DC current gain	I _C = 15 A V _{CE} = 5 V I _C = 20 A V _{CE} = 5 V	15	22 11		
INDUCTIVE LOAD		(see test circuit)				
t _s	Storage time	I _C = 15A I _B = 1.5 A V _{BE OFF} = −5 V		1.80		μs
t _f	Fall time	V _{CC} = 50V L = 500 μH V _{CL} = 300V		0.33		μs
		T _j = 25°C				
t _s	Storage time	I _C = 15A I _B = 1.5 A V _{BE OFF} = −5 V		2.40	5.0	μs
t _f	Fall time	V _{CC} = 50V L = 500 μH V _{CL} = 300V		0.66	1.5	μs
		T _j = 125°C				
V _f	Diode forward voltage	I _f = 15 A				

* Pulsed: Pulse duration = 300 μs , duty cycle = 1.5%.

ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
t_{rr}	Diode reverse recovery time	$I_f = 15\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$		0.20	0.5	μs
I_{rm}	Diode reverse recovery current			12		A
I_{frm}	Diode forward current	$t = 1\text{ ms}$	160			A

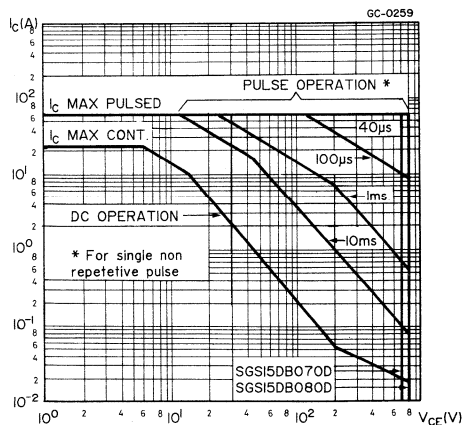
INSULATION TESTING

The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.

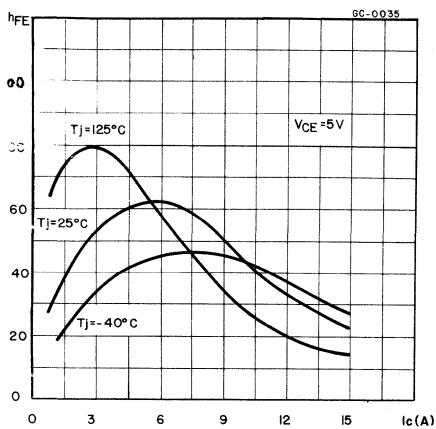
If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/VDE 0558 part 1/8.77, section 5.7.9., only a voltage slowly increasing up to the above value should be used. If the voltage is applied for one minute as recommended by the above standards then the specified value of 2000 V should be taken.

During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

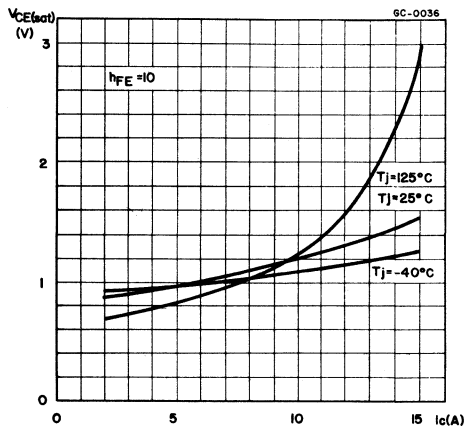
Safe operating areas for each section



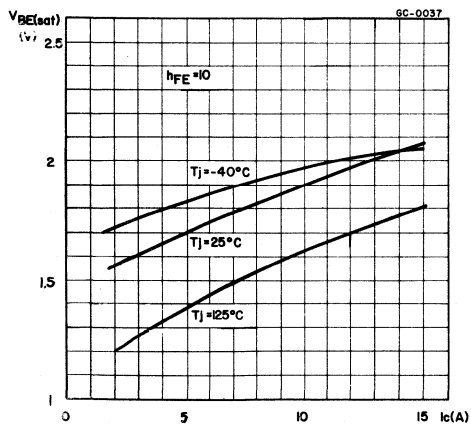
DC current gain



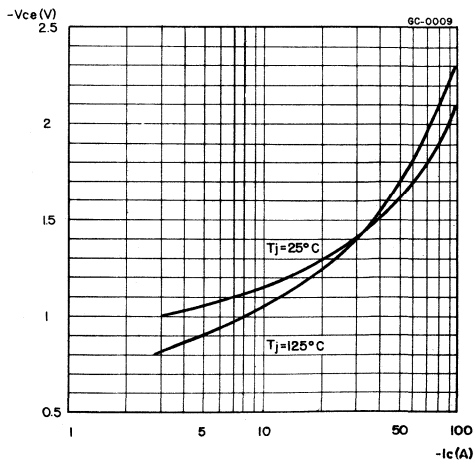
Collector-emitter saturation voltage



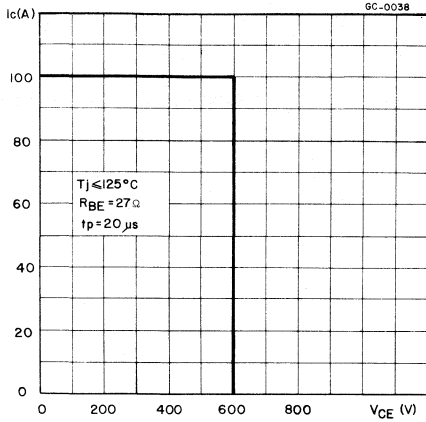
Base-emitter saturation voltage



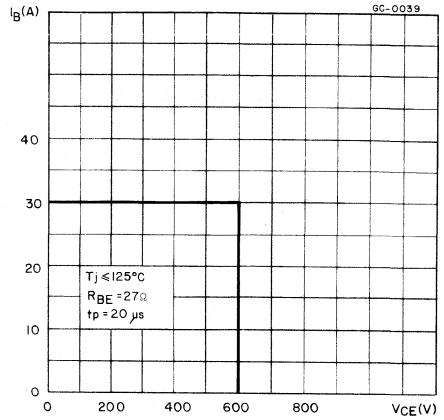
Typical V_F versus $-I_C$



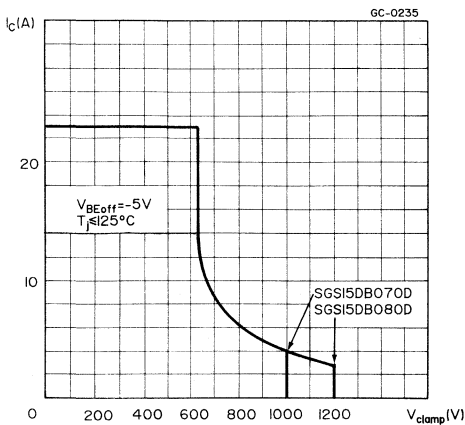
Collector overload SOA (see fig. 1)



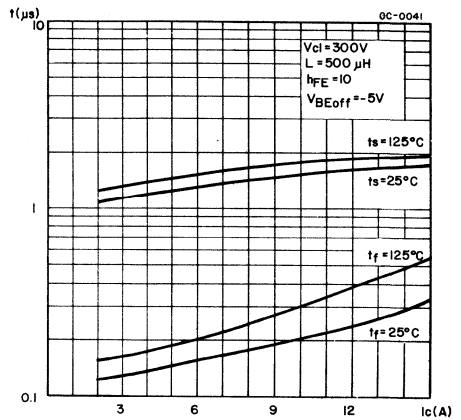
Base overload SOA (see fig. 1)



Reverse biased SOA (see fig. 2)



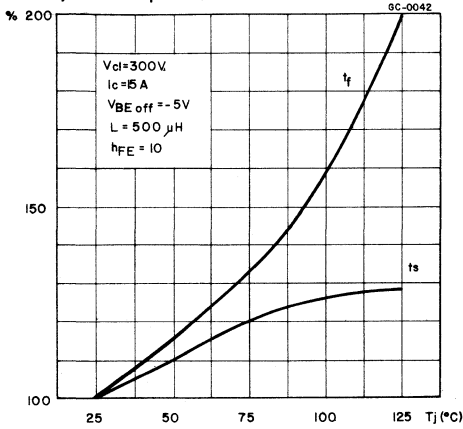
Switching times inductive load (see fig. 3)



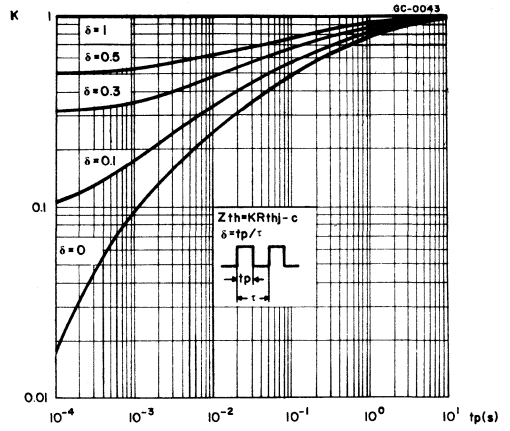


SGS15DB070D
SGS15DB080D

Switching times inductive load vs
junc. temp.

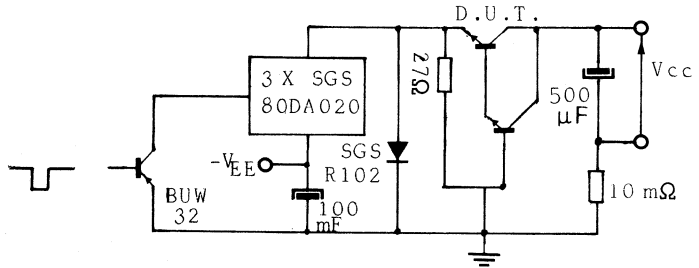


Thermal impedance



OVERLOAD

- Collector
Test circuit



OVERLOAD

- Base
Test circuit

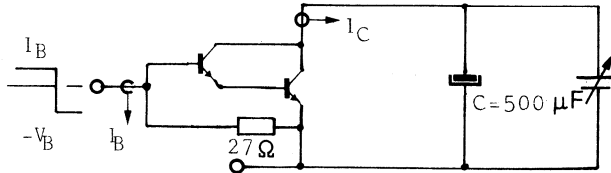
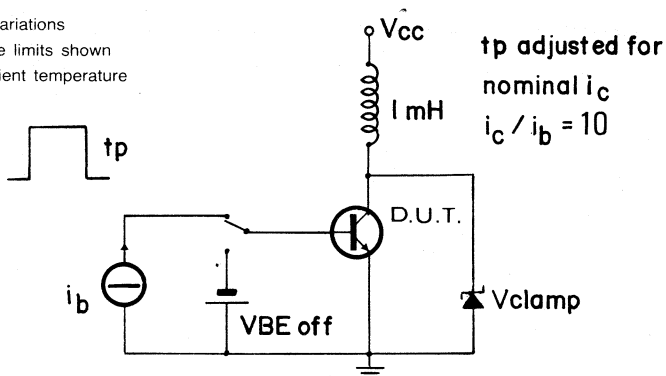


Fig. 1

SC-0001 a

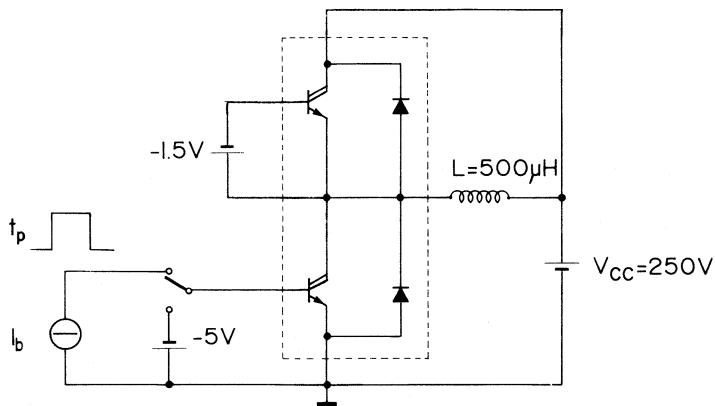
Fig. 2 RBSOA TEST CIRCUIT

RBSOA test circuit has been driven by the switching times test circuit with $R_{B2} = 0$. RBSOA sensitivity to T_j variations is very limited, so that the limits shown can be kept valid at ambient temperature as well.



SC-0002

Fig. 3 Switching times test circuit



SC-0160

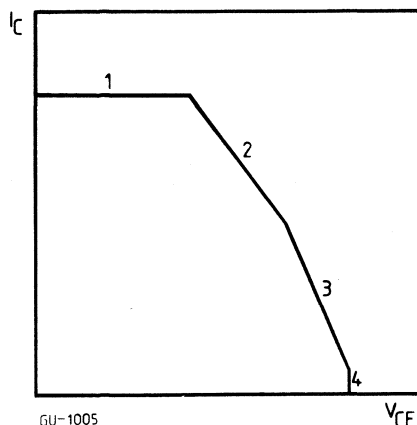
FORWARD BIAS SAFE OPERATING AREA

The I_C/V_{CE} limits of a transistor which have to be observed for reliable operation are specified by the safe operating area curves. The transistor must not be subjected to a greater dissipation than that indicated by the SOA boundary, operation outside these limits could result in either rapid or long term failure of the transistor.

The safe operating boundary is defined by four limits:

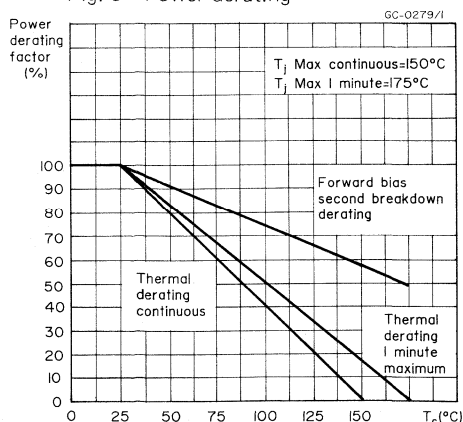
1. The limit of maximum current.
2. The limit of thermal dissipation.
3. The limit of secondary breakdown.
4. The limit of maximum voltage.

Fig. 4



Maximum voltage and current limits are fixed whereas thermal dissipation and secondary breakdown are dependant on the temperature. The normal figures given in the RBSOA diagram are tied to a fixed $T_C = 25^\circ\text{C}$ and for temperatures $>25^\circ\text{C}$ the Power Derating curve (fig. 5) has to be used. As thermal limitations do not derate in the same way as second breakdown limitations, the Power Derating diagram has two curves and the allowable current at the voltages shown on the RBSOA diagram may be found for any case temperature by using the appropriate power derating curve. For power levels under area 2 (fig. 4) the thermal derating curve is effective and for power levels under area 3, the second breakdown derating is used. At extreme case temperatures the thermal limitations reduce power handling to lower values than the limitations caused by second breakdown.

Fig. 5 - Power derating



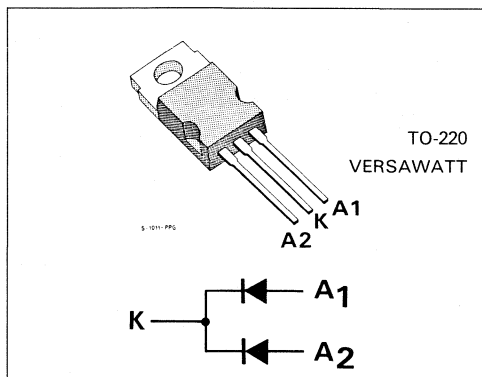


SGS16DR05
SGS16DR10
SGS16DR15
SGS16DR20

HIGH SPEED SWITCHING APPLICATIONS

- VOLTAGE RANGE: 50V→200V
- AVERAGE CURRENT: 16A
- VERY LOW REVERSE RECOVERY TIME: t_{rr} 35ns
- VERY LOW SWITCHING LOSSES
- LOW NOISE TURN-OFF SWITCHING

Typical applications include secondary rectification in high frequency switching power supplies.



ABSOLUTE MAXIMUM RATINGS

		SGS				
		16DR05	16DR10	16DR15	16DR20	
V _{RRM}	Peak repetitive reverse voltage	50	100	150	200	V
V _{RWM}	Working peak reverse voltage	50	100	150	200	V
V _R	Continuous reverse voltage	50	100	150	200	V
I _{FRM}	Repetitive peak forward current (t = 10μs)	120				A
I _{F(AV)}	Average forward current T _{case} = 70°C (switching operation, δ = 0.5)	16				A
I _{FSM}	Surge non repetitive forward current (t = 10ms)	100				A
P _{tot}	Total dissipation at T _{case} = 70°C	70				W
T _{stg}	Storage temperature	− 65 to 150				°C
T _j	Max. operating junction temperature	150				°C

THERMAL DATA

R _{thj-case}	Thermal resistance junction-case	max 1.15 °C/W
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ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified) (per leg)

Parameters	Test Contitions	Min.	Typ.	Max.	Unit
I _R Reverse Current	V = V _R T _j = 25°C V = V _R T _j = 100°C			10 0.6	μA mA
V _F (*) Forward voltage	I _F = 5A T _{case} = 100°C I _F = 20A T _{case} = 25°C I _F = 8A T _{case} = 25°C			0.85 1.3 1	V V V
t _{rr} Reverse recovery time	I _F = 1A di/dt = 50A/μs V _R = 30V I _F = 2A di/dt = 20A/μs V _R = 30V I _F = 5A di/dt = 20A/μs T _j = 100°C			35 50 70	ns ns ns
Q _{rr} Recovered charge	I _F = 2A di/dt = 20A/μs V _R = 30V			15	nC
V _{FP} Forward recovery overvoltage	I _F = 1A di/dt = 10A/μs		1		V

* Pulsed: pulse duration ≤300μs, duty cycle ≤2%

Fig. 1 Average forward current vs. air temperature and cooling system

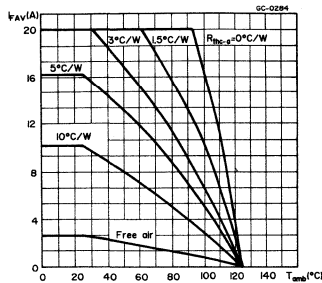


Fig. 2 Voltage drop vs. forward current

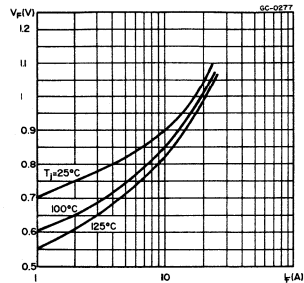


Fig. 3 Reverse leakage current vs. junction temperature.

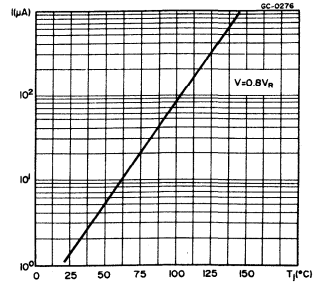


Fig. 4 Recovery time and peak reverse current vs. I_F

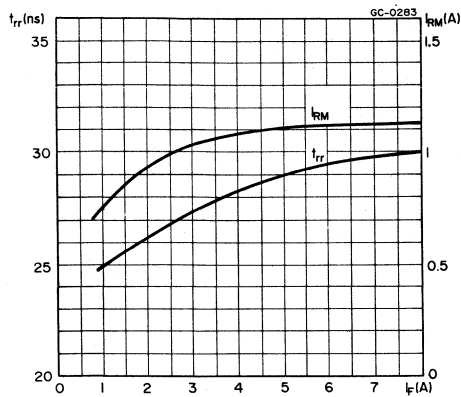


Fig. 5 Recovered time vs. di_F/dt

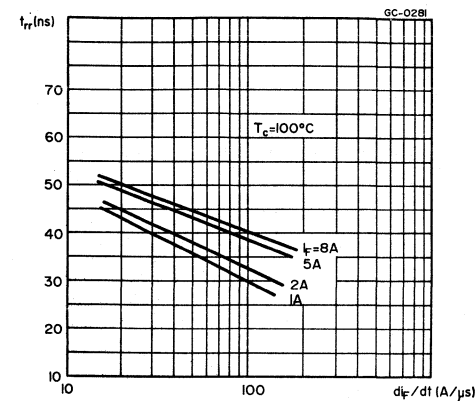


Fig. 6 Recovery charge vs. di_F/dt

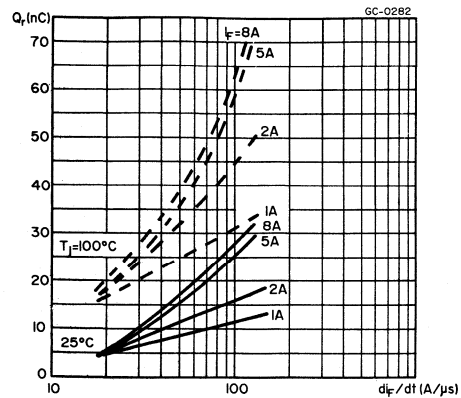
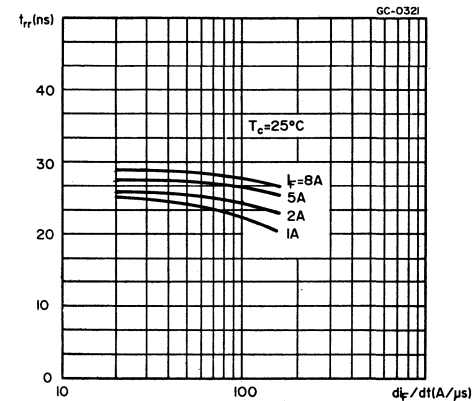


Fig. 7 Recovery time vs. di_F/dt





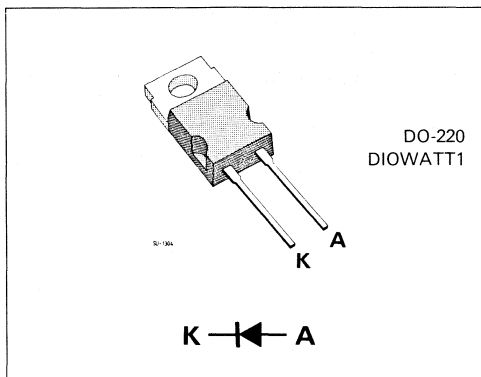
SGS20R05
SGS20R10
SGS20R15
SGS20R20

ADVANCE DATA

HIGH SPEED SWITCHING APPLICATIONS SECONDARY RECTIFICATION

- VOLTAGE RANGE: 50V → 200V
- AVERAGE CURRENT: 20A
- VERY LOW REVERSE RECOVERY TIME: t_{rr} 35ns
- VERY LOW SWITCHING LOSSES
- LOW NOISE TURN-OFF SWITCHING

Typical applications include secondary rectification in high frequency switching power supplies and freewheel diodes in stepper motor control systems.



ABSOLUTE MAXIMUM RATINGS

		SGS				
		20R05	20R10	20R15	20R20	
V_{RRM}	Peak repetitive reverse voltage	50	100	150	200	V
V_{RWM}	Working peak reverse voltage	50	100	150	200	V
V_R	Continuous reverse voltage	50	100	150	200	V
I_{FRM}	Repetitive peak forward current ($t = 10\mu s$)	250				A
$I_{F(AV)}$	Average forward current $T_{case} = 70^\circ C$ (switching operation, $\delta = 0.5$)	20				A
I_{FSM}	Surge non repetitive forward current ($t = 10ms$)	200				A
P_{tot}	Total dissipation at $T_{case} = 70^\circ C$	60				W
T_{stg}	Storage temperature	- 65 to 150				$^\circ C$
T_j	Max. operating junction temperature	150				$^\circ C$



SGS20R05
SGS20R10
SGS20R15
SGS20R20

THERMAL DATA

$R_{thj-case}$	Thermal resistance junction-case	max 1.4 °C/W
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ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

Parameters	Test Contitions	Min.	Typ.	Max.	Unit
I_R Reverse Current	$V = V_R$ $T_j = 25^{\circ}C$ $V = V_R$ $T_j = 100^{\circ}C$			40 1.5	μA mA
$V_F(*)$ Forward voltage	$I_F = 20A$ $T_{case} = 100^{\circ}C$ $I_F = 20A$ $T_{case} = 25^{\circ}C$			0.9 1	V V
t_{rr} Reverse recovery time	$I_F = 1A$ $di/dt = -50A/\mu s$ $V_R = 30V$ $I_F = 1A$ $di/dt = -20A/\mu s$ $V_R = 30V$			35 50	ns ns
Q_{rr} Recovered charge	$I_F = 2A$ $di/dt = -20A/\mu s$ $V_R = 30V$			8	nC
V_{FP} Forward recovery overvoltage	$I_F = 1A$ $di/dt = 10A/\mu s$		1		V

* Pulsed: pulse duration $\leq 300\mu s$, duty cycle $\leq 2\%$



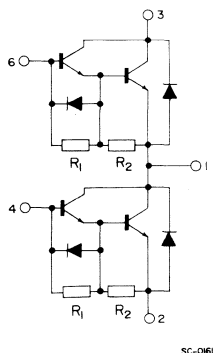
SGS25DB070D
SGS25DB080D

TRANSPACK NPN POWER DARLINGTON MODULE

APPLICATIONS: The SGS25DB070D and SGS25DB080D are silicon NPN power fast darlingtontons in half bridge configuration for industrial switching applications with three-phase mains operation.

ISOLATED POWER MODULE (24KVA-375W)		FAST FREEWHEEL DIODES	
ABSOLUTE MAXIMUM RATINGS		SGS25DB070D	SGS25DB080D
V _{CBO}	Collector-base voltage (I _E = 0)	1000	1200
V _{CES}	Collector-emitter voltage (V _{BE} = 0)	1000	1200
V _{CEX}	Collector-emitter voltage (V _{BE} = -1.5V)	1000	1200
V _{CEO}	Collector-emitter voltage (I _B = 0)	700	800
V _{CEOL}	Overload switch-off at 1.5 times I _{C (sat)} *	650	
V _{EBO}	Emitter-base voltage (I _C = 0)	7	
I _C	Collector current	37	
I _{CM}	Collector peak current (t _p <10 ms)	80	
I _{CP}	Collector peak current non repetitive (t _p <20 μs)	150	
I _B	Base current	9	
I _{BP}	Base peak current non repetitive (t _p <20 μs)	30	
T _{stg}	Storage temperature	- 40 to 150 °C	
T _j	Max. operating junction temperature (continuous)	150	°C
T _i	Max. operating junction temperature (1 minute)	175	°C

INTERNAL SCHEMATIC DIAGRAM

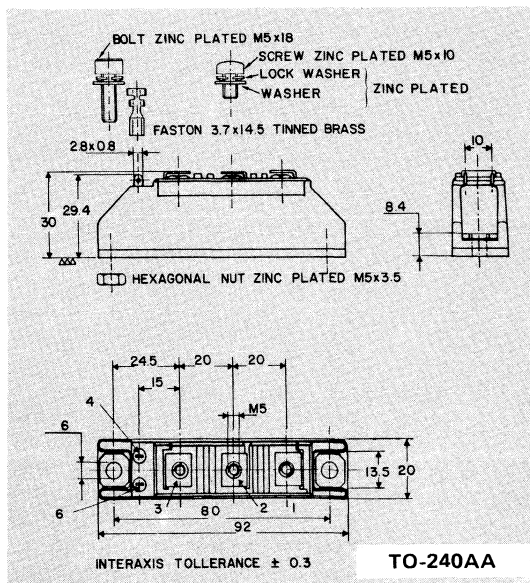


R_1 typ 10 Ω

R_2 typ 50 Ω

MECHANICAL DATA

Dimensions in mm





SGS25DB070D
SGS25DB080D

THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case (quarter bridge)	max 0.66	°C/W
$R_{th\ j-case}$	Thermal resistance junction-case (diode)	max 1.10	°C/W
$R_{th\ c-h}$	Thermal resistance case-heatsink	max 0.20	°C/W

ELECTRICAL CHARACTERISTICS

($T_j = 25^\circ\text{C}$ unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector cutoff current ($V_{BE} = 0$)	$V_{CE} = V_{CES}$		0.05	2	mA
		$V_{CE} = V_{CEOL}$ $T_j = 125^\circ\text{C}$		3	10	mA
I_{CEX}	Collector cutoff current	$V_{CE} = V_{CEX}$ $V_{BE} = -1.5\text{ V}$		0.05	2	mA
		$V_{CE} = V_{CEOL}$ $V_{BE} = -1.5\text{ V}$ $T_j = 125^\circ\text{C}$		3	10	mA
I_{EBO}	Emitter cutoff current ($I_C = 0$)	$V_{BE} = -2\text{ V}$			120	mA
$V_{CEO(sus)*}$	Collector emitter sustaining voltage	$I_C = 0.2\text{ A}$ for SGS25DB070D $L = 2\text{ mH}$ for SGS25DB080D	700 800			V V
V_{CEOL}	Max voltage to switch-off 1.5 times $I_{C(sat)}$ (top right corner of RBSOA)	$I_C = 37\text{ A}$	650			V
$V_{CE(sat)*}$	Collector-emitter saturation voltage	$I_C = 25\text{ A}$ $I_B = 2.5\text{ A}$		1.1	3	V
$V_{BE(sat)*}$	Base-emitter saturation voltage	$I_C = 25\text{ A}$ $I_B = 2.5\text{ A}$		1.9	3.5	V
h_{FE}^*	DC current gain	$I_C = 25\text{ A}$ $V_{CE} = 5\text{ V}$	30	60		
INDUCTIVE LOAD		(see test circuit)				
t_s	Storage time	$I_C = 25\text{ A}$ $I_B = 2.5\text{ A}$ $V_{BE\ OFF} = -5\text{ V}$		1.8		μs
t_f	Fall time	$V_{CC} = 250\text{ V}$ $L = 500\text{ }\mu\text{H}$ $V_{CL} = 300\text{ V}$		0.33		μs
t_s	Storage time	$I_C = 25\text{ A}$ $I_B = 2.5\text{ A}$ $V_{BE\ OFF} = -5\text{ V}$		2.40	5	μs
t_f	Fall time	$V_{CC} = 250\text{ V}$ $L = 500\text{ }\mu\text{H}$ $V_{CL} = 300\text{ V}$ $T_j = 125^\circ\text{C}$		0.66	1.5	μs

* Pulsed: Pulse duration = 300 μs , duty cycle = 1.5%.

ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_f	Diode forward voltage	$I_f = 25\text{ A}$		1.4	2	V
		$I_f = 25\text{ A } T_j = 125\text{ }^\circ\text{C}$		1.4		V
t_{rr}	Diode reverse recovery time	$I_f = 25\text{ A } di/dt = 100\text{A}/\mu\text{s}$		0.2	0.5	μs
I_{rm}	Diode reverse recovery time			12		A
I_{frm}	Diode forward current	$t = 1\text{ ms}$	200			A

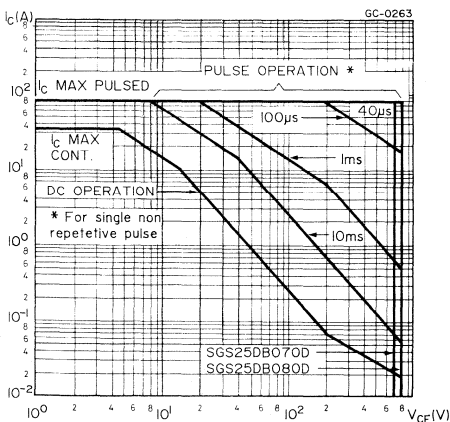
INSULATION TESTING

The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.

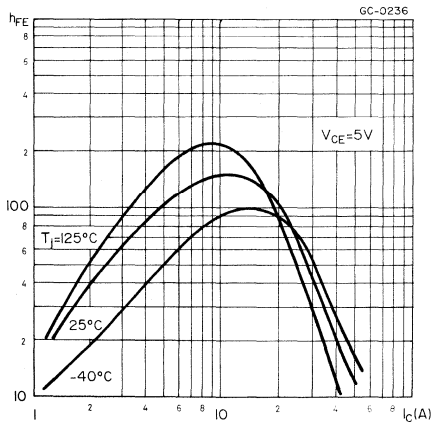
If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/VDE 0558 part 1/8.77, section 5.7.9., only a voltage slowly increasing up to the above value should be used. If the voltage is applied for one minute as recommended by the above standards then the specified value of 2000 V should be taken.

During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

Safe operating areas for each section



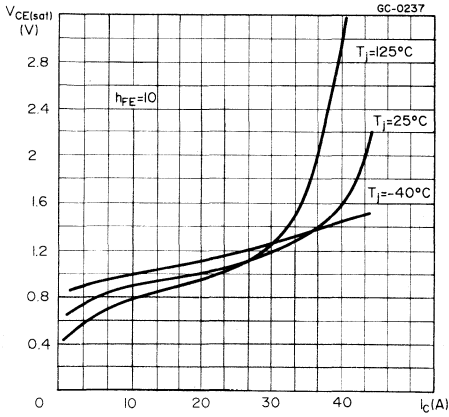
DC current gain



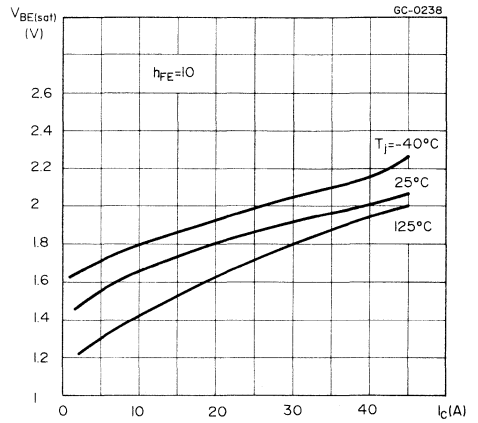


SGS25DB070D
SGS25DB080D

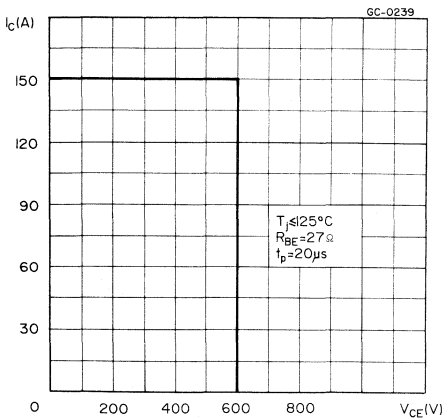
Collector-emitter saturation voltage



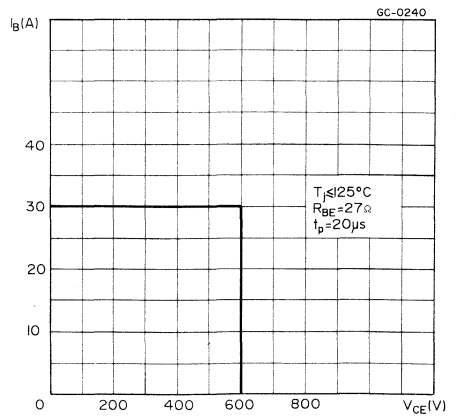
Base-emitter saturation voltage



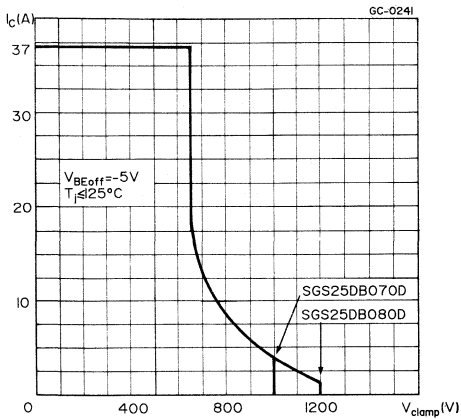
Collector overload SOA (see fig. 1)



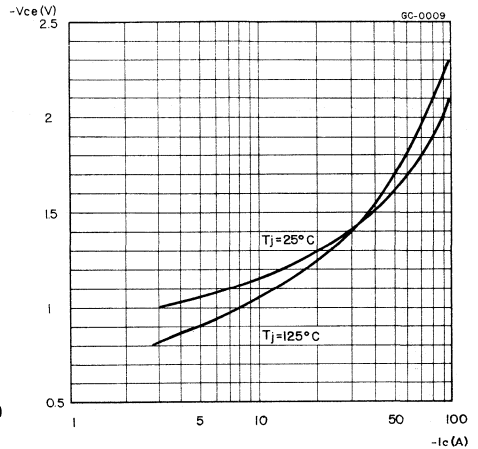
Base overload SOA (see fig. 1)



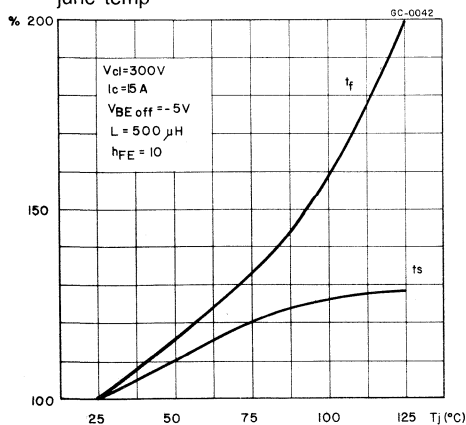
Reverse biased SOA (see fig. 2)



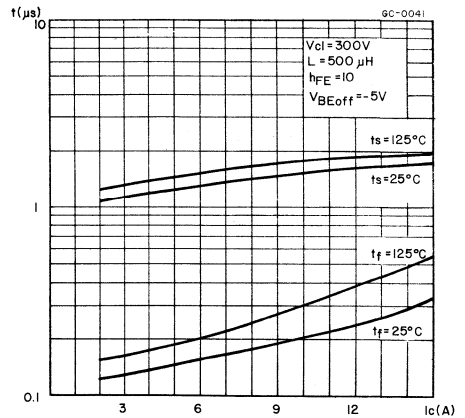
Typical V_F versus $-I_C$



Switching times inductive load vs
junc temp



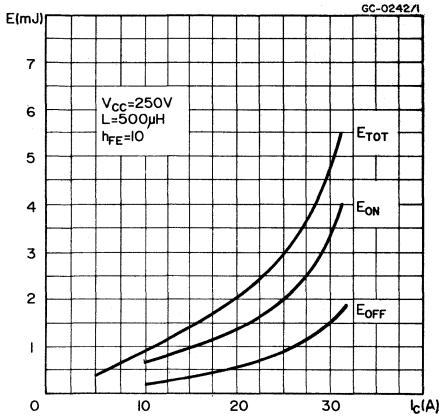
Switching times inductive load (see fig. 3)



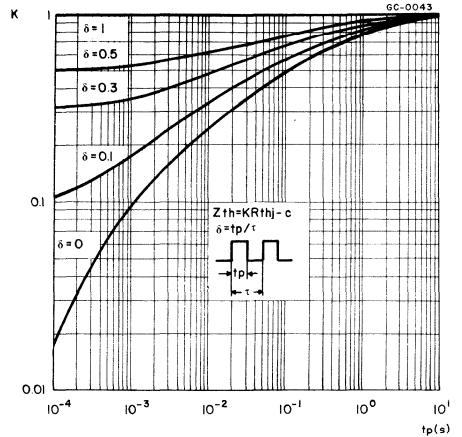


SGS25DB070D
SGS25DB080D

Switch energy losses (see fig. 3)

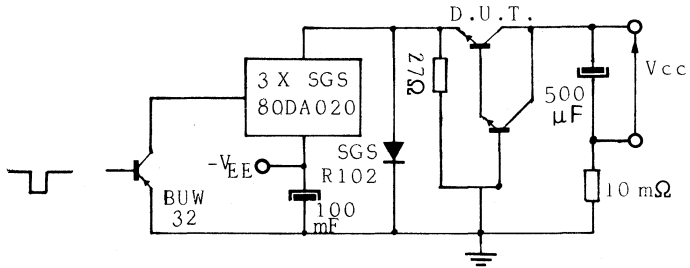


Thermal impedance



OVERLOAD

- Collector
Test circuit



OVERLOAD

- Base
Test circuit

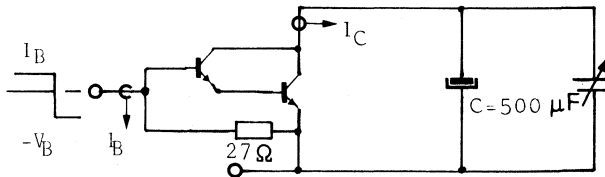


Fig. 1

SC-0001a

Fig. 2 RBSOA TEST CIRCUIT

RBSOA test circuit has been driven by the switching times test circuit with $R_{B2} = 0$. RBSOA sensitivity to T_j variations is very limited, so that the limits shown can be kept valid at ambient temperature as well.

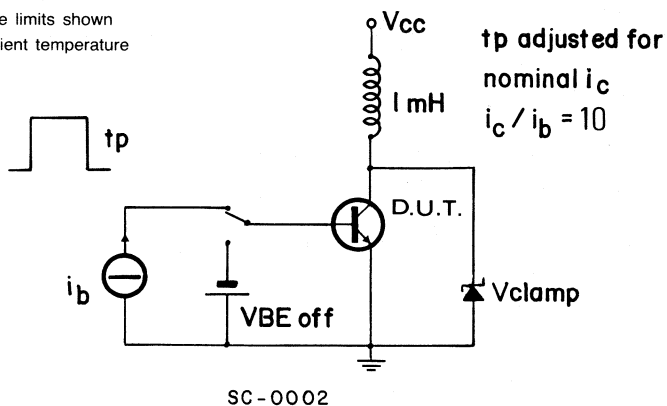
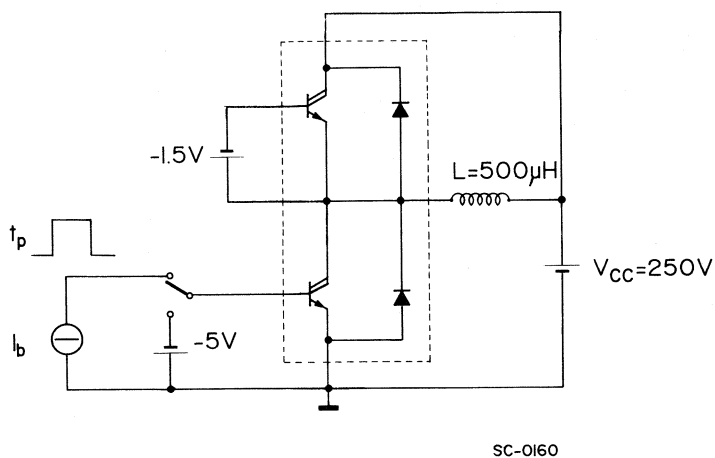


Fig. 3 Switching times test circuit





SGS25DB070D
SGS25DB080D

FORWARD BIAS SAFE OPERATING AREA

The I_C/V_{CE} limits of a transistor which have to be observed for reliable operation are specified by the safe operating area curves. The transistor must not be subjected to a greater dissipation than that indicated by the SOA boundary, operation outside these limits could result in either rapid or long term failure of the transistor.

The safe operating boundary is defined by four limits:

1. The limit of maximum current.
2. The limit of thermal dissipation.
3. The limit of secondary breakdown.
4. The limit of maximum voltage.

Maximum voltage and current limits are fixed whereas thermal dissipation and secondary breakdown are dependant on the temperature. The normal figures given in the RBSOA diagram are tied to a fixed $T_C = 25^\circ\text{C}$ and for temperatures $>25^\circ\text{C}$ the Power Derating curve (fig. 5) has to be used. As thermal limitations do not derate in the same way as second breakdown limitations, the Power Derating diagram has two curves and the allowable current at the voltages shown on the RBSOA diagram may be found for any case temperature by using the appropriate power derating curve. For power levels under area 2 (fig. 4) the thermal derating curve is effective and for power levels under area 3, the second breakdown derating is used. At extreme case temperatures the thermal limitations reduce power handling to lower values than the limitations caused by second breakdown.

Fig. 4

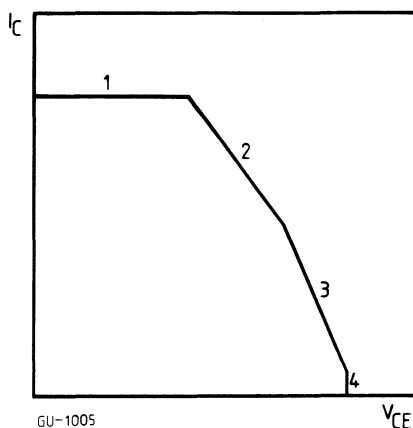
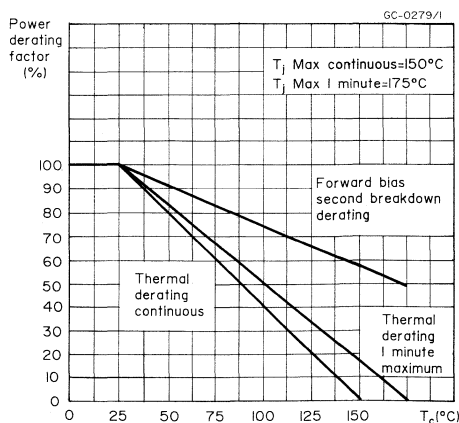


Fig. 5 - Power derating





SGS30DA060D
SGS30DA070D

TRANSPACK NPN POWER DARLINGTON MODULE

APPLICATIONS: These products are silicon NPN power darlingtontons for industrial switching applications with three-phase mains operation.

ISOLATED POWER MODULE (30KVA - 375W)

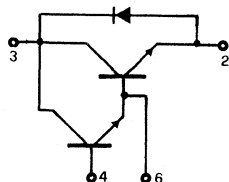
FAST FREEWHEEL DIODE

ABSOLUTE MAXIMUM RATINGS

V_{CBO}	Collector-base voltage ($I_E = 0$)
V_{CES}	Collector-emitter voltage ($V_{BE} = 0$)
V_{CEX}	Collector-emitter voltage ($V_{BE} = -1.5V$)
V_{CEO}	Collector-emitter voltage ($I_B = 0$)
V_{CEOL}	Overload switch-off at 1.5 times $I_{C(sat)}$
V_{EBO}	Emitter-base voltage ($I_C = 0$)
I_C	Collector current
I_{CM}	Collector peak current ($t_p < 10$ ms)
I_{CP}	Collector peak current non repetitive ($t_p < 20$ μ s)
I_B	Base current
I_{BP}	Base peak current non repetitive ($t_p < 20$ μ s)
T_{stg}	Storage temperature
T_J	Max. operating junction temperature (continuous)
T_J	Max. operating junction temperature (1 minute)

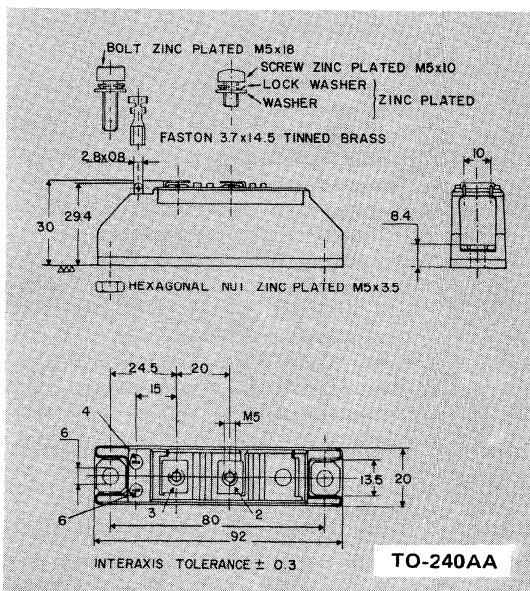
SGS30DA060D	SGS30DA070D	
1000	1200	V
1000	1200	V
1000	1200	V
600	700	V
	650	V
	7	V
	45	A
	120	A
	200	A
	3	A
	20	A
	- 40 to 150	$^{\circ}C$
	150	$^{\circ}C$
	175	$^{\circ}C$

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case (darlington)	max 0.33°C/W
$R_{th\ j-case}$	Thermal resistance junction-case (diode)	max 1.10°C/W
$R_{th\ c-h}$	Thermal resistance case-heatsink	max 0.20°C/W

ELECTRICAL CHARACTERISTICS

($T_j = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CER} Collector cutoff current ($R_{BE1} = 3.3\text{Kohm}$ $R_{BE2} = 100\text{ohm}$)	$V_{CE} = V_{CEOL}$			2	mA
	$V_{CE} = V_{CEOL} \quad T_j = 125^\circ\text{C}$			10	mA
I_{CES} Collector cutoff current ($V_{BE1} = V_{BE2} = 0$)	$V_{CE} = V_{CES}$		0.05	2	mA
	$V_{CE} = V_{CEOL} \quad T_j = 125^\circ\text{C}$		3	10	mA
I_{CEX} Collector cutoff current	$V_{CE} = V_{CEX} \quad V_{BE} = -1.5\text{V}$		0.05	2	mA
	$V_{CE} = V_{CEOL} \quad V_{BE} = -1.5\text{V} \quad T_j = 125^\circ\text{C}$		3	10	mA
I_{EBO} Emitter cutoff current ($I_C = 0$)	$V_{BE} = -5\text{V}$			2	mA
$V_{CEO(sus)*}$ Collector emitter sustaining voltage	$I_C = 0.2\text{A}$ for SGS30DA060D $L = 2\text{mH}$ for SGS30DA070D	600 700			V V
V_{CEOL} Max voltage to switch-off 1.5 times $I_C(sat)$ (top right corner of RBSOA)	$I_C = 45\text{A}$	650			V
$V_{CE(sat)*}$ Collector-emitter saturation voltage	$I_C = 30\text{A} \quad I_B = 1.5\text{A}$		2.2	2.5	V
$V_{BE(sat)*}$ Base-emitter saturation voltage	$I_C = 30\text{A} \quad I_B = 1.5\text{A}$			2.8	V
h_{FE*} DC current gain	$I_C = 30\text{A} \quad V_{CE} = 5\text{V}$	80	100		
INDUCTIVE LOAD (see test circuit)					
t_s Storage time	$I_C = 30\text{A} \quad I_B = 1.5\text{A} \quad V_{BE\ OFF} = -5\text{V}$		2.20		μs
t_f Fall time	$V_{CC} = 50\text{V} \quad L = 500\text{ }\mu\text{H} \quad V_{CL} = 300\text{V}$ $T_j = 25^\circ\text{C}$		0.36		μs
t_s Storage time	$I_C = 30\text{A} \quad I_B = 1.5\text{A} \quad V_{BE\ OFF} = -5\text{V}$		3	6	μs
t_f Fall time	$V_{CC} = 50\text{V} \quad L = 500\text{ }\mu\text{H} \quad V_{CL} = 300\text{V}$ $T_j = 125^\circ\text{C}$		0.45	0.8	μs

* Pulsed: Pulse duration = 300 μs , duty cycle = 1.5%.

ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_f Diode forward voltage	$I_f = 30\text{ A}$ $T_j = 25^\circ\text{C}$ $T_j = 125^\circ\text{C}$		1.4 1.4	2	V V
t_{rr} Diode reverse recovery time	$I_f = 30\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$		0.2	0.5	μs
I_{rm} Diode reverse recovery current			10		A
I_{frrm} Diode forward current	$t = 1\text{ ms}$	200			A

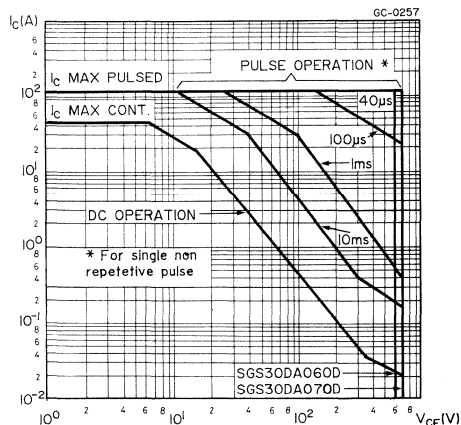
INSULATION TESTING

The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.

If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/VDE 0558, section 5.7.9., only a voltage slowly increasing up to the above value should be used. If the voltage is applied for one minute as recommended by the above standards then the specified value of 2000 V should be taken.

During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

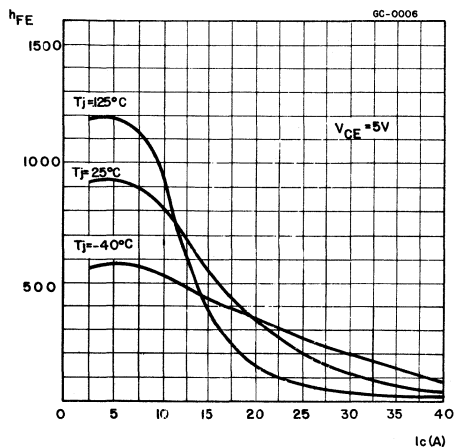
Safe operating areas



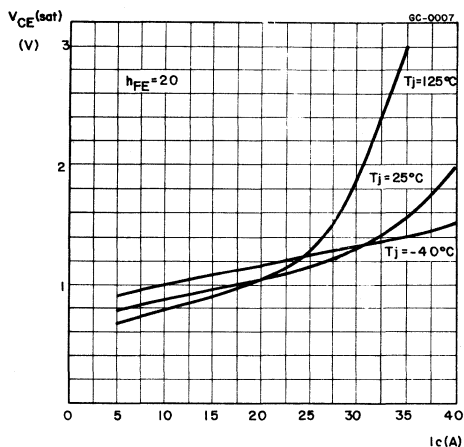


SGS30DA060D
SGS30DA070D

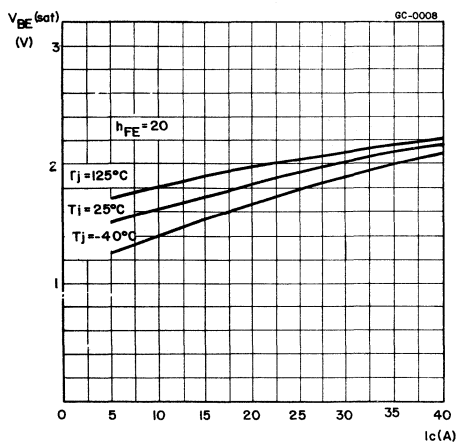
DC current gain



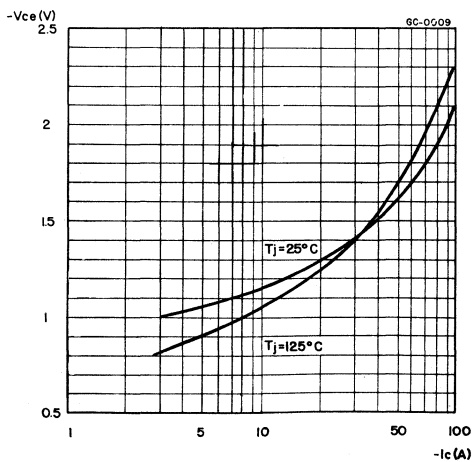
Collector-emitter saturation voltage



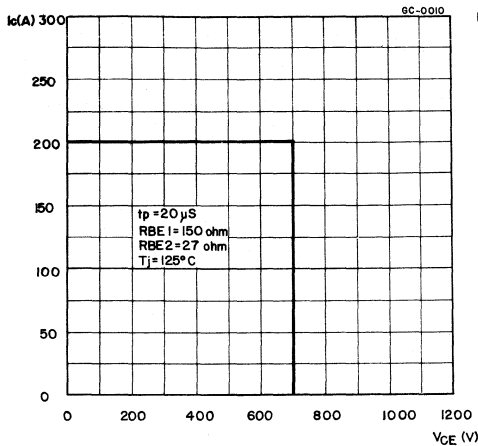
Base-emitter saturation voltage



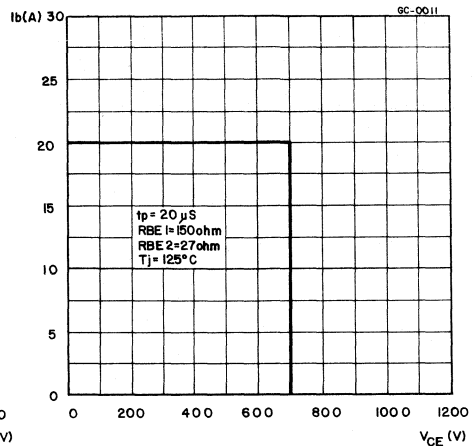
Typical V_F versus $-I_c$



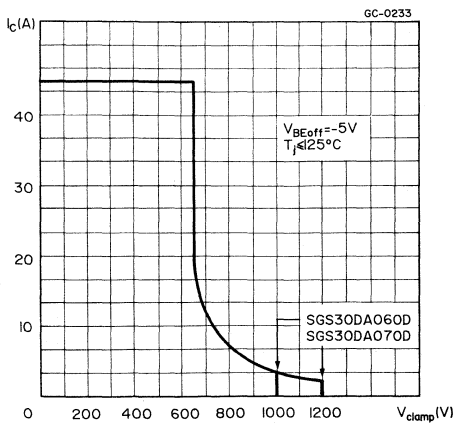
Collector overload SOA (see fig. 1)



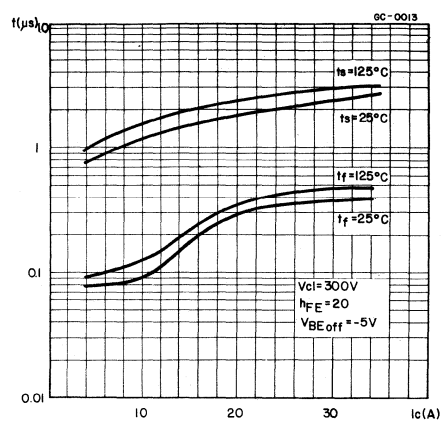
Base overload SOA (see fig. 1)



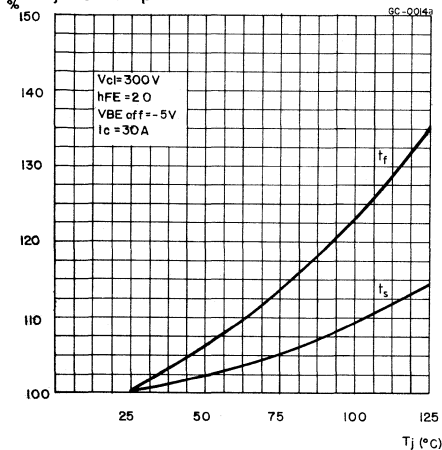
Reverse biased SOA (see fig. 2)



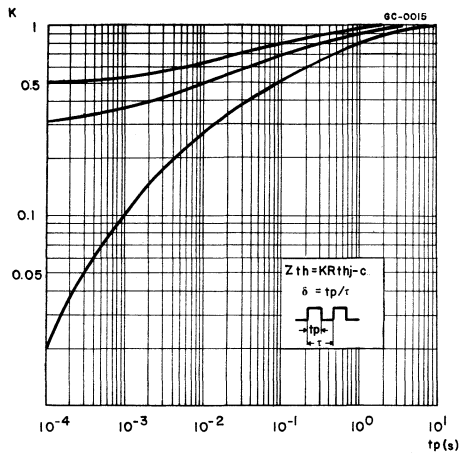
Switching times inductive load (see fig. 3)



Switching times inductive load vs junc. temp.



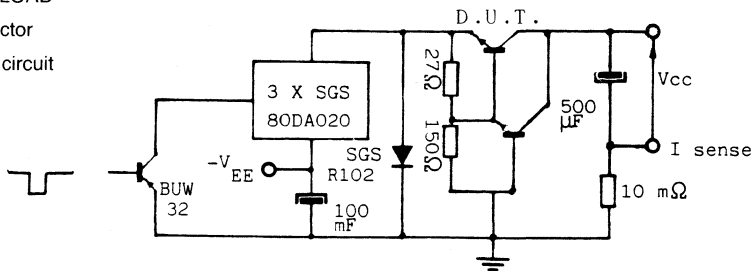
Thermal impedance



OVERLOAD

- Collector

Test circuit



OVERLOAD

- Base

Test circuit

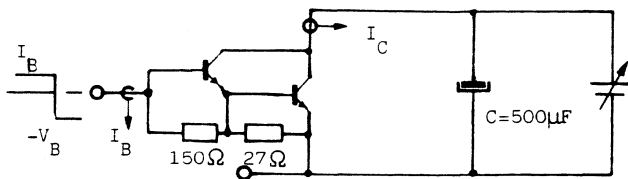
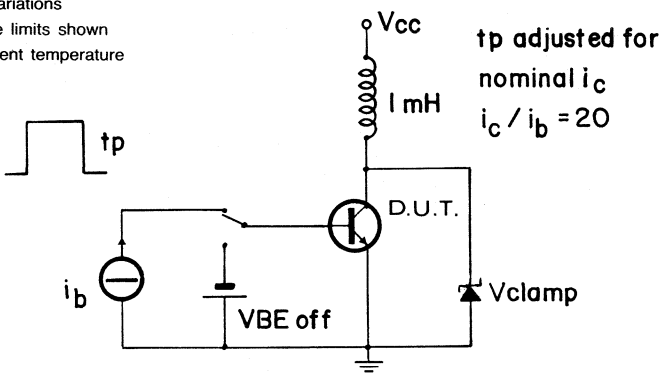


Fig. 1

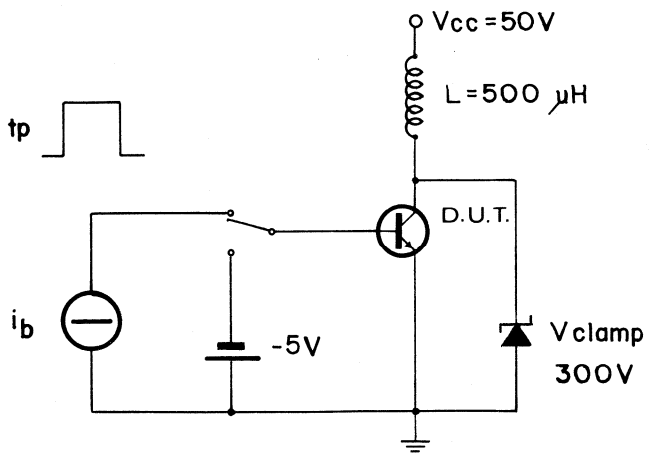
Fig. 2 RBSOA TEST CIRCUIT

RBSOA test circuit has been driven by the switching times test circuit with $R_{B2} = 0$. RBSOA sensitivity to T_j variations is very limited, so that the limits shown can be kept valid at ambient temperature as well.



SC-0002

Fig. 3 Switching times test circuit.



SC-0003

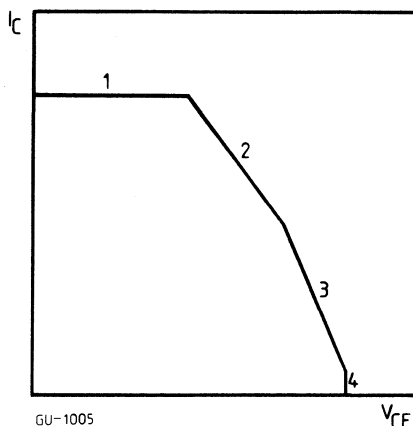
FORWARD BIAS SAFE OPERATING AREA

The I_C/V_{CE} limits of a transistor which have to be observed for reliable operation are specified by the safe operating area curves. The transistor must not be subjected to a greater dissipation than that indicated by the SOA boundary, operation outside these limits could result in either rapid or long term failure of the transistor.

The safe operating boundary is defined by four limits:

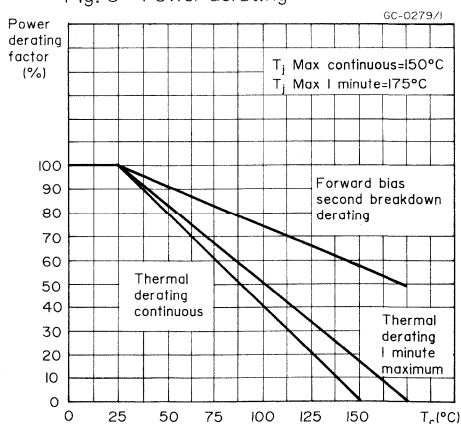
1. The limit of maximum current.
2. The limit of thermal dissipation.
3. The limit of secondary breakdown.
4. The limit of maximum voltage.

Fig. 4



Maximum voltage and current limits are fixed whereas thermal dissipation and secondary breakdown are dependant on the temperature. The normal figures given in the RBSOA diagram are tied to a fixed $T_C = 25^\circ\text{C}$ and for temperatures $>25^\circ\text{C}$ the Power Derating curve (fig. 5) has to be used. As thermal limitations do not derate in the same way as second breakdown limitations, the Power Derating diagram has two curves and the allowable current at the voltages shown on the RBSOA diagram may be found for any case temperature by using the appropriate power derating curve. For power levels under area 2 (fig. 4) the thermal derating curve is effective and for power levels under area 3, the second breakdown derating is used. At extreme case temperatures the thermal limitations reduce power handling to lower values than the limitations caused by second breakdown.

Fig. 5 - Power derating





SGS30DB040D
SGS30DB045D

TRANSPACK NPN POWER DARLINGTON MODULE

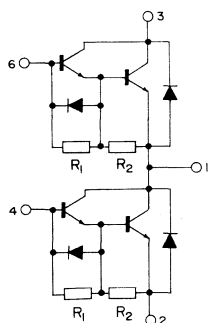
APPLICATIONS: These products are silicon NPN power fast darlingtontons in half bridge configuration for industrial switching applications from the mains.

ISOLATED POWER MODULE (15KVA - 375W)

FAST FREEWHEEL DIODES

ABSOLUTE MAXIMUM RATINGS	SGS30DB040D	SGS30DB045D	
V_{CBO} Collector-base voltage ($I_E = 0$)	500	600	V
V_{CES} Collector-emitter voltage ($V_{BE} = 0$)	500	600	V
V_{CEX} Collector-emitter voltage ($V_{BE} = -1.5V$)	500	600	V
V_{CEO} Collector-emitter voltage ($I_B = 0$)	400	450	V
V_{CEOL} Overload switch-off at 1.5 times $I_{C(sat)}$	400		V
V_{EBO} Emitter-base voltage ($I_C = 0$)	7		V
I_C Collector current	45		A
I_{CM} Collector peak current ($t_p < 10$ ms)	60		A
I_{CP} Collector peak current non repetitive ($t_p < 20$ μ s)	200		A
I_B Base current	6		A
I_{BP} Base peak current non repetitive ($t_p < 20$ μ s)	10		A
T_{stg} Storage temperature	- 40 to 150		°C
T_j Max. operating junction temperature (continuous)	150		°C
T_j Max. operating junction temperature (1 minute)	175		°C

INTERNAL SCHEMATIC DIAGRAM

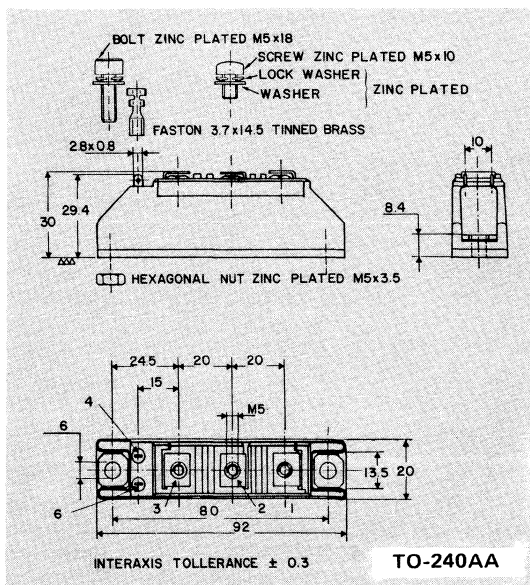


R_1 typ. 80 Ω

R_2 typ. 150 Ω

MECHANICAL DATA

Dimensions in mm





THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case (quarter bridge)	max 0.66°C/W
$R_{th\ j-case}$	Thermal resistance junction-case (diode)	max 1.10°C/W
$R_{th\ c-h}$	Thermal resistance case- heatsink	max 0.20°C/W

ELECTRICAL CHARACTERISTICS

($T_j = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES} Collector cutoff current ($V_{BE} = 0$)	$V_{CE} = V_{CES}$			2	mA
	$V_{CE} = V_{CEOL}$ $T_j = 125^\circ\text{C}$		3	10	mA
I_{CEX} Collector cutoff current	$V_{CE} = V_{CEX}$ $V_{BE} = -1.5\text{V}$			2	mA
	$V_{CE} = V_{CEOL}$ $V_{BE} = -1.5\text{V}$ $T_j = 125^\circ\text{C}$		3	10	mA
I_{EBO} Emitter cutoff current ($I_C = 0$)	$V_{BE} = -2\text{V}$			90	mA
$V_{CEO(sus)*}$ Collector emitter sustaining voltage	$I_C = 0.2\text{ A}$ for SGS30DB040D $L = 2\text{mH}$ for SGS30DB045D	400			V
		450			V
V_{CEOL} Max voltage to switch-off 1.5 times $I_{C(sat)}$ (top right corner of RBSOA)	$I_C = 45\text{A}$	400			V
$V_{CE(sat)*}$ Collector-emitter saturation voltage	$I_C = 30\text{ A}$ $I_B = 2\text{ A}$ $I_C = 30\text{ A}$ $I_B = 2\text{ A}$ $T_j = 125^\circ\text{C}$ $I_C = 40\text{ A}$ $I_B = 4\text{ A}$ for SGS30DB040D for SGS30DB045D		1.5	3	V
			1.8		V
			1.9	2.5	V
			2.0	3.0	V
$V_{BE(sat)*}$ Base-emitter saturation voltage	$I_C = 40\text{ A}$ $I_B = 4\text{ A}$ $I_C = 40\text{ A}$ $I_B = 4\text{ A}$ $T_j = 125^\circ\text{C}$		2.6	3.3	V
			2.6		V
h_{FE}^* DC current gain	$I_C = 30\text{ A}$ $V_{CE} = 5\text{ V}$	40	50		
INDUCTIVE LOAD (see test circuit)					
t_s Storage time	$I_C = 30\text{A}$ $I_B = 2\text{ A}$ $V_{BE\ off} = -5\text{ V}$ $V_{CC} = 50\text{V}$ $L = 500\text{ }\mu\text{H}$ $V_{CL} = 300\text{V}$ $T_j = 25^\circ\text{C}$		1.20		μs
t_f Fall time			0.15		μs
t_s Storage time	$I_C = 30\text{A}$ $I_B = 2\text{ A}$ $V_{BE\ off} = -5\text{ V}$ $V_{CC} = 50\text{V}$ $L = 500\text{ }\mu\text{H}$ $V_{CL} = 300\text{V}$ $T_j = 125^\circ\text{C}$			3.0	μs
t_f Fall time			0.20	0.7	μs

* Pulsed: Pulse duration = 300 μs , duty cycle = 1.5%.

ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_f	Diode forward voltage	$I_f = 30\text{ A}$ $T_j = 25^\circ\text{C}$ $T_j = 125^\circ\text{C}$		1.30 1.20	2.0	V V
t_{rr}	Diode reverse recovery time	$I_f = 30\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$		0.20	0.5	μs
I_{rm}	Diode reverse recovery current			10		A
I_{frm}	Diode forward current	$t = 1\text{ ms}$	250			A

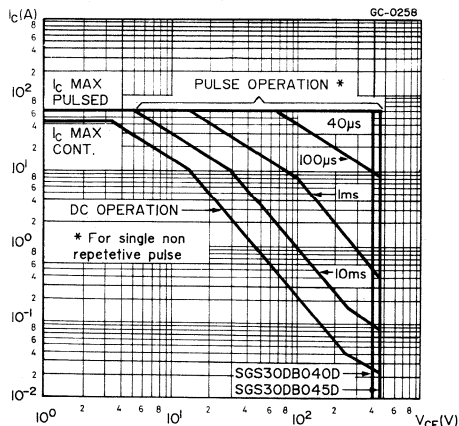
INSULATION TESTING

The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.

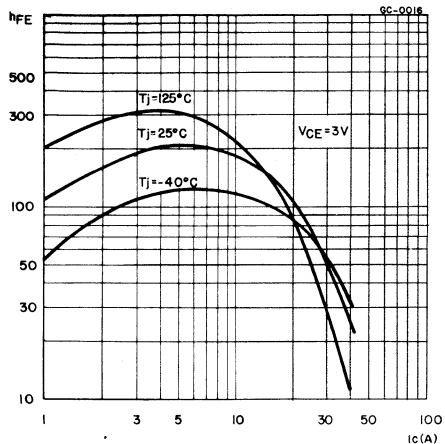
If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/8.77, section 5.7.9., only a voltage slowly increasing up to the above value should be used. If the voltage is applied for one minute as recommended by the above standards then the specified value of 2000 V should be taken.

During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

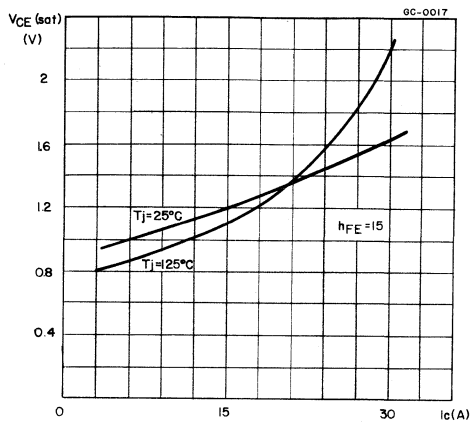
Safe operating areas for each section



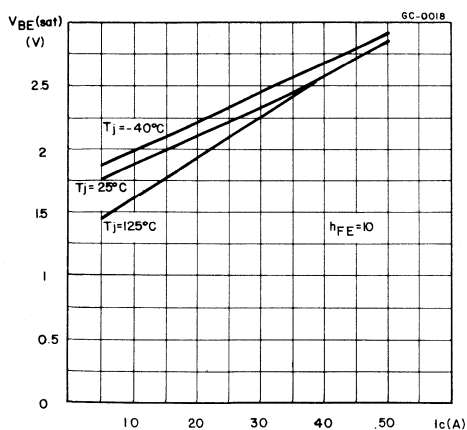
DC current gain



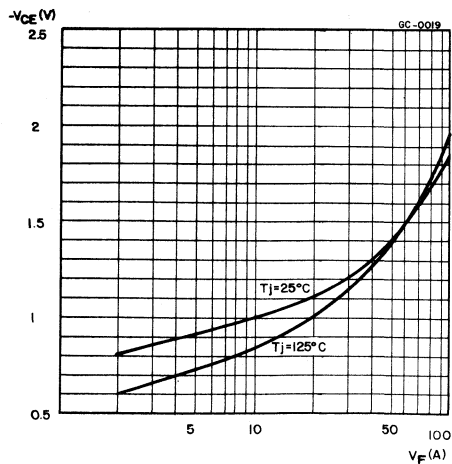
Collector-emitter saturation voltage



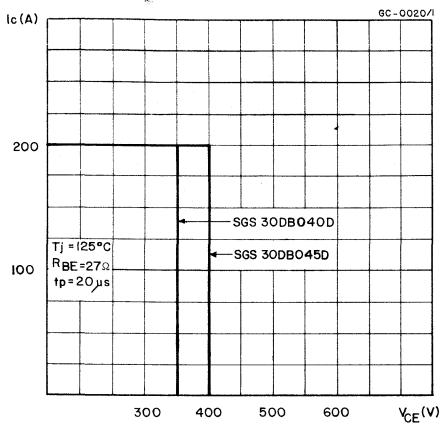
Base-emitter saturation voltage



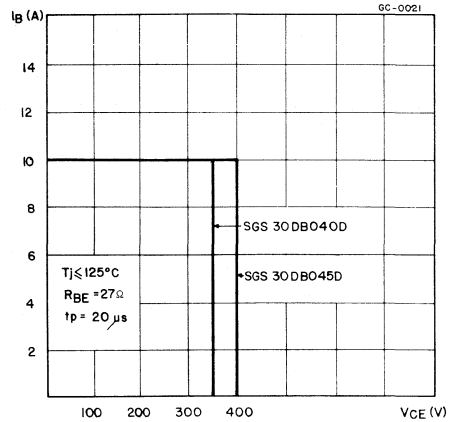
Typical V_F versus - I_C



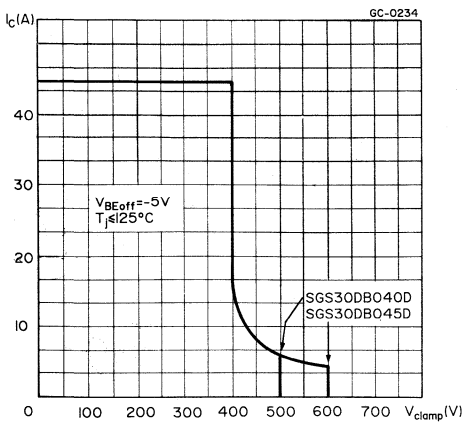
Collector overload SOA (see fig. 1)



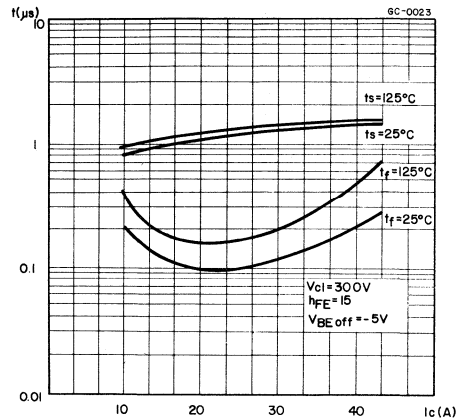
Base overload SOA (see fig. 1)



Reverse biased SOA (see fig. 2)



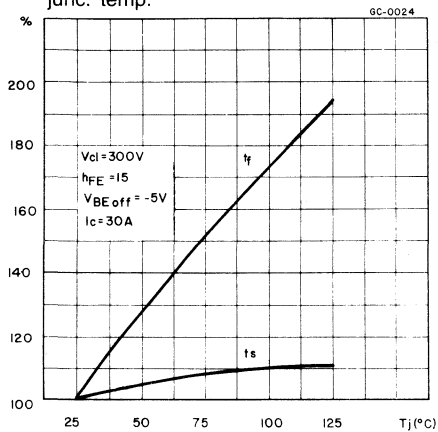
Switching times inductive load (see fig. 3)



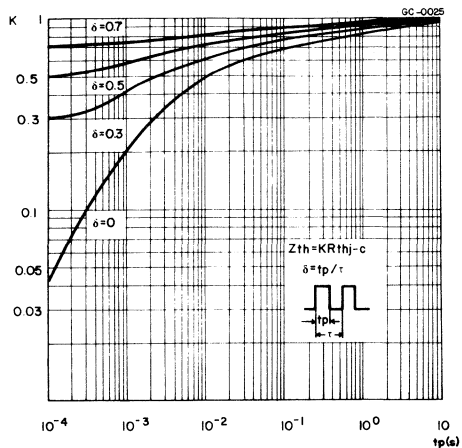


SGS30DB040D
SGS30DB045D

Switching times inductive load vs
junc. temp.

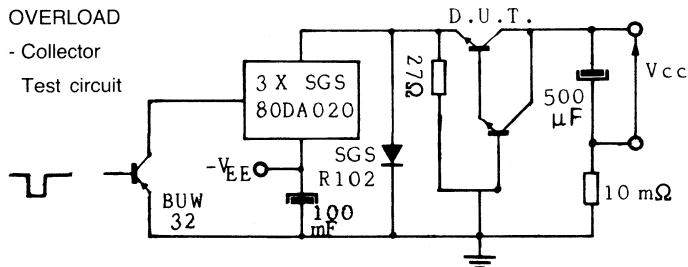


Thermal impedance



OVERLOAD

- Collector
Test circuit



OVERLOAD

- Base
Test circuit

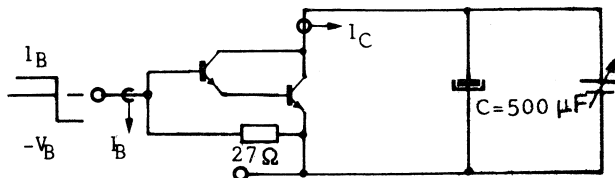


Fig. 1

Fig. 2 RBSOA TEST CIRCUIT

RBSOA test circuit has been driven by the switching times test circuit with $R_{B2} = 0$. RBSOA sensitivity to T_J variations is very limited, so that the limits shown can be kept valid at ambient temperature as well.

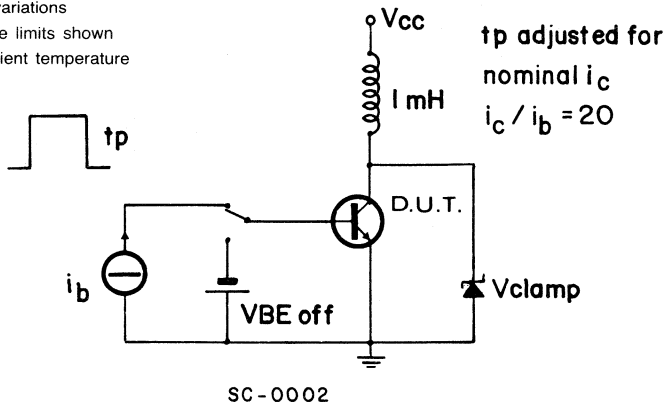
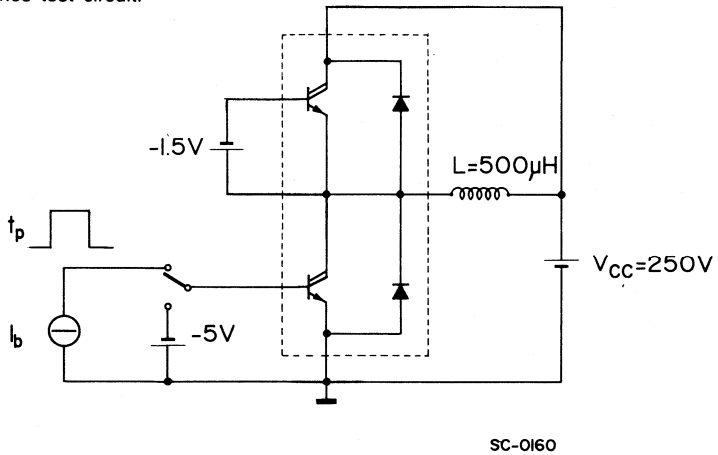


Fig. 3 Switching times test circuit.





FORWARD BIAS SAFE OPERATING AREA

The I_C/V_{CE} limits of a transistor which have to be observed for reliable operation are specified by the safe operating area curves. The transistor must not be subjected to a greater dissipation than that indicated by the SOA boundary, operation outside these limits could result in either rapid or long term failure of the transistor.

The safe operating boundary is defined by four limits:

1. The limit of maximum current.
2. The limit of thermal dissipation.
3. The limit of secondary breakdown.
4. The limit of maximum voltage.

Maximum voltage and current limits are fixed whereas thermal dissipation and secondary breakdown are dependant on the temperature. The normal figures given in the RBSOA diagram are tied to a fixed $T_C = 25^\circ\text{C}$ and for temperatures $>25^\circ\text{C}$ the Power Derating curve (fig. 5) has to be used. As thermal limitations do not derate in the same way as second breakdown limitations, the Power Derating diagram has two curves and the allowable current at the voltages shown on the RBSOA diagram may be found for any case temperature by using the appropriate power derating curve. For power levels under area 2 (fig. 4) the thermal derating curve is effective and for power levels under area 3, the second breakdown derating is used. At extreme case temperatures the thermal limitations reduce power handling to lower values than the limitations caused by second breakdown.

Fig. 4

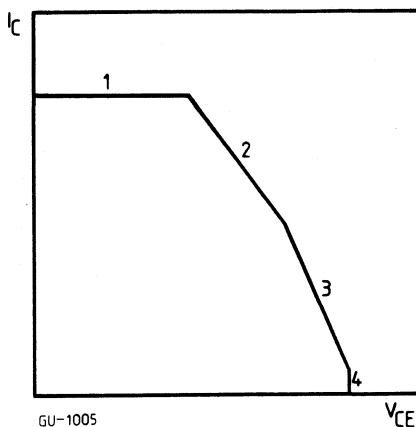
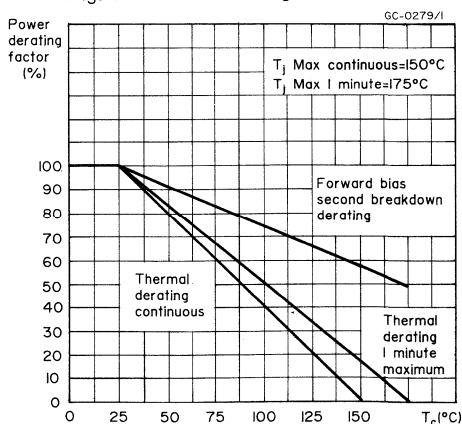


Fig. 5 - Power derating





SGS30MA050D1

ADVANCE DATA

TRANSPACK N-CHANNEL POWER MOS MODULE

APPLICATIONS: The SGS30MA050D1 is a N-Channel POWER MOS MODULE for industrial applications (quarter bridge configuration).

ISOLATED POWER MODULE (15KVA - 375W)

INTERNAL FREEWHEEL DIODE

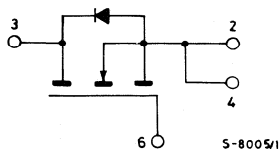
ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)
V_{DGR}	Drain-gate voltage ($R_{GS} = 20\text{ K}\Omega$)
V_{GS}	Gate-source voltage
I_D	Drain current (continuous) $T_C = 25^\circ\text{C}$
I_{DM}	Drain current ($t_p < 10\text{ ms}$, repetitive)
I_{DLM}	Drain current ($t_p = 20\mu\text{s}$, not repetitive)
P_{tot}	Total dissipation at $T_C < 25^\circ\text{C}$
	Derating factor
T_{stg}	Storage temperature
T_j	Max. operating junction temperature (continuous)
T_j	Max. operating junction temperature (1 minute)

SGS30MA050D1

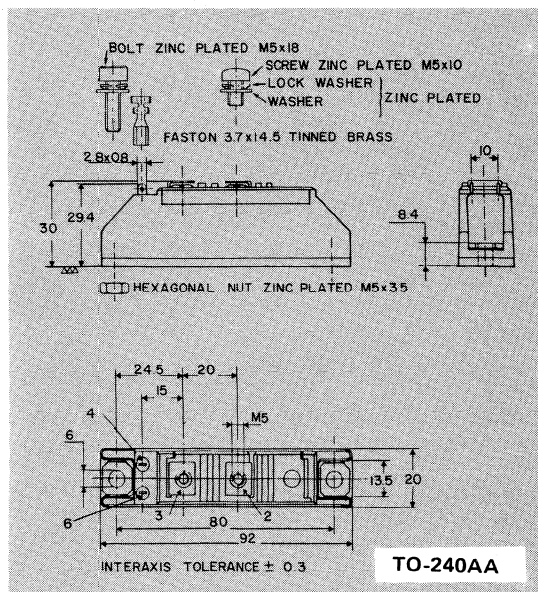
500	V
500	V
± 20	V
30	A
45	A
75	A
300	W
3	W/ $^\circ\text{C}$
-55 to 150	$^\circ\text{C}$
150	$^\circ\text{C}$
175	$^\circ\text{C}$

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm





THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max 0.33	°C/W
$R_{th\ c-h}$	Thermal resistance case-heatsink	max 0.20	°C/W

ELECTRICAL CHARACTERISTICS

($T_j = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
-----------	-----------------	------	------	------	------

OFF

$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 2\text{ mA}$ $V_{GS} = 0$	500			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$			2	mA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			100	nA

ON (*)

$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 2\text{ mA}$	2		4	V
$V_{DS(on)}$	Drain-source voltage	$V_{GS} = 10\text{V}$ $I_D = 30\text{ A}$ $V_{GS} = 10\text{V}$ $I_D = 15\text{ A}$		5.4 2.7	3.75	V V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$ $I_D = 15\text{ A}$		0.18	0.25	Ω
g_{fs}	Forward transconductance	$V_{DS} = 25\text{V}$ $I_D = 15\text{ A}$	.36	50		mho

DYNAMIC

C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$	7000			pF
C_{oss}	Output capacitance		1500			pF
C_{rss}	Reverse transfer capacitance		1000			pF

SWITCHING TIMES INDUCTIVE LOAD (see note A)

$t_{d(on)}$	Turn-on time	$V_{CC} = 250\text{ V}$ $I_D = 30\text{ A}$ $V_i = 10\text{ V}$ $R_i = 50\text{ }\Omega$	100			ns
$(di/dt)_{on}$	Turn-on current slope		150			A/ μs
$t_{d(off)}$	Turn-off delay time		1.1			μs
t_f	Fall time		130			ns

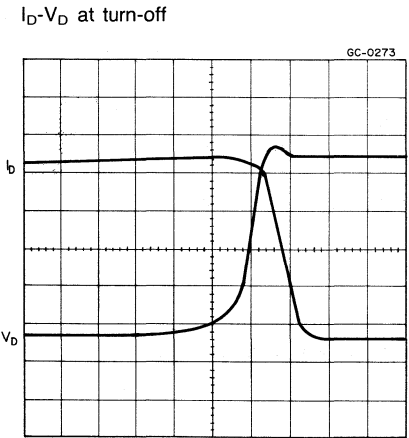
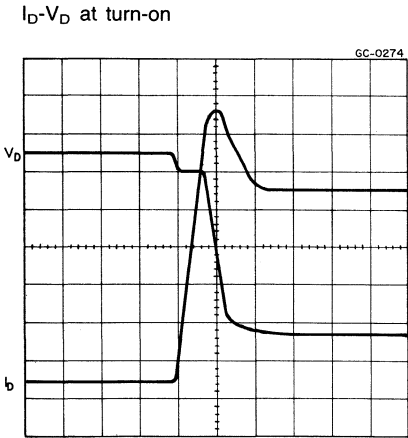
* Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

ELECTRICAL CHARACTERISTICS
 (Continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE (see note B)					
I_{SD}	Source-drain current (continuous)			30	A
I_{SDM}	Source-drain current (pulsed)			45	A
V_{SD}	Forward on voltage	$I_{SD} = 30\text{ A } V_{GS} = 0$		2	V
t_{rr}	Reverse recovery time	$I_{SD} = 30\text{ A } V_{GS} = 0$ $di/dt = 150\text{ A}/\mu\text{s}$		600	ns

Note A: switching times inductive load have been tested by the circuit shown in fig. 1 (by paralleling the load with SGS fast recovery diode...).

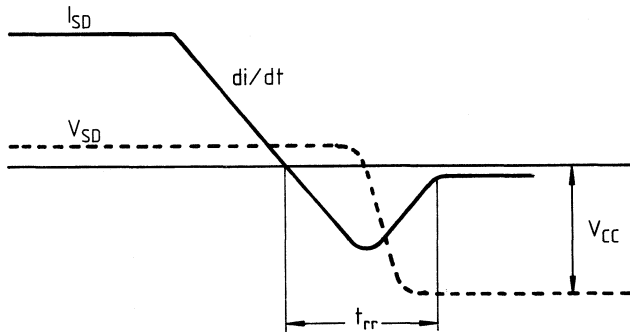
Typical waveforms obtained for V_D and I_D are schematically shown here below.



Note that di/dt does not depend on the performances of the freewheeling diode, but on the D.U.T. and its drive circuit only.



Note B: The switching performances of the source drain diode have been tested by the circuit shown in fig. 1 (by paralleling it to the load using another identical module for switching). Typical waveforms obtained for V_{SD} and I_{SD} are schematically shown here below.



SC-0162

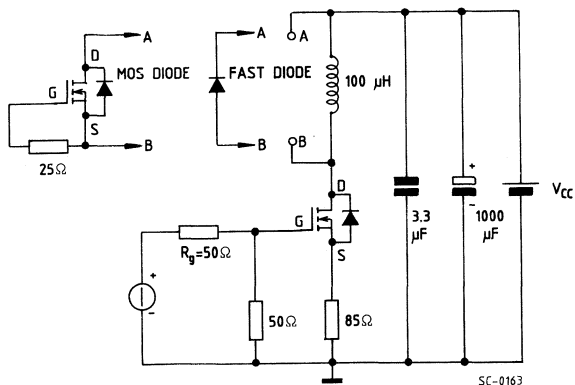


Fig. 1: Switching times inductive load and body drain diode t_{rr} , Q_{rr} test circuit.



SGS35MA050D1

ADVANCE DATA

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

V_{DS}	$R_{DS(on)}$	I_D
500V	0.16Ω	35A

• ISOLATED POWERMOS MODULE

• HIGH POWER

• FAST SWITCHING

• EASY DRIVE

• EASY TO PARALLEL

INDUSTRIAL APPLICATION:

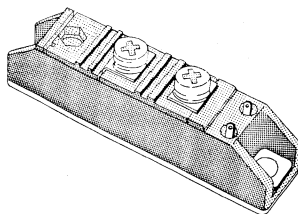
• SWITCHING MODE POWER SUPPLIES

• UNINTERRUPTIBLE POWER SUPPLIES

N-Channel enhancement mode POWERMOS field effect transistors. Easy drive and fast switching of these TRANSPACK modules make them ideal for high power, high speed switching applications.

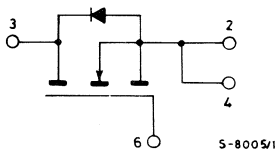
Typical applications include DC motor control (speed, soft start and torque), AC motor control (variable frequency control) switching mode power supplies, uninterruptible power supplies, DC/DC convertors and high frequency welding equipment.

The large RBSOA and absence of second breakdown in POWERMOS make these TRANSPACK modules very rugged. This, together with the isolated package with its optimised thermal performance, make these modules extremely effective in high power application.



TO-240AA

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)
V_{GS}	Gate-source voltage
I_D	Drain current (continuous) $T_c = 25^\circ C$
I_{DM}	Drain current ($t_p \leq 10$ ms, repetitive)
I_{DLM}	Drain current ($t_p = 20\mu s$, not repetitive)
P_{tot}	Total dissipation at $T_{case} < 25^\circ C$
	Derating factor
T_{stg}	Storage temperature
T_j	Max. operating junction temperature (continuous)

SGS30MA050D1

500	V
500	V
± 20	V
35	A
50	A
80	A
400	W
3.2	W/ $^\circ C$
-55 to 150	$^\circ C$
150	$^\circ C$

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max.	0.31 °C/W
R_{thc-h}	Thermal resistance case-heatsink	max.	0.20 °C/W

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
-----------	-----------------	------	------	------	------

OFF

$V_{(BR)\ DSS}$	Drain-source breakdown voltage	$I_D = 2\ mA\ V_{GS} = 0$	500			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$			2	mA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			100	nA

ON*

$V_{GS\ (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}\ I_D = 2\ mA$	2		4	V
$V_{DS(on)}$	Drain-source voltage	$V_{GS} = 10V\ I_D = 17.5A$			2.8	V
$R_{DS\ (on)}$	Static drain-source on-resistance	$V_{GS} = 10V\ I_D = 17.5A$			0.16	Ω
g_{fs}	Forward transconductance	$V_{DS} = 25V\ I_D = 17.5A$	20			mho

DYNAMIC

C_{iss}	Input capacitance	$V_{DS} = 25V\ f = 1\ MHz$		8500		pF
C_{oss}	Output capacitance	$V_{GS} = 0$		1100		pF
C_{rss}	Reverse transfer capacitance			750		pF

SWITCHING TIMES INDUCTIVE LOAD (see note A)

$t_{d\ (on)}$	Turn-on time	$V_{CC} = 250V\ I_D = 17.5A$		100		ns
$(di/dt)_{on}$	Turn-on current slope	$V_i = 10V\ R_i = 50\Omega$		150		A/ μs
$t_{d(off)}$	Turn off delay time			1.1		μs
t_f	Fall time			130		ns

* Pulsed: Pulse duration = 300 μs , duty cycle = 1.5%

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit.
-----------	-----------------	------	------	------	-------

SOURCE DRAIN DIODE (see note B)

I_{SD}	Source-Drain current (continuous)			35	A
I_{SDM}	Source-Drain current (pulsed)			50	A
V_{SD}	Forward on voltage	$I_{SD} = 35A$ $V_{GS} = 0$		2	V
t_{rr}	Reverse recovery time	$di/dt = 150A/\mu s$ $I_{SD} = 30A$ $V_{GS} = 0$		600	ns

INSULATION TESTING

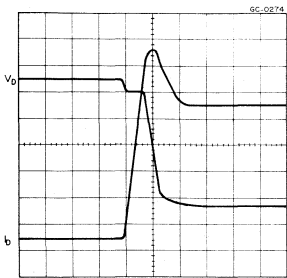
The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.

If this test is repeated by the user either as a good inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/VDE 0558, part 1/8.77, section 5.7.9., only a voltage slowly increasing up to the above standards then the specified value of 2000 V should be taken.

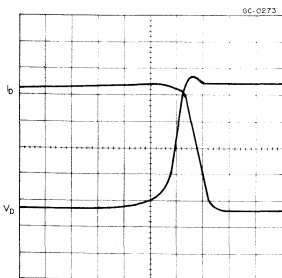
During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

Note A: switching times inductive load have been tested by the circuit shown in fig. 1 (by paralleling the load with SGS fast recovery diode SGS45R80).
Typical waveforms obtained for V_D and I_D are schematically shown here below.

I_D - V_D at turn-on

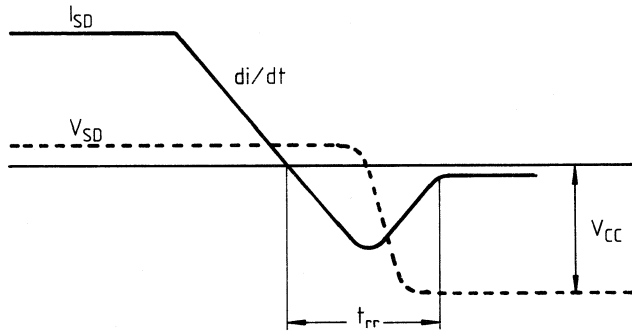


I_D - V_D at turn-off



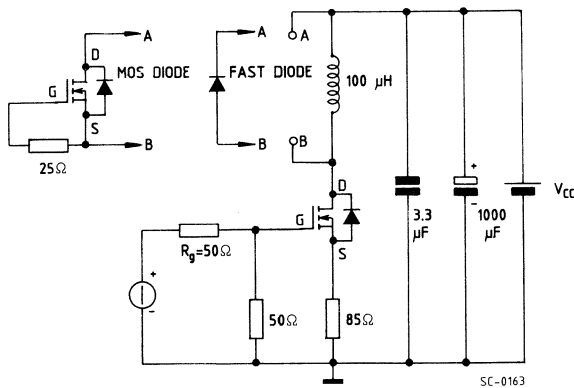
Note that di/dt does not depend on the performances of the freewheeling diode, but on the D.U.T. and its drive circuit only.

Note B: The switching performances of the source drain diode have been tested by the circuit shown in fig. 1 (by paralleling it to the load using another identical module for switching). Typical waveforms obtained for V_{SD} and I_{SD} are schematically shown here below.



SC-0162

Fig. 1: Switching times inductive load and body drain diode t_{rr} , Q_{rr} test circuit.



SC-0163



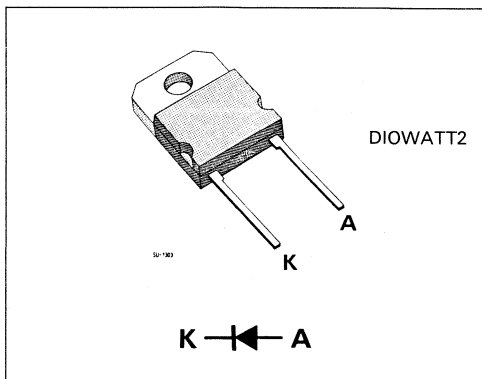
SGS35R120

ADVANCE DATA

HIGH SPEED SWITCHING APPLICATIONS

- VOLTAGE RANGE: 1200V
- AVERAGE CURRENT: 35A
- VERY LOW REVERSE RECOVERY TIME: t_{rr} 150ns
- VERY LOW SWITCHING LOSSES
- LOW NOISE TURN-OFF SWITCHING

Typical applications include freewheel diodes in motor control systems.



ABSOLUTE MAXIMUM RATINGS

V_{RRM}	Peak repetitive reverse voltage	1200	V
V_{RWM}	Working peak reverse voltage	1200	V
V_R	Continuous reverse voltage	1200	V
I_{FRM}	Repetitive peak forward current ($t = 10\mu s$)	500	A
$I_{F(AV)}$	Average forward current $T_{case} = 70^\circ C$ (switching operation, $\delta = 0.5$)	35	A
I_{FSM}	Surge non repetitive forward current ($t = 10ms$)	350	A
P_{tot}	Total dissipation at $T_{case} = 70^\circ C$	90	W
T_{stg}	Storage temperature	-65 to 150	$^\circ C$
T_j	Max. operating junction temperature	150	$^\circ C$

THERMAL DATA

R _{thj-case}	Thermal resistance junction-case	max 0.9 °C/W
-----------------------	----------------------------------	--------------

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters	Test Contitions	Min.	Typ.	Max.	Unit
I _R Reverse Current	V = V _R T _j = 25°C V = V _R T _j = 125°C			100 4	μA mA
V _F (*) Forward voltage	I _F = 35A T _{case} = 25°C I _F = 35A T _{case} = 125°C		1.5 1.5	1.7 1.7	V V
t _{rr} Reverse recovery time	I _F = 1A di/dt = 25A/μs V _R = 30V I _F = 35A di/dt = 100A/μs V _R = 30V			150 400	ns ns
Q _{rr} Recovered charge	I _F = 35A di/dt = 100A/μs V _R = 30V		3		μC
V _{FEP} Forward recovery overvoltage	I _F = 35A di/dt = 100A/μs		12		V

* Pulsed: pulse duration ≤300μs, duty cycle ≤2%

Fig. 1 Forward overvoltage vs. current slope

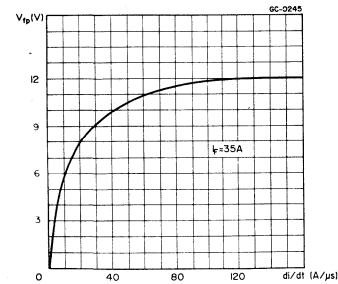


Fig. 2 Reverse leakage current vs. junction temperature

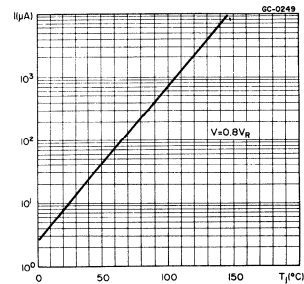
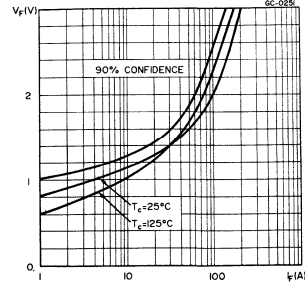


Fig. 3 Voltage drop vs. forward current





SGS40TA045
SGS40TA045D

TRANSPACK NPN POWER TRANSISTOR MODULE

APPLICATIONS: These products are silicon NPN power transistors for industrial switching applications from the mains.

ISOLATED POWER MODULE (30KVA - 375W)

FAST FREEWHEEL DIODE (D - suffix)

ABSOLUTE MAXIMUM RATINGS

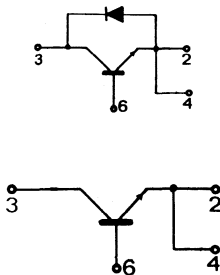
V_{CBO}	Collector-base voltage ($I_E = 0$)
V_{CES}	Collector-emitter voltage ($V_{BE} = 0$)
V_{CEX}	Collector-emitter voltage ($V_{BE} = -1.5V$)
V_{CEO}	Collector-emitter voltage ($I_B = 0$)
V_{CEOL}	Overload switch-off at 1.5 times $I_{C(sat)}$
V_{EBO}	Emitter-base voltage ($I_C = 0$)
I_C	Collector current
I_{CM}	Collector peak current ($t_p < 10$ ms)
I_{CP}	Collector peak current non repetitive ($t_p < 20$ μ s)
I_B	Base current
I_{BP}	Base peak current non repetitive ($t_p < 20$ μ s)
T_{stg}	Storage temperature
T_j	Max. operating junction temperature (continuous)
T_j	Max. operating junction temperature (1 minute)

SGS40TA045

SGS40TA045D

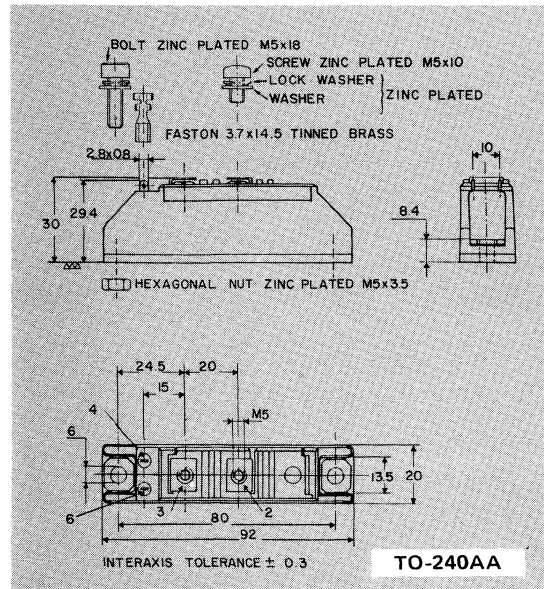
850	V
850	V
850	V
450	V
500	V
7	V
60	A
120	A
300	A
12	A
50	A
- 40 to 150	°C
150	°C
175	°C

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm





SGS40TA045
SGS40TA045D

THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case (transistor)	max 0.33°C/W
$R_{th\ j-case}$	Thermal resistance junction-case (diode)	max 1.10°C/W
$R_{th\ c-h}$	Thermal resistance case-heatsink	max 0.20°C/W

ELECTRICAL CHARACTERISTICS

($T_j = 25^\circ\text{C}$ unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I_{CEO}	Collector cutoff current ($I_B = 0$)	$V_{CE} = V_{CE0}$			5	mA
I_{CES}	Collector cutoff current ($V_{BE} = 0$)	$V_{CE} = V_{CES}$ $V_{CE} = V_{CEOL}$ $T_j = 125^\circ\text{C}$		0.05 3.00	2 10	mA mA
I_{CEX}	Collector cutoff current	$V_{CE} = V_{CEX}$ $V_{BE} = -1.5\text{V}$ $V_{CE} = V_{CEOL}$ $V_{BE} = -1.5\text{V}$ $T_j = 125^\circ\text{C}$		3	1 10	mA mA
I_{EBO}	Emitter cutoff current ($I_C = 0$)	$V_{BE} = -5\text{V}$			2	mA
$V_{CEO(sus)*}$	Collector-emitter sustaining voltage	$I_C = 0.2\text{A}$ $L = 2\text{mH}$	450			V
V_{CEOL}	Max voltage to switch-off 1.5 times $I_{C(sat)}$ (top right corner of RBSOA)	$I_C = 60\text{A}$	500			V
$V_{CE(sat)*}$	Collector-emitter saturation voltage	$I_C = 40\text{ A}$ $I_B = 8\text{ A}$ $I_C = 40\text{ A}$ $I_B = 8\text{ A}$ $T_j = 125^\circ\text{C}$		0.5 0.6	2.0	V V
$V_{BE(sat)*}$	Base-emitter saturation voltage	$I_C = 40\text{ A}$ $I_B = 8\text{ A}$ $I_C = 40\text{ A}$ $I_B = 8\text{ A}$ $T_j = 125^\circ\text{C}$		1.1 1.3	2.2	V V
h_{FE}^*	DC current gain	$I_C = 40\text{ A}$ $V_{CE} = 3\text{ V}$ $I_C = 60\text{ A}$ $V_{CE} = 5\text{ V}$	7 5	12 8.5		
INDUCTIVE LOAD		(see test circuit)				
t_s	Storage time	$I_C = 40\text{A}$ $I_B = 8\text{ A}$ $V_{BE\ OFF} = -5\text{ V}$		2.00		μs
t_f	Fall time	$V_{CC} = 50\text{V}$ $L = 100\text{ }\mu\text{H}$ $V_{CL} = 300\text{V}$ $T_j = 25^\circ\text{C}$		0.12		μs
t_s	Storage time	$I_C = 50\text{A}$ $I_B = 2\text{ A}$ $V_{BE\ OFF} = -5\text{ V}$		2.30	5.0	μs
t_f	Fall time	$V_{CC} = 50\text{V}$ $L = 100\text{ }\mu\text{H}$ $V_{CL} = 300\text{V}$ $T_j = 125^\circ\text{C}$		0.25	0.5	μs

* Pulsed: Pulse duration = 300 μs , duty cycle = 1.5%.

ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_f	Diode forward voltage	$I_f = 40\text{ A}$ $T_J = 25^\circ\text{C}$ for SGS40TA045D $T_J = 125^\circ\text{C}$		1.50 1.55	2.0	V V
t_{rr}	Diode reverse recovery time	$I_f = 40\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ for SGS40TA045D		0.20	0.5	μs
I_{rm}	Diode reverse recovery current			10		A
I_{frm}	Diode forward current	$t = 1\text{ ms}$ for SGS40TA045D	250			A

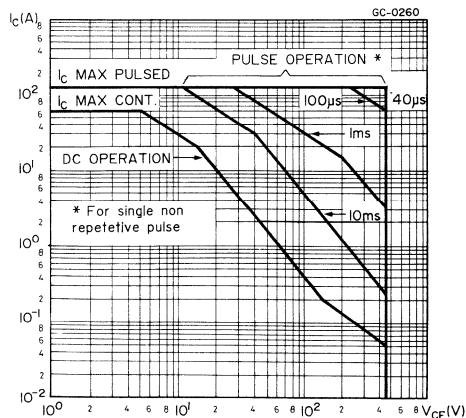
INSULATION TESTING

The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.

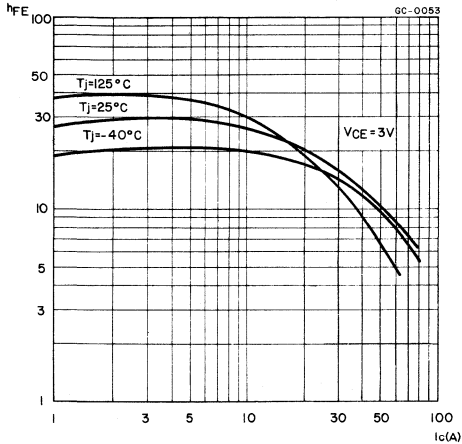
If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/VDE 0558, section 5.7.9., only a voltage slowly increasing up to the above value should be used. If the voltage is applied for one minute as recommended by the above standards then the specified value of 2000 V should be taken.

During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

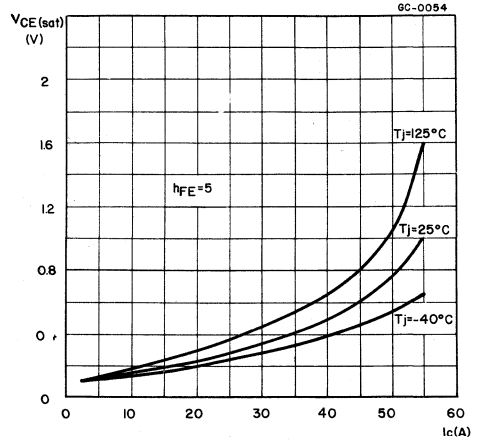
Safe operating areas



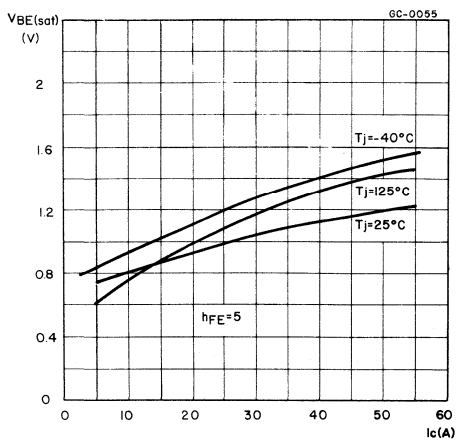
DC current gain



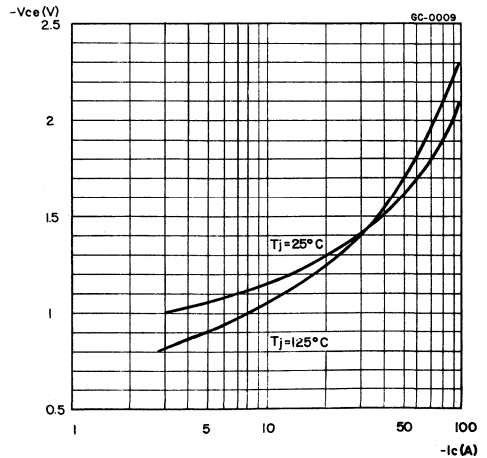
Collector-emitter saturation voltage



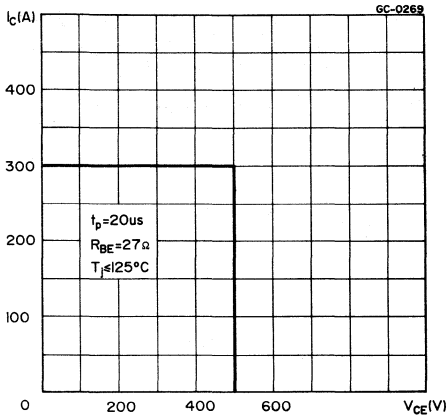
Base-emitter saturation voltage



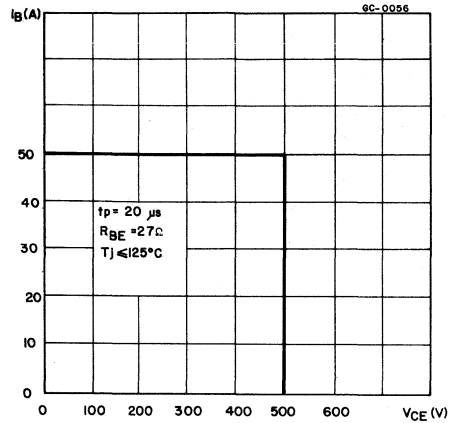
Typical V_F versus $-I_c$



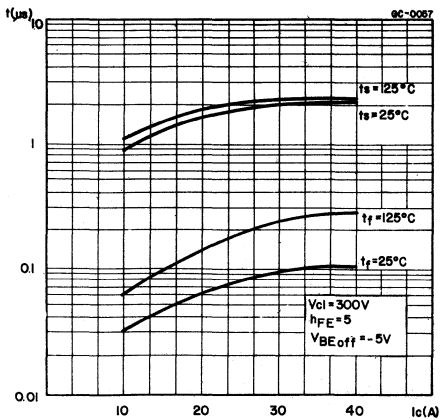
Collector overload SOA (see fig. 1)



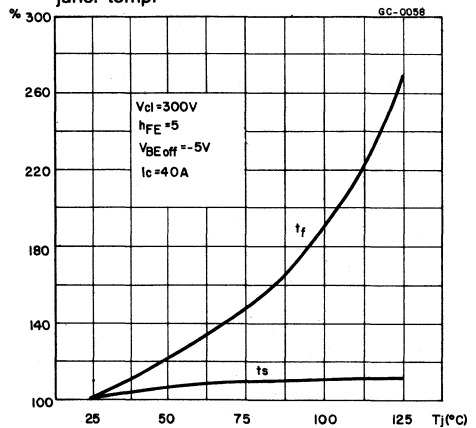
Base overload SOA (see fig. 1)



Switching times inductive load (see fig. 3)



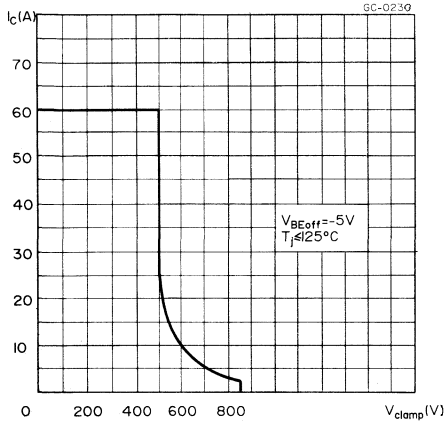
Switching times inductive load vs
junc. temp.



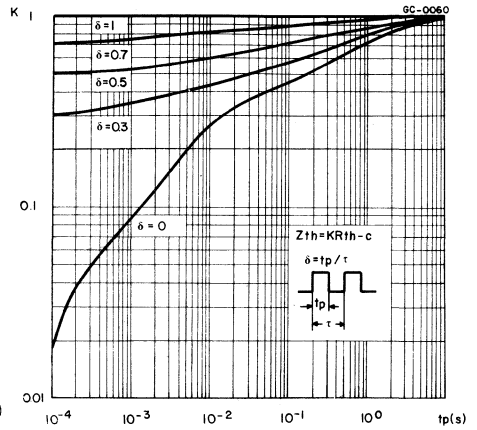


SGS40TA045
SGS40TA045D

Reverse biased SOA (see fig. 2)

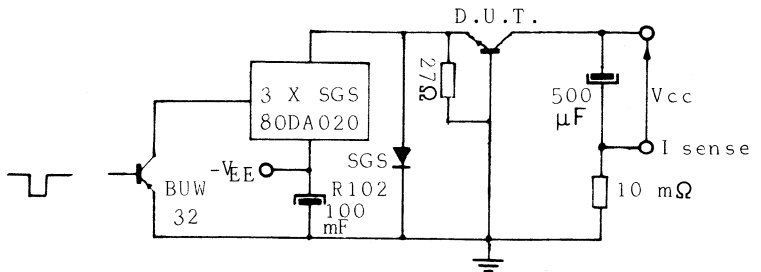


Thermal impedance



OVERLOAD

- Collector
- Test circuit



OVERLOAD

- Base
- Test circuit

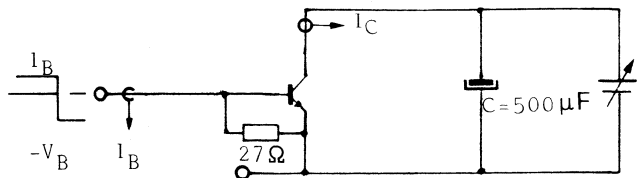


Fig. 1

SC-0001b

Fig. 2 RBSOA TEST CIRCUIT

RBSOA test circuit has been driven by the switching times test circuit with $R_{E2} = 0$.
RBSOA sensitivity to T_j variations is very limited, so that the limits shown can be kept valid at ambient temperature as well.

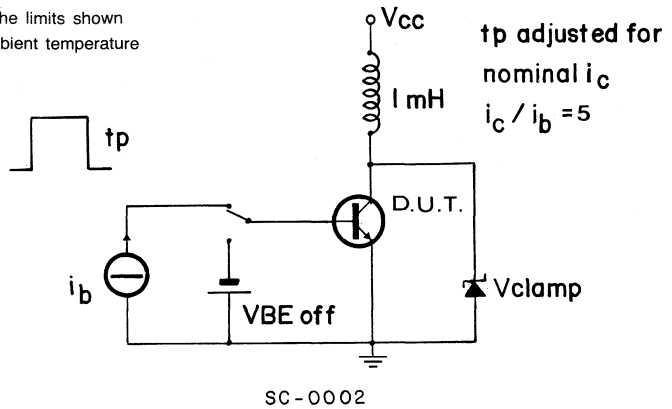
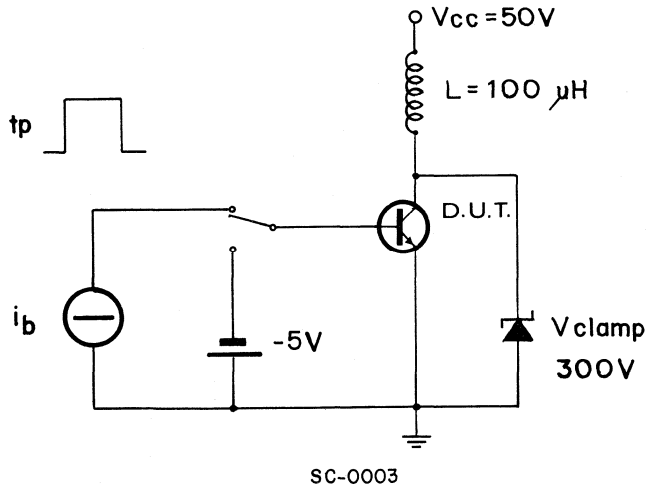


Fig. 3 Switching times test circuit.



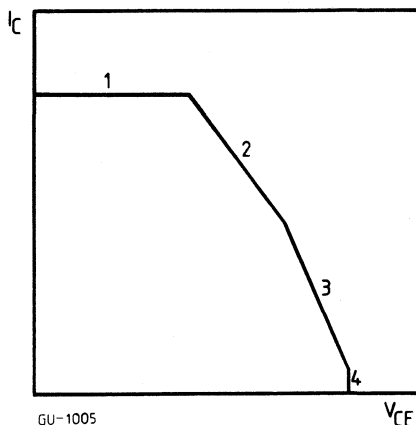
FORWARD BIAS SAFE OPERATING AREA

The I_C/V_{CE} limits of a transistor which have to be observed for reliable operation are specified by the safe operating area curves. The transistor must not be subjected to a greater dissipation than that indicated by the SOA boundary, operation outside these limits could result in either rapid or long term failure of the transistor.

The safe operating boundary is defined by four limits:

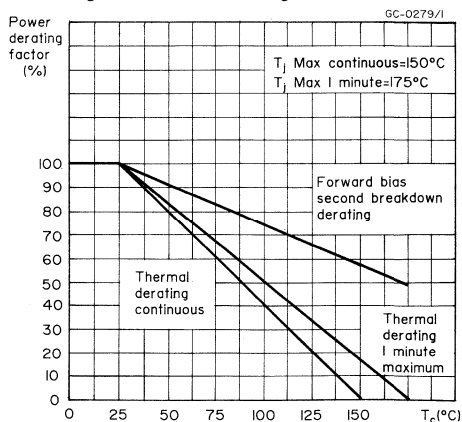
1. The limit of maximum current.
2. The limit of thermal dissipation.
3. The limit of secondary breakdown.
4. The limit of maximum voltage.

Fig. 4



Maximum voltage and current limits are fixed whereas thermal dissipation and secondary breakdown are dependant on the temperature. The normal figures given in the RBSOA diagram are tied to a fixed $T_C = 25^\circ\text{C}$ and for temperatures $>25^\circ\text{C}$ the Power Derating curve (fig. 5) has to be used. As thermal limitations do not derate in the same way as second breakdown limitations, the Power Derating diagram has two curves and the allowable current at the voltages shown on the RBSOA diagram may be found for any case temperature by using the appropriate power derating curve. For power levels under area 2 (fig. 4) the thermal derating curve is effective and for power levels under area 3, the second breakdown derating is used. At extreme case temperatures the thermal limitations reduce power handling to lower values than the limitations caused by second breakdown.

Fig. 5 - Power derating





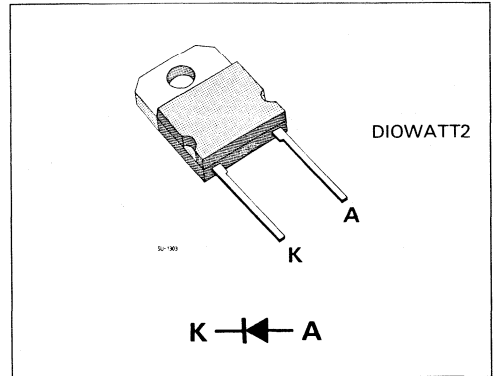
SGS45R80

ADVANCE DATA

HIGH SPEED SWITCHING APPLICATIONS

- VOLTAGE RANGE: 800V
- AVERAGE CURRENT: 45A
- VERY LOW REVERSE RECOVERY TIME: t_{rr} 125ns
- VERY LOW SWITCHING LOSSES
- LOW NOISE TURN-OFF SWITCHING

Typical applications include freewheel diodes in motor control systems.



ABSOLUTE MAXIMUM RATINGS

V_{RRM}	Peak repetitive reverse voltage	800	V
V_{RWM}	Working peak reverse voltage	800	V
V_R	Continuous reverse voltage	800	V
I_{FRM}	Repetitive peak forward current ($t = 10\mu s$)	600	A
$I_{F(AV)}$	Average forward current $T_{case} = 70^\circ C$ (switching operation, $\delta = 0.5$)	45	A
I_{FSM}	Surge non repetitive forward current ($t = 10ms$)	450	A
P_{tot}	Total dissipation at $T_{case} = 70^\circ C$	90	W
T_{stg}	Storage temperature	-65 to 150	$^\circ C$
T_j	Max. operating junction temperature	150	$^\circ C$

THERMAL DATA

$R_{thj-case}$	Thermal resistance junction-case	max 0.9 °C/W
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ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

Parameters	Test Contitions	Min.	Typ.	Max.	Unit
I_R Reverse Current	$V = V_R$ $T_j = 25^{\circ}C$ $V = V_R$ $T_j = 125^{\circ}C$			100 4	μA mA
$V_F(*)$ Forward voltage	$I_F = 45A$ $T_{case} = 25^{\circ}C$ $I_F = 45A$ $T_{case} = 125^{\circ}C$		1.3 1.3	1.5 1.5	V V
t_{rr} Reverse recovery time	$I_F = 1A$ $di/dt = 50A/\mu s$ $V_R = 30V$ $I_F = 45A$ $di/dt = 100A/\mu s$ $V_R = 30V$			125 400	ns ns
Q_{rr} Recovered charge	$I_F = 45A$ $di/dt = 100A/\mu s$ $V_R = 30V$		3		μC
V_{FP} Forward recovery overvoltage	$I_F = 45A$ $di/dt = 100A/\mu s$		11		V

* Pulsed: pulse duration $\leq 300\mu s$, duty cycle $\leq 2\%$

Fig. 1 Forward overvoltage vs. current slope

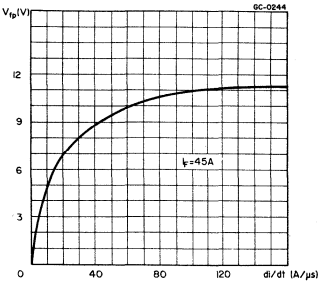


Fig. 2 Reverse leakage current vs. junction temperature

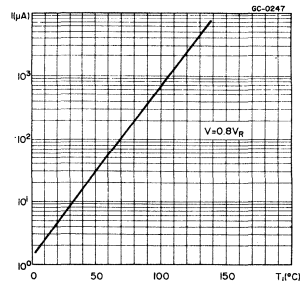
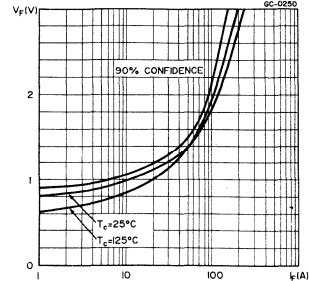


Fig. 3 Voltage drop vs. forward current



TRANSPACK NPN POWER DARLINGTON MODULE

APPLICATIONS: The product is a silicon NPN power darlington for industrial switching applications from the mains.

ISOLATED POWER MODULE (37KVA - 375W)

FAST FREEWHEEL DIODE

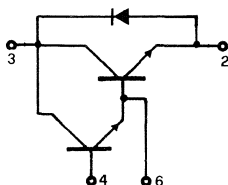
ABSOLUTE MAXIMUM RATINGS

V_{CBO}	Collector-base voltage ($I_E = 0$)
V_{CES}	Collector-emitter voltage ($V_{BE} = 0$)
V_{CEX}	Collector-emitter voltage ($V_{BE} = -1.5V$)
V_{CEO}	Collector-emitter voltage ($I_B = 0$)
V_{CEOL}	Overload switch-off at 1.5 times $I_{C(sat)}$
V_{EBO}	Emitter-base voltage ($I_C = 0$)
I_C	Collector current
I_{CM}	Collector peak current ($t_p < 10$ ms)
I_{CP}	Collector peak current non repetitive ($t_p < 20$ μ s)
I_B	Base current
I_{BP}	Base peak current non repetitive ($t_p < 20$ μ s)
T_{stg}	Storage temperature
T_J	Max. operating junction temperature (continuous)
T_J	Max. operating junction temperature (1 minute)

SGS50DA045D

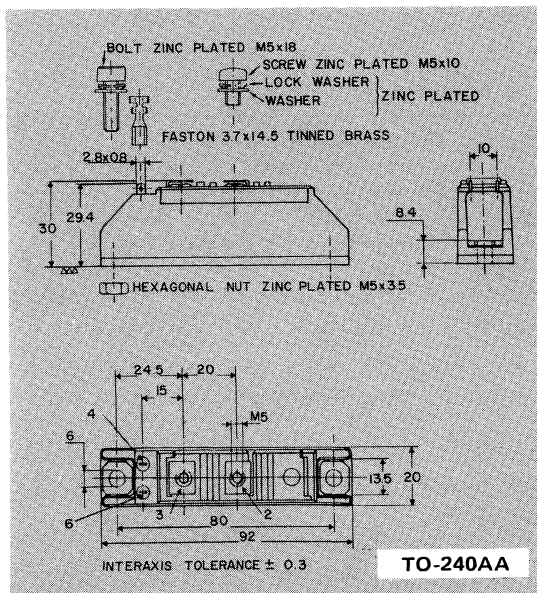
850	V
850	V
850	V
450	V
500	V
7	V
75	A
120	A
300	A
3	A
10	A
- 40 to 150	°C
150	°C
175	°C

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



**SGS50DA045D****THERMAL DATA**

$R_{th\ j-case}$	Thermal resistance junction-case (darlington)	max 0.33°C/W
$R_{th\ j-case}$	Thermal resistance junction-case (diode)	max 1.10°C/W
$R_{th\ c-h}$	Thermal resistance case-heatsink	max 0.20°C/W

ELECTRICAL CHARACTERISTICS(T_j = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I _{CER}	Collector cutoff current (R _{BE1} = 3.3Kohm R _{BE2} = 100ohm)	V _{CE} = V _{CEOL}			2	mA
		V _{CE} = V _{CEOL} T _j = 125°C			10	mA
I _{CES}	Collector cutoff current (V _{BE1} = V _{BE2} = 0)	V _{CE} = V _{CES}		0.05	2	mA
		V _{CE} = V _{CEOL} T _j = 125°C		3	10	mA
I _{CEX}	Collector cutoff current	V _{CE} = V _{CEX} V _{BE} = -1.5V		0.05	2	mA
		V _{CE} = V _{CEOL} V _{BE} = -1.5V T _j = 125°C		3	10	mA
I _{EBO}	Emitter cutoff current (I _C = 0)	V _{BE} = -5V			2	mA
V _{CEO (sus)*}	Collector-emitter sustaining voltage	I _C = 0.2A L = 2mH	450			V
V _{CEOL}	Max voltage to switch-off 1.5 times I _{C (sat)} (top right corner of RBSOA)	I _C = 75A	500			V
V _{CE (sat)*}	Collector-emitter saturation voltage	I _C = 50 A I _B = 2 A		1.6	2.5	V
		I _C = 50 A I _B = 2 A T _j = 125°C		2.2		V
V _{BE (sat)*}	Base-emitter saturation voltage	I _C = 50 A I _B = 2 A		2.2	3	V
		I _C = 50 A I _B = 2 A T _j = 125°C		2.0		V
h _{FE} *	DC current gain	I _C = 50 A V _{CE} = 5 V	80	150		
		I _C = 70 A V _{CE} = 5 V		110		
INDUCTIVE LOAD		(see test circuit)				
t _s	Storage time	I _C = 50A I _B = 2 A V _{BE OFF} = -5 V		1.90		μs
t _f	Fall time	V _{CC} = 50V L = 100 μH V _{CL} = 300V T _j = 25°C		0.15		μs
t _s	Storage time	I _C = 50A I _B = 2 A V _{BE OFF} = -5 V		2.20	5.0	μs
t _f	Fall time	V _{CC} = 50V L = 100 μH V _{CL} = 300V T _j = 125°C		0.30	0.6	μs

* Pulsed: Pulse duration = 300 μs , duty cycle = 1.5%.

ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_f	Diode forward voltage	$I_f = 50\text{ A}$ $T_j = 25^\circ\text{C}$ $T_j = 125^\circ\text{C}$		1.60 1.70	2.2	V V
t_{rr}	Diode reverse recovery time	$I_f = 50\text{ A}$ $di/dt = 100\text{A}/\mu\text{s}$		0.20	0.5	μs
I_{rm}	Diode reverse recovery current			12		A
I_{frm}	Diode forward current	$t = 1\text{ms}$	250			A

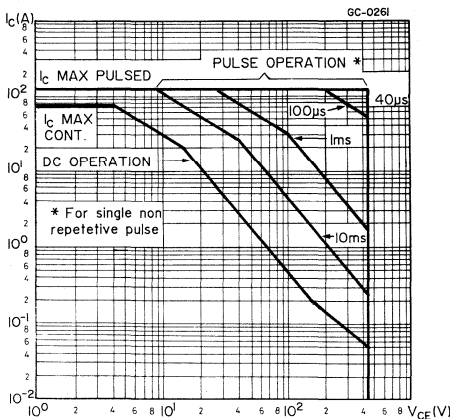
INSULATION TESTING

The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.

If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/VDE 0558, part 1/8.77, section 5.7.9., only a voltage slowly increasing up to the above value should be used. If the voltage is applied for one minute as recommended by the above standards then the specified value of 2000 V should be taken.

During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

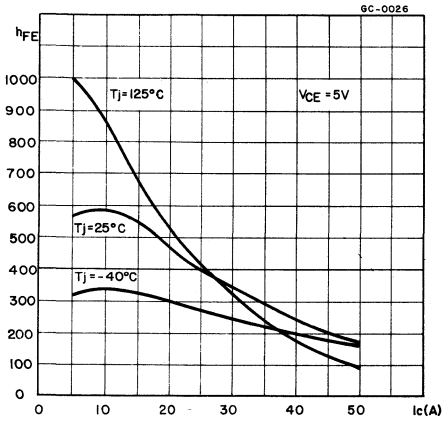
Safe operating areas



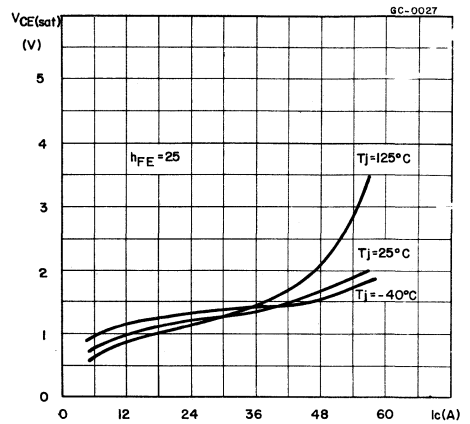


SGS50DA045D

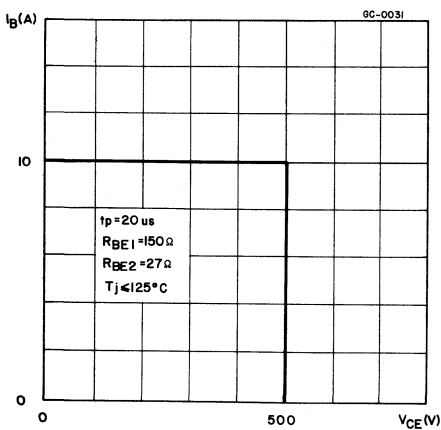
DC current gain



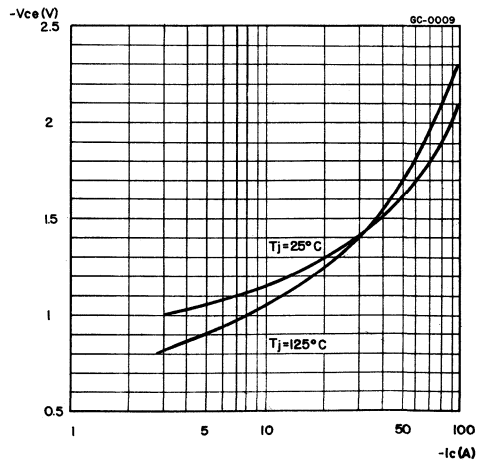
Collector-emitter saturation voltage



Base overload SOA (see fig. 1)

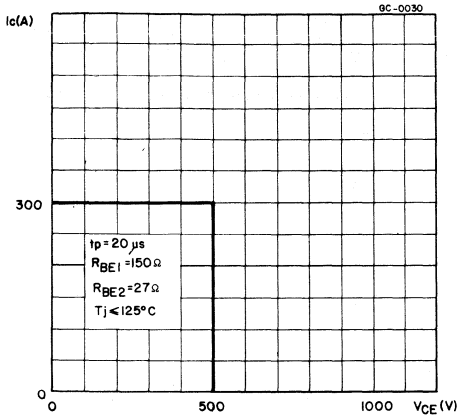


Typical V_F versus $-I_C$

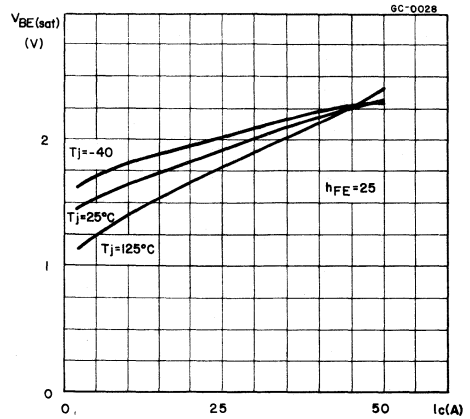




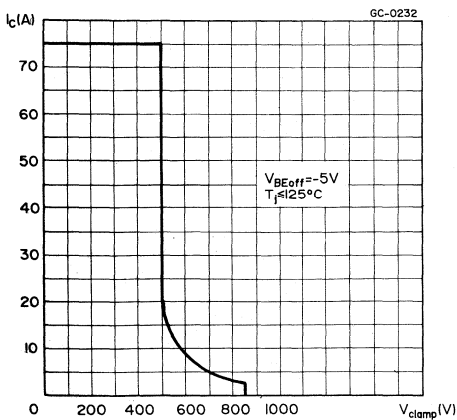
Collector overload SOA (see fig. 1)



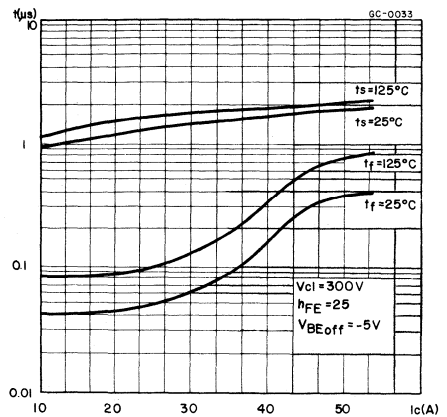
Base-emitter saturation voltage



Reverse biased SOA (see fig. 2)



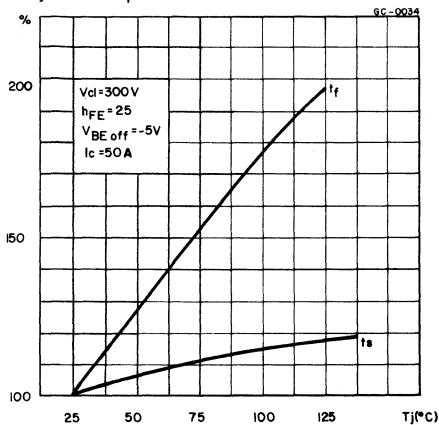
Switching times inductive load (see fig. 3)



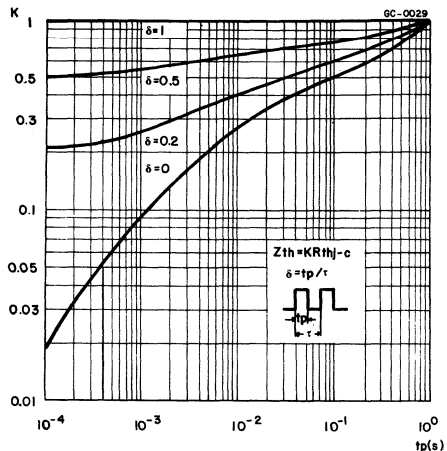


SGS50DA045D

Switching times inductive load vs
junc. temp.

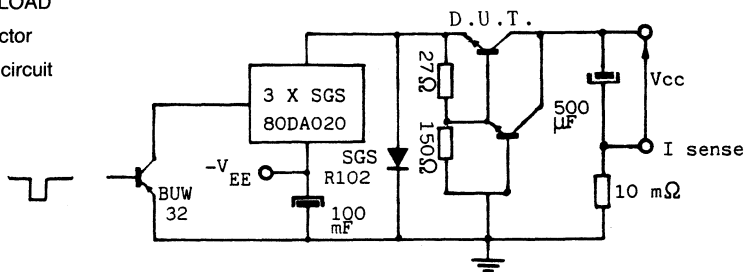


Thermal impedance



OVERLOAD

- Collector
Test circuit



OVERLOAD

- Base
Test circuit

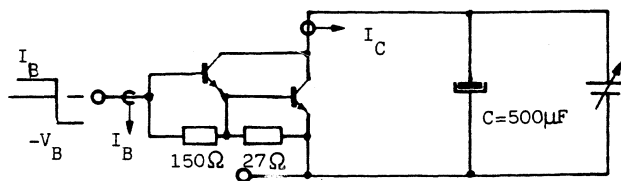


Fig. 1

Fig. 2 RBSOA TEST CIRCUIT

RBSOA test circuit has been driven by the switching times test circuit with $R_{B2} = 0$. RBSOA sensitivity to T_j variations is very limited, so that the limits shown can be kept valid at ambient temperature as well.

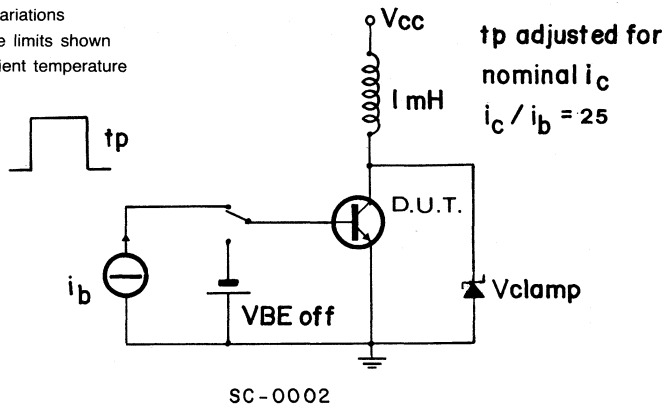
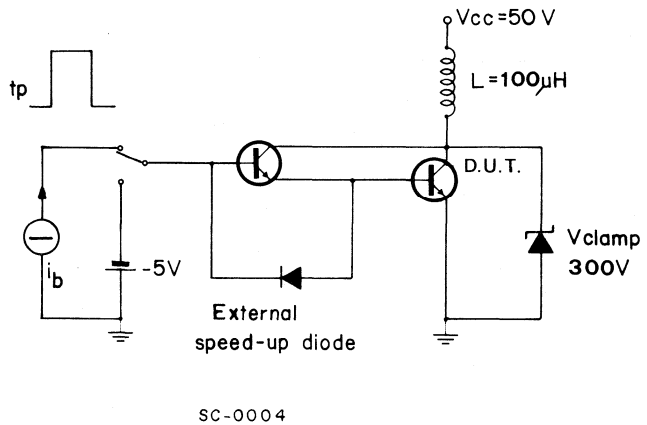


Fig. 3 Switching times test circuit.





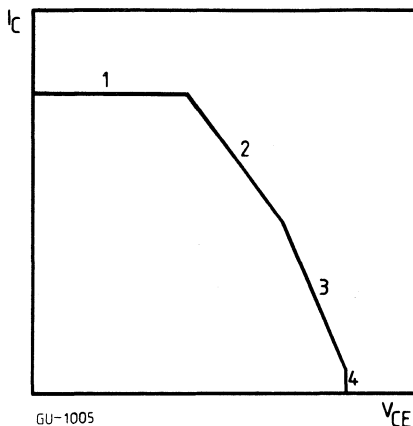
FORWARD BIAS SAFE OPERATING AREA

The I_C/V_{CE} limits of a transistor which have to be observed for reliable operation are specified by the safe operating area curves. The transistor must not be subjected to a greater dissipation than that indicated by the SOA boundary, operation outside these limits could result in either rapid or long term failure of the transistor.

The safe operating boundary is defined by four limits:

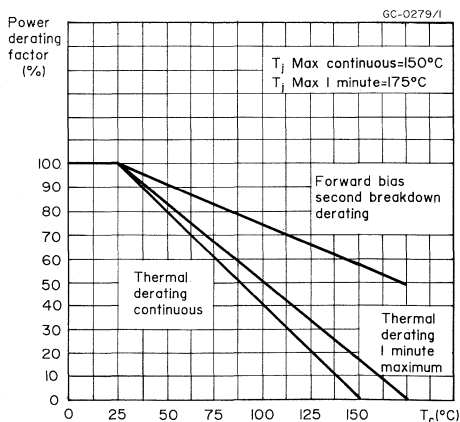
1. The limit of maximum current.
2. The limit of thermal dissipation.
3. The limit of secondary breakdown.
4. The limit of maximum voltage.

Fig. 4



Maximum voltage and current limits are fixed whereas thermal dissipation and secondary breakdown are dependant on the temperature. The normal figures given in the RBSOA diagram are tied to a fixed $T_C = 25^\circ\text{C}$ and for temperatures $>25^\circ\text{C}$ the Power Derating curve (fig. 5) has to be used. As thermal limitations do not derate in the same way as second breakdown limitations, the Power Derating diagram has two curves and the allowable current at the voltages shown on the RBSOA diagram may be found for any case temperature by using the appropriate power derating curve. For power levels under area 2 (fig. 4) the thermal derating curve is effective and for power levels under area 3, the second breakdown derating is used. At extreme case temperatures the thermal limitations reduce power handling to lower values than the limitations caused by second breakdown.

Fig. 5 - Power derating



TRANSPACK NPN POWER DARLINGTON MODULE

APPLICATIONS: The SGS50DB040D and SGS50DB045D are silicon NPN power fast darlingtontons in half bridge configuration for industrial switching applications from the mains.

ISOLATED POWER MODULE (26KVA-375W)

FAST FREEWHEEL DIODES

ABSOLUTE MAXIMUM RATINGS

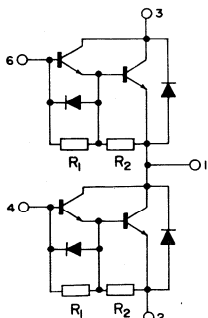
V_{CBO}	Collector-base voltage ($I_E = 0$)
V_{CES}	Collector-emitter voltage ($V_{BE} = 0$)
V_{CEX}	Collector-emitter voltage ($V_{BE} = -1.5V$)
V_{CEO}	Collector-emitter voltage ($I_B = 0$)
V_{CEOL}	Overload switch-off at 1.5 times $I_{C(sat)}$
V_{EBO}	Emitter-base voltage ($I_C = 0$)
I_C	Collector current
I_{CM}	Collector peak current ($t_p < 10$ ms)
I_{CP}	Collector peak current non repetitive ($t_p < 20$ μs)
I_B	Base current
I_{BP}	Base peak current non repetitive ($t_p < 20$ μs)
T_{stg}	Storage temperature
T_j	Max. operating junction temperature (continuous)
T_j	Max. operating junction temperature (1 minute)

SGS50DB040D

SGS50BD045D

500	600	V
500	600	V
500	600	V
400	450	V
400		V
7		V
75		A
120		A
250		A
10		A
20		A
- 40 to 150		°C
150		°C
175		°C

INTERNAL SCHEMATIC DIAGRAM



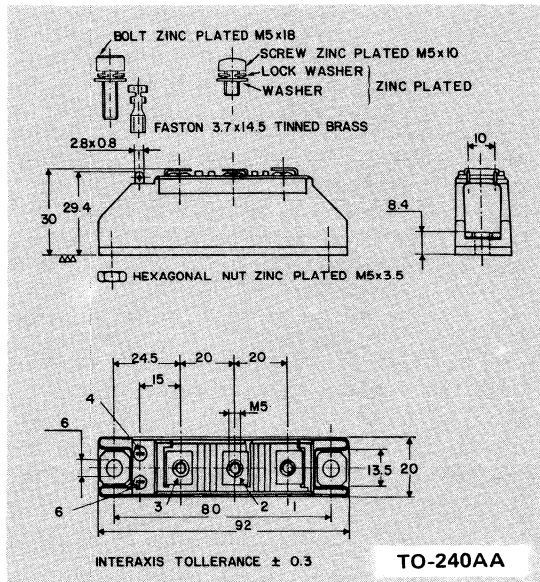
SC-061

R_1 typ 80 Ω

R_2 typ 150 Ω

MECHANICAL DATA

Dimensions in mm



TO-240AA



SGS50DB040D
SGS50DB045D

THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case (quarter bridge)	max 0.66	°C/W
$R_{th\ j-case}$	Thermal resistance junction-case (diode)	max 1.10	°C/W
$R_{th\ c-h}$	Thermal resistance case-heatsink	max 0.20	°C/W

ELECTRICAL CHARACTERISTICS

($T_j = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES} Collector cutoff current ($V_{BE} = 0$)	$V_{CE} = V_{CES}$ $V_{CE} = V_{CEOL}$ $T_j = 125^\circ\text{C}$		3	2 10	mA mA
I_{CEX} Collector cutoff current	$V_{CE} = V_{CEX}$ $V_{BE} = -1.5\text{ V}$ $V_{CE} = V_{CEOL}$ $V_{BE} = -1.5\text{ V}$ $T_j = 125^\circ\text{C}$		3	2 10	mA mA
I_{EBO} Emitter cutoff current ($I_C = 0$)	$V_{BE} = -2\text{ V}$		50	90	mA
$V_{CEO(sus)}^*$ Collector emitter sustaining voltage	$I_C = 0.2\text{ A}$ for SGS50DB040D $L = 2\text{ mH}$ for SGS50DB045D	400 450			V V
V_{CEOL} Max voltage to switch-off 1.5 times $I_{C(sat)}$ (top right corner of RBSOA)	$I_C = 75\text{ A}$	400			V
$V_{CE(sat)}^*$ Collector-emitter saturation voltage	$I_C = 50\text{ A}$ $I_B = 5\text{ A}$ $I_C = 50\text{ A}$ $I_B = 5\text{ A}$ $T_j = 125^\circ\text{C}$		1.5 1.7	3	V V
$V_{BE(sat)}^*$ Base-emitter saturation voltage	$I_C = 50\text{ A}$ $I_B = 5\text{ A}$ $I_C = 50\text{ A}$ $I_B = 5\text{ A}$ $T_j = 125^\circ\text{C}$		2.3 2.5	3.3	V V
h_{FE}^* DC current gain	$I_C = 50\text{ A}$ $V_{CE} = 5\text{ V}$	70	130		
INDUCTIVE LOAD	(see test circuit)				
t_s Storage time	$I_C = 50\text{ A}$ $I_B = 4\text{ A}$ $V_{BE\ OFF} = -5\text{ V}$ $V_{CC} = 250\text{ V}$ $L = 500\text{ }\mu\text{H}$ $V_{CL} = 300\text{ V}$		1.2 0.15		μs μs
t_f Fall time	$I_C = 50\text{ A}$ $I_B = 4\text{ A}$ $V_{BE\ OFF} = -5\text{ V}$ $V_{CC} = 250\text{ V}$ $L = 500\text{ }\mu\text{H}$ $V_{CL} = 300\text{ V}$ $T_j = 125^\circ\text{C}$		0.20	3 0.7	μs μs

* Pulsed: Pulse duration = 300 μs , duty cycle = 1.5%.

ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_f Diode forward voltage	$I_f = 50\text{ A}$ $I_f = 50\text{ A } T_j = 125\text{ }^\circ\text{C}$		1.4 1.5	2	V V
t_{rr} Diode reverse recovery time	$I_f = 50\text{ A } di/dt = 100\text{ A}/\mu\text{s}$		0.2	0.5	μs
I_{rm} Diode reverse recovery time			10		A
I_{frm} Diode forward current	$t = 1\text{ ms}$	250			A

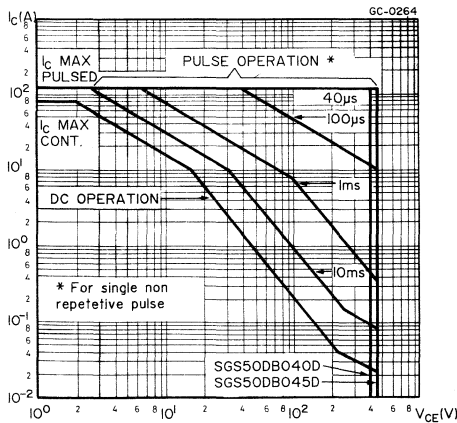
INSULATION TESTING

The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.

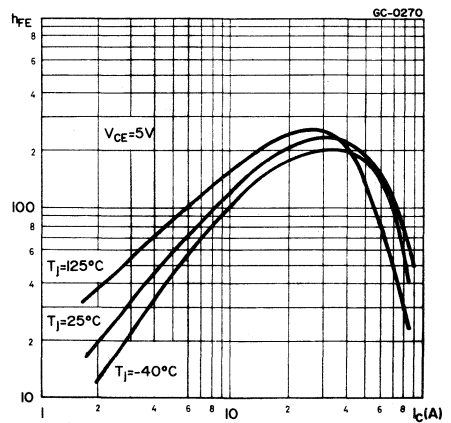
If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/VDE 0558 part 1/8.77, section 5.7.9., only a voltage slowly increasing up to the above value should be used. If the voltage is applied for one minute as recommended by the above standards then the specified value of 2000 V should be taken.

During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

Safe operating areas for each section



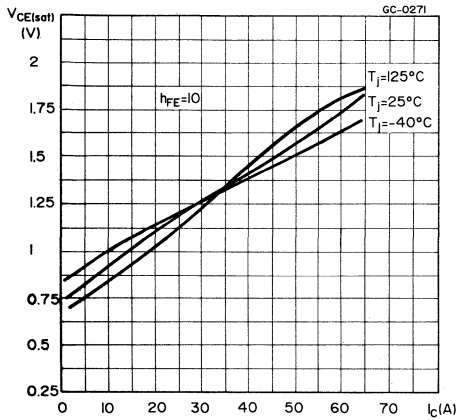
DC current gain



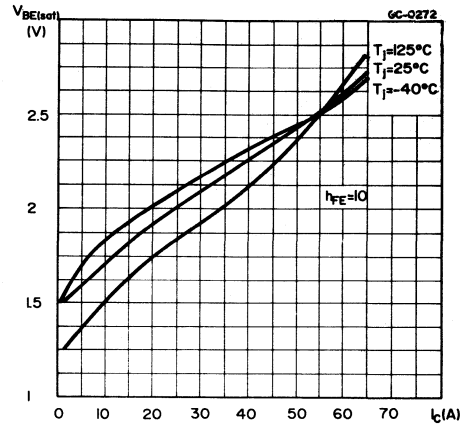


SGS50DB040D
SGS50DB045D

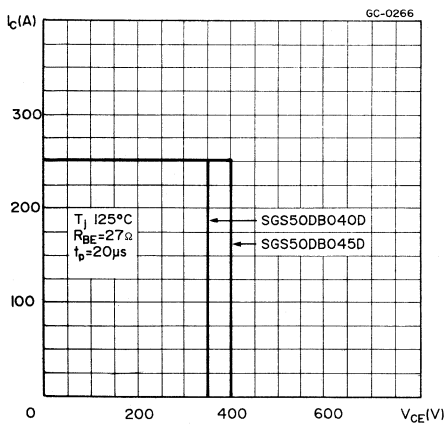
Collector-emitter saturation voltage



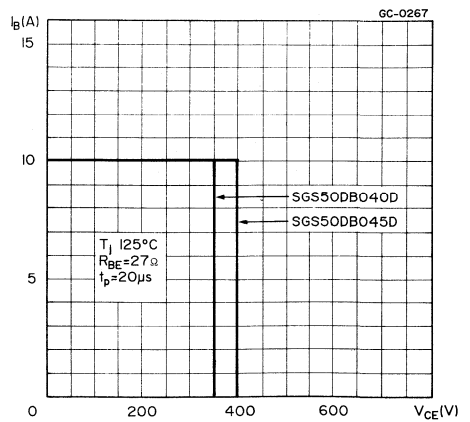
Base-emitter saturation voltage



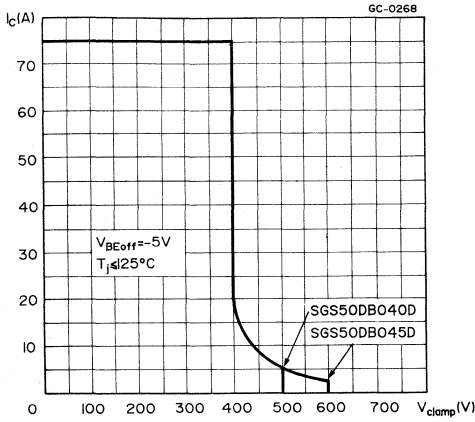
Collector overload SOA (see fig. 1)



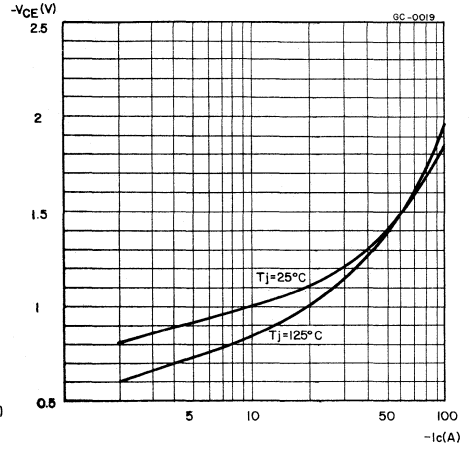
Base overload SOA (see fig. 1)



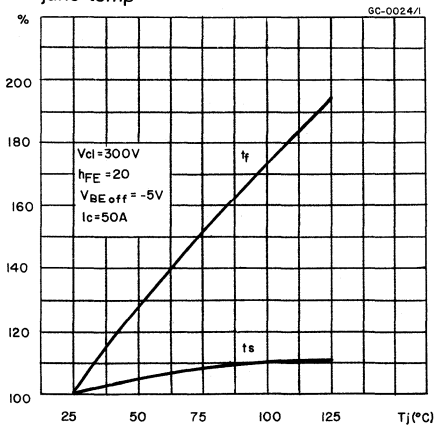
Reverse biased SOA (see fig. 2)



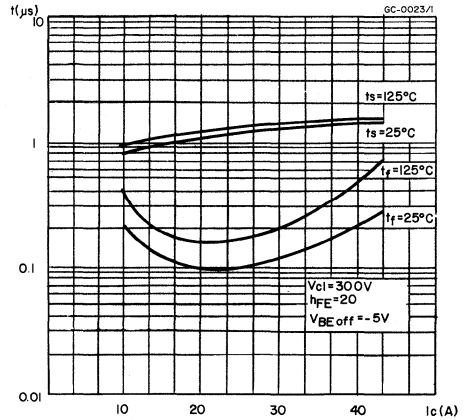
Typical V_F versus $-I_C$



Switching times inductive load vs
junc temp



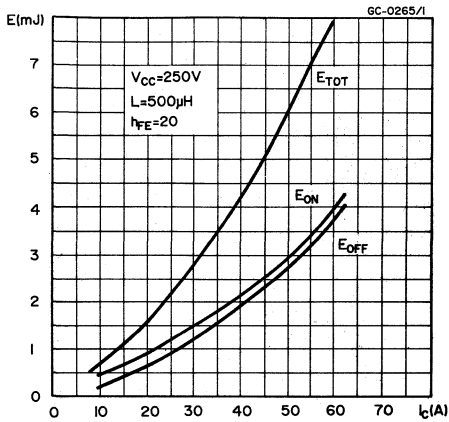
Switching times inductive load (see fig. 3)



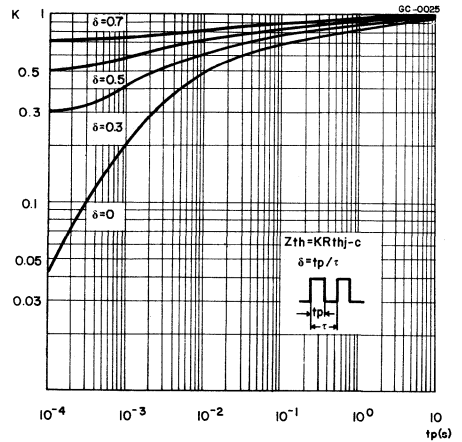


SGS50DB040D
SGS50DB045D

Switch energy losses (see fig. 3)



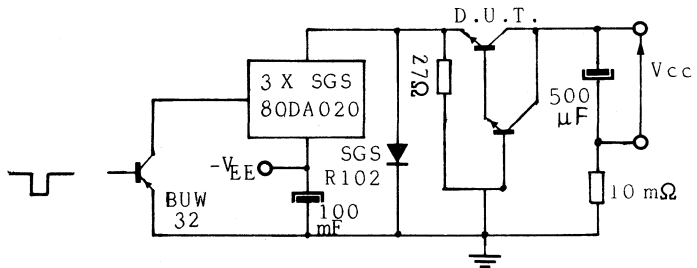
Thermal impedance



OVERLOAD

- Collector

Test circuit



OVERLOAD

- Base

Test circuit

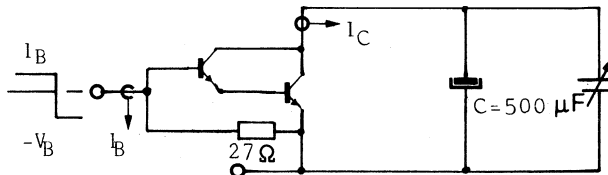


Fig. 1

SC-0001a

Fig. 2 RBSOA TEST CIRCUIT

RBSOA test circuit has been driven by the switching times test circuit with $R_{B2} = 0$.

RBSOA sensitivity to T_j variations is very limited, so that the limits shown can be kept valid at ambient temperature as well.

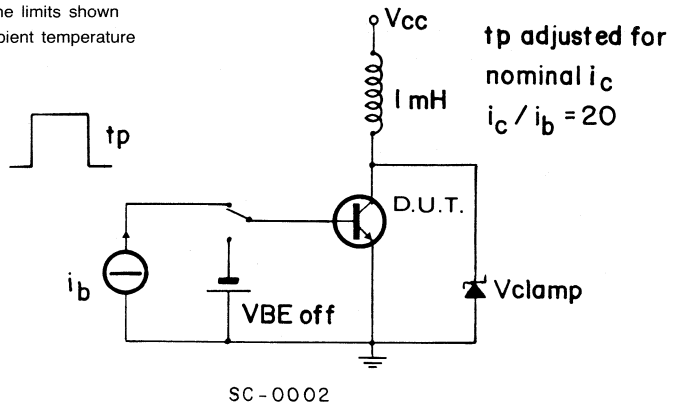
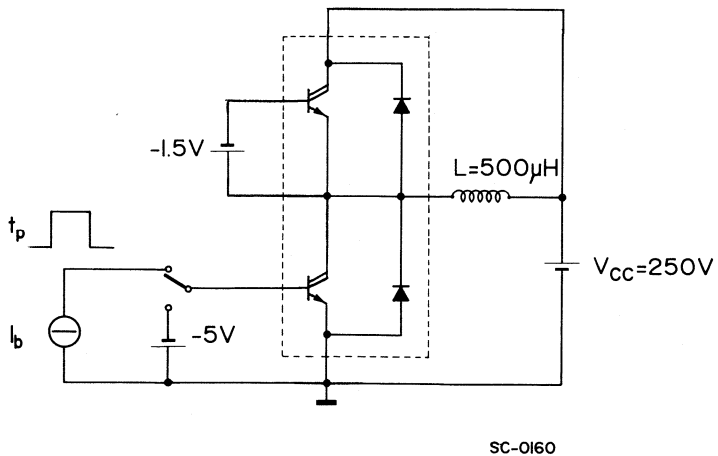


Fig. 3 - Switching time test circuit





FORWARD BIAS SAFE OPERATING AREA

The I_C/V_{CE} limits of a transistor which have to be observed for reliable operation are specified by the safe operating area curves. The transistor must not be subjected to a greater dissipation than that indicated by the SOA boundary, operation outside these limits could result in either rapid or long term failure of the transistor.

The safe operating boundary is defined by four limits:

1. The limit of maximum current.
2. The limit of thermal dissipation.
3. The limit of secondary breakdown.
4. The limit of maximum voltage.

Maximum voltage and current limits are fixed whereas thermal dissipation and secondary breakdown are dependant on the temperature. The normal figures given in the RBSOA diagram are tied to a fixed $T_C = 25^\circ\text{C}$ and for temperatures $>25^\circ\text{C}$ the Power Derating curve (fig. 5) has to be used. As thermal limitations do not derate in the same way as second breakdown limitations, the Power Derating diagram has two curves and the allowable current at the voltages shown on the RBSOA diagram may be found for any case temperature by using the appropriate power derating curve. For power levels under area 2 (fig. 4) the thermal derating curve is effective and for power levels under area 3, the second breakdown derating is used. At extreme case temperatures the thermal limitations reduce power handling to lower values than the limitations caused by second breakdown.

Fig. 4

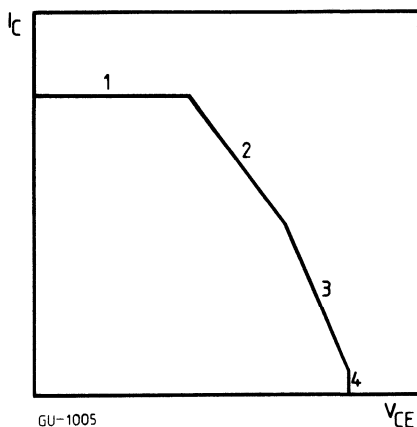
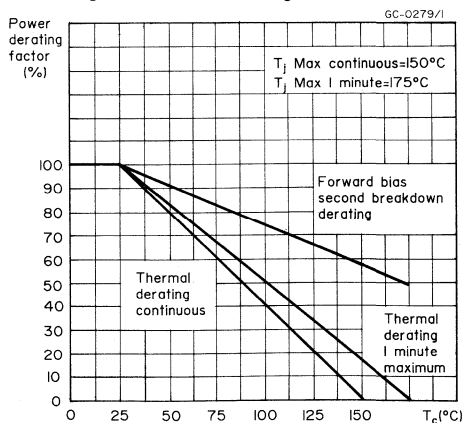


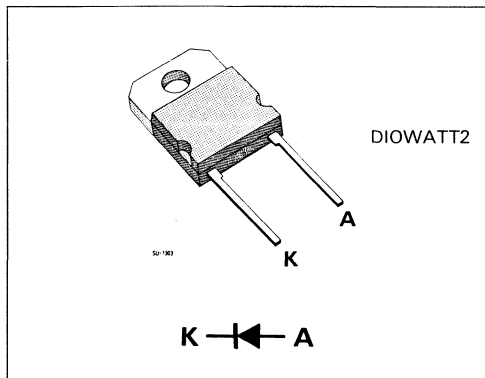
Fig. 5 - Power derating



HIGH SPEED SWITCHING APPLICATIONS

- VOLTAGE RANGE: 400V
- AVERAGE CURRENT: 60A
- VERY LOW REVERSE RECOVERY TIME: t_{rr} 125ns
- VERY LOW SWITCHING LOSSES
- LOW NOISE TURN-OFF SWITCHING

Typical applications include freewheel diodes in motor control systems.



ABSOLUTE MAXIMUM RATINGS

V_{RRM}	Peak repetitive reverse voltage	400	V
V_{RWM}	Working peak reverse voltage	400	V
V_R	Continuous reverse voltage	400	V
I_{FRM}	Repetitive peak forward current ($t = 10\mu s$)	700	A
$I_{F(AV)}$	Average forward current $T_{case} = 70^\circ C$ (switching operation, $\delta = 0.5$)	60	A
I_{FSM}	Surge non repetitive forward current ($t = 10ms$)	600	A
P_{tot}	Total dissipation at $T_{case} = 70^\circ C$	90	W
T_{stg}	Storage temperature	- 65 to 150	$^\circ C$
T_j	Max. operating junction temperature	150	$^\circ C$

THERMAL DATA

R _{thj-case}	Thermal resistance junction-case	max 0.9 °C/W
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ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters	Test Contitions	Min.	Typ.	Max.	Unit
I _R Reverse Current	V = V _R T _j = 25°C V = V _R T _j = 125°C			100 4	μA mA
V _F (*) Forward voltage	I _F = 60A T _{case} = 25°C I _F = 60A T _{case} = 125°C		1.2 1.2	1.5 1.5	V V
t _{rr} Reverse recovery time	I _F = 1A di/dt = 50A/μs V _R = 30V I _F = 60A di/dt = 100A/μs V _R = 30V			125 400	ns ns
Q _{rr} Recovered charge	I _F = 60A di/dt = 100A/μs V _R = 30V		3		μC
V _{FP} Forward recovery overvoltage	I _F = 60A di/dt = 100A/μs		3.5		V

* Pulsed: pulse duration ≤300μs, duty cycle ≤2%

Fig. 1 Forward overvoltage vs. current slope

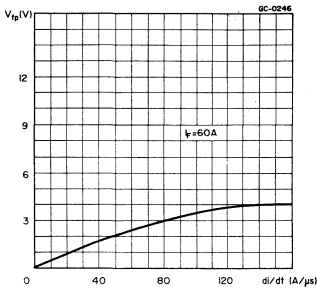


Fig. 2 Reverse leakage current vs. junction temperature

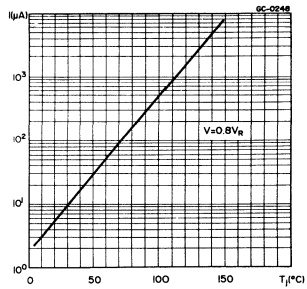
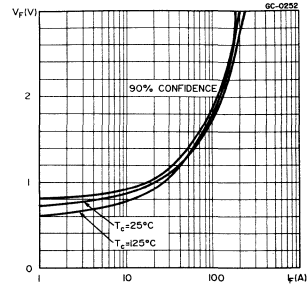


Fig. 3 Voltage drop vs. forward current





SGS80DA020D

TRANSPACK NPN POWER DARLINGTON MODULE

APPLICATIONS: The product is a silicon NPN power darlington for industrial applications.

ISOLATED POWER MODULE (30KVA - 375W)

FAST FREEWHEEL DIODE

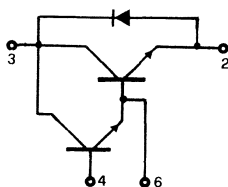
ABSOLUTE MAXIMUM RATINGS

V_{CBO}	Collector-base voltage ($I_E = 0$)
V_{CES}	Collector-emitter voltage ($V_{BE} = 0$)
V_{CEX}	Collector-emitter voltage ($V_{BE} = -1.5V$)
V_{CEO}	Collector-emitter voltage ($I_B = 0$)
V_{CEOL}	Overload switch-off at 1.5 times $I_{C(sat)}$
V_{EBO}	Emitter-base voltage ($I_C = 0$)
I_C	Collector current
I_{CM}	Collector peak current ($t_p < 10$ ms)
I_{CP}	Collector peak current non repetitive ($t_p < 20$ μ s)
I_B	Base current
I_{BP}	Base peak current non repetitive ($t_p < 20$ μ s)
T_{stg}	Storage temperature
T_j	Max. operating junction temperature (continuous)
T_j	Max. operating junction temperature (1 minute)

SGS80DA020D

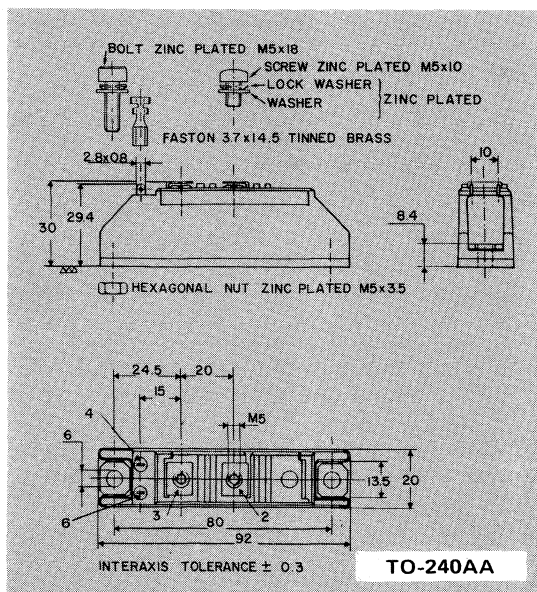
300	V
300	V
300	V
200	V
250	V
7	V
120	A
240	A
500	A
2	A
50	A
- 40 to 150	$^{\circ}C$
150	$^{\circ}C$
175	$^{\circ}C$

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case (darlington)	max 0.33°C/W
$R_{th\ j-case}$	Thermal resistance junction-case (diode)	max 1.10°C/W
$R_{th\ c-h}$	Thermal resistance case-heatsink	max 0.20°C/W

ELECTRICAL CHARACTERISTICS

($T_j = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CER} Collector cutoff current ($R_{BE1} = 3.3\text{Kohm}$ $R_{BE2} = 100\text{ohm}$)	$V_{CE} = V_{CEOL}$			2	mA
	$V_{CE} = V_{CEOL} \quad T_j = 125^\circ\text{C}$			10	mA
I_{CES} Collector cutoff current ($V_{BE1} = V_{BE2} = 0$)	$V_{CE} = V_{CES}$		0.05	2	mA
	$V_{CE} = V_{CEOL} \quad T_j = 125^\circ\text{C}$		3	10	mA
I_{CEX} Collector cutoff current	$V_{CE} = V_{CEX} \quad V_{BE} = -1.5\text{V}$		0.05	2	mA
	$V_{CE} = V_{CEOL} \quad V_{BE} = -1.5\text{V} \quad T_j = 125^\circ\text{C}$		3	10	mA
I_{EBO} Emitter cutoff current ($I_C = 0$)	$V_{BE} = -5\text{V}$			2	mA
$V_{CEO(sus)*}$ Collector-emitter sustaining voltage	$I_C = 0.2\text{A}$ $L = 2\text{mH}$	200			V
V_{CEOL} Max voltage to switch-off 1.5 times $I_{C(sat)}$ (top right corner of RBSOA)	$I_C = 120\text{A}$	250			V
$V_{CE(sat)*}$ Collector-emitter saturation voltage	$I_C = 80\text{ A} \quad I_B = 1\text{ A}$			2	V
$V_{BE(sat)*}$ Base-emitter saturation voltage	$I_C = 80\text{ A} \quad I_B = 1\text{ A}$			3	V
h_{FE}^* DC current gain	$I_C = 80\text{ A} \quad V_{CE} = 5\text{ V}$	500	1000		
INDUCTIVE LOAD (see test circuit)					
t_s Storage time	$I_C = 80\text{ A} \quad I_B = 1\text{ A} \quad V_{BE\ OFF} = -5\text{ V}$		1.60		μs
t_f Fall time	$V_{CC} = 50\text{V} \quad L = 50\text{ }\mu\text{H} \quad V_{CL} = 150\text{V}$ $T_j = 25^\circ\text{C}$		0.18		μs
t_s Storage time	$I_C = 80\text{ A} \quad I_B = 1\text{ A} \quad V_{BE\ OFF} = -5\text{ V}$		1.85	4.0	μs
t_f Fall time	$V_{CC} = 50\text{V} \quad L = 50\text{ }\mu\text{H} \quad V_{CL} = 150\text{V}$ $T_j = 125^\circ\text{C}$		0.30	0.6	μs

* Pulsed: Pulse duration = 300 μs , duty cycle = 1.5%.

ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_f Diode forward voltage	$I_f = 80\text{ A}$ $T_j = 25^\circ\text{C}$ $T_j = 125^\circ\text{C}$		1.60 1.70	2	V V
t_{rr} Diode reverse recovery time	$I_f = 80\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$		0.20	0.5	μs
I_{rm} Diode reverse recovery current			12		A
I_{frm} Diode forward current	$t = 1\text{ ms}$	300			A

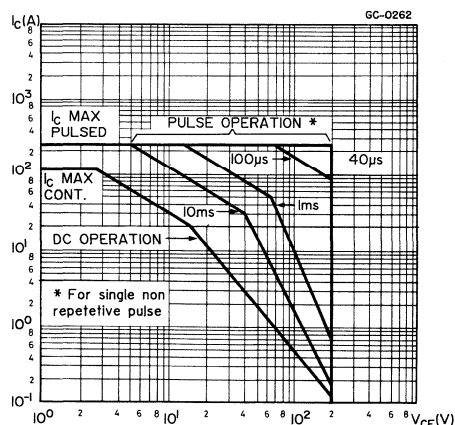
INSULATION TESTING

The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.

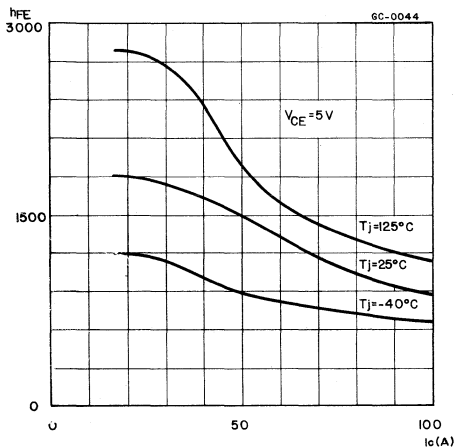
If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/VDE 0558, part 1/8.77, section 5.7.9., only a voltage slowly increasing up to the above value should be used. If the voltage is applied for one minute as recommended by the above standards then the specified value of 2000 V should be taken.

During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

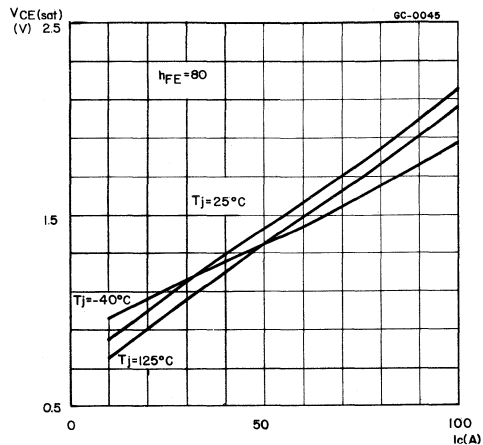
Safe operating areas



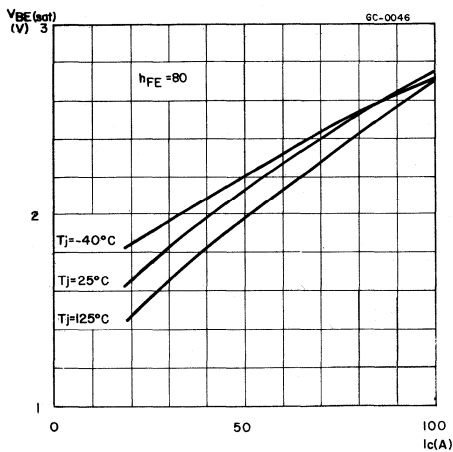
DC current gain



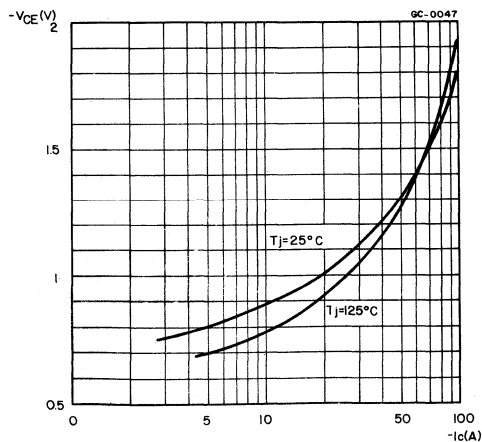
Collector-emitter saturation voltage



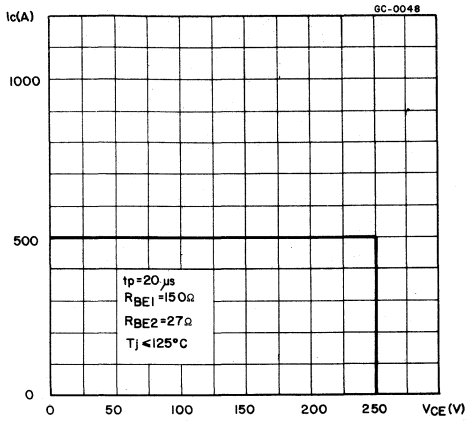
Base-emitter saturation voltage



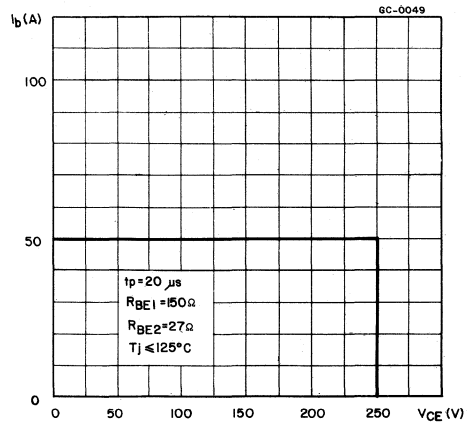
Typical V_F versus $-I_c$



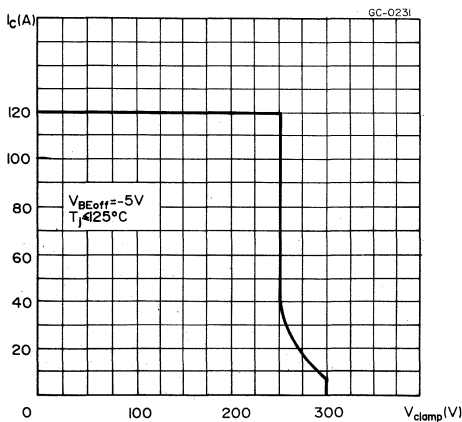
Collector overload SOA (see fig. 1)



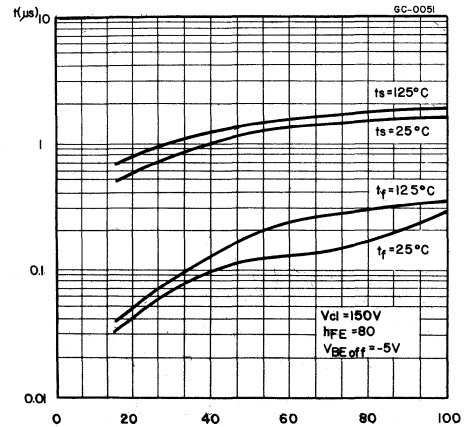
Base overload SOA (see fig. 1)



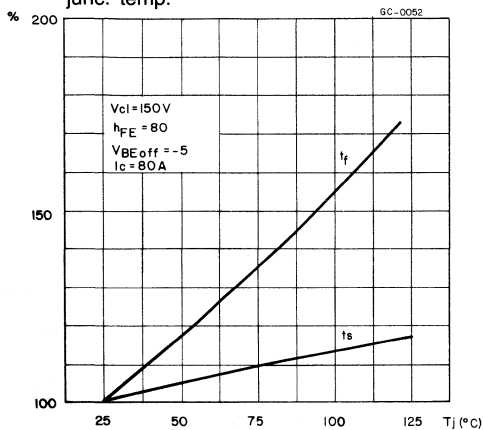
Reverse biased SOA (see fig. 2)



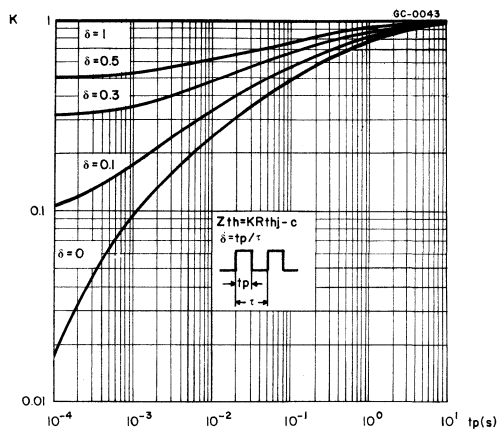
Switching times inductive load (see fig. 3)



Switching times inductive load vs
junc. temp.

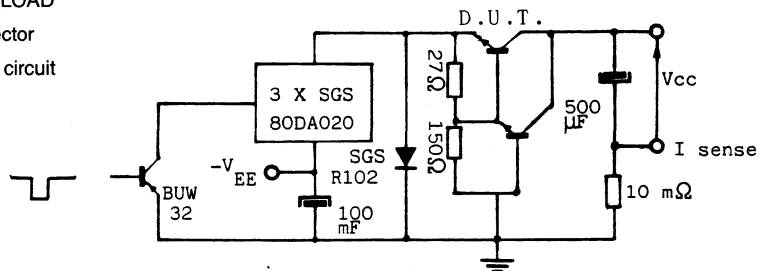


Thermal impedance



OVERLOAD

- Collector
Test circuit



OVERLOAD

- Base
Test circuit

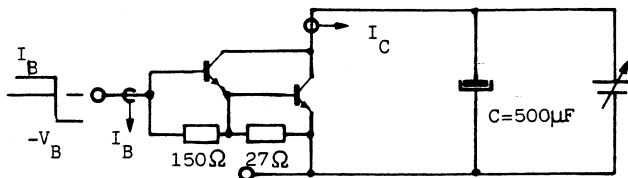


Fig. 1

Fig. 2 RBSOA TEST CIRCUIT

RBSOA test circuit has been driven by the switching times test circuit with $R_{B2} = 0$.

RBSOA sensitivity to T_j variations is very limited, so that the limits shown can be kept valid at ambient temperature as well.

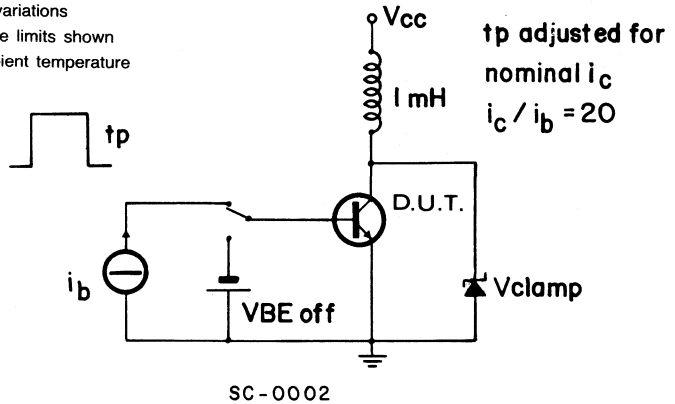
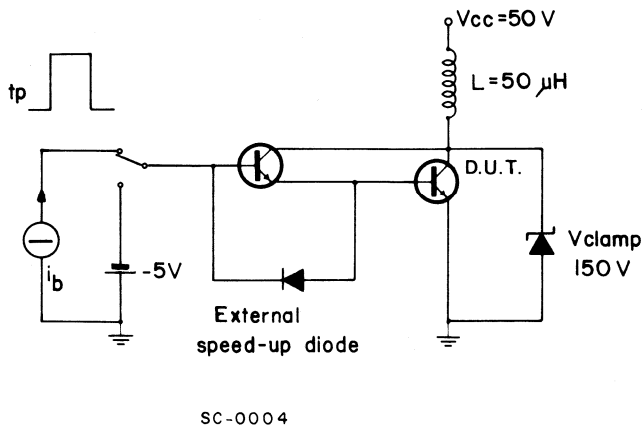


Fig. 3 Switching times test circuit.



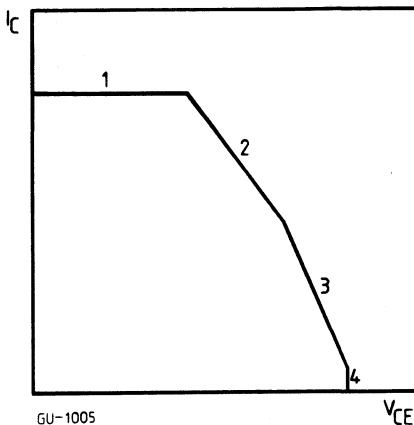
FORWARD BIAS SAFE OPERATING AREA

The I_C/V_{CE} limits of a transistor which have to be observed for reliable operation are specified by the safe operating area curves. The transistor must not be subjected to a greater dissipation than that indicated by the SOA boundary, operation outside these limits could result in either rapid or long term failure of the transistor.

The safe operating boundary is defined by four limits:

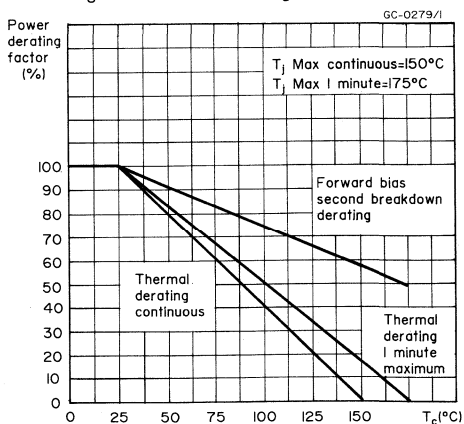
1. The limit of maximum current.
2. The limit of thermal dissipation.
3. The limit of secondary breakdown.
4. The limit of maximum voltage.

Fig. 4



Maximum voltage and current limits are fixed whereas thermal dissipation and secondary breakdown are dependant on the temperature. The normal figures given in the RBSOA diagram are tied to a fixed $T_C = 25^\circ\text{C}$ and for temperatures $>25^\circ\text{C}$ the Power Derating curve (fig. 5) has to be used. As thermal limitations do not derate in the same way as second breakdown limitations, the Power Derating diagram has two curves and the allowable current at the voltages shown on the RBSOA diagram may be found for any case temperature by using the appropriate power derating curve. For power levels under area 2 (fig. 4) the thermal derating curve is effective and for power levels under area 3, the second breakdown derating is used. At extreme case temperatures the thermal limitations reduce power handling to lower values than the limitations caused by second breakdown.

Fig. 5 - Power derating



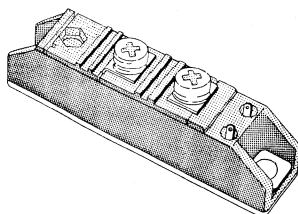
TRANSPACK NPN POWER DARLINGTON MODULE

APPLICATIONS: The product is a silicon NPN power darlington for industrial applications.

- ISOLATED POWER MODULE (UP TO 2500V)
- FAST FREEWHEEL DIODE
- VERY HIGH CURRENT
- VERY HIGH POWER (UP TO 37.5 KVA)

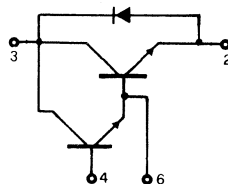
INDUSTRIAL APPLICATIONS

- MOTOR CONTROLS
- UNINTERRUPTABLE POWER SUPPLIES
- HIGH POWER REGULATED DC SUPPLIES



TO-240AA

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SGS100DA025D

V_{CBO}	Collector-base voltage ($I_E = 0$)	300	V
V_{CES}	Collector-emitter voltage ($V_{BE} = 0$)	300	V
V_{CEX}	Collector-emitter voltage ($V_{BE} = -1.5V$)	300	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	250	V
V_{CEOL}	Overload switch-off at 1.5 times $I_{C(sat)}$	250	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	7	V
I_C	Collector current	150	A
I_{CM}	Collector peak current ($t_p < 10$ ms)	300	A
I_{CP}	Collector peak current non repetitive ($t_p < 20$ μ s)	600	A
I_B	Base current	2	A
I_{BP}	Base peak current non repetitive ($t_p < 20$ μ s)	60	A
T_{stg}	Storage temperature	-40 to 150	°C
T_j	Max. operating junction temperature (continuous)	150	°C
T_j	Max. operating junction temperature (1 minute)	175	°C

**THERMAL DATA**

$R_{thj-case}$	Thermal resistance junction-case	max	0.30°C/W
$R_{thj-case}$	Thermal resistance junction-case (diode)	max	1.10°C/W
R_{thc-h}	Thermal resistance case-heatsink	max	0.20°C/W

ELECTRICAL CHARACTERISTICS(T_j = 25°C unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CER} Collector cutoff current ($R_{BE1} = 3K\Omega$ $R_{BE2} = 100\Omega$)	$V_{CE} = V_{CEOL}$ $V_{CE} = V_{CEOL}$ T _j = 125°C			2 10	mA mA
I_{CES} Collector cutoff current ($V_{BE1} = V_{BE2} = 0$)	$V_{CE} = V_{CES}$ $V_{CE} = V_{CEOL}$ T _j = 125°C			2 10	mA mA
I_{CEX} Collector cutoff current	$V_{CE} = V_{CEX}$ $V_{BE} = -1.5V$ $V_{CE} = V_{CEOL}$ $V_{BE} = -1.5V$ T _j = 125°C			2 10	mA mA
I_{EBO} Emitter cutoff current ($I_C = 0$)	$V_{BE} = -5V$			2	mA
$V_{CEO(sus)}$ * Collector emitter 'sustaining voltage'	$I_C = 0.2A$ L = 2mH	250			V
V_{CEOL} Max voltage to switch-off 1.5 times $I_{C(sat)}$ (top right corner of RBSOA)	$I_C = 150A$	250			V
$V_{CE(sat)}$ * Collector-emitter saturation voltage	$I_C = 100A$ $I_B = 1A$			2	V
$V_{BE(sat)}$ * Base-emitter saturation voltage	$I_C = 100A$ $I_B = 1A$			3	V
h_{FE} * DC current gain	$I_C = 100A$ $V_{CE} = 5V$	500	1000		
INDUCTIVE LOAD (see test circuit)					
t_s Storage time	$I_C = 100A$ $I_B = 1A$ $V_{BE OFF} = -5V$		1.6		μs
t_f Fall time	$V_{CC} = 50V$ L = 50 μH $V_{CL} = 150V$ T _j = 25°C		0.18		μs
t_s Storage time	$I_C = 100A$ $I_B = 1A$ $V_{BE OFF} = -5V$			4	μs
t_f Fall time	$V_{CC} = 50V$ L = 50 μH $V_{CL} = 150V$ T _j = 125°C			0.6	μs

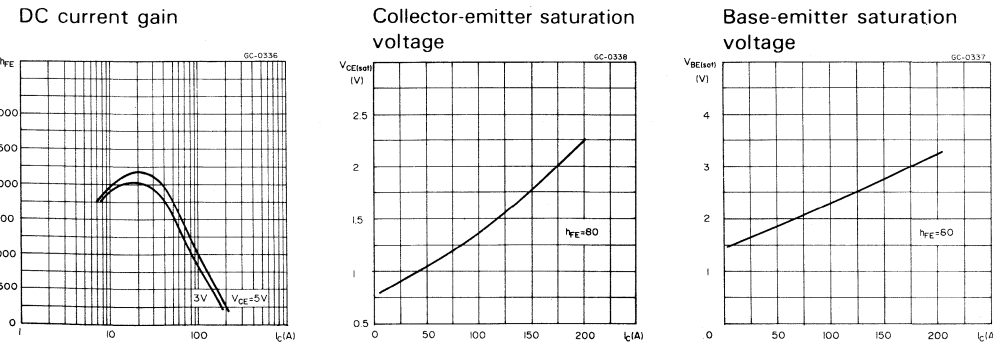
* Pulsed: Pulse duration = 300 μs , duty cycle = 1.5%

ELECTRICAL CHARACTERISTICS
 (Continued)

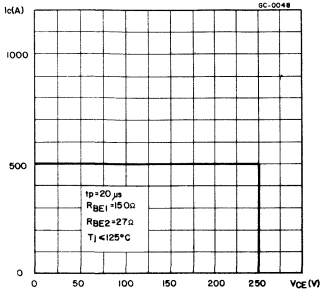
Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_f Diode Forward voltage	$I_f = 100A$ $I_f = 100A$ $T_j = 125^{\circ}C$		1.6 1.7	2	V
t_{rr} Diode reverse recovery time I_{rm} Diode reverse recovery current	$I_f = 100A$ $di/dt = 100A/\mu s$		0.2 15	0.5	μs A
I_{frm} Diode forward current	$t = 1ms$	300			A

INSULATION TESTING

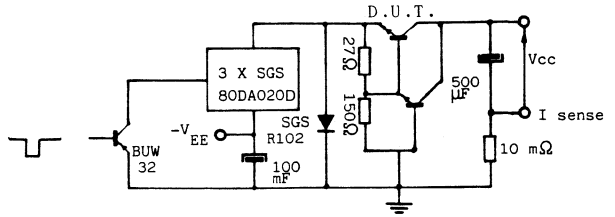
The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.
 If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492. 1 or DIN 57558 part. 1/VDE 0558, part 1/8.77, section 5.7.9., only a voltage slowly increasing up to the above standards then the specified value of 2000 V should be taken.
 During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.



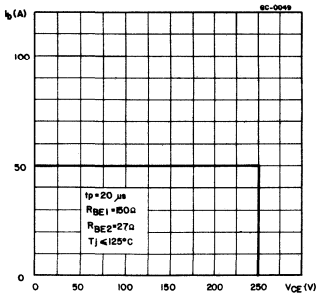
Collector overload SOA



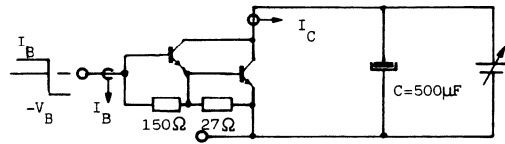
Collector overload test circuit



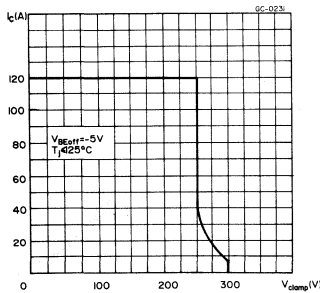
Base overload SOA



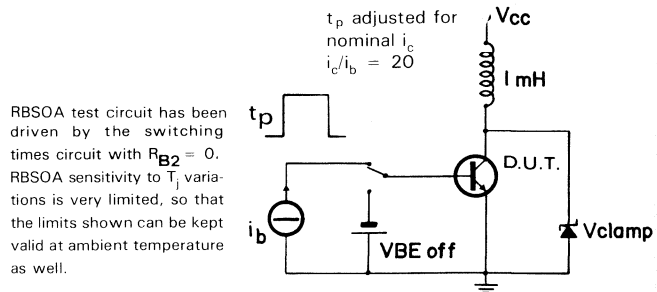
Base overload test circuit



Reverse biased SOA

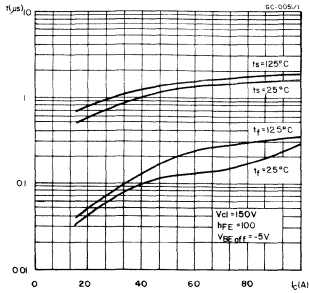


RBSOA test circuit

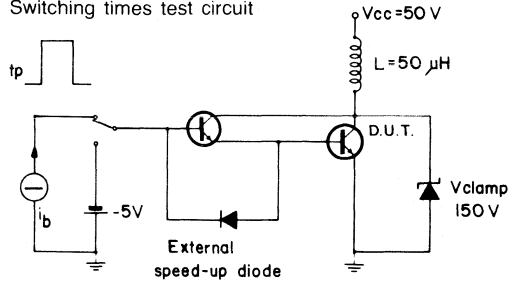


SC-0002

Switching times inductive load

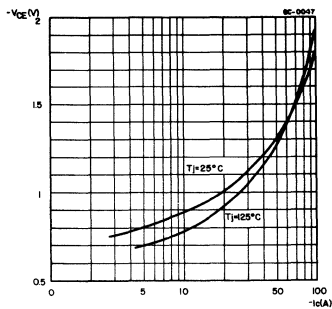


Switching times test circuit

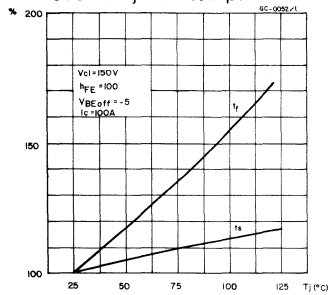


SC-0004

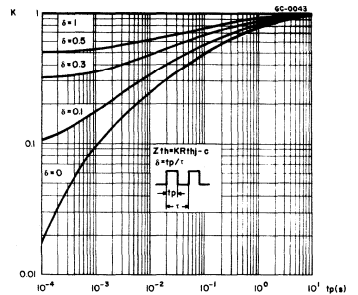
Typical V_F versus $-I_C$



Switching times inductive load vs. junc. temp.



Thermal impedance



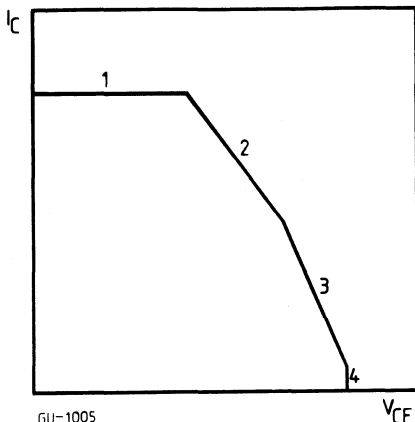
FORWARD BIAS SAFE OPERATING AREA

The I_C/V_{CE} limits of a transistor which have to be observed for reliable operation are specified by the safe operating area curves. The transistor must not be subjected to a greater dissipation than that indicated by the SOA boundary, operation outside these limits could result in either rapid or long term failure of the transistor.

The safe operating boundary is defined by four limits:

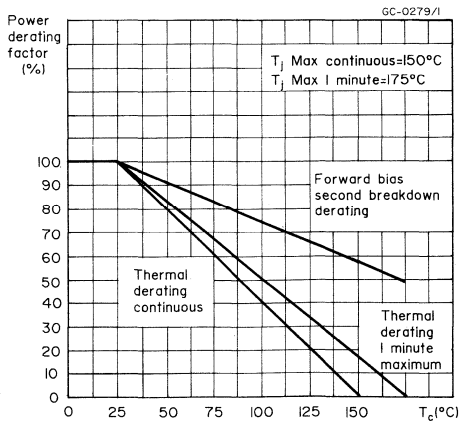
1. The limit of maximum current.
2. The limit of thermal dissipation.
3. The limit of secondary breakdown.
4. The limit of maximum voltage.

Fig. 1



Maximum voltage and current limits are fixed whereas thermal dissipation and secondary breakdown are dependant on the temperature. The normal figures given in the RBSOA diagram are tied to a fixed $T_C = 25^\circ\text{C}$ and for temperatures $>25^\circ\text{C}$ the Power Derating curve (fig. 2) has to be used. As thermal limitations do not derate in the same way as second breakdown limitations, the Power Derating diagram has two curves and the allowable current at the voltages shown on the RBSOA diagram may be found for any case temperature by using the appropriate power derating curve. For power levels under area 2 (fig 1) the thermal derating curve is effective and for power levels under area 3, the second breakdown derating is used. At extreme case temperatures the thermal limitations reduce power handling to lower values than the limitations caused by second breakdown.

Fig. 2 - Power derating





SGS100MA010D1

ADVANCE DATA

TRANSPACK N-CHANNEL POWER MOS MODULE

APPLICATIONS: The SGS100MA010D1 is a N-Channel POWER MOS MODULE for industrial applications (quarter bridge configuration).

ISOLATED POWER MODULE (10KVA - 375W)

INTERNAL FREEWHEEL DIODE

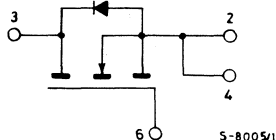
ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)
V_{DGR}	Drain-gate voltage ($R_{GS} = 20\text{ K}\Omega$)
V_{GS}	Gate-source voltage
I_D	Drain current (continuous) $T_C = 25^\circ\text{C}$
I_{DM}	Drain current ($t_p < 10\text{ ms}$, repetitive)
I_{DLM}	Drain current ($t_p = 20\mu\text{s}$, not repetitive)
P_{tot}	Total dissipation at $T_C < 25^\circ\text{C}$
	Derating factor
T_{stg}	Storage temperature
T_j	Max. operating junction temperature (continuous)
T_j	Max. operating junction temperature (1 minute)

SGS100MA010D1

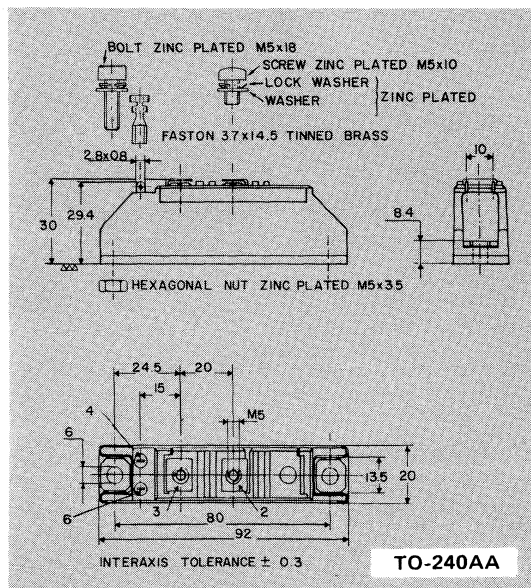
100	V
100	V
± 20	V
100	A
150	A
250	A
300	W
3	W/ $^\circ\text{C}$
-55 to 150	$^\circ\text{C}$
150	$^\circ\text{C}$
175	$^\circ\text{C}$

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.



SGS100MA010D1

THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max 0.33	°C/W
$R_{th\ c-h}$	Thermal resistance case-heatsink	max 0.20	°C/W

ELECTRICAL CHARACTERISTICS $(T_j = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 2\text{ mA}$ $V_{GS} = 0$	100			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max. Rating}$			2	mA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			100	nA

ON (*)

$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 2\text{ mA}$	2		4	V
$V_{DS(on)}$	Drain-source voltage	$V_{GS} = 10\text{V}$ $I_D = 50\text{ A}$ $V_{GS} = 10\text{V}$ $I_D = 100\text{ A}$		0.7 1.18	0.9	V V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$ $I_D = 50\text{ A}$			.018	Ω
g_{fs}	Forward transconductance	$V_{DS} = 50\text{V}$ $I_D = 25\text{ A}$	36	50		mho

DYNAMIC

C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$		7200		pF
C_{oss}	Output capacitance			2600		pF
C_{rss}	Reverse transfer capacitance			1200		pF

SWITCHING TIMES INDUCTIVE LOAD (see note A)

$t_{d(on)}$	Turn-on time	$V_{CC} = 50\text{ V}$ $I_D = 50\text{ A}$ $V_i = 10\text{ V}$ $R_i = 50\text{ }\Omega$ $L = 100\text{ }\mu\text{H}$		100		ns
$(di/dt)_{on}$	Turn-on current slope			250		A/ μs
$t_{d(off)}$	Turn-off delay time			1.1		μs
t_f	Fall time			130		ns

* Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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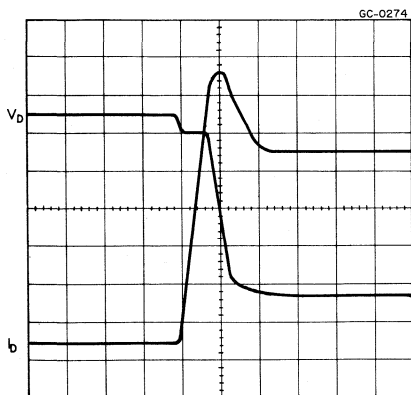
SOURCE DRAIN DIODE (see note B)

I_{SD}	Source-drain current (continuous)			100	A
I_{SDM}	Source-drain current (pulsed)			250	A
V_{SD}	Forward on voltage	$I_{SD} = 100\text{ A}$ $V_{GS} = 0$		2	V
t_{rr}	Reverse recovery time	$I_{SD} = 100\text{ A}$ $V_{GS} = 0$ $di/dt = 250\text{ A}/\mu\text{s}$	400		ns

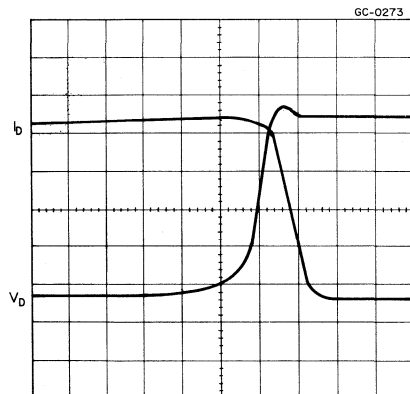
Note A: switching times inductive load have been tested by the circuit shown in fig. 1 (by paralleling the load with SGS fast recovery diode...).

Typical waveforms obtained for V_D and I_D are schematically shown here below.

I_D - V_D at turn-on



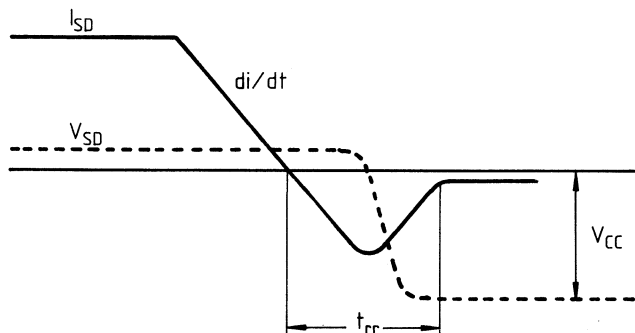
I_D - V_D at turn-off



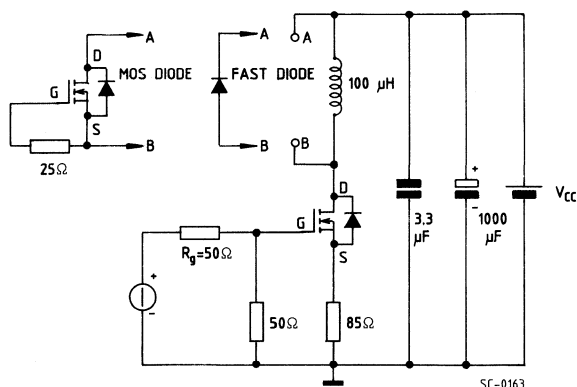
Note that di/dt does not depend on the performances of the freewheeling diode, but on the D.U.T. and its drive circuit only.



Note B: The switching performances of the source drain diode have been tested by the circuit shown in fig. 1 (by paralleling it to the load using another identical module for switching). Typical waveforms obtained for V_{SD} and I_{SD} are schematically shown here below.



SC-0162



SC-0163

Fig. 1: Switching times inductive load and body drain diode t_{rr} , Q_{rr} test circuit.



N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

V_{DS}	$R_{DS(on)}$	I_D
100V	0.009 Ω	150A

- ISOLATED POWERMOS MODULE
- HIGH POWER
- FAST SWITCHING
- EASY DRIVE

- EASY TO PARALLEL

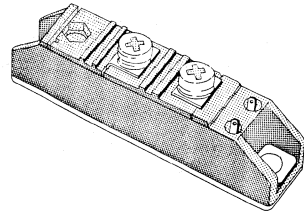
INDUSTRIAL APPLICATION:

- SWITCHING MODE POWER SUPPLIES
- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS
- INVERTERS

N-Channel enhancement mode POWERMOS field effect transistors. Easy drive and fast switching of these TRANSPACK modules makes them ideal for high power, high speed switching applications.

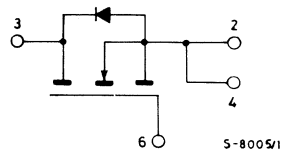
Typical applications include DC motor control (speed, soft start and torque), switching mode power supplies, uninterruptible power supplies, DC/DC converters and high frequency welding equipment.

The large RBSOA and absence of second breakdown in POWERMOS make these TRANSPACK modules very rugged. This, together with the isolated package with its optimised thermal performance, make these modules extremely effective in high power application.



TO-240AA

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)
V_{GS}	Gate-source voltage
I_D	Drain current (continuous) $T_c = 25^\circ C$
I_{DM}	Drain current ($t_p \leq 10$ ms, repetitive)
I_{DLM}	Drain current, ($t_p = 20\mu s$, not repetitive)
P_{tot}	Total dissipation at $T_{case} < 25^\circ C$
	Derating factor
T_{stg}	Storage temperature
T_j	Max. operating junction temperature (continuous)

SGS150MA010D1

100	V
100	V
± 20	V
150	A
225	A
375	A
400	W
3.2	W/ $^\circ C$
-55 to 150	$^\circ C$
150	$^\circ C$

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

**SGS150MA010D1****THERMAL DATA**

$R_{th\ j-case}$	Thermal resistance junction-case	max.	0.31 °C/W
R_{thc-h}	Thermal resistance case-heatsink	max.	0.20 °C/W

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
-----------	-----------------	------	------	------	------

OFF

$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 2\text{ mA}$ $V_{GS} = 0$	100			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$			2	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			100	nA

ON*

$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 2\text{ mA}$	2		4	V
$V_{DS(on)}$	Drain-source voltage	$V_{GS} = 10V$ $I_D = 75A$			0.675	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10V$ $I_D = 75A$			0.009	Ω
g_{fs}	Forward transconductance	$V_{DS} = 25V$ $I_D = 75A$		60		mho

DYNAMIC

C_{iss}	Input capacitance	$V_{DS} = 25V$ $f = 1\text{ MHz}$		10000		pF
C_{oss}	Output capacitance	$V_{GS} = 0$		3800		pF
C_{rss}	Reverse transfer capacitance			1600		pF

SWITCHING TIMES INDUCTIVE LOAD (see note A)

$t_{d(on)}$	Turn-on time	$V_{CC} = 50V$ $I_D = 75A$		100		ns
$(di/dt)_{on}$	Turn-on current slope	$V_i = 10V$ $R_i = 50\Omega$		250		A/ μs
$t_{d(off)}$	Turn off delay time	$L = 100/\mu H$		1.1		μs
t_f	Fall time			130		ns

* Pulsed: Pulse duration = 300 μs , duty cycle = 1.5%

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit.
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SOURCE DRAIN DIODE

I_{SD}	Source-Drain current (continuous)			150	A
I_{SDM}	Source-Drain current (pulsed)			375	A
V_{SD}	Forward on voltage	$I_{SD} = 150A$ $V_{GS} = 0$		2	V
t_{rr}	Reverse recovery time	$di/dt = 250A/\mu s$ $I_{SD} = 150A$ $V_{GS} = 0$	400		ns

INSULATION TESTING

The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.

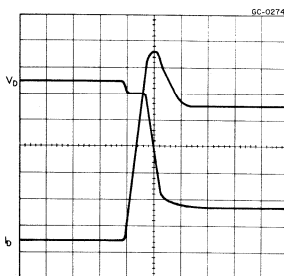
If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/VDE 0558, part 1/8.77, section 5.7.9., only a voltage slowly increasing up to the above standards then the specified value of 2000 V should be taken.

During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

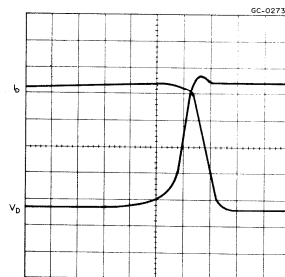
Note A: switching times inductive load have been tested by the circuit shown in fig. 1 (by paralleling the load with SGS fast recovery diode SGS45R80).

Typical waveforms obtained for V_D and I_D are schematically shown here below.

I_D - V_D at turn-on

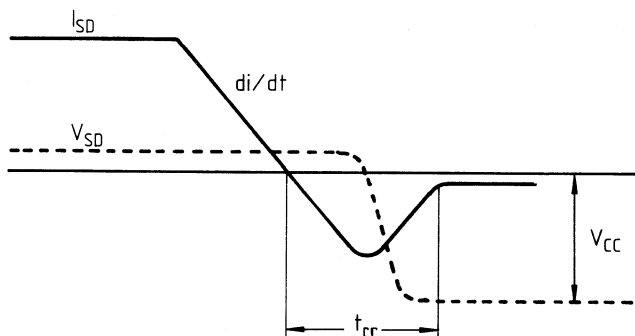


I_D - V_D at turn-off



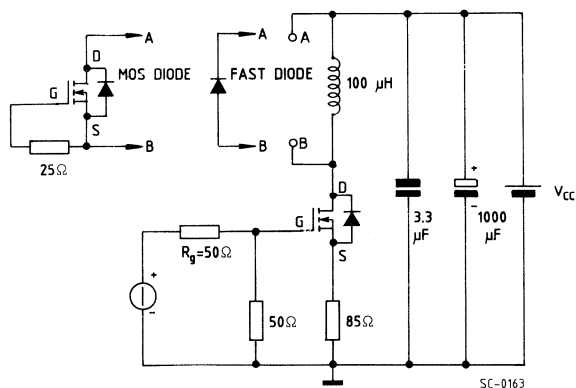
Note that di/dt does not depend on the performances of the freewheeling diode, but on the D.U.T. and its drive circuit only.

Note B: The switching performances of the source drain diode have been tested by the circuit shown in fig. 1 (by paralleling it to the load using another identical module for switching). Typical waveforms obtained for V_{SD} and I_{SD} are schematically shown here below.



SC-0162

Fig. 1: Switching times inductive load and body drain diode t_{rr} , Q_{rr} test circuit.



SC-0163



SGS10004
SGS10004P
SGS10005
SGS10005P

ADVANCE DATA

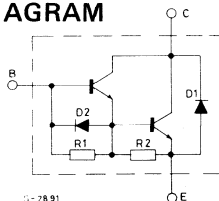
HIGH VOLTAGE FAST SWITCHING

The SGS10004/10005 are silicon power Darlington transistors with integrated base-emitter speed-up diode, mounted in Jedec TO-3 metal case designed for high-power, fast switching applications. The SGS10004P and SGS10005P are mounted in SOT-93 case similar to TO-218. This family is an economic alternative to MJ10004 or MJ10005 particularly suitable for applications at 8A operating currents.

ABSOLUTE MAXIMUM RATING

	SOT-93 TO-3	SGS10004P SGS10004	SGS10005P SGS10005
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	350V	400V
V_{CEX}	Collector-emitter voltage ($V_{BE} = -5V$)	400V	450V
V_{CEV}	Collector-emitter voltage ($V_{BE} = 1.5V$)	450V	500V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	8V	
I_C	Collector current	16A	
I_{CM}	Collector peak current	25A	
I_B	Base current	2.5A	
I_{BM}	Base peak current	5A	
P_{tot}	Total power dissipation at $T_{case} \leq 25^\circ C$	(TO-3) 175W	(SOT-93) 150W
T_{stg}	Storage temperature	-65 to $200^\circ C$	-65 to $175^\circ C$
T_j	Junction temperature	$200^\circ C$	$175^\circ C$

INTERNAL SCHEMATIC DIAGRAM

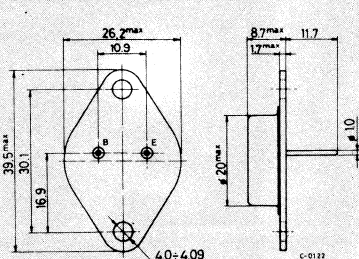


R1 Typ. 100 Ω
R2 Typ. 350 Ω

MECHANICAL DATA

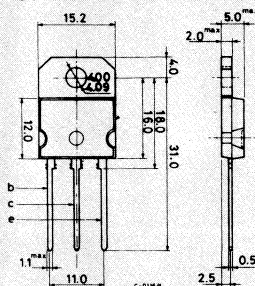
Dimension in mm

Collector connected to case



TO-3

Collector connected to tab



(sim. to TO-218) SOT-93

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max	1	$^{\circ}C/W$
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ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

Parameter		Test conditions	Min. Typ. Max.	Unit
I_{EBO}	Emitter cutoff current ($I_C = 0$)	$V_{EB} = 2V$	25	mA
I_{CER}	Collector cutoff current ($R_{BE} = 50\Omega$)	$V_{CE} = \text{Rated } V_{CEV}$ $T_C = 100^{\circ}C$	5	mA
I_{CEV}	Collector cutoff current ($V_{BE} = 1.5V$)	$V_{CEV} = \text{Rated Value}$ $V_{CEV} = \text{Rated Value}$ $T_{case} = 150^{\circ}C$	0.25	mA
			5	mA
h_{FE}^*	DC Current gain	$I_C = 5A \quad V_{CE} = 5V$	50	—
		$I_C = 8A \quad V_{CE} = 5V$	40	—
		$I_C = 16A \quad V_{CE} = 5V$	10	—
$V_{CEO(sus)}^*$	Collector-emitter sustaining voltage ($I_B = 0$)	$I_C = 250mA$ $V_{Clamp} = \text{Rated } V_{CEO}$ for SGS10004 for SGS10005	350 400	V V
$V_{CEX(sus)}^*$	Collector-emitter sustaining voltage ($V_{BE} = -5V$)	$I_C = 2A$ $V_{Clamp} = \text{Rated } V_{CEX}$ $T_{case} = 100^{\circ}C$ for SGS10004 for SGS10005 $I_C = 10A \quad T_{case} = 100^{\circ}C$ $V_{Clamp} = \text{Rated } V_{CEX}$ for SGS10004 for SGS10005	400	V
			450	V
			275 325	V V
$V_{CE(sat)}^*$	Collector-emitter saturation voltage	$I_C = 8A \quad I_B = 400mA$ $I_C = 8A \quad I_B = 400mA$ $T_{case} = 100^{\circ}C$	1.8	V
			2	V
$V_{BE(sat)}^*$	Base-emitter saturation voltage	$I_C = 8A \quad I_B = 400mA$ $I_C = 8A \quad I_B = 400mA$ $T_{case} = 100^{\circ}C$	2.5	V
			2.5	V



ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_f^*	Diode forward voltage	$I_F = 10A$	3	5		V
h_{fe}	Small-signal current gain	$I_C = 1A$ $V_{CE} = 10V$ $f_{test} = 1MHz$	10			—
C_{OB}	Output capacitance	$V_{CB} = 10V$ $I_E = 0$ $f_{test} = 100MHz$	100		325	pF
t_{on}	Turn-on time	$V_{CC} = 250V$ $I_C = 8A$ $I_{B1} = -I_{B2} = 400mA$ $V_{BE (off)} = 5V$	0.22	0.8		μs
t_r	Rise Time		0.6	1.5		μs
t_f	Fall time		0.15	0.5		μs

* Pulsed: pulse duration = 300 μs duty cycle = 1.5% .



SGSD00030
SGSD00031
SGSID312

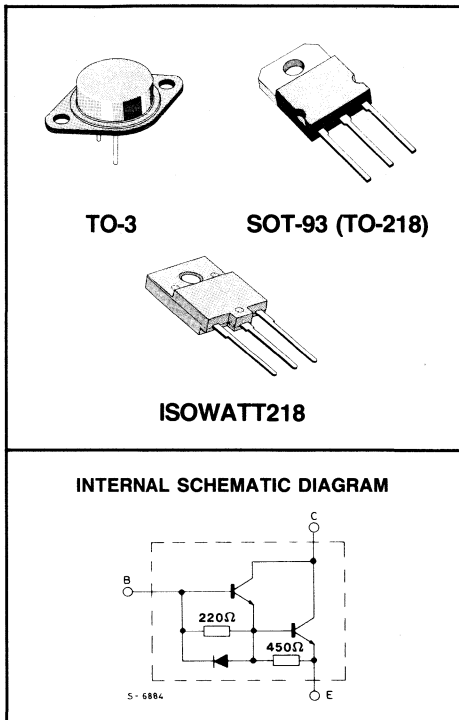
HIGH VOLTAGE, HIGH POWER, FAST SWITCHING

- INTEGRATED SPEED-UP DIODE
- MOTOR CONTROLS

The SGSD00031, SGS00030 and SGSID312 are silicon multiepitaxial planar NPN transistors in monolithic darlington configuration with integrated speed-up diode, mounted respectively in Jedec TO-3 metal case, SOT-93 plastic package and ISOWATT218 fully isolated package.

No parasitic collector-emitter diode, so that an external fast recovery free wheeling diode can be added.

They are particularly suitable as output stage in high power, fast switching applications.



ABSOLUTE MAXIMUM RATINGS

V_{CER}	Collector-emitter voltage ($R_{BE} = 50 \text{ ohm}$)	600	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	400	V
I_C	Collector current	28	A
I_{CM}	Collector peak current ($t_p \leq 10\text{ms}$)	40	A
I_B	Base current	6	A
I_{BM}	Base peak current ($t_p \leq 10\text{ms}$)	12	A
V_{ISO}	Isolation voltage (DC)		
P_{tot}	Total dissipation at $T_c \leq 25^\circ\text{C}$		
T_{stg}	Storage temperature		
T_j	Max. operating junction temperature		
		TO-3	SOT-93
			ISOWATT218
			4000
		150	125
		50	50
		-65 to 175	-65 to 150
		-65 to 150	-65 to 150
		175	150
			150
			°C



SGSD00030
SGSD00031
SGSID312

THERMAL DATA

			TO-3	SOT-93	ISOWATT218	
$R_{th\ j-case}$	Thermal resistance junction-case	max	1	1	2.5•	°C/W

• See notes on ISOWATT218 in this datasheet.

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CEV} Collector cutoff current ($V_{BE} = -1.5\ V$)	$V_{CE} = 600\ V$ $V_{CE} = 600\ V\ T_c = 100^{\circ}C$			100 2	μA mA
I_{EBO} Emitter cutoff Current ($I_C = 0$)	$V_{EB} = 2\ V$			30	mA
$V_{CEO(sus)}$ *Collector-emitter sustaining voltage	$I_C = 100mA$	400			V V
$V_{CE(sat)}$ * Collector-emitter saturation voltage	$I_C = 10\ A\ I_B = 0.1\ A$ $I_C = 18\ A\ I_B = 1.8\ A$			2.5 3.5	V V
h_{FE} * DC current gain	$I_C = 10\ A\ V_{CE} = 5\ V$ $I_C = 18\ A\ V_{CE} = 5\ V$	30 20			
I_{ol} Output current overload	accidental overload switch-off current $V_{clamp} = 400\ V\ L = 100\mu H$ $t_{ol} = 10\ \mu s\ T_j = 125^{\circ}C$	28			A

RESISTIVE LOAD

t_{on} Turn-on time	$V_{CC} = 250\ V\ I_C = 12\ A$			0.6	μs
t_s Storage time	$I_{B1} = 0.1\ A\ V_{BE(off)} = -5\ V$			1.5	μs
t_f Fall time				0.6	μs

INDUCTIVE LOAD

t_s Storage time	$V_{CC} = 250\ V\ I_C = 12\ A$			1.5	μs
t_f Fall time	$I_{B1} = 0.1\ A\ V_{BE(off)} = -5\ V$ $L = 180\ \mu H$			0.5	μs
t_s Storage time	$V_{CC} = 250\ V\ I_C = 18\ A$			1.5	μs
t_f Fall time	$I_{B1} = 0.1\ A\ V_{BE(off)} = -5\ V$ $L = 180\ \mu H$			0.7	μs

* Pulsed: Pulse duration = 300 μs , duty cycle = 1.5%



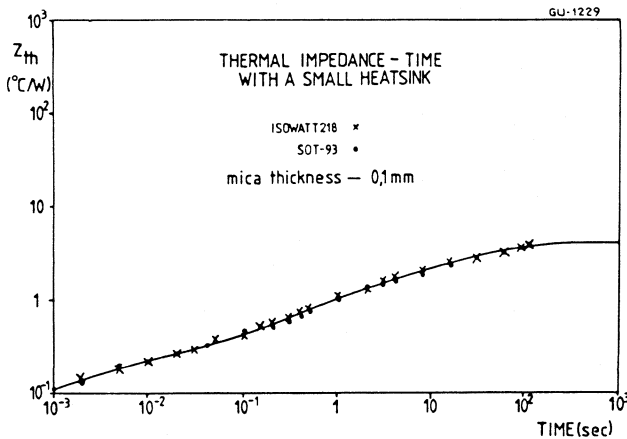
SGSD00030
SGSD00031
SGSID312

THERMAL RESISTANCE OF THE ISOWATT218

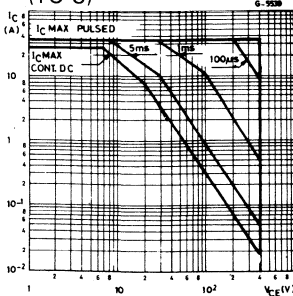
The junction to case thermal resistance of 2.5 °C/W for the ISOWATT218 package may seem quite high at first glance but if compared to a conventional SOT-93 (TO-218) package with a 0.1 mm mica insulating washer, the differences are marginal. The 0.1 mm isolating washer gives 1500V to 2000V DC isolation for the SOT-93 package, SGS guarantee 4000V DC isolation for the ISOWATT218.

The comparison in fig. 1 shows the dynamic thermal resistance of both devices mounted using a thermal compound. The test illustrates that the ISOWATT218 has an R_{th} very close to that of conventional SOT-93 (TO-218) and any small increase is more than compensated for by the convenience of the ISOWATT218 package. The collector to heatsink capacitance of the ISOWATT218 is typically 17pF.

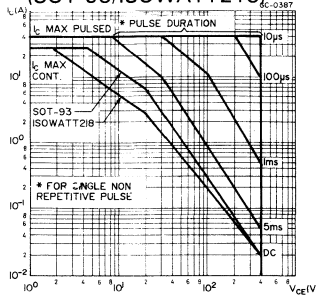
Fig. 1



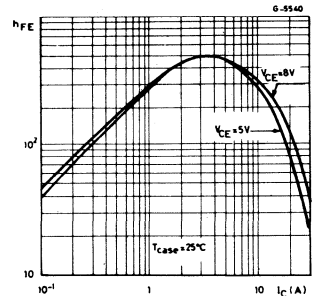
Safe operating area (TO-3)



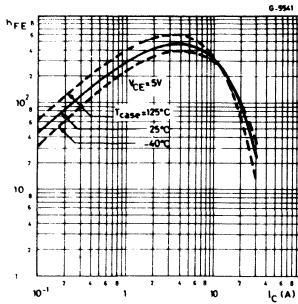
Safe operating area (SOT-93/ISOWATT218)



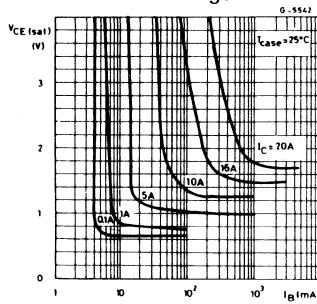
DC current gain



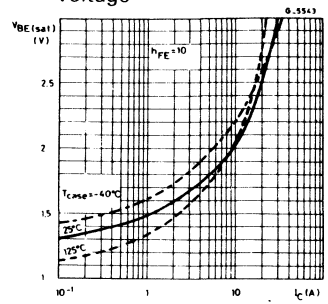
DC current gain



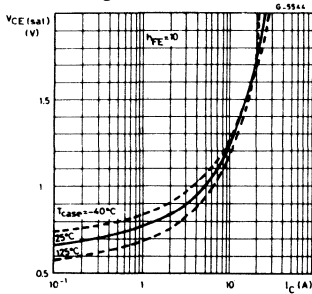
Collector-emitter saturation voltage



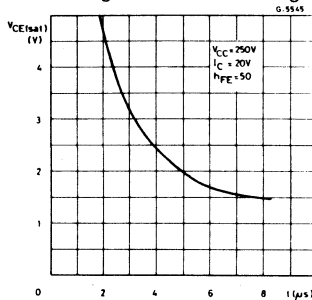
Base-emitter saturation voltage



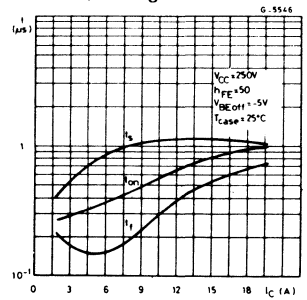
Collector emitter saturation voltage



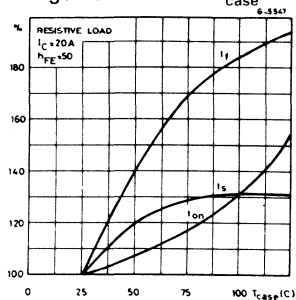
Collector-emitter saturation voltage dynamic (see fig. 2)



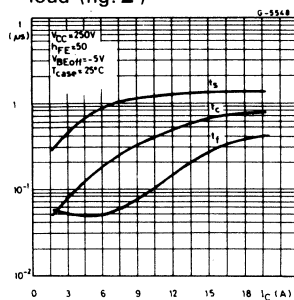
Switching times resistive load (see fig. 2)



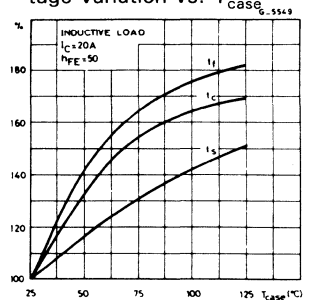
Switching times percentage variation vs. T_{case}



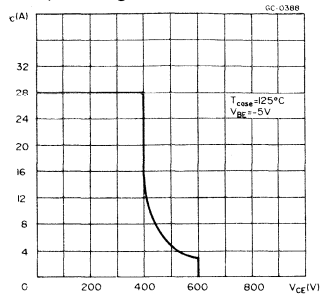
Switching times inductive load (fig. 2)



Switching times percentage variation vs. T_{case}

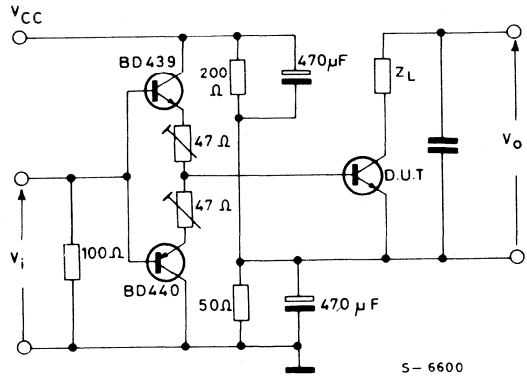


Clamped reverse bias safe operating areas



TEST CIRCUIT

Fig. 2





**SGSD310
SGSD311
SGSID311**

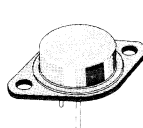
HIGH VOLTAGE, HIGH POWER, FAST SWITCHING

- INTEGRATED SPEED-UP DIODE
- MOTOR CONTROLS

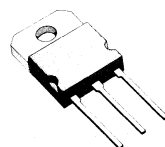
The SGSD310, SGSD311 and SGSID311 are silicon multiepitaxial planar NPN transistors in monolithic darlington configuration with integrated speed-up diode, mounted respectively in Jedec TO-3 metal case, SOT-93 plastic package and ISOWATT218 fully isolated package.

No parasitic collector-emitter diode, so that an external fast recovery free wheeling diode can be added.

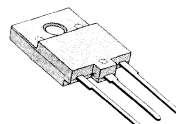
They are particularly suitable as output stage in high power, fast switching applications.



TO-3

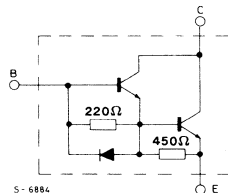


SOT-93 (TO-218)



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{CER}	Collector-emitter voltage ($R_{BE} = 50 \text{ ohm}$)	600	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	400	V
I_C	Collector current	28	A
I_{CM}	Collector peak current ($t_p \leq 10\text{ms}$)	40	A
I_B	Base current	6	A
I_{BM}	Base peak current ($t_p \leq 10\text{ms}$)	12	A
V_{ISO}	Isolation voltage (DC)		
P_{tot}	Total dissipation at $T_c \leq 25^\circ\text{C}$	150	W
T_{stg}	Storage temperature	-65 to 175	$^\circ\text{C}$
T_j	Max. operating junction temperature	175	$^\circ\text{C}$

TO-3 SOT-93 ISOWATT218

		4000	V
		50	W
	-65 to 150	-65 to 150	$^\circ\text{C}$
	150	150	$^\circ\text{C}$



SGSD310
SGSD311
SGSID311

THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max	TO-3	SOT-93	ISOWATT218
			1	1	2.5• °C/W

• See notes on ISOWATT218 in this datasheet.

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CEV} Collector cutoff current ($V_{BE} = -1.5\ V$)	$V_{CE} = 600\ V$ $V_{CE} = 600\ V\ T_c = 100^{\circ}C$			100 2	μA mA
I_{EBO} Emitter cutoff current ($I_C = 0$)	$V_{EB} = 2\ V$			30	mA
$V_{CEO(sus)}$ * Collector-emitter sustaining voltage	$I_C = 100\ mA$	400			V
$V_{CE(sat)}$ * Collector-emitter saturation voltage	$I_C = 10\ A\ I_B = 0.5\ A$ $I_C = 18\ A\ I_B = 1.8\ A$ $I_C = 22\ A\ I_B = 2.2\ A$ $I_C = 28\ A\ I_B = 5.6\ A$			2 2.5 3 5	V V V V
$V_{BE(sat)}$ * Base-emitter saturation voltage	$I_C = 10\ A\ I_B = 0.5\ A$ $I_C = 18\ A\ I_B = 1.8\ A$ $I_C = 22\ A\ I_B = 2.2\ A$			2.5 3 3.3	V V V
h_{FE} * DC current gain	$I_C = 10\ A\ V_{CE} = 5\ V$ $I_C = 18\ A\ V_{CE} = 5\ V$	30 20			
I_{ol} Output current overload	accidental overload switch-off current $V_{clamp} = 400\ V\ L = 100\ \mu H$ $t_{ol} = 10\ \mu s\ T_j = 125^{\circ}C$	28			A

RESISTIVE LOAD

t_{on} Turn-on time	$V_{CC} = 250\ V\ I_C = 10\ A$			0.6	μs
t_s Storage time	$I_{B1} = 0.5\ A\ V_{BE(off)} = -5\ V$			1.5	μs
t_f Fall time				0.6	μs

INDUCTIVE LOAD

t_s Storage time	$V_{CC} = 250\ V\ I_C = 10\ A$			1.5	μs
t_f Fall time	$I_{B1} = 0.5\ A\ V_{BE(off)} = -5\ V$ $L = 180\ \mu H$			0.5	μs
t_s Storage time	$V_{CC} = 250\ V\ I_C = 20\ A$			1.5	μs
t_f Fall time	$I_{B1} = 2\ A\ V_{BE(off)} = -5\ V$ $L = 180\ \mu H$			0.7	μs

* Pulsed: Pulse duration = 300 μs , duty cycle = 1.5%



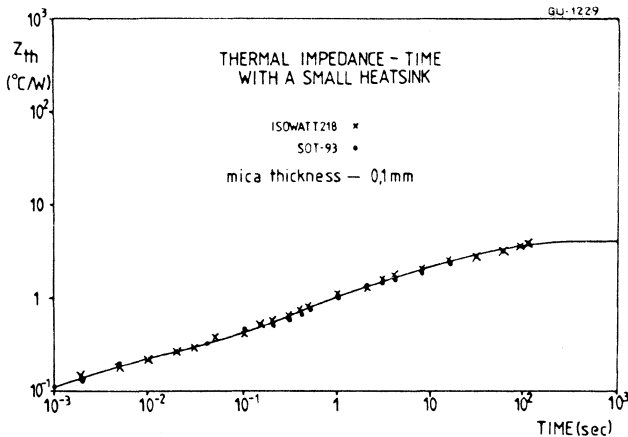
SGSD310
SGSD311
SGSID311

THERMAL RESISTANCE OF THE ISOWATT218

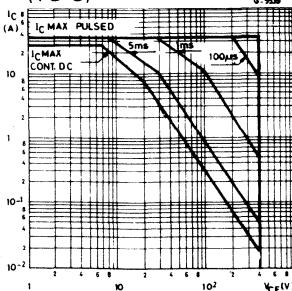
The junction to case thermal resistance of 2.5 °C/W for the ISOWATT218 package may seem quite high at first glance but if compared to a conventional SOT-93 (TO-218) package with a 0.1 mm mica insulating washer, the differences are marginal. The 0.1 mm isolating washer gives 1500V to 2000V DC isolation for the SOT-93 package, SGS guarantee 4000V DC isolation for the ISOWATT218.

The comparison in fig. 1 shows the dynamic thermal resistance of both devices mounted using a thermal compound. The test illustrates that the ISOWATT218 has an R_{th} very close to that of conventional SOT-93 (TO-218) and any small increase is more than compensated for by the convenience of the ISOWATT218 package. The collector to heatsink capacitance of the ISOWATT218 is typically 17pF.

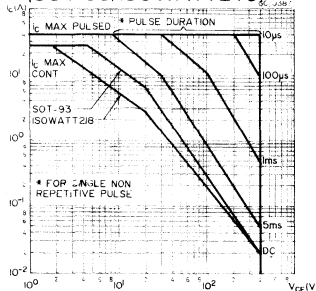
Fig. 1



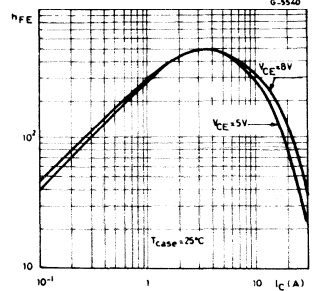
Safe operating area (TO-3)



Safe operating area (SOT-93/ISOWATT218)



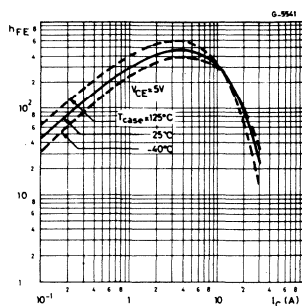
DC current gain



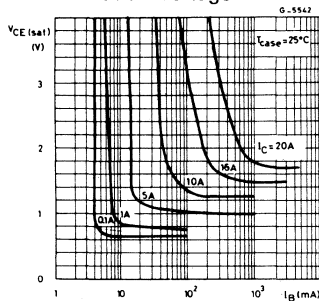


SGSD310
SGSD311
SGSID311

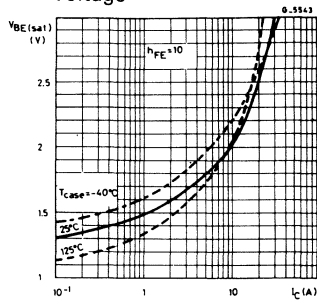
DC current gain



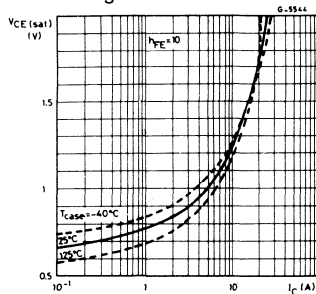
Collector-emitter saturation voltage



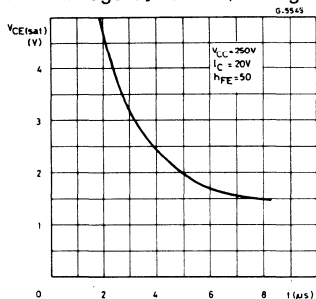
Base-emitter saturation voltage



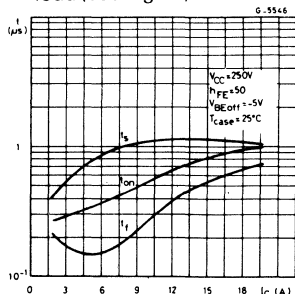
Collector emitter saturation voltage



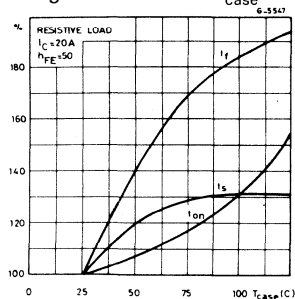
Collector-emitter saturation voltage dynamic (see fig. 2)



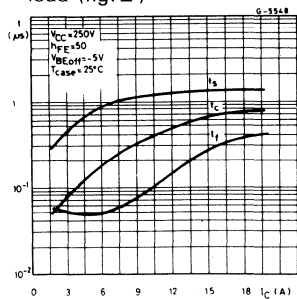
Switching times resistive load (see fig. 2)



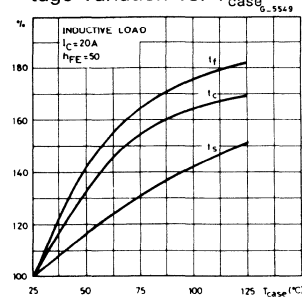
Switching times percentage variation vs. Tcase



Switching times inductive load (fig. 2)



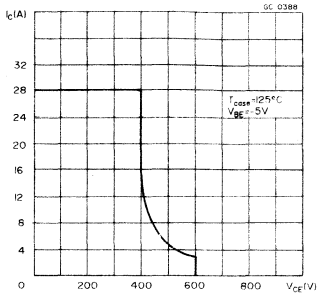
Switching times percentage variation vs. Tcase





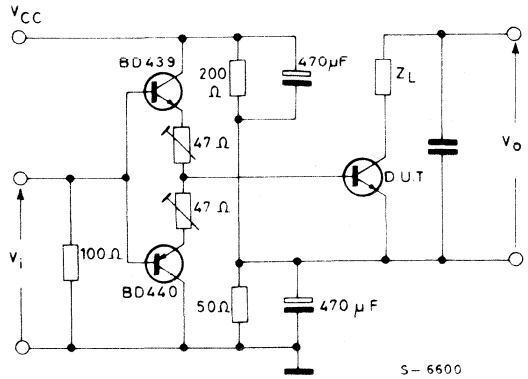
SGSD310
SGSD311
SGSID311

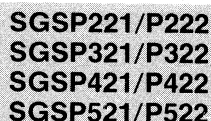
Clamped reverse bias safe operating areas



TEST CIRCUIT

Fig. 2





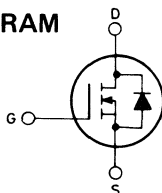
These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

V_{DSS}	R_{DS(ON)}	I_D
50V/60V	0.13Ω	10A

SOT-82
TO-220
SOT-93
TO-3

ABSOLUTE MAXIMUM RATINGS		SOT-82 TO-220 SOT-93 TO-3	SGSP221 SGSP321 SGSP421 SGSP521	SGSP222 SGSP322 SGSP422 SGSP522
V _{DS}	Drain-source voltage (V _{GS} = 0)		60V	50V
V _{DGR}	Drain gate voltage (R _{GS} = 20KΩ)		60V	50V
V _{GS}	Gate-source voltage			± 20V
I _D	Drain current (continuous) at T _{case} = 25°C			10A
	at T _{case} = 100°C			6.5A
I _{DM} (●)	Drain current (pulsed)			40A
I _{DLM} (●)	Drain inductive current, clamped			40A
P _{tot}	Total power dissipation at T _{case} ≤ 25°C	SOT-82	TO-220/SOT93/TO-3	
	Derating factor	50W	75W	
		0.4W/°C	0.6W/°C	
T _{stg}	Storage temperature		-55 to 150°C	
T _j	Junction temperature		150°C	

INTERNAL SCHEMATIC DIAGRAM



Dimensions in mm





SGSP221/P222
SGSP321/P322
SGSP421/P422
SGSP521/P522

THERMAL DATA

		TO220/SOT-93/TO-3	SOT-82
$R_{th\ j-case}$	Thermal resistance junction-case	max	1.67°C/W
T_L	Max. lead temp. for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ $V_{GS} = 0$ for SGSP221/321/421/521 for SGSP222/322/422/522	60 50		V V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max. Rating}$		250	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$		100	nA

ON *

$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu\text{A}$	2		4	V
$V_{DS(on)}$	Drain-source voltage	$V_{GS} = 10\text{V}$ $I_D = 5\text{A}$ $I_D = 10\text{A}$ ($T_{case} = 100^\circ\text{C}$) $I_D = 5\text{A}$			0.65 1.4 1.3	V V V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$ $I_D = 5\text{A}$			0.13	Ω
g_{fs}	Forward transconductance	$V_{DS} = 25\text{V}$ $I_D = 5\text{A}$	3			mho

DYNAMIC

C_{iss}	Input capacitance	$V_{DS} = 25\text{V}$ $f = 1\text{MHz}$	460	550	pF
C_{oss}	Output capacitance			350	pF
C_{rss}	Reverse transfer capacitance			180	pF



SGSP221/P222
SGSP321/P322
SGSP421/P422
SGSP521/P522

ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
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SWITCHING

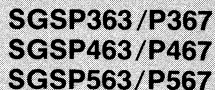
$t_{d(on)}$	Turn-on delay time	$V_{cc} = 25V$ $I_D = 5A$ (see test circuit)	$V_i = 10V$ $R_i = 50 \Omega$	30	ns
t_r	Rise time			130	ns
$t_{d(off)}$	Turn-off delay time			80	ns
t_f	Fall time			130	ns

SOURCE DRAIN DIODE

I_{SD}	Source-drain current			10	A
$I_{SDM} (\bullet)$	Source-drain current (pulsed)			40	A
V_{SD}	Forward on voltage	$I_{SD} = 10A$	$V_{GS} = 0$	1.4	V
t_{on}	Turn-on time	$di/dt = 25A/\mu s$ $I_{SD} = 10A$	$V_{GS} = 0$	60	ns
t_{rr}	Reverse recovery time			100	ns

* Pulsed: pulse duration $\leq 300 \mu s$, duty cycle $\leq 2\%$

($\bullet$) Pulse width limited by safe operating area



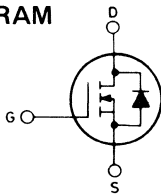
These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

V_{DSS}	R_{DS(ON)}	I_D
200V	0.33Ω	10A
250V	0.45Ω	10A

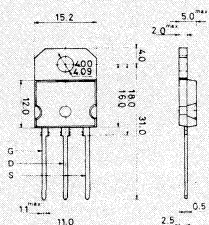
TO-220
SOT-93
TO-3

ABSOLUTE MAXIMUM RATINGS		TO-220 SOT-93 TO-3	SGSP363 SGSP463 SGSP563	SGSP367 SGSP467 SGSP567
V_{DS}	Drain-source voltage ($V_{GS} = 0$)		250V	200V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)		250V	200V
V_{GS}	Gate-source voltage			$\pm 20V$
I_D	Drain current (continuous) $T_{case} = 25^\circ C$ $T_{case} = 100^\circ C$			10A 6.4A
$I_{DM}(\bullet)$	Drain current (pulsed)			40A
$I_{DLM}(\bullet)$	Drain inductive current, clamped			40A
P_{tot}	Total power dissipation $T_{case} = 25^\circ C$		TO-220 100W	SOT-93/TO-3 125W 125W
	Derating factor		0.8W/ $^\circ C$	1W/ $^\circ C$ 1W/ $^\circ C$
T_{stg}	Storage temperature			- 55 to 150 $^\circ C$
T_j	Junction temperature			150 $^\circ C$

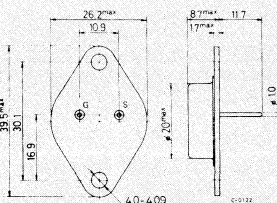
INTERNAL SCHEMATIC DIAGRAM



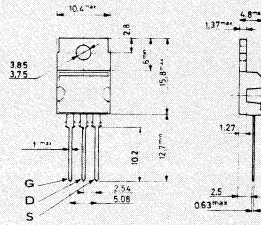
Dimensions in mm



Drain connected to case



TO-3



TO-220



SGSP363/P367
SGSP463/P467
SGSP563/P567

THERMAL DATA

		TO-220	SOT-93	TO-3
$R_{th \text{ j-case}}$	Thermal resistance junction-case	max	1.25°C/W	1°C/W
T_L	Maximum lead temperature for soldering purpose		275°C	1°C/W

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR) DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ $V_{GS} = 0$ for SGSP363/463/563 for SGSP367/467/567	250 200		V V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max. Rating}$		250	μA
I_{GSS}	Gate-body leakage current ($V_{GS} = 0$)	$V_{GS} = \pm 20\text{V}$		100	nA

ON *

$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 250 \mu\text{A}$	2		4	V
$V_{DS(on)}$	Drain-source voltage	$V_{GS} = 10\text{V}$ $I_D = 5\text{A}$ for SGSP363/463/563 for SGSP367/467/567 $V_{GS} = 10\text{V}$ $I_D = 10\text{A}$ for SGSP363/463/563 for SGSP367/467/567 $T_{case} = 100^\circ\text{C}$ $I_D = 5\text{A}$ for SGSP363/463/563 for SGSP367/467/567			2.25 1.65 4.75 3.50 4.5 3.3	V V V V V V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$ $I_D = 5\text{A}$ for SGSP363/463/563 for SGSP367/467/567			0.45 0.33	Ω Ω
g_{fs}	Forward transconductance	$V_{DS} = 25\text{V}$ $I_D = 5\text{A}$	3			mho



SGSP363/P367
SGSP463/P467
SGSP563/P567

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
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DYNAMIC

C_{iss}	Input capacitance	$V_{DS} = 25V \quad f = 1MHz$ $V_{GS} = 0$	980	1200	pF
C_{oss}	Output capacitance		200	260	pF
C_{rss}	Reverse transfer Capacitance		80	100	pF

SWITCHING

$t_{d(on)}$	Turn-on delay time	$V_{CC} = 25V \quad V_i = 10V$ $I_D = 5A \quad R_i = 15\Omega$ (see test circuit)	10		ns
t_r	Rise time		25		ns
$t_{d(off)}$	Turn-off delay time		50		ns
t_f	Fall time		32		ns

SOURCE DRAIN DIODE

I_{SD}	Source drain current			10	A
$I_{SDM}(\cdot)$	Source drain current (pulsed)			40	A
V_{SD}	Forward on voltage	$I_{SD} = 10A \quad V_{GS} = 0$		1.3	V
t_{on}	Turn-on time	$I_{SD} = 10A \quad V_{GS} = 0$ $di/dt = 100A/\mu s$	130		ns
t_{rr}	Reverse recovery time		250		ns

* Pulsed: pulse duration $\leq 300\mu s$, duty cycle $\leq 0.2\%$

($\cdot$) Pulse width limited by safe operating area



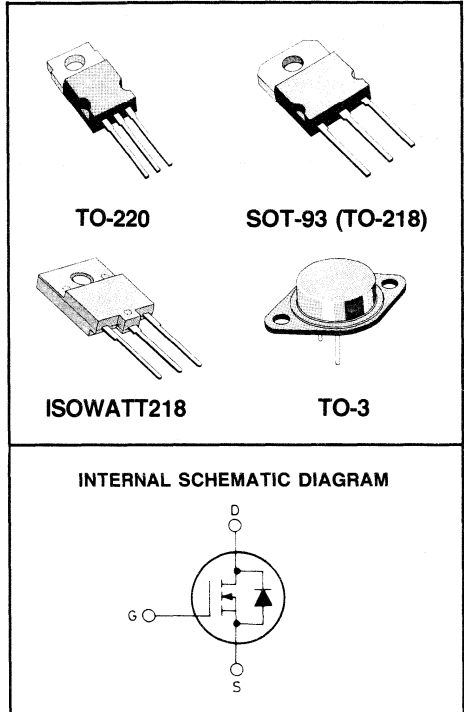
SGSP364/P365/P366
SGSP464/P465/P466
SGSIP464/IP465/IP466
SGSP564/P565/P566

HIGH SPEED SWITCHING APPLICATIONS

V_{DSS}	$R_{DS(on)}$	I_D
350/400 V	1 Ω	6 A
450 V	1.5 Ω	6 A

- HIGH VOLTAGE - FOR ELECTRONIC LAMP BALLAST
 - ULTRA FAST SWITCHING
 - EASY DRIVE - REDUCES COST AND SIZE
- INDUSTRIAL APPLICATIONS:**
- ELECTRONIC LAMP BALLAST
 - DC SWITCH

N-Channel enhancement mode POWERMOS field effect transistors. Easy drive and very fast switching times make these POWERMOS transistors ideal for high speed switching applications. Applications include DC switch, constant current source, ultrasonic equipment and electronic ballast for fluorescent lamps. The package range for this device includes the isolated case ISOWATT218. This provides isolation to 2500V ac, 4000V dc and the creepage distance requirement of VDE, IEC and UL specifications.



ABSOLUTE MAXIMUM RATINGS

TO-220
SOT-93
ISOWATT218
TO-3

SGSP364	SGSP365	SGSP366
SGSP464	SGSP465	SGSP466
SGSIP464	SGSIP465	SGSIP466
SGSP564	SGSP565	SGSP566

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	450	400	350	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)	450	400	350	V
V_{GS}	Gate-source voltage		± 20		V
I_D	Drain current (continuous) $T_c = 25^\circ C$ at $T_c = 100^\circ C$		6 4		A A
$I_{DM}(\bullet)$	Drain current (pulsed)		24		A
I_{DLM}	Drain inductive current, clamped		24		A
V_{ISO}	Isolation voltage (DC)			4000	V
P_{tot}	Total dissipation at $T_{case} = 25^\circ C$ Derating factor	100 0.8	125 1	50 0.4	125 W 1 W/ $^\circ C$
T_{stg}	Storage temperature		-55 to 150		$^\circ C$
T_j	Max. operating junction temperature		150		$^\circ C$

($\bullet$) Pulse width limited by safe operating area.



SGSP364/P365/P366
SGSP464/P465/P466
SGSIP464/P465/IP466
SGSP564/P565/P566

THERMAL DATA

		TO-220	SOT-93	ISOWATT218	TO-3
$R_{th \text{ j-case}}$	Thermal resistance junction-case max	1.25	1	2.5*	1° °C/W
T_L	Maximum lead temperature for soldering purpose			275	°C

* See notes on ISOWATT218 in this datasheet.

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR) DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ $V_{GS} = 0$ for SGSP364/P464/IP464/P564 for SGSP365/P465/IP465/P565 for SGSP366/P466/IP466/P566	450 400 350			V V V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$			250	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			100	nA

ON*

$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 250 \mu\text{A}$	2		4	V
$V_{DS(on)}$	Drain-source voltage	$V_{GS} = 10\text{V}$ $I_D = 3\text{A}$ for SGSP364/P464/IP464/P564 for SGSP365/P465/IP465/P565 for SGSP366/P466/IP466/P566 $V_{GS} = 10\text{V}$ $I_D = 6\text{A}$ for SGSP364/P464/IP464/P564 for SGSP365/P465/IP465/P565 for SGSP366/P466/IP466/P566 $V_{GS} = 10\text{V}$ $I_D = 3\text{A}$ $T_c = 100^{\circ}\text{C}$ for SGSP364/P464/IP464/P564 for SGSP365/P465/IP465/P565 for SGSP366/P466/IP466/P566			4.5 3 3 10 6.7 6.7 9 6 6	V V V V V V V V V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{V}$ $I_D = 3\text{A}$ for SGSP364/P464/IP464/P564 for SGSP365/P465/IP465/P565 for SGSP366/P466/IP466/P566			1.5 1 1	Ω Ω Ω



SGSP364/P365/P366
SGSP464/P465/P466
SGSIP464/P465/IP466
SGSP564/P565/P566

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit.
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DYNAMIC

g_{fs}	Forward transconductance	$V_{DS} = 25V$ $I_D = 3A$	3			mho
C_{iss}	Input capacitance	$V_{DS} = 25V$ $f = 1\text{ MHz}$ $V_{GS} = 0$	780	1000		pF
C_{oss}	Output capacitance		150	200		pF
C_{rss}	Reverse transfer capacitance		100	130		pF
C_{D-HS}	Drain-Heatsink capacitance	$V_{D-HS} = 25V$ $f = 1\text{ MHz}$		19	23	pF

SWITCHING

$t_{d(on)}$	Turn-on time	$V_{CC} = 250V$ $I_D = 3A$ $V_i = 10V$ $R_i = 10\Omega$ (see test circuit)	30			ns
t_r	Rise time		30			ns
$t_{d(off)}$	Turn off delay time		100			ns
t_f	Fall time		50			ns

SOURCE DRAIN DIODE

I_{SD}	Source-Drain current				6	A
$I_{SDM} (*)$	Source-Drain current (pulsed)				24	A
V_{SD}	Forward on voltage	$I_{SD} = 6A$ $V_{GS} = 0$			1.2	V
t_{on}	Turn-on time	$I_{SD} = 6A$ $V_{GS} = 0$ $di/dt = 25A/\mu s$	250			ns
t_{rr}	Reverse recovery time		350			ns

* Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

(*) Pulse width limited by safe operating area



SGSP368/369
SGSP468/469
SGSIP468/469
SGSP568/569

HIGH SPEED SWITCHING APPLICATIONS

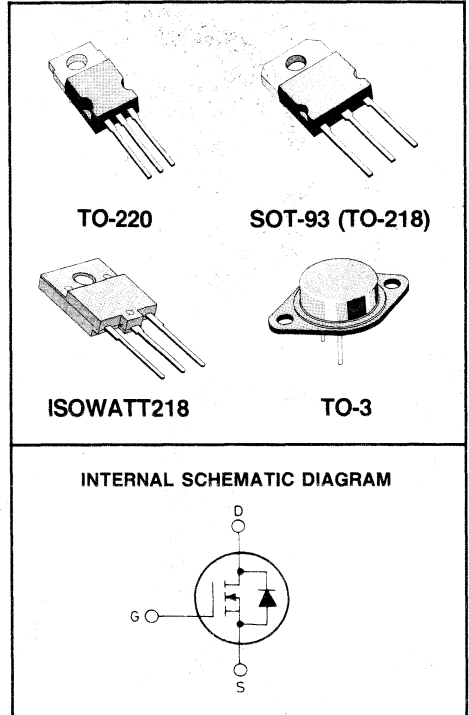
V_{DS}	$R_{DS(on)}$	I_D
500V	1.5 Ω	5A
550V	2.5 Ω	5A

- HIGH VOLTAGE - FOR ELECTRONIC LAMP BALLAST AND SMPS
 - ULTRA FAST SWITCHING - UP TO 200KHz OPERATIONS
 - EASY DRIVE - REDUCES COST AND SIZE
- INDUSTRIAL APPLICATIONS:**
- SMPS
 - ELECTRONIC LAMP BALLAST
 - DC SWITCH

N-Channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications.

Applications include DC switch, constant current source, ultrasonic equipment electronic ripple control and electronic ballast for fluorescent lamps.

The package range for this devices includes the isolated case ISOWATT218. This provides isolation to 2500V ac, 4000V dc and the creepage distance requirement of VDE, IEC, and UL specifications.



ABSOLUTE MAXIMUM RATINGS

	TO-220	SGSP368	SGSP369
	SOT-93	SGSP468	SGSP469
	ISOWATT218	SGSIP468	SGSIP469
	TO-3	SGSP568	SGSP569
V_{DS}		550	500
V_{DGR}		550	500
V_{GS}			± 20
I_D			5
			3.2
$I_{DM}(\bullet)$			20
I_{DLM}			20
			4000
V_{ISO}			
P_{tot}	100	125	50
	0.8	1	0.4
T_{stg}			-55 to 150
T_j			150

(•) Pulse width limited by safe operating area.



SGSP368/369
SGSP468/469
SGSIP468/469
SGSP568/569

THERMAL DATA

			TO-220	SOT-93	ISOWATT218	TO-3
$R_{th \text{ j-case}}$	Thermal resistance junction-case	max	1.25	1	2.5*	1° °C/W
T_L	Maximum lead temperature for soldering purpose				275	°C

* See notes on ISOWATT218 in this datasheet.

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR) DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ $V_{GS} = 0$ for SGSP368/P468/IP468/P568 for SGSP369/0469/IP469/P569	550 500			V V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$			250	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			100	nA

ON*

$V_{GS (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 250 \mu\text{A}$	2		4	V
$V_{DS(on)}$	Drain-source voltage	$V_{GS} = 10\text{V}$ $I_D = 2.5\text{A}$ for SGSP368/P468/IP468/P568 for SGSP369/P469/IP469/P569			6.25 3.75	V V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{V}$ $I_D = 2.5\text{A}$ for SGSP368/P468/IP468/P568 for SGSP369/P469/IP469/P569			2.5 1.5	Ω Ω

DYNAMIC

g_{fs}	Forward transconductance	$V_{DS} = 25\text{V}$ $I_D = 2.5\text{A}$	3			mho
C_{iss}	Input capacitance	$V_{DS} = 25\text{V}$ $f = 1\text{MHz}$ $V_{GS} = 0$		780	1000	pF
C_{oss}	Output capacitance			150	190	pF
C_{rss}	Reverse transfer capacitance			80	100	pF
C_{D-HS}	Drain-Heatsink ¹ capacitance	$V_{D-HS} = 25\text{V}$ $f = 1\text{MHz}$		19	23	pF



SGSP368/369
SGSP468/469
SGSIP468/469
SGSP568/569

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit.
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SWITCHING

$t_{d(on)}$	Turn-on time	$V_{CC} = 250V$ $I_D = 2.5A$ $V_i = 10V$ $R_i = 10\Omega$ (see test circuit)	30		ns
t_r	Rise time		15		ns
$t_{d(off)}$	Turn off delay time		80		ns
t_f	Fall time		40		ns

SOURCE DRAIN DIODE

I_{SD}	Source-Drain current			5	A
$I_{SDM} (*)$	Source-Drain current (pulsed)			20	A
V_{SD}	Forward on voltage	$I_{SD} = 5A$ $V_{GS} = 0$		1.15	V
t_{on}	Turn-on time	$I_{SD} = 5A$ $V_{GS} = 0$ $di/dt = 150A/\mu s$	85		ns
t_{rr}	Reverse recovery time		320		ns

* Pulsed: Pulse duration = 300/ μs , duty cycle 1.5%

(*) Pulse width limited by safe operating area



SGSP386/SGSP387
SGSP486/SGSP487
SGSP586/SGSP587

PRELIMINARY DATA

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

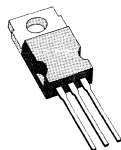
These products are diffused multi-cells silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

V_{DS}	$R_{DS(on)}$	I_D
60V	0.04 Ω	40A
50V	0.04 Ω	40A

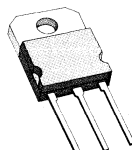
- HIGH CURRENT
- VERY LOW THERMAL RESISTANCE
- VERY LOW ON-LOSSES
- EASY DRIVE

AUTOMOTIVE APPLICATIONS

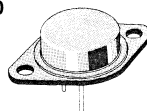
- POWER ACTUATORS



TO-220

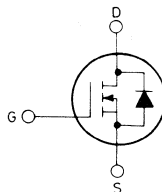


SOT-93



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	TO-220 SOT-93 TO-3	SGSP386 SGSP486 SGSP586	SGSP387 SGSP487 SGSP587	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	60	50	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)	60	50	V
V_{GS}	Gate-source voltage		± 20	V
I_D	Drain current (continuous) $T_{case} = 25^\circ C$		40	A
	at $T_{case} = 100^\circ C$		25	A
$I_{DM}(\bullet)$	Drain current (pulsed)		120	A
I_{DLM}	Drain inductive current, clamped		120	A
P_{tot}	Total dissipation at $T_{case} = 25^\circ C$		125	W
	Derating factor		1	$W/^\circ C$
T_{stg}	Storage temperature		-55 to 150	$^\circ C$
T_j	Max. operating junction temperature		150	$^\circ C$

• Pulse width limited by safe operating area



SGSP386/SGSP387
SGSP486/SGSP487
SGSP586/SGSP587

THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max.	1 °C/W
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ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR)\ DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu A$ $V_{GS} = 0$ for SGSP386/P486/P586 for SGSP387/P487/P587	60 50			V V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $T_{case} = 25^{\circ}C$ $T_{case} = 125^{\circ}C$			250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			100	nA

ON*

$V_{GS\ (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu A$	2		4	V
$R_{DS\ (on)}$	Static drain-source on-resistance	$V_{GS} = 10V$ $I_D = 15A$ $V_{GS} = 10V$ $I_D = 15A$ $T_{case} = 100^{\circ}C$		0.03	0.04 0.08	Ω Ω
g_{fs}	Forward transconductance	$I_D = 15A$ $V_{GS} = 25V$	6			mho

DYNAMIC

C_{iss}	Input capacitance	$V_{DS} = 25V$ $f = 1\ MHz$		1640	1900	pF
C_{oss}	Output capacitance	$V_{GS} = 0$		950	1200	pF
C_{rss}	Reverse transfer capacitance			450	600	pF



SGSP386/SGSP387
SGSP486/SGSP487
SGSP586/SGSP587

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit.
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SWITCHING

$t_{d(on)}$	Turn-on delay time	$V_{CC} = 30V$ $I_D = 15A$ $V_{GS} = 10V$ $R_{GS} = 50 \Omega$ (see test circuit)	40		ns
t_r	Rise time		150		ns
$t_{d(off)}$	Turn-off delay time		150		ns
t_f	Fall time		180		ns

SOURCE DRAIN DIODE

I_{SD}	Source-Drain current			40	A
$I_{SDM} (\bullet)$	Source-Drain current (pulsed)			120	A
V_{SD}	Forward on voltage	$V_{GS} = 0$ $I_{SD} = 40A$		1.8	V
t_{rr}	Reverse recovery time	$I_{SD} = 40A$ $di/dt = 100 A/\mu s$	80		ns
Q_{rr}	Reverse recovered charge		0.2		μC

* Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

($\bullet$) Pulse width limited by safe operating area.



SGSP473/P477
SGSIP473/IP477
SGSP573/P577

HIGH SPEED SWITCHING APPLICATIONS

V_{DS}	$R_{DS(on)}$	I_D
200 V	0.17 Ω	20 A
250 V	0.22 Ω	20 A

- 200-250V - FOR TELECOMS APPLICATIONS
- HIGH CURRENT - FOR PULSED LASER DRIVES
- ULTRA FAST SWITCHING
- EASY DRIVE - REDUCES COST AND SIZE

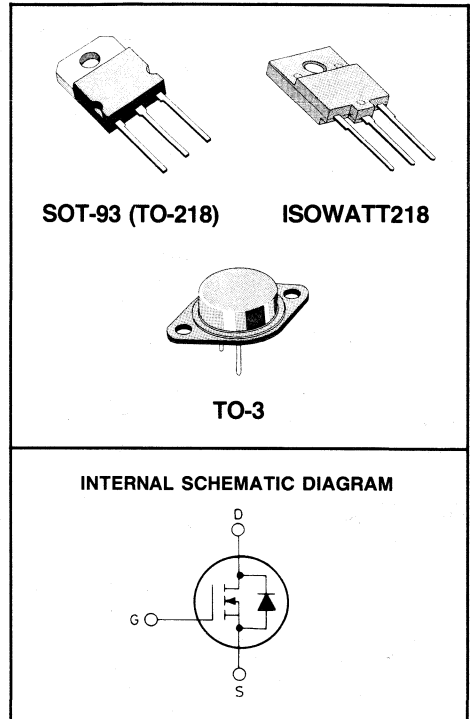
INDUSTRIAL APPLICATIONS:

- SWITCHING MODE POWER SUPPLY
- MOTOR CONTROL FOR ROBOTICS

N-Channel enhancement mode POWERMOS field effect transistors. Easy drive and fast switching times make these POWERMOS transistors ideal for high speed switching applications.

Typical applications include electronics, laser diode drivers, UPS, SMPS, DC/DC, DC switch for telecoms and electronic vehicle drivers.

The package range for this device includes the isolated case ISOWATT218. This provides isolation to 2500V ac, 4000V dc and the creepage requirements of VDE, IEC and UL specifications.



ABSOLUTE MAXIMUM RATINGS

	SOT-93 ISOWATT218 TO-3	SGSP473 SGSIP473 SGSP573	SGSP477 SGSIP477 SGSP577	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	250	200	$\checkmark$
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)	250	200	V
V_{GS}	Gate-source voltage	± 20		V
I_D	Drain current (continuous) $T_c = 25^\circ C$	20	20	A
	at $T_c = 100^\circ C$	13	13	A
$I_{DM}^{(*)}$	Drain current (pulsed)	80	80	A
I_{DLM}	Drain inductive current, clamped	80	80	A
V_{ISO}	Isolation voltage (DC)	4000		V
P_{tot}	Total dissipation at $T_{case} = 25^\circ C$	150	50	150
	Derating factor	1.2	0.4	1.2
T_{stg}	Storage temperature	-55 to 150		$^\circ C$
T_j	Max. operating junction temperature	150		$^\circ C$

(*) Pulse width limited by safe operating area.



SGSP473/P477
SGSIP473/IP477
SGSP573/P577

THERMAL DATA

			SOT-93	ISOWATT218	TO-3
$R_{th\ j-case}$	Thermal resistance junction-case	max	0.84	2.5•	0.84 °C/W
T_L	Maximum lead temperature for soldering purpose			275	°C

• See notes on ISOWATT218 in this datasheet.

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR)\ DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu A$ $V_{GS} = 0$ for SGSP473/IP4743/P573 for SGSP477/IP477/P577	250 200		V V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$		250	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$		100	nA

ON*

$V_{GS\ (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu A$	2		4	V
$V_{DS(on)}$	Drain-source voltage	$V_{GS} = 10V$ $I_D = 10A$ for SGSP473/IP473/P573 for SGSP477/IP477/P577 $V_{GS} = 10V$ $I_D = 20A$ for SGSP473/IP473/P573 for SGSP477/IP477/P577 $V_{GS} = 10V$ $I_D = 10A$ $T_c = 100^{\circ}C$ for SGSP473/IP473/P573 for SGSP477/IP477/P577			2.2 1.7 4.7 3.6 4.4 3.4	V V V V V V
$R_{DS\ (on)}$	Static drain-source on-resistance	$V_{GS} = 10V$ $I_D = 10A$ for SGSP473/IP473/P573 for SGSP477/IP477/P577			0.22 0.17	Ω Ω

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit.
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DYNAMIC

g_{fs}	Forward transconductance	$V_{DS} = 25V$ $I_D = 10A$	8			mho
C_{iss}	Input capacitance	$V_{DS} = 25V$ $f = 1\text{ MHz}$ $V_{GS} = 0$		1900	2200	pF
C_{oss}	Output capacitance			450	550	pF
C_{rss}	Reverse transfer capacitance			200	260	pF
C_{D-HS}	Drain-Heatsink capacitance	$V_{D-HS} = 25V$ $f = 1\text{ MHz}$		19	23	pF

SWITCHING

$t_{d(on)}$	Turn-on time	$V_{CC} = 75V$ $I_D = 10A$ $V_i = 10V$ $R_i = 10\Omega$ (see test circuit)		30		ns
t_r	Rise time			25		ns
$t_{d(off)}$	Turn off delay time			90		ns
t_f	Fall time			20		ns

SOURCE DRAIN DIODE

I_{SD}	Source-Drain current			20	A
$I_{SDM} (\bullet)$	Source-Drain current (pulsed)				
				80	A
V_{SD}	Forward on voltage	$I_{SD} = 20A$ $V_{GS} = 0$			1.3 V
t_{on}	Turn-on time	$I_{SD} = 18A$ $V_{GS} = 0$ $di/dt = 100A/\mu s$		300	ns
t_{rr}	Reverse recovery time			300	ns

* Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

($\bullet$) Pulse width limited by safe operating area



SGSP474/P475/476
SGSIP474/IP475/IP476
SGSP574/P575/P576

HIGH SPEED SWITCHING APPLICATIONS

V_{DS}	$R_{DS(on)}$	I_D
350/400 V	0.55 Ω	12 A
450 V	0.7 Ω	12 A

- HIGH VOLTAGE - FOR OFF-LINE SMPS
- HIGH CURRENT - FOR UP TO 350W
- ULTRA FAST SWITCHING - FOR OPERATION AT $\geq 100\text{KHz}$

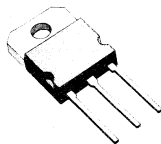
- EASY DRIVE - REDUCES SIZE AND COST

INDUSTRIAL APPLICATIONS:

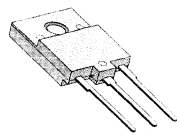
- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS

N-Channel enhancement mode POWERMOS field effect transistors. Fast switching and easy drive make these POWERMOS transistors ideal for high voltage switching applications.

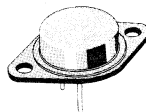
These applications include electronic welders, switched mode power supplies and sonar equipment. The package range for this devices includes the isolated case ISOWATT218. This provides isolation to 2500V ac, 4000V dc and the creepeage distance requirement of VDE, IEC and UL specifications.



SOT-93 (TO-218)

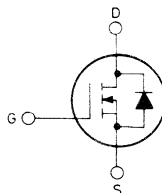


ISOWATT218



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		SOT-93	ISOWATT218	TO-3	SGSP474	SGSP475	SGSP476	
					SGSIP474	SGSIP475	SGSIP476	
					SGSP574	SGSP575	SGSP576	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)				450	400	350	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20\text{K}\Omega$)				450	400	350	V
V_{GS}	Gate-source voltage					± 20		V
I_D	Drain current (continuous) $T_c = 25^\circ\text{C}$					12		A
	at $T_c = 100^\circ\text{C}$					7.6		A
$I_{DM}^{(*)}$	Drain current (pulsed)					48		A
I_{DLM}	Drain inductive current, clamped					48		A
V_{ISO}	Isolation voltage (DC)					4000		V
P_{tot}	Total dissipation at $T_{case} = 25^\circ\text{C}$				150	50	150	W
	Derating factor				1.2	0.4	1.2	W/ $^\circ\text{C}$
T_{stg}	Storage temperature					-55 to 150		$^\circ\text{C}$
T_j	Max. operating junction temperature					150		$^\circ\text{C}$

(*) Pulse width limited by safe operating area.



THERMAL DATA			SOT-93	ISOWATT218	TO-3
$R_{th\ j-case}$	Thermal resistance junction-case	max	0.83	2.5•	0.83 °C/W
T_L	Maximum lead temperature for soldering purpose			275	°C

• See notes on ISOWATT218 in this datasheet.

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$ Drain-source breakdown voltage	$I_D = 250\ \mu A$ $V_{GS} = 0$ for SGSP474/IP474/P574 for SGSP475/IP475/P575 for SGSP476/IP476/P576	450 400 350			V V V
I_{DSS} Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$			250	μA
I_{GSS} Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			100	nA

ON*

$V_{GS\ (th)}$ Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu A$	2		4	V
$V_{DS(on)}$ Drain-source voltage	$V_{GS} = 10V$ $I_D = 6A$ for SGSP474/IP474/P574 for SGSP475/IP475/P575 for SGSP476/IP476/P576 $V_{GS} = 10V$ $I_D = 12A$ for SGSP474/IP474/P574 for SGSP475/IP475/P575 for SGSP476/IP476/P576 $V_{GS} = 10V$ $I_D = 6A$ $T_c = 100^{\circ}C$ for SGSP474/IP474/P574 for SGSP475/IP475/P575 for SGSP476/IP476/P576			4.2 3.3 3.3 9.3 7.1 7.1 8.4 6.6 6.6	V V V V V V V V V
$R_{DS\ (on)}$ Static drain-source on-resistance	$V_{GS} = 10V$ $I_D = 6A$ for SGSP474/IP474/P574 for SGSP475/IP475/P575 for SGSP476/IP476/P576			0.70 0.55 0.55	Ω Ω Ω

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit.
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DYNAMIC

g_{fs}	Forward transconductance	$V_{DS} = 25V$ $I_D = 6A$	6			mho
C_{iss}	Input capacitance	$V_{DS} = 25V$ $f = 1$ MHz $V_{GS} = 0$		1600	2100	pF
C_{oss}	Output capacitance			300	390	pF
C_{rss}	Reverse transfer capacitance			200	260	pF
C_{D-HS}	Drain-Heatsink capacitance	$V_{D-HS} = 25V$ $f = 1$ MHz		19	23	pF

SWITCHING

$t_{d(on)}$	Turn-on time	$V_{CC} = 100V$ $I_D = 6A$ $V_i = 10V$ $R_i = 4.7\Omega$ (see test circuit)		20		ns
t_r	Rise time			25		ns
$t_{d(off)}$	Turn off delay time			70		ns
t_f	Fall time			20		ns

SOURCE DRAIN DIODE

I_{SD}	Source-Drain current			12	A
$I_{SDM} (*)$	Source-Drain current (pulsed)			48	A
V_{SD}	Forward on voltage	$I_{SD} = 12A$ $V_{GS} = 0$		1.2	V
t_{on}	Turn-on time	$I_{SD} = 12A$ $V_{GS} = 0$ $di/dt = 25A/\mu s$		700	ns
t_{rr}	Reverse recovery time			800	ns

* Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

(*) Pulse width limited by safe operating area



SGSP478/479
SGSIP478/479
SGSP578/579

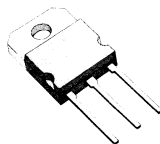
HIGH SPEED SWITCHING APPLICATIONS

V_{DS}	$R_{DS(on)}$	I_D
500V	0.7 Ω	10A
550V	1 Ω	10A

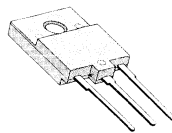
- HIGH VOLTAGE - 500 FOR OFF-LINE SMPS
 - HIGH CURRENT - 10A FOR UP 350W SMPS
 - ULTRA FAST SWITCHING - FOR OPERATION AT $\geq 100\text{KHz}$
 - EASY DRIVE - REDUCES COST AND SIZE
- INDUSTRIAL APPLICATION:**
- SWITCHING MODE POWER SUPPLIES
 - MOTOR CONTROL

N-Channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Typical applications include switched mode power supplies, uninterruptable power supplies and motor speed control.

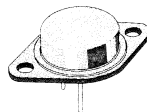
The package range for this devices includes the isolated case ISOWATT218. This provides isolation to 2500V ac, 4000V dc and the creepage distance requirement of VDE, IEC, and UL specifications.



SOT-93 (TO-218)

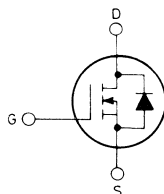


ISOWATT218



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SOT-93
ISOWATT218
TO-3

SGSP478
SGSIP478
SGSP578

SGSP479
SGSIP479
SGSP579

V_{DS}	Drain-source voltage ($V_{GS} = 0$)
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)
V_{GS}	Gate-source voltage
I_D	Drain current (continuous) $T_c = 25^\circ\text{C}$ at $T_c = 100^\circ\text{C}$
$I_{DM}(\bullet)$	Drain current (pulsed)
I_{DLM}	Drain inductive current, clamped
V_{ISO}	Isolation voltage (DC)
P_{tot}	Total dissipation at $T_{case} = 25^\circ\text{C}$ Derating factor
T_{stg}	Storage temperature
T_j	Max. operating junction temperature

550	500	V
550	500	V
± 20		V
10		A
6.3		A
40		A
40		A
SOT-93 ISOWATT218	TO-3	
4000		V
150	50	150 W
1.2	0.4	1.2 W/ $^\circ\text{C}$
	-55 to 150	$^\circ\text{C}$
	150	$^\circ\text{C}$

(*) Pulse width limited by safe operating area.



SGSP478/479
SGSIP478/479
SGSP578/579

THERMAL DATA

			SOT-93	ISOWATT218	TO-3	
$R_{th\ j-case}$	Thermal resistance junction-case	max	0.83	2.5*	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose			275		°C

* See notes on ISOWATT218 in this datasheet.

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR)\ DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu A$ $V_{GS} = 0$ for SGSP478/IP478/P578 for SGSP479/IP479/P579	550 500			V V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$			250	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			100	nA

ON*

$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu A$	2		4	V
$V_{DS(on)}$	Drain-source voltage	$V_{GS} = 10V$ $I_D = 5A$ for SGSP478/IP478/P578 for SGSP479/IP479/P579			5 3.5	V V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10V$ $I_D = 5A$ for SGSP478/IP478/P578 for SGSP479/IP479/P579			1 0.7	Ω Ω

DYNAMIC

g_{fs}	Forward transconductance	$V_{DS} = 25V$ $I_D = 5A$	5			mho
C_{iss}	Input capacitance	$V_{DS} = 25V$ $f = 1\ MHz$ $V_{GS} = 0$		1600	1900	pF
C_{oss}	Output capacitance			230	280	pF
C_{rss}	Reverse transfer capacitance			140	170	pF
C_{D-HS}	Drain-Heatsink capacitance	$V_{D-HS} = 25\ V$ $f = 1\ MHz$		19	23	pF



SGSP478/479
SGSIP478/479
SGSP578/579

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit.
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SWITCHING

t_d (on)	Turn-on time	$V_{CC} = 250V$ $I_D = 5A$ $V_i = 10V$ $R_i = 10\Omega$ (see test circuit)	25		ns
t_r	Rise time		30		ns
$t_{d(off)}$	Turn off delay time		80		ns
t_f	Fall time		20		ns

SOURCE DRAIN DIODE

I_{SD}	Source-Drain current			10	A
I_{SDM} (*)	Source-Drain current (pulsed)			40	A
V_{SD}	Forward on voltage	$I_{SD} = 10A$ $V_{GS} = 0$		1.15	V
t_{on}	Turn-on time	$I_{SD} = 10A$ $V_{GS} = 0$ $di/dt = 100A/\mu s$	75		ns
t_{rr}	Reverse recovery time		500		ns

* Pulsed: Pulse duration = 300/ μs , duty cycle 1.5%

(*) Pulse width limited by safe operating area



2N7056

ADVANCE DATA

HIGH SPEED SWITCHING APPLICATIONS

V_{DS}	$R_{DS(on)}$	I_D
200V	0.100 Ω	19A

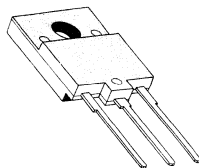
- FULLY ISOLATED PACKAGE
- 200 VOLTS - FOR SMPS UPS AND DC/DC CONVERTERS
- ULTRA FAST SWITCHING
- EASY DRIVE - REDUCES EQUIPMENT SIZE AND COST

INDUSTRIAL APPLICATIONS:

- DC/DC CONVERTERS
- MOTOR CONTROLS
- ROBOTICS

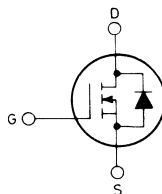
N-Channel enhancement mode POWER MOS field effect transistors. Easy drive, very fast switching times and simple mounting make these POWER MOS transistors ideal for high speed switching applications in a wide range of equipment.

The ISOWATT218 package requires only simple single hole mounting and provides isolation to 2500V ac, 4000V dc. and meets with the creepage distance requirements of VDE, IEC, and UL specifications. The package thermal characteristics are optimised to provide the best isolation with excellent thermal coupling.



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	200	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 1\text{ M}\Omega$)	200	V
I_D	Drain current (continuous) $T_c = 25^\circ\text{C}$	± 19	A
	$T_c = 100^\circ\text{C}$	± 12	A
$I_{DM}(*)$	Drain current (pulsed)	± 120	A
V_{GS}	Gate-source voltage	± 40	V
P_{tot}	Total dissipation at $T_c \leq 25^\circ\text{C}$	70	W
	Total dissipation at $T_c = 100^\circ\text{C}$	28	W
Junction to case - linear derating factor		0.56	W/ $^\circ\text{C}$
Junction to ambient - linear derating factor		0.029	W/ $^\circ\text{C}$
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$
Lead Temperature - 1/16" from case for 10s		300	$^\circ\text{C}$

(*) Pulse width limited by safe operating area.

This is advanced information on a new product in development or undergoing evaluation. Details are subject to change without notice.

**2N7056****THERMAL DATA**

$R_{th\ j-case}$	Thermal resistance junction-case	max.	1.80°C/W
$R_{th\ j-amb}$	Thermal resistance junction-ambient		35°C/W

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR)\ DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ $V_{GS} = 0\text{V}$	200			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$ $T_{case} = 125^{\circ}\text{C}$			250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = +20\text{V}$ (forward) $V_{GS} = -20\text{V}$ (reverse)			100 -100	nA nA

ON*

$V_{GS\ (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 1.0\ \text{mA}$	2		4	V
$V_{DS(on)}$	Drain-source voltage	$V_{GS} = 10\text{V}$ $I_D = 16\text{A}$		1.12	1.60	V
$R_{DS\ (on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{V}$ $I_D = 16\text{A}$ $V_{GS} = 10\text{V}$ $I_D = 9\text{A}$ $T_{case} = 125^{\circ}\text{C}$		0.07 0.12	0.10 0.175	Ω Ω

DYNAMIC

g_{fs}	Forward transconductance	$V_{DS} \geq 2 \times V_{DS(on)}$ $I_D = 16\text{A}$	8.0	12		mho
C_{iss}	Input capacitance	$V_{DS} = 25\text{V}$ $f = 1\ \text{MHz}$ $V_{GS} = 0$		2400	3300	pF
C_{oss}	Output capacitance			600	1200	pF
C_{rss}	Reverse transfer capacitance			250	600	pF
C_{D-HS}	Drain-Heatsink capacitance	$V_{D-HS} = 25\text{V}$ $f = 1\text{MHz}$		19		pF

**2N7056****ELECTRICAL CHARACTERISTICS** (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit.
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SWITCHING

$t_{d(on)}$	Turn-on time	$V_{DD} = 750V$ $I_D = 16A$ $V_{gen} = 10V$ $R_g = 5\Omega$ $R_f = 4.5\Omega$	25	35	ns
t_r	Rise time		60	100	ns
$t_{d(off)}$	Turn off delay time		85	125	ns
t_f	Fall time		38	100	ns

SOURCE DRAIN DIODE

I _{SD}	Source-Drain current	T _c = 100°C			19	A
I _{SDM} (*)	Source-Drain current (pulsed)				12	A
					120	A
V _{SD} *	Forward on voltage	V _{GS} = 0 I _{SD} = 28A		1.6	2.0	V
t _{rr}	Reverse recovery	I _{SD} = 19A di/dt = 100A/μs		150	400	ns

* Pulsed: Pulse duration = 300 μs , duty cycle 2%

(*) Pulse width limited by safe operating area



2N7059

ADVANCE DATA

HIGH SPEED SWITCHING APPLICATIONS

V_{DSS}	$R_{DS(on)}$	I_D
500V	0.45 Ω	8A

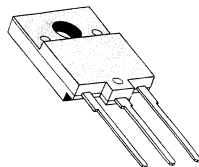
- FULLY ISOLATED PACKAGE
- HIGH VOLTAGE - FOR OFF-LINE SMPS
- HIGH CURRENT - 8A FOR UP TO 1200W SMPS
- ULTRA FAST SWITCHING - FOR OPERATION AT $\geq 100\text{KHz}$
- EASY DRIVE - REDUCES EQUIPMENT SIZE AND COST

INDUSTRIAL APPLICATIONS:

- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS

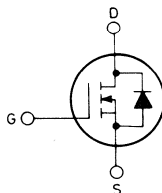
N-Channel enhancement mode POWER MOS field effect transistors. Easy drive, very fast switching times and simple mounting make these POWER MOS transistors ideal for high speed switching applications in a wide range of equipment.

The ISOWATT218 package requires only simple single hole mounting and provides isolation to 2500V ac, 4000V dc. and meets with the creepage distance requirements of VDE, IEC, and UL specifications. The package thermal characteristics are optimised to provide the best isolation with excellent thermal coupling.



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	500	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 1\text{ M}\Omega$)	500	V
I_D	Drain current (continuous) $T_c = 25^\circ\text{C}$	± 8	A
	$T_c = 100^\circ\text{C}$	± 5	A
$I_{DM}(\bullet)$	Drain current (pulsed)	± 52	A
V_{GS}	Gate-source voltage	± 40	V
P_{tot}	Total dissipation at $T_c \leq 25^\circ\text{C}$	70	W
	Total dissipation at $T_c = 100^\circ\text{C}$	28	W
	Junction to case - linear derating factor	0.56	W/ $^\circ\text{C}$
	Junction to ambient - linear derating factor	0.029	W/ $^\circ\text{C}$
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$
	Lead Temperature - 1/16" from case for 10s	300	$^\circ\text{C}$

($\bullet$) Pulse width limited by safe operating area.

This is advanced information on a new product in development or undergoing evaluation. Details are subject to change without notice.

**2N7059****THERMAL DATA**

$R_{th\ j-case}$	Thermal resistance junction-case	max.	1.80°C/W
$R_{th\ j-amb}$	Thermal resistance junction-ambient		35°C/W

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR)\ DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ $V_{GS} = 0\text{V}$	500			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$ $T_{case} = 125^{\circ}\text{C}$			250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = +20\text{V}$ (forward) $V_{GS} = -20\text{V}$ (reverse)			100 -100	nA nA

ON*

$V_{GS\ (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 1.0\ \text{mA}$	2		4	V
$V_{DS(on)}$	Drain-source voltage	$V_{GS} = 10\text{V}$ $I_D = 7\text{A}$		2.66	3.15	V
$R_{DS\ (on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{V}$ $I_D = 7\text{A}$ $V_{GS} = 10\text{V}$ $I_D = 4\text{A}$ $T_{case} = 125^{\circ}\text{C}$		0.38 0.72	0.45 0.86	Ω Ω

DYNAMIC

g_{fs}	Forward transconductance	$V_{DS} \geq 2 \times V_{DS(on)}$ $I_D = 7\text{A}$ $I_D = 16\text{A}$	6.0	7.2		mho
C_{iss}	Input capacitance	$V_{DS} = 25\text{V}$ $f = 1\ \text{MHz}$		2600	3300	pF
C_{oss}	Output capacitance	$V_{GS} = 0$		280	700	pF
C_{rss}	Reverse transfer capacitance			40	300	pF
C_{D-HS}	Drain Heatsink capacitance	$V_{D-HS} = 25\text{V}$ $f = 1\ \text{MHz}$		19		pF

**2N7059****ELECTRICAL CHARACTERISTICS** (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit.
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SWITCHING

$t_{d(on)}$	Turn-on time	$V_{DD} = 210V$ $I_D = 7A$ $V_{gen} = 10V$ $R_g = 5\Omega$ $R_i = 30\Omega$	25	40	ns
t_r	Rise time		25	50	ns
$t_{d(off)}$	Turn off delay time		75	150	ns
t_f	Fall time		31	70	ns

SOURCE DRAIN DIODE

I_{SD}	Source-Drain current	$T_c = 100^{\circ}C$			8	A	
$I_{SDM} (*)$	Source-Drain current (pulsed)				52	A	
V_{SD}^*	Forward on voltage	$V_{GS} = 0$	$I_{SD} = 12A$		1.2	1.5	V
t_{rr}	Reverse recovery	$I_{SD} = 8A$	$di/dt = 100A/\mu s$		400	600	ns

* Pulsed: Pulse duration = $300\mu s$, duty cycle 2%

(*) Pulse width limited by safe operating area

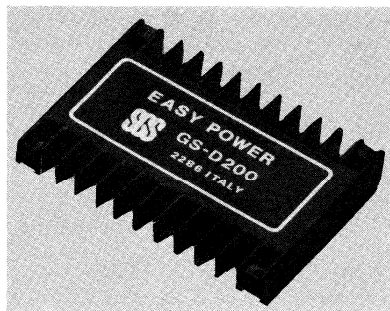
SWITCH MODE BIPOLAR STEPPER MOTOR DRIVER MODULE

The GS-D200 is a complete controller and driver for bipolar stepper motors that directly interfaces a microprocessor and two phase permanent magnet motors.

The motor current is controlled in a chopping mode up to 2 A. High flexibility in use is provided by GS-D200 that, furthermore, reduces the burden on the microprocessor and simplifies the software development in a complete microprocessor controlled stepper motor system.

FEATURES

- No external component required
- Normal, wave, half step drive capability
- Inputs TTL/CMOS compatible
- Chopper regulation of motor current
- Programmable motor current (2 A max)
- Wide voltage range (10-46 V)
- Selectable slow/fast current decay
- Synchronization for multiple application
- Remote inhibit/enable
- Home position indicator
- Overtemperature protection



Order Number: GS-D200

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage (pin 18)	48 V
V_{ss}	Supply voltage (pin 12)	7 V
I_o	Peak output current	2 A
T_{stg}	Storage temperature range	- 40 to + 105°C
T_{cop}	Operating case temperature range	- 20 to + 85°C

Recommended maximum operating input voltage is 46 V.

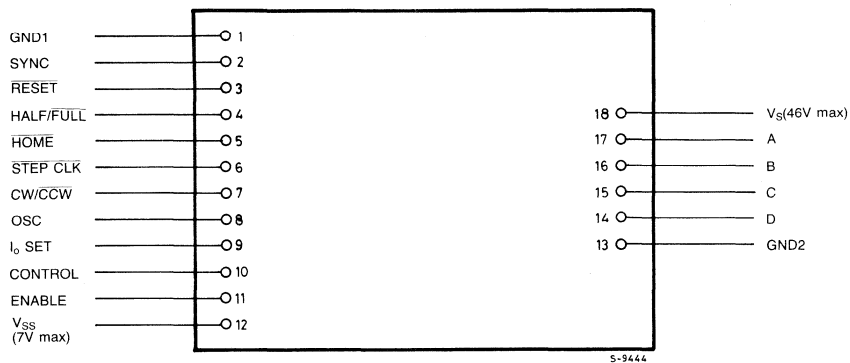
THERMAL DATA

$R_{th (c-a)}$	case-ambient thermal resistance	Max	5.0 °C/W
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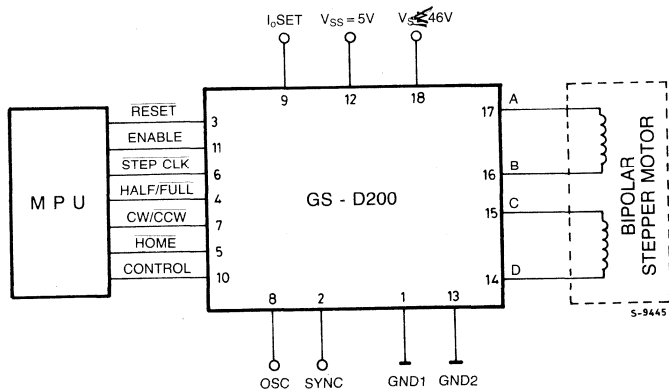


GS-D200

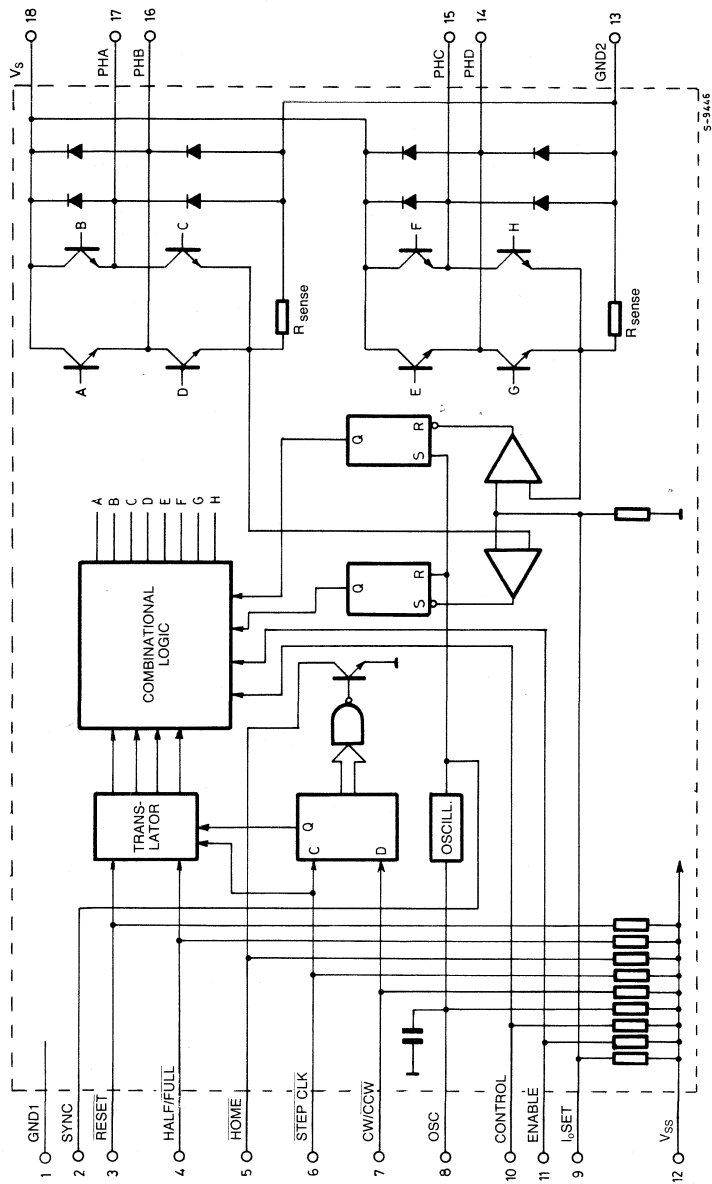
CONNECTION DIAGRAM (top view)



TYPICAL APPLICATION



EQUIVALENT BLOCK DIAGRAM OF GS-D200



**PIN FUNCTIONS**

PIN	FUNCTION
1 – GND1	Common ground for low current path.
2 – SYNC	Output of the module chopper oscillator. Several GS-D200 can be synchronized by connecting together all SYNC pins (see later). An external chopper clock source, if used, must be injected at this pin.
3 – RESET	Reset asynchronous input. An active low pulse on this input restores the module to the HOME position (ABCD=0101).
4 – HALF/FULL	Half/Full step select input. When high or not connected, it selects half step operation, when low it selects full step operation.
5 – HOME	Output that indicates when the module is in its initial state (Active low: ABCD=0101=state 1). This signal should be ANDed with the output of a mechanical home position sensor of the motor.
6 – STEPCLK	A pulse on this input moves the motor by one step. The step occurs on the rising edge of this signal.
7 – CW/CCW	Clockwise/counterclockwise direction control input. When high or not connected clockwise rotation is selected. Physical direction of motor rotation depends also on connection of windings. Direction can be changed at any time being this signal synchronized inside the module.
8 – OSC	The chopper frequency of the module is internally fixed at ~17 KHz. This frequency can be increased by connecting a resistor between this pin and V_{ss} or decreased by connecting a capacitor between this pin and GND1. When multi-GS-D200 configurations must be synchronized, this pin is connected to ground on all but one module.
9 – I_o SET	The motor phase current is set at 1 A. This current can be decreased by connecting a resistor between this pin and GND1, or increased by connecting a 10 K Ω min resistor between this pin and V_{ss} .
10 – CONTROL	Control input that defines the motor current decay inherent to chop mode control. When low, a fast decay is obtained; when high, or not connected, slow current decay is imposed to the motor current.
11 – ENABLE	Module enable input. When low the module is inhibited. When high or not connected the module is active.
12 – V_{ss}	5 V supply input. Maximum voltage must not exceed 7 V.
13 – GND2	Common ground for high current path.

PIN FUNCTIONS (Continued)

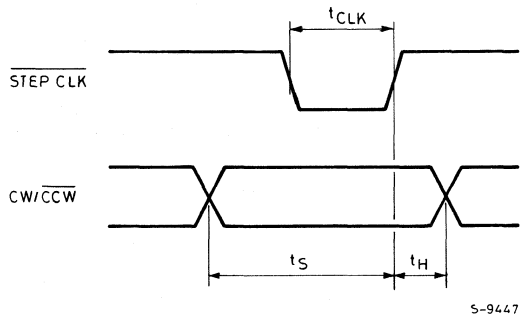
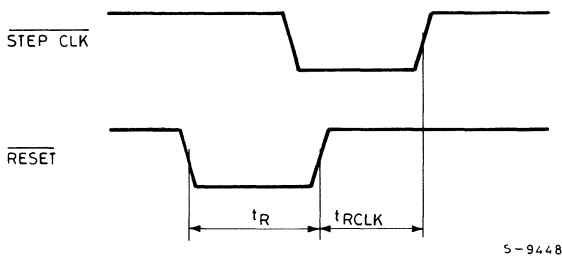
PIN	FUNCTION
14—D	Phase D output
15—C	Phase C output
16—B	Phase B output
17—A	Phase A output
18—V _s	Module supply voltage. Maximum voltage must not exceed 46 V.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter	Test Conditions	Min	Typ	Max	Unit
V _s Supply Voltage	Pin 18	10		46	V
V _{ss} Supply Voltage	Pin 12	4.75	5	5.25	
I _s Quiescent Supply Current	Pin 18 I _{out} = 0 V _s = 42V		15	20	mA
I _{ss} Quiescent Supply Current	Pin 12. All inputs high I _{out} = 0 V _{ss} = 5V		60		mA
V _i Input Voltage	Pin 3, 4, 6, 7, 10 low high	2.0		0.8 V _{ss}	V V
I _i Input Current	Pin 3, 4, 6, 7, 10 V _i = low V _i = high			0.6 10	mA μA
V _{en} Enable Input Voltage	Pin 11 low high	2.0		0.8 V _{ss}	V V
I _{en} Enable Input Current	Pin 11 V _{en} = low V _{en} = high			0.6 10	mA μA
V _{home} Home Output Voltage	Pin 5 I _{home} = 5mA low high			0.4 V _{ss}	V V
V _{sat} Source Saturat. Voltage	Pin 14, 15, 16, 17 I _o = 1A			1.8	V
V _{sat} Sink Saturat. Voltage	Pin 14, 15, 16, 17 I _o = 1A			1.8	V
f _c Chopper Freq.			17		KHz

**ELECTRICAL CHARACTERISTICS** (continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
t_{clk} Stepclk Width	Pin 6 see fig. a	0.5			μS
t_{s} Set up Time	see fig. a	1.0			μS
t_{h} Hold Time	see fig. a	1.0			μS
t_{R} Reset Width	see fig. b	1.0			μS
t_{Rclk} Reset to Clock Set up Time	see fig. b	1.0			μS

**Fig. a****Fig. b**

MODULE OPERATION

The GS-D200 is a complete bipolar stepper motor driver that incorporates all the small signal and power functions to directly interface a microprocessor and a two phase permanent magnet motor (see the typical application). Very few information must be delivered by the microprocessor to the module:

- step clock
- direction (clockwise or counterclockwise)
- mode (half or full step)
- reset and enable
- current decay (slow or fast)

Based on this information, the module generates the proper four phases sequence to directly drive a two phase bipolar motor. Therefore the GS-D200 greatly simplifies the task of the microprocessor and of the system programmer.

No external component is needed to operate the GS-D200. However, to add flexibility in use, some internally set functions can be modified externally, like the maximum current flowing through the motor windings and the switching frequency of the current chopper, by addition of few inexpensive passive components (resistor and capacitor).

If any of logic input is left open, the module forces them to high level.

The GS-D200 is housed in a metal case that provides heatsink and shielding against radiated EMI. The thermal resistance case to ambient is about 5 °C/W. This means that for each watt of internal power dissipation the case temperature is + 5°C above ambient temperature. It is recommended to keep the case temperature below 85°C in operating conditions.

According to ambient temperature and/or to power dissipation, an additional heatsink may be required: the mounting of optional heatsink is made easy by the four holes provided on the top of the metal case.

The GS-D200 incorporates a thermal protection that switches off the power stages when the junction temperature of active components reaches 150 °C.

To keep the power dissipation to a minimum, two level supply voltages must be applied to the module: 5 V for logic functions and V_s from 10 to 46 V for power section.



GS-D200

A - BIPOLAR STEPPER MOTOR BASICS

Simplified to the bare essentials, a bipolar permanent magnet motor consists of a rotating permanent magnet surrounded by stator poles carrying the windings (fig. 1).

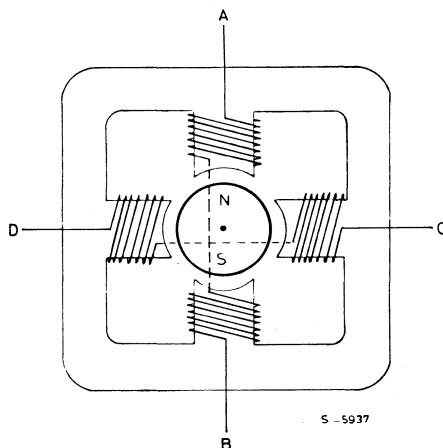


Fig. 1 - Simplified bipolar two phase motor

Bidirectional drive current is imposed on windings A-B and C-D and the motor is stepped by commutating the voltage applied to the windings in sequence.

For a motor of this type there are three possible drive sequences.

A1 - ONE-PHASE-ON or WAVE DRIVE

Only one winding is energized at any given time according to the sequence:

AB - CD - BA - DC

(BA means that the current is flowing from B to A).

Fig. 2 shows the sequence for a clockwise rotation and the corresponding rotor position.

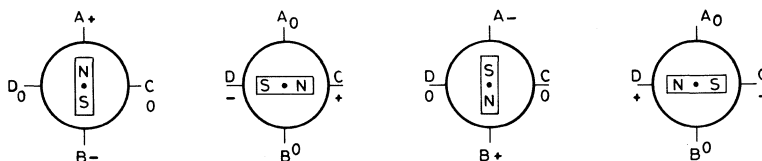


Fig. 2 - One-phase-on (wave mode) drive

S-5952

A2 - TWO-PHASE-ON or NORMAL DRIVE

This mode gives the highest torque since two windings are energized at any given time according to the sequence (for clockwise rotation)

AB & CD; CD & BA; BA & DC; DC & AB

Fig. 3 shows the sequence and the corresponding position of the rotor.

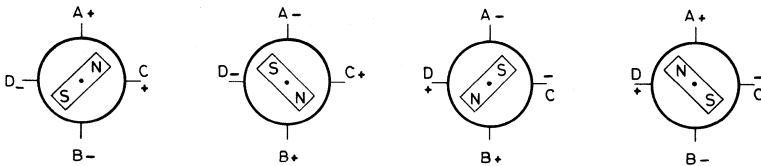


Fig. 3 - Two-phase-on (normal mode) drive

S-5953

A3 - HALF STEP DRIVE

This sequence halves the effective step angle of the motor but gives a less regular torque being one winding or two windings alternatively energized. Eight steps are required for a complete revolution of the rotor.

The sequence is:

AB; AB & CD; CD; CD & BA; BA; BA & DC; DC; DC & AB

as shown in fig. 4.

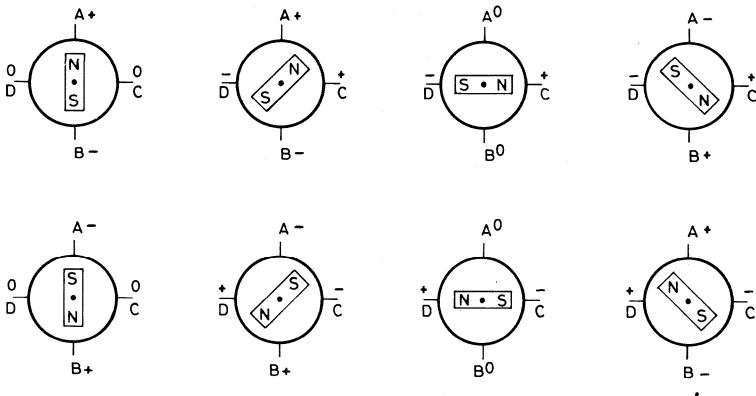


Fig. 4 - Half step sequence.

S-5938

By the configurations of fig. 2,3,4 the motor would have a step angle of 90° (or 45° in half step). Real motors have multiple poles pairs to reduce the step angle to a few degrees but the number of windings (two) and the drive sequence are unchanged.

B - PHASE SEQUENCE GENERATION INSIDE THE GS-D200

The GS-D200 contains a three bit counter plus some combinational logic which generate suitable phase sequences for half step, wave and normal full step drive. This 3 bit counter generates a basic eight-step Gray code master sequence as shown in fig. 5. To select this sequence, that corresponds to half step mode, the HALF/FULL input (pin 4) must be kept high or left open.

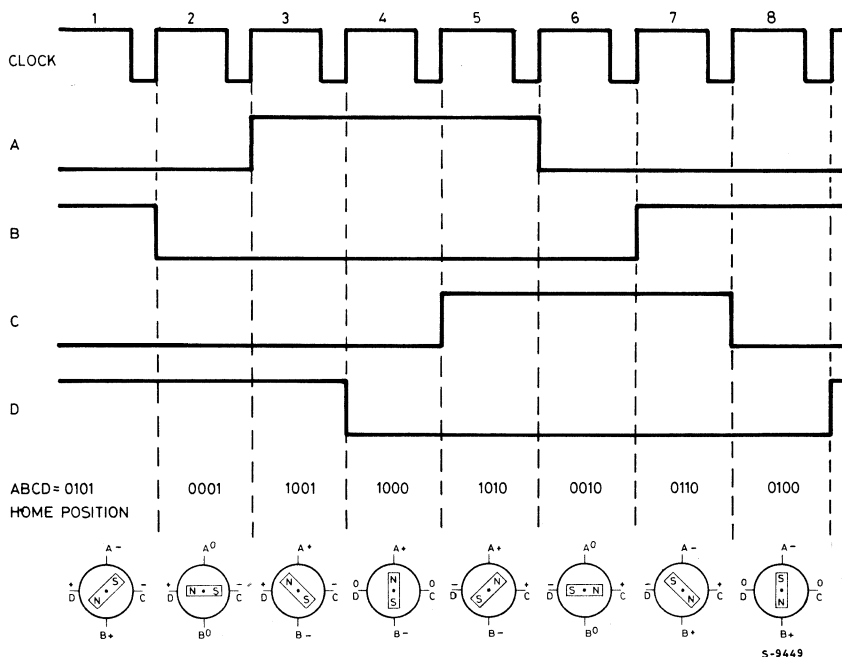


Fig. 5 - The eight step master sequence corresponding to half step mode.

The full step mode (normal and wave drive) are both obtained from the eight step master sequence by skipping alternate states. This is achieved by forcing the step clock to bypass the first stage of the 3 bit counter. The least significant bit of this counter is not affected and therefore the generated sequence depends on the state of the counter when full step mode is selected by forcing pin 4 (HALF/FULL) low. If full step is selected when the counter is at any odd-numbered state, the two-phase-on (normal mode) is implemented (see fig. 6).

On the contrary, if the full mode is selected when the counter is at an even-numbered state, the one-phase-on (wave drive) is implemented (see fig. 7).

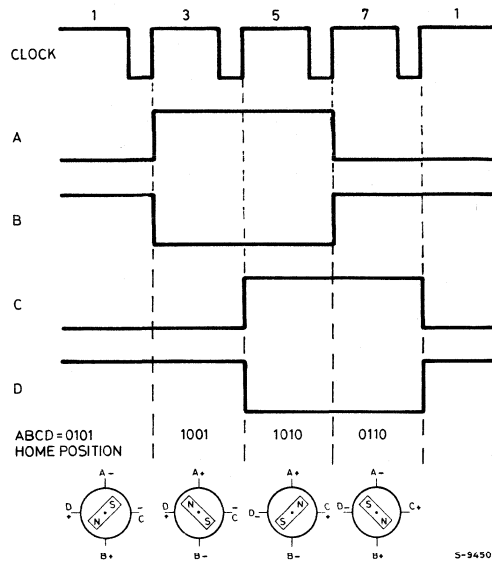


Fig. 6 - Two-phase-on (normal mode) drive

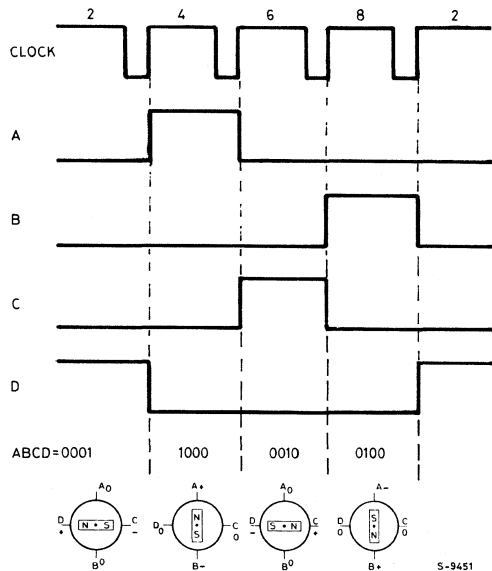


Fig. 7 - One-phase-on (Wave mode) drive.



C - RESET, ENABLE AND HOME SIGNALS

The RESET is an asynchronous reset input which restores the module to the home position (state 1:ABCD = 0101). Reset is active when low.

The HOME output signals this condition and it is intended to be ANDed with the output of a mechanical home position sensor.

The ENABLE input is used to start up the module after the system initialization. ENABLE is active when high or open.

D - MOTOR CURRENT REGULATION

The two bipolar winding currents are controlled by two internal choppers in a PWM mode to obtain good speed and torque characteristics.

An internal oscillator supplies pulses at the chopper frequency to both choppers.

When the outputs are enabled, the current through the windings raises until a peak value set by I_{oSET} and R_{sense} (see the equivalent block diagram) is reached. At this moment the outputs are disabled and the current decays until the next oscillator pulse arrives.

The decay time of the current can be selected by the CONTROL input (pin 10). If the CONTROL input is kept high or open the decay is slow, as shown in fig. 8, where the equivalent power stage of GS-D200, the voltages on A and B are shown as well as the current waveform on winding AB.

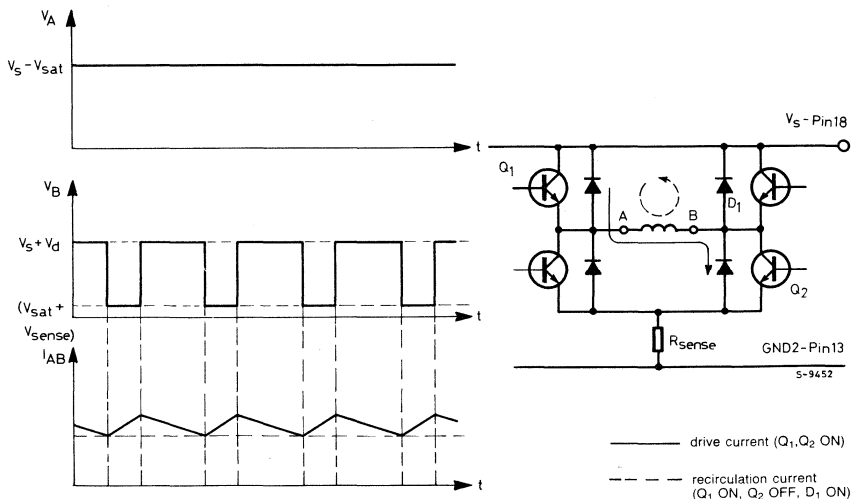


Fig. 8 - Chopper control with slow decay

When the CONTROL input is forced low, the decay is fast as shown in fig. 9.

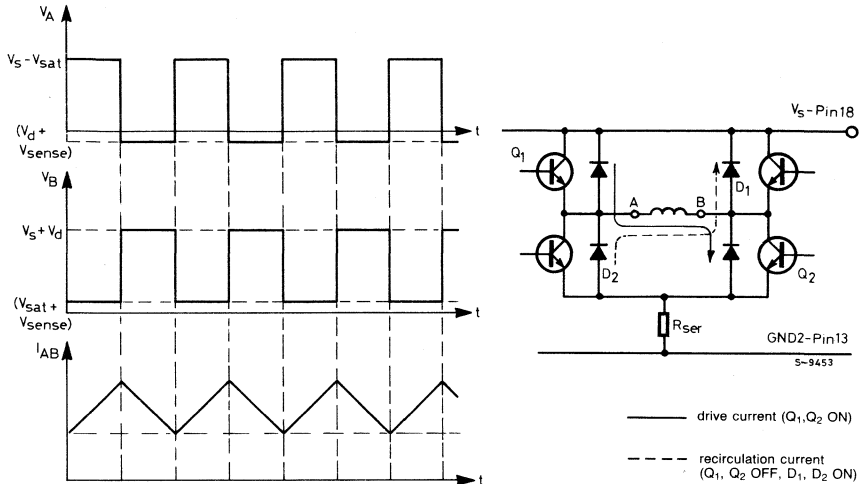


Fig. 9 - Chopper control with fast decay

The CONTROL input is provided on GS-D200 to allow maximum flexibility in application.

If the GS-D200 must drive a large motor that does not store much energy in the windings, the chopper frequency must be decreased: this is easily obtained by connecting an external capacitor between OSC pin and GND1. In these conditions a fast decay (CONTROL LOW) would impose a low average current and the torque could be inadequate. By selecting CONTROL HIGH, the average current is increased thanks to the slow decay.

E - MODULE PROGRAMMING

When no external component is used, the GS-D200 is set at the following conditions:

$$I_{out,peak} \cong 1 \text{ A}$$

$$f_c \text{ chopper frequency} \cong 17 \text{ KHz}$$

By addition of inexpensive passive components the working conditions can be modified as follows.

**E1 - OUTPUT CURRENT PROGRAMMING**

The output peak current (initially set at 1 A) can be re-programmed by addition of an external resistor.

If a lower peak current is desired, a resistor R1 must be connected between I_o SET and GND1 as shown in fig. 10.

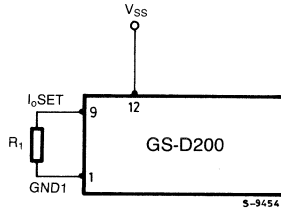


Fig. 10 - Peak current reduction

The value of output current, for V_{ss} = 5 V, is related to the value of R1 by

$$I_{out} = \frac{12}{11.2 + \frac{12}{R1}} \text{ A where } R1 \text{ is in } K\Omega$$

For example, for R1 = 1K Ω $I_{out} \cong 0.5 \text{ A}$.

If a higher peak current is needed, a resistor R2 must be connected between I_o SET and V_{ss} as shown in fig. 11.

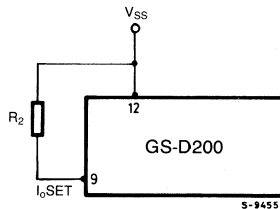


Fig. 11 - Peak current increase

The output current, for V_{ss} = 5 V, is related to the value of R2 by

$$I_{out} = \frac{12 + \frac{10}{R2}}{11.2 + \frac{12}{R2}} \text{ A where } R2 \text{ is in } K\Omega$$

For example, for R2 = 24 K Ω $I_{out} \cong 1.45 \text{ A}$

Minimum Value of R2 is 10 kΩ.

This current programmability can be used in half step sequence to increase the current when only one phase is on: a more regular torque is so obtained.

E2 - CHOPPER FREQUENCY PROGRAMMING

The chopper frequency is internally set at about 17 KHz. This frequency can be changed by addition of external components as follows.

To increase the chopper frequency a resistor R3 must be connected between OSC pin and V_{SS} as shown in fig. 12.

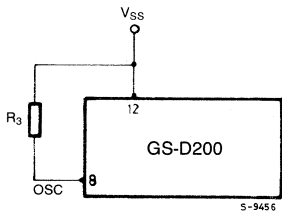


Fig. 12 - Chopper frequency increase

The new chopper frequency is given by:

$$f_c = 17 \left(1 + \frac{18}{R3} \right) \text{ KHz} \quad \text{where } R3 \text{ is in } K\Omega$$

For example, if V_{SS} = 5 V and R3 = 18 KΩ, f_c ≈ 34 KHz

To decrease the chopper frequency a capacitor C must be connected between OSC pin and GND1 as shown in fig. 13.

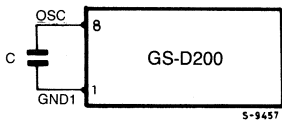


Fig. 13 - Chopper frequency decrease.

The new chopper frequency is given by:

$$f_c = \frac{80.5}{4.7 + C} \text{ KHz} \quad \text{where } C \text{ is in nF}$$

For example, if V_{SS} = 5 V and C = 4.7nF, f_c ≈ 8.5 KHz.



F - MULTI MODULES APPLICATION

In complex systems, many motors must be controlled and driven. In such a case more than one GS-D200 must be used.

To avoid chopper frequencies noise and beats, all the GS-D200 should be synchronized.

If all the motors are relatively small, the fast decay may be used, the chopper frequency does not need any adjustment and fig. 14 shows how to synchronize several modules.

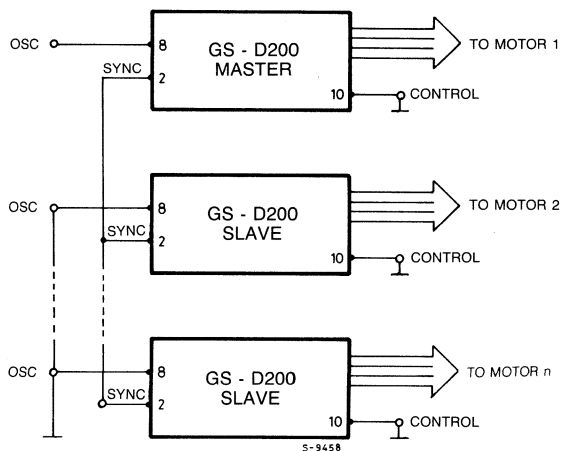


Fig. 14 - Multimotor synchronization. Small motors and fast current decay.

When at least one motor is relatively large a lower chopper frequency and a slow decay may be required. In such a case the overall system chopper frequency is determined by the largest motor in the system as shown in fig. 15.

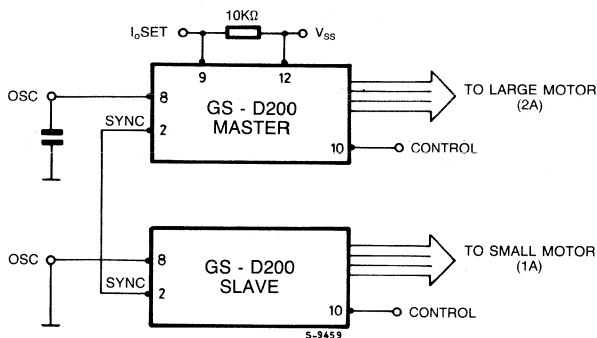


Fig. 15 - Multimotor synchronization. Large and small motors. Slow current decay.

G - THERMAL OPERATING CONDITIONS

In many cases the GS-D200 module does not require any additional cooling because the dimensions and the shape of the metal box are studied to offer the minimum possible thermal resistance case-to-ambient for a given volume.

It should be remembered that the GS-D200 module is a power device and, depending on ambient temperature, an additional heat-sink or forced ventilation or both may be required to keep the unit within safe temperature range. ($T_{\text{case max}} < 85^{\circ}\text{C}$ during operation).

The concept of maximum operating ambient temperature is totally meaningless when dealing with power components because the maximum operating ambient temperature depends on how a power device is used.

What can be unambiguously defined is the case temperature of the GS-D200 module.

To calculate the maximum case temperature of the module in a particular application environment the designer must know the following data:

- Input voltage
- Motor phase current
- Motor phase resistance
- Maximum ambient temperature

From these data it is easy to determine whether an additional heat-sink is required or not, and the relevant size i.e. the thermal resistance.

The step by step calculation is shown for the following example:

$V_{\text{in}} = 40 \text{ V}$, $I_{\text{phase}} = 1 \text{ A}$, Rph Phase resistance = 10Ω , Max. $T_{\text{amb}} = 50^{\circ}\text{C}$

G1. Calculate the power dissipated by the indexer logic and the level shifter (see electrical characteristics):

$$P_{\text{logic}} = (5 \text{ V} \cdot 60 \text{ mA}) + (40 \text{ V} \cdot 20 \text{ mA}) = 1.1 \text{ W}$$

G2. Calculate the average voltage across the winding resistance:

$$V_{out} = R_{ph} \cdot I_{out} = 10 \, \Omega \cdot 1 \, A = 10 \, V$$

G3. Calculate the required ON duty cycle (D.C.) of the output stage to obtain the average voltage (this D.C. is automatically adjusted by the GS-D200):

$$D.C. = \frac{V_{out}}{V_{in}} = \frac{10}{40} = 0.25$$

G4. Calculate the power dissipation of the GS-D200 output power stage. The power dissipation depends on two main factors:

- the selected operating mode (FAST or SLOW DECAY)
- the selected drive sequence (WAVE, NORMAL, HALF STEP)

G4.1 FAST DECAY. For this mode of operation, the internal voltage drop is $V_{sat_{source}} + V_{sat_{sink}}$ during the ON period i.e. for 25% of the time. During the recirculation period (75% of the time), the current recirculates on two internal diodes that have a voltage drop $V_d = 1 \, V$, and the internal sense resistor ($0.5 \, \Omega$). For this example, by assuming maximum values for conservative calculations, the power dissipation during one cycle is:

$$P_{pw} = 1.1 \cdot [2 \, V_{sat} \cdot I_{ph} \cdot DC + 2 \, V_d \cdot I_{ph} \cdot (1-DC) + 0.5 \cdot I_{ph}^2]$$

$$P_{pw} = 1.1 \cdot [2 \cdot 1.8 \cdot 1 \cdot 0.25 + 2 \cdot 1 \cdot 1 \cdot 0.75 + 0.5 \cdot 1]$$

$$P_{pw} = 1.1 \cdot [0.9 + 1.5 + 0.5] = 3.19 \, W$$

The factor 1.1 takes into account the power dissipation during the switching transient.

G4.2 SLOW DECAY. The power dissipation during the ON period is the same. The RECIRCULATION is made internally through a power transistor ($V_{sat_{sink}}$) and a diode. The power dissipation is, therefore:

$$P_{pw} = 1.1 \cdot [2 \, V_{sat} \cdot I_{ph} \cdot DC + (V_{sat} + V_d) \cdot I_{ph} \cdot (1-DC)]$$

$$P_{pw} = 1.1 \cdot [2 \cdot 1.8 \cdot 1 \cdot 0.25 + (1.8 + 1) \cdot 1 \cdot 0.75]$$

$$P_{pw} = 1.1 \cdot [0.9 + 2.1] = 3.3 \, W$$

G4.3 WAVE MODE. When operating in this mode the power dissipation is given by values of 4.1 or 4.2 paragraphes, because one phase is energized at any given time.

G4.4 NORMAL MODE. At any given time, two windings are always energized. The power dissipation of the power output stage is therefore multiplied by a factor 2.



G4.5 HALF STEP. The power sequence, one phase ON, two phase ON forces the power dissipation to be 1.5 times higher than in WAVE MODE when the motor is running. In stall condition the worst case for power dissipation is with two phase ON i.e. a power dissipation as in NORMAL MODE.

The following table summarizes the power dissipations of the output power stage of the GS-D200 when running for this example:

	Wave	Normal	Half Step
Fast Decay	3.19 W	6.38 W	6.38 W
Slow Decay	3.30 W	6.60 W	6.60 W

G5. Calculate the total power dissipation for the GS-D200:

$$P_{\text{tot}} = P_{\text{logic}} + P_{\text{pw}}$$

In this example, for slow decay and normal mode

$$P_{\text{tot}} = 1.1 + 6.6 = 7.7 \text{ W}$$

G6. The case temperature can now be calculated:

$$T_{\text{case}} = T_{\text{amb}} + (P_{\text{tot}} \cdot R_{\text{th}}) = 55 + (7.7 \cdot 5) = 93.5 \text{ }^{\circ}\text{C}$$

G7. If the calculated case temperature exceeds the maximum allowed case temperature, as in this example, an external heat-sink is required and the thermal resistance can be calculated according to:

$$R_{\text{th}_{\text{tot}}} = \frac{T_{\text{cmax}} - T_{\text{amb}}}{P_{\text{tot}}} = \frac{85 - 55}{7.7} = 3.9 \text{ }^{\circ}\text{C/W}$$

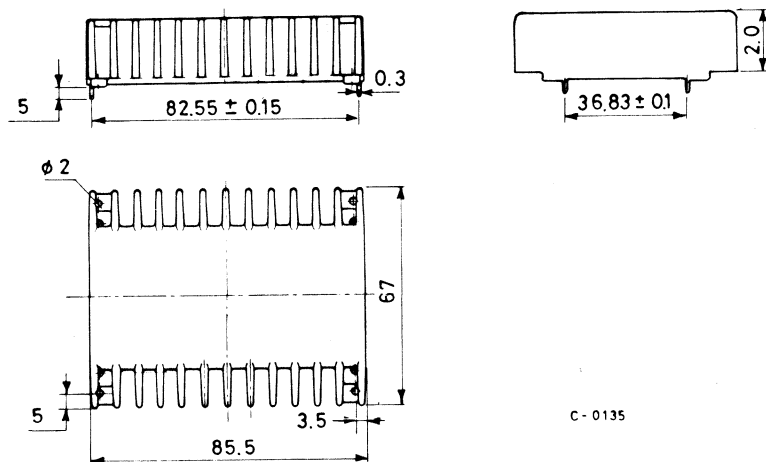
and then

$$R_{\text{th}_{\text{hs}}} = \frac{R_{\text{th}} - R_{\text{th}_{\text{tot}}}}{P_{\text{tot}}} = \frac{5 - 3.9}{5 - 3.9} = 17.7^{\circ}\text{C/W}$$

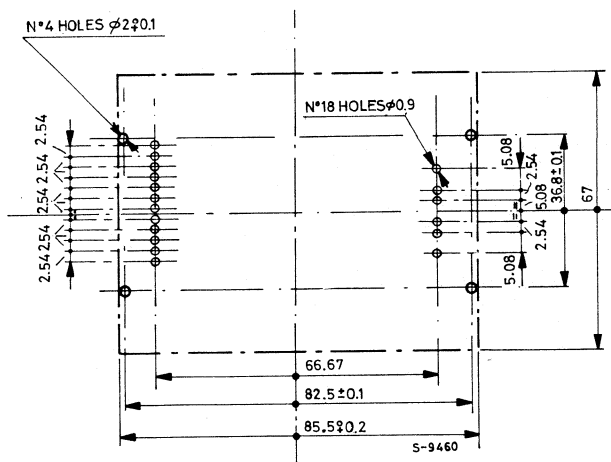
The following table gives the thermal resistance of some commercially available heat-sinks that fit on the GS-D200 module.

Manufacturer	Part Number	R_{th} ($^{\circ}\text{C/W}$)	Mounting
Thermalloy	6177	3	Horizontal
Thermalloy	6152	4	Vertical
Thermalloy	6111	10	Vertical
Fischer	SK18	3	Vertical
Assman	V5440	4	Vertical
Assman	V5382	4	Horizontal

MECHANICAL DATA (dimensions in mm)



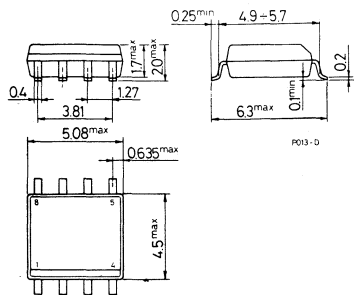
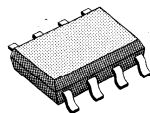
MOTHER BOARD LAYOUT



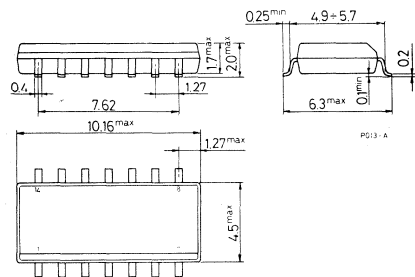
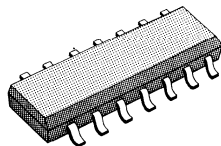
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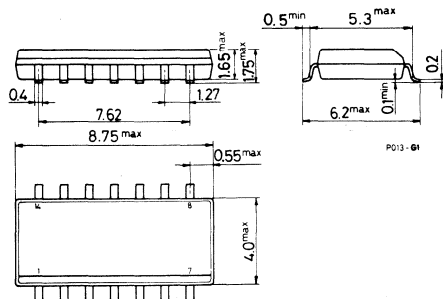
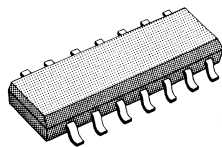
SO-8



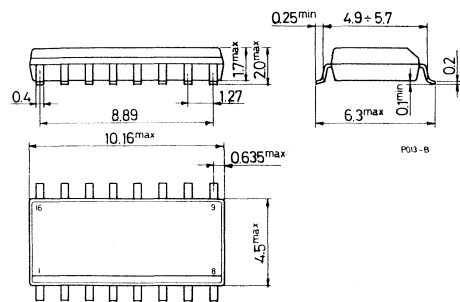
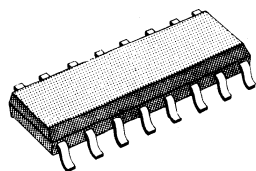
SO-14



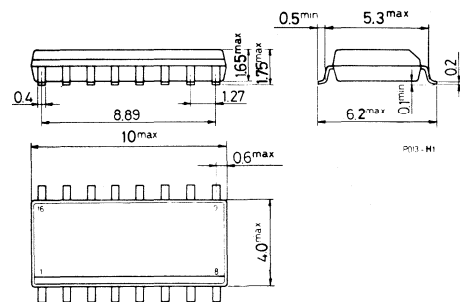
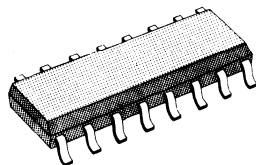
SO-14 Jedec



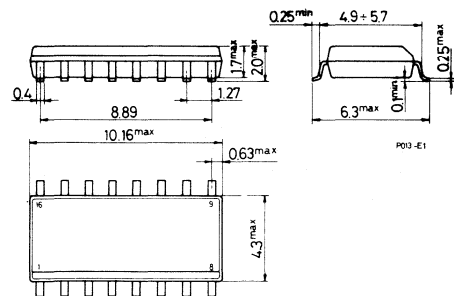
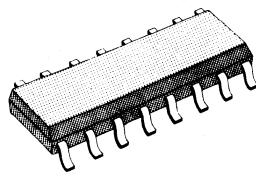
SO-16



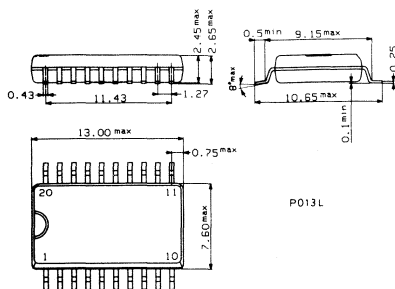
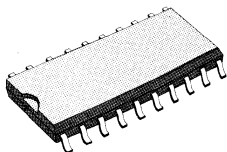
SO-16 Jedec



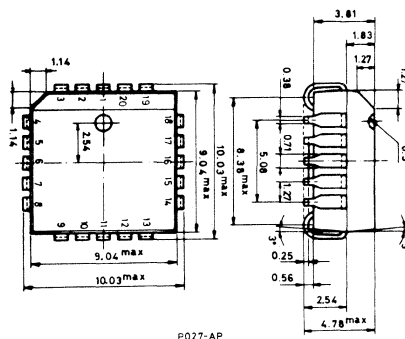
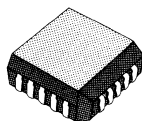
SO-16P



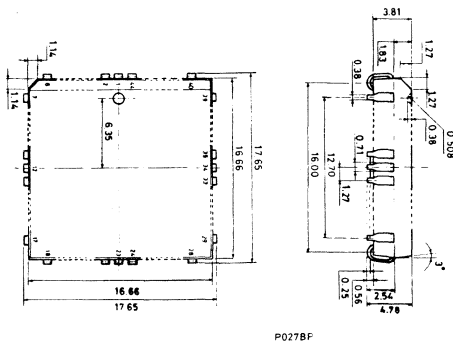
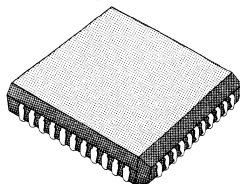
SO-20L



PLCC-20 Plastic Chip Carrier

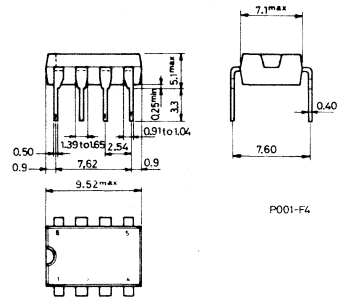
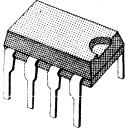


PLCC-44 Plastic Chip Carrier

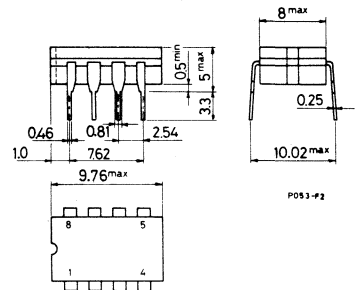
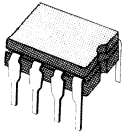


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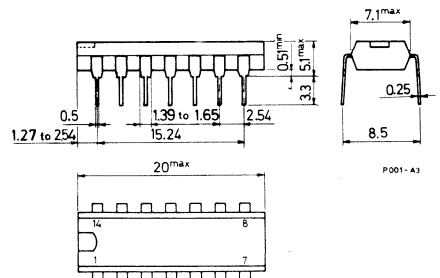
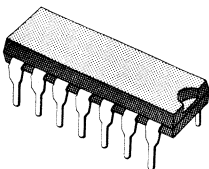
8 lead Plastic Minidip



8 lead Ceramic Minidip

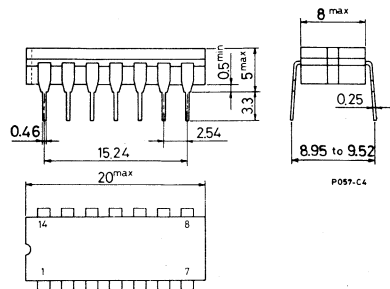
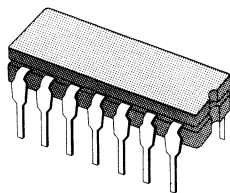


14 lead Plastic Dip

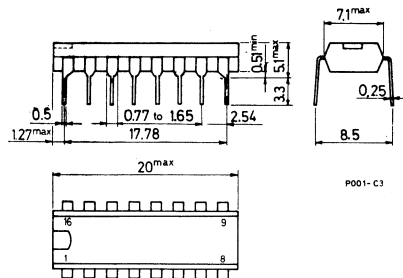
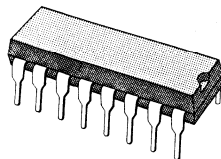


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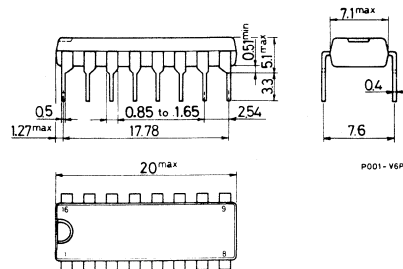
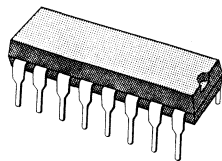
14 lead Ceramic Dip



16 lead Plastic Dip (0.25)

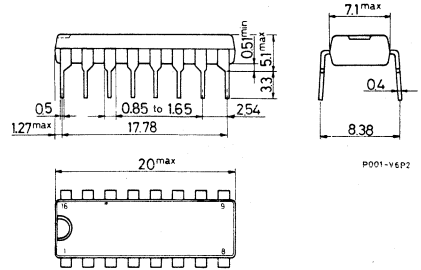
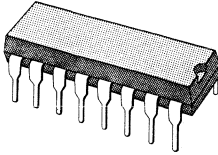


16 lead Plastic Dip (0.4) 8 + 8 lead Powerdip 12 + 2 + 2 lead Powerdip

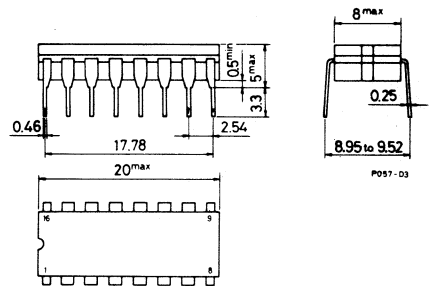
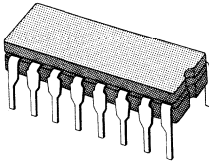


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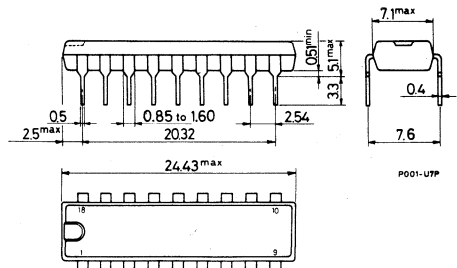
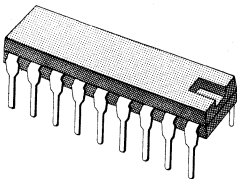
16 lead Plastic Dip (V6P2)
8 + 8 lead Powerdip (V6P2)
12 + 2 + 2 lead Powerdip (V6P2)



16-lead Ceramic Dip

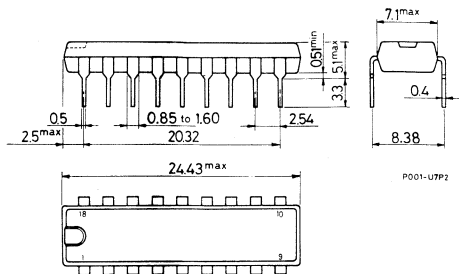
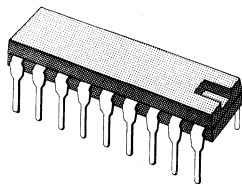


18 lead Plastic Dip (0.4)
9 + 9 lead Powerdip

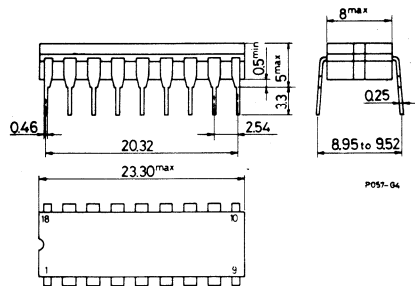
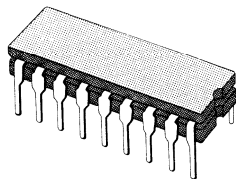


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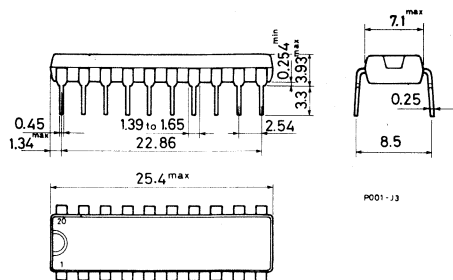
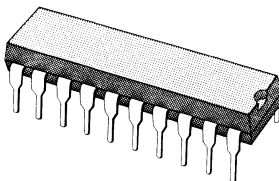
18 lead Plastic Dip (U7P2)
12 + 3 + 3 lead Powerdip



18 lead Ceramic Dip

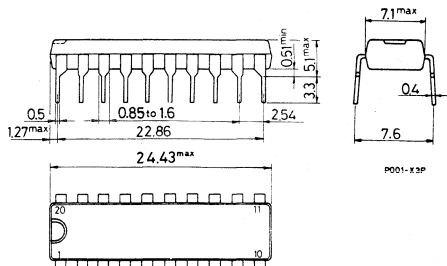
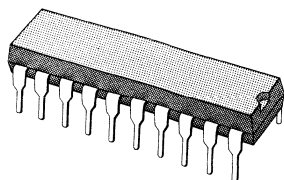


20 lead Plastic Dip (0.25)

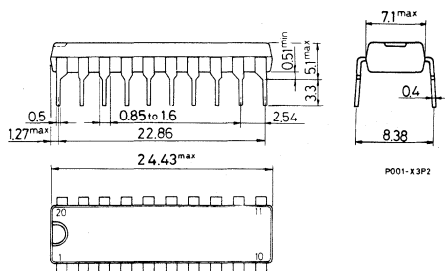
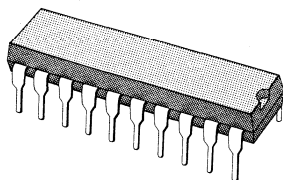


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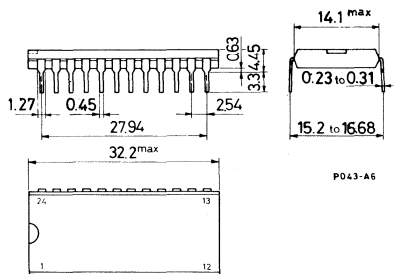
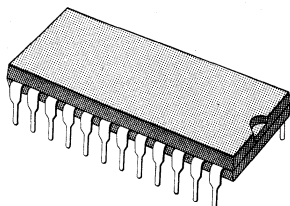
20 lead Plastic Dip (0.4)
16 + 2 + 2 lead Powerdip



20 lead Plastic Dip (X3P2)

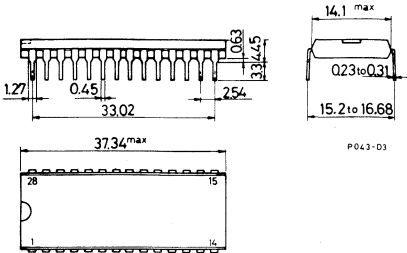
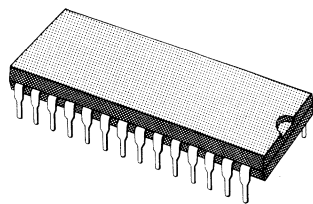


24 lead Plastic Dip

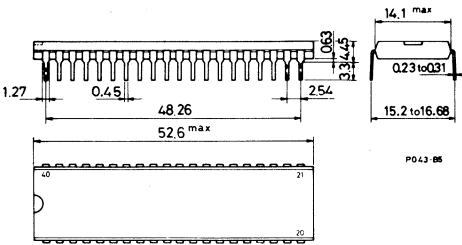
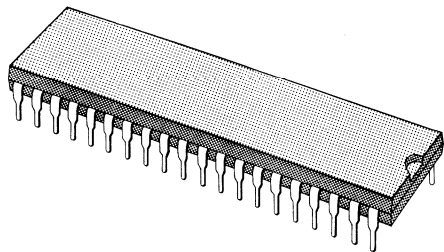


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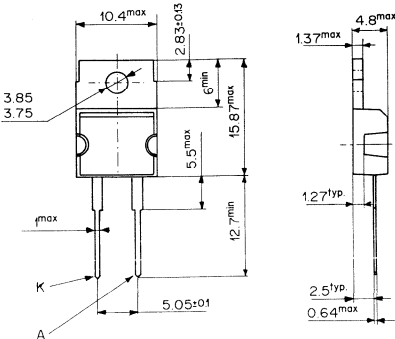
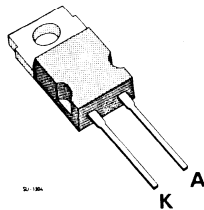
28 lead Plastic Dip



40 lead Plastic Dip

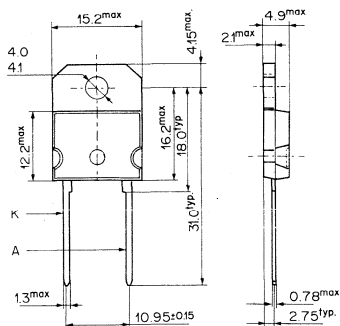
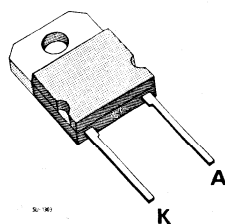


D10WATT1



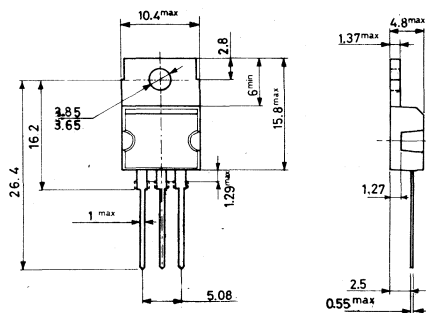
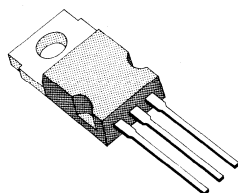
PACKAGES

DIOWATT2



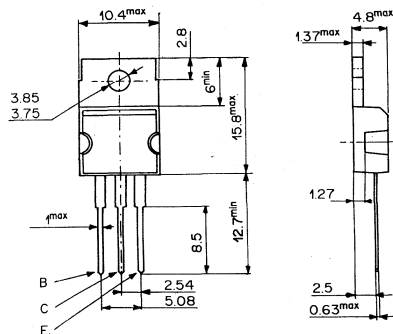
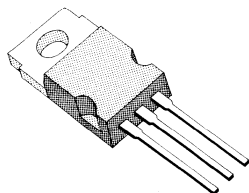
PC-0272/2

TO-220 (ICs)



P011-Dc

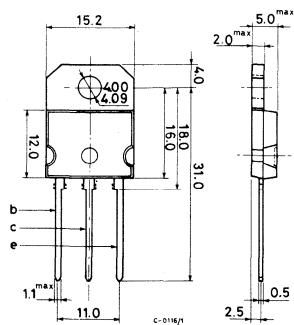
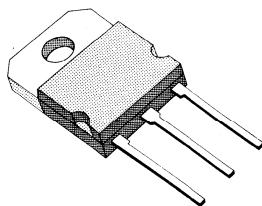
TO-220 (Discrete Power)



PR-0966/1

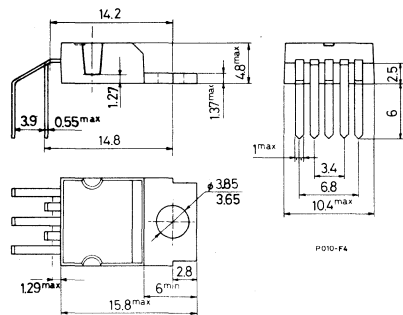
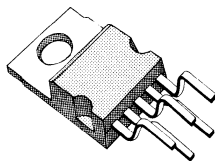
PACKAGES

SOT-93 (TO-218)

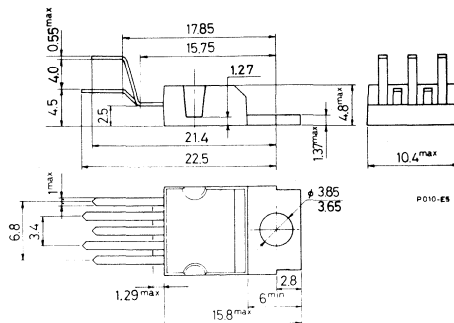


PENTAWATT

Horizontal Version

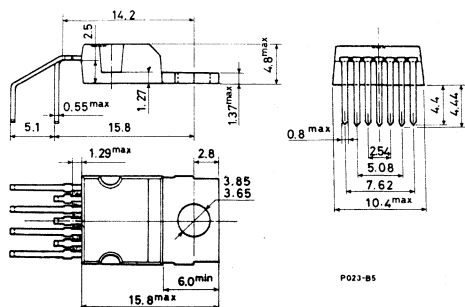
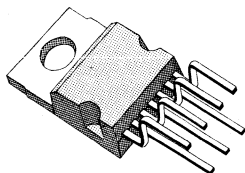


Vertical Version

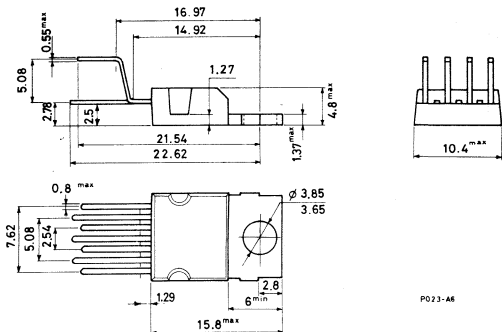


HEPTAWATT

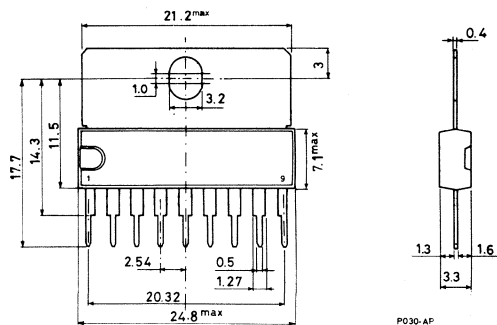
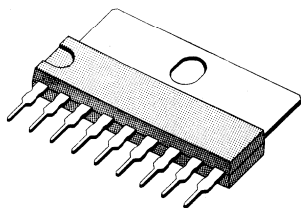
Horizontal Version

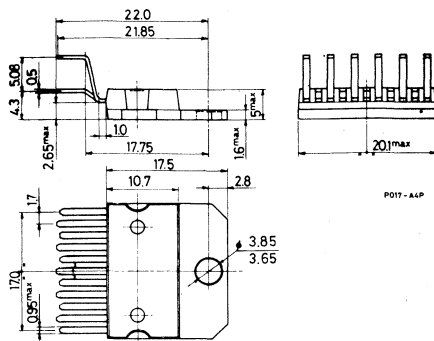
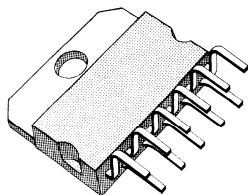


Vertical Version

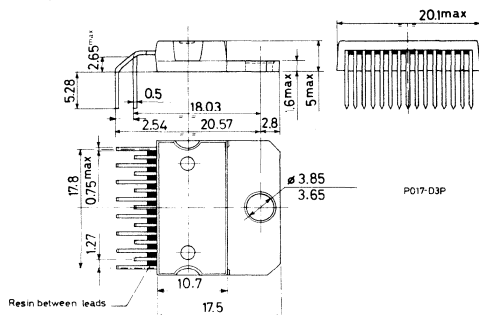
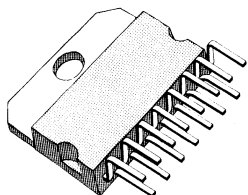


SIP-9

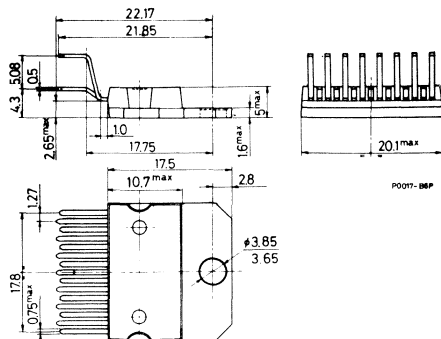


MULTIWATT-11

Horizontal Version

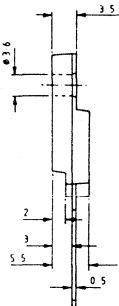
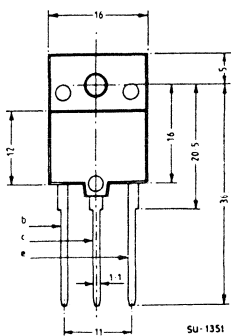
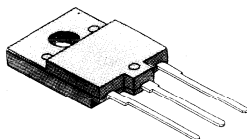


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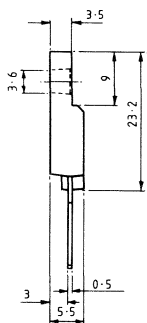
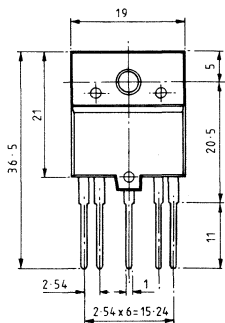
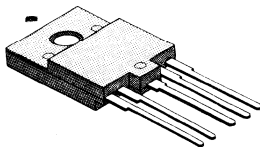


PACKAGES

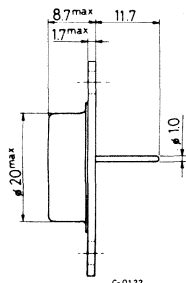
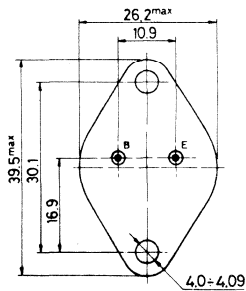
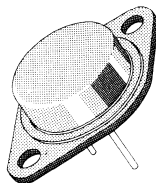
ISOWATT218



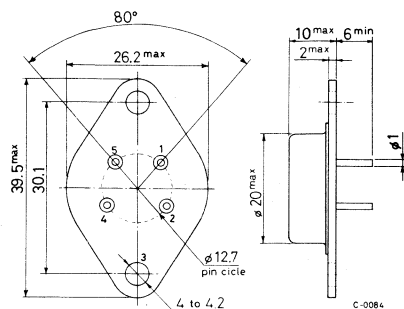
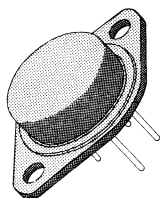
ISOWATT5



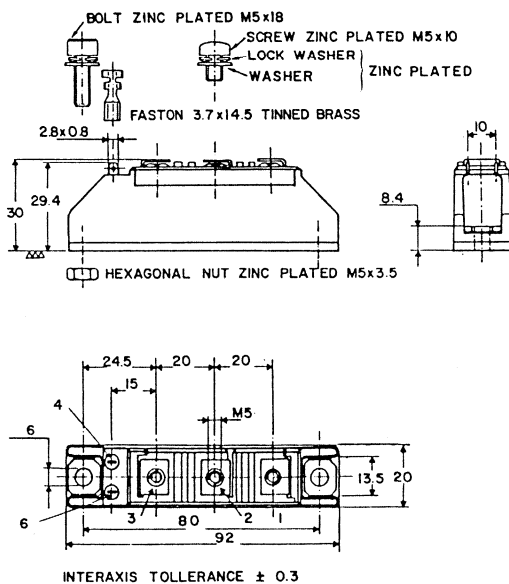
TO-3



TO-3 (4 lead)



A perspective view of a battery pack. It consists of three cylindrical cells connected in series, each with a '+' sign on its top. The cells are housed in a dark, rectangular plastic casing. On the right side of the casing, there is a single terminal with a '+' sign and a small rectangular cutout at the bottom.



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